THE DATASHEET OF

ICS673M-01I

PLL BUILDING BLOCK

ICS673-01

Description

The ICS673-01 is a low cost, high-performance Phase Locked Loop (PLL) designed for clock synthesis and synchronization. Included on the chip are the phase detector, charge pump, Voltage Controlled Oscillator (VCO), and two output buffers. One output buffer is a divide by two of the other. Through the use of external reference and VCO dividers (the ICS674-01), the user can customize the clock to lock to a wide variety of input frequencies.

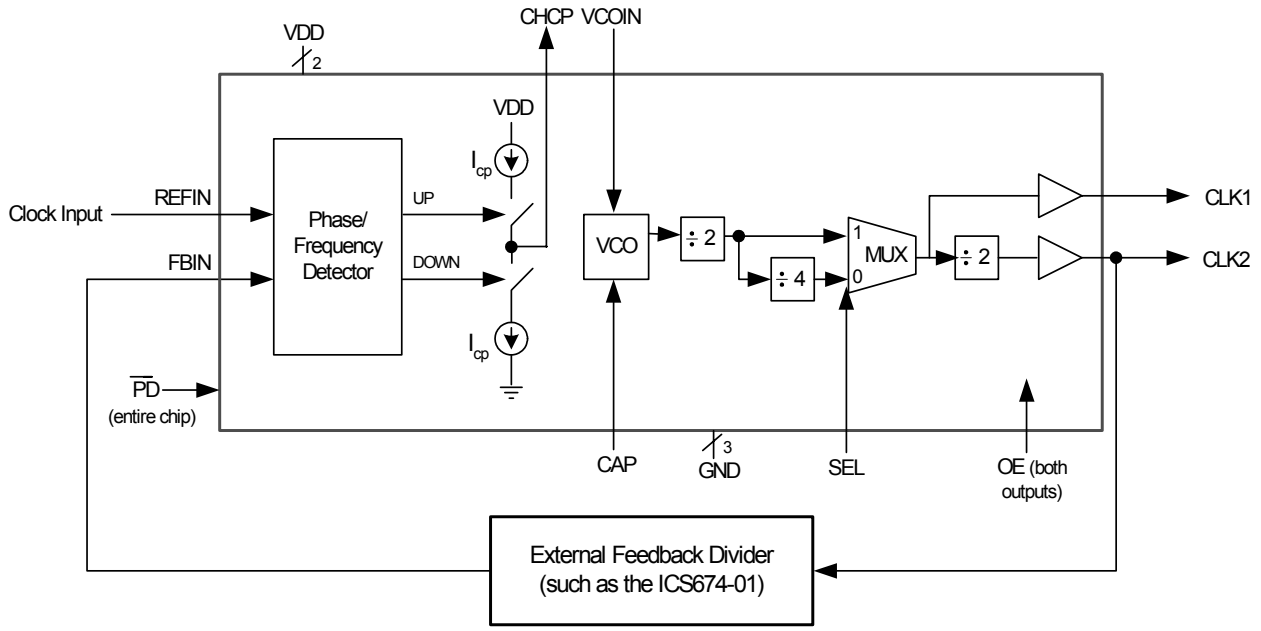
The ICS673-01 also has an output enable function that puts both outputs into a high-impedance state. The chip also has a power-down feature which turns off the entire device.

For applications that require low jitter or jitter attenuation, see the MK2069.

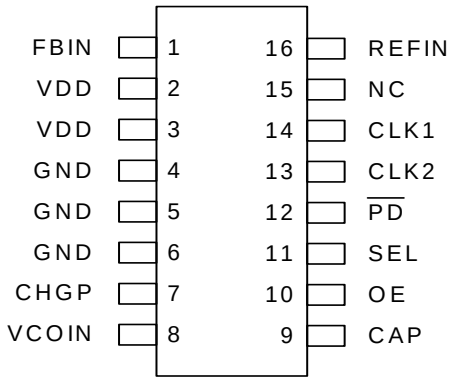
Features

- Packaged in 16-pin SOIC
- Available in RoHS compliant package
- Access to VCO input and feedback paths of PLL
- Output operating range up to 120 MHz (5 V)
- Able to lock MHz range outputs to kHz range inputs through the use of external dividers
- Output Enable tri-states outputs
- Low skew output clocks
- Power-down turns off chip
- VCO predivide to feedback divider of 1 or 4
- 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- Single supply +3.3 V (±5%) or +5 V (±10%) operating voltage
- Industrial and commercial temperature ranges
- Forms a complete PLL, using the ICS674-01
- For better jitter performance, use the MK1575

Block Diagram



Pin Assignment



16 pin narrow (150 mil) SOIC

VCO Predivide Select Table

SEL	VCO Predivide
0	4
1	1

0 = connect pin directly to ground
1 = connect pin directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	FBIN	Input	Feedback clock input. Connect the feedback clock to this pin. Triggered on falling edge.
2	VDD	Power	Connect to +3.3 V or +5 V and to VDD on pin 3.
3	VDD	Power	Connect to VDD on pin 2.
4	GND	Power	Connect to ground.
5	GND	Power	Connect to ground.
6	GND	Power	Connect to ground.
7	CHGP	Output	Charge pump output. Connect to VCOIN under normal operation.
8	VCOIN	Input	Input to internal VCO.
9	CAP	Input	Loop filter return.
10	OE	Input	Output enable. Active when high. Tri-states both outputs when low. Internal weak pull-up resistor.
11	SEL	Input	Select pin for VCO predivide to feedback divider per table above. Internal weak pull-up resistor.
12	$\overline{PD}$	Input	Power down. Turns off entire chip when pin is low. Outputs stop low. Internal weak pull-up resistor.
13	CLK2	Output	Clock output 2. Low skew divide by two version of CLK1.
14	CLK1	Output	Clock output 1.
15	NC	-	No connect. Nothing is connected internally to this pin.
16	REFIN	Input	Reference input. Connect reference clock to this pin. Triggered on falling edge.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS673-01. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70° C
Industrial Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	° C
Ambient Operating Temperature (industrial)	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.13		+5.50	V

DC Electrical Characteristics

VDD=3.3 V ±5% or 5.0 V ±10%, Ambient temperature -40 to +85° C, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.13		5.50	V
Logic Input High Voltage	V_{IH}	REFIN, FBIN, SEL	2			V
Logic Input Low Voltage	V_{IL}	REFIN, FBIN, SEL			0.8	V
LF Input Voltage Range	V_I		0		VDD	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -8 mA	VDD-0.4			
Operating Supply Current	IDD	VDD = 5.0 V, No load, 40 MHz		15		mA
Short Circuit Current	I_{OS}	CLK		±100		mA
Input Capacitance	C_{IN}	SEL		5		pF

AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature -40 to +85° C, C_{LOAD} at CLK = 15 pF, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Clock Frequency (from pin CLK)	f_{CLK}	SEL = 1	1		100	MHz
		SEL = 0	0.25		25	MHz
Input Clock Frequency (into pins REFIN or FBIN)	f_{REF}		Note 1		8	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V		1.2	2	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V		0.75	1.5	ns
Output Clock Duty Cycle	t_{DC}	At VDD/2	40	50	60	%
Jitter, Absolute peak-to-peak	t_J			250		ps
VCO Gain	K_O			190		MHz/V
Charge Pump Current	I_{cp}			2.5		µA

VDD = 5.0 V ±10%, Ambient Temperature -40 to +85° C, C_{LOAD} at CLK = 15 pF, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Clock Frequency (from pin CLK)	f_{CLK}	SEL = 1	1		120	MHz
		SEL = 0	0.25		30	MHz
Input Clock Frequency (into pins REFIN or FBIN)	f_{REF}		Note 1		8	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V		0.5	1	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V		0.5	1	ns
Output Clock Duty Cycle	t_{DC}	At VDD/2	45	50	55	%
Jitter, Absolute peak-to-peak	t_J			150		ps
VCO Gain	K_O			190		MHz/V
Charge Pump Current	I_{cp}			2.4		µA

Note 1: Minimum input frequency is limited by loop filter design. 1 kHz is a practical minimum limit.

External Components

The ICS673-01 requires a minimum number of external components for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD and GND as close to the ICS673-01 as possible. A series termination resistor of 33Ω may be used at the clock output.

Special considerations must be made in choosing loop components C_S and C_P. These can be found online at http://www.icst.com/products/telecom/loopfiltercap.htm

Avoiding PLL Lockup

In some applications, the ICS673-01 can “lock up” at the maximum VCO frequency. This is usually caused by power supply glitches or a very slow power supply ramp. This situation also occurs if the external divider starts to fail at high input frequencies. The usual failure mode of a divider circuit is that the output of the divider begins to miss clock edges. The phase detector interprets this as a too low output frequency and increases the VCO frequency. The

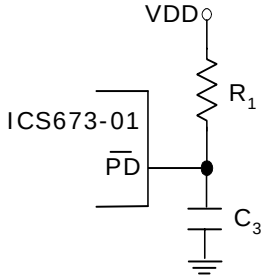
feedback divider begins to miss even more clock edges and the VCO frequency is continually increased until it is running at its maximum frequency. Whether caused by power supply issues or by the external divider, the loop can only recover by powering down the circuit or asserting PD.

The simplest way to avoid this problem is to use an external divider that always operates correctly regardless of the VCO speed. Figures 2 and 3 show that the VCO is capable of high speeds. By using the internal divide-by-four and/or the CLK2 output, the maximum VCO frequency can be divided by 2, 4, or 8 and a slower counter can be used. Using the ICS673 internal dividers in this manner does reduce the number of frequencies that can be exactly synthesized by forcing the total VCO divide to change in increments of 2, 4, or 8.

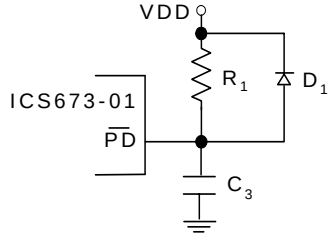
If this lockup problem occurs, there are several solutions; three of which are described below.

1. If the system has a reset or power good signal, this should be applied to the PD pin, forcing the chip to stay powered down until the power supply voltage has stabilized. If the dividers are implemented in an FPGA or other circuit configured on power-up, it is critical keep the ICS673 powered down until the dividers are working properly.

2. If no power good signal is available, a simple power-on reset circuit can be attached to the PD pin, as shown in Figure 1. When the power supply ramps up, this circuit holds PD asserted (device powered down) until the capacitor charges.



A. Basic Circuit



B. Faster Discharge

Fig 1. Power on Reset Circuits

The circuit of Figure 1A is adequate in most cases, but the discharge rate of capacitor C3 when VDD goes low is limited by R1. As this discharge rate determines the minimum reset time, the circuit of Figure 1B may be used when a faster reset time is desired. The values of R1 and C3 should be selected to ensure that PD stays below 1.0 V until the power supply is stable.

3. A comparator circuit may be used to monitor the loop filter voltage as shown in Figure 2. This circuit will dump the charge off the loop filter by asserting PD if the VCO begins to run too fast and the PLL can recover. A good choice for the comparator is the National Semiconductor LMC7211BIM5X. It is low power, version of the small (SOT-23), low cost, and has high input impedance.

The trigger voltage of the comparator is set by the voltage divider formed by R2 and R3. The voltage should be set to a value higher than the VCO input is expected to run during normal operation. Typically, this might be 0.5 V below VDD. Hysteresis should be added to the circuit by connecting R4.

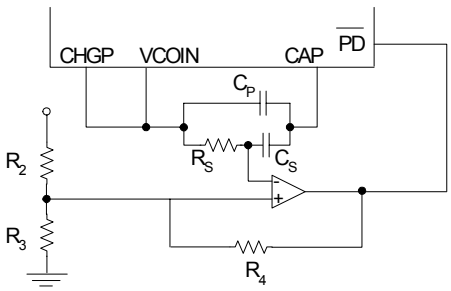


Figure 2. Using an External Comparator to Reset the VCO

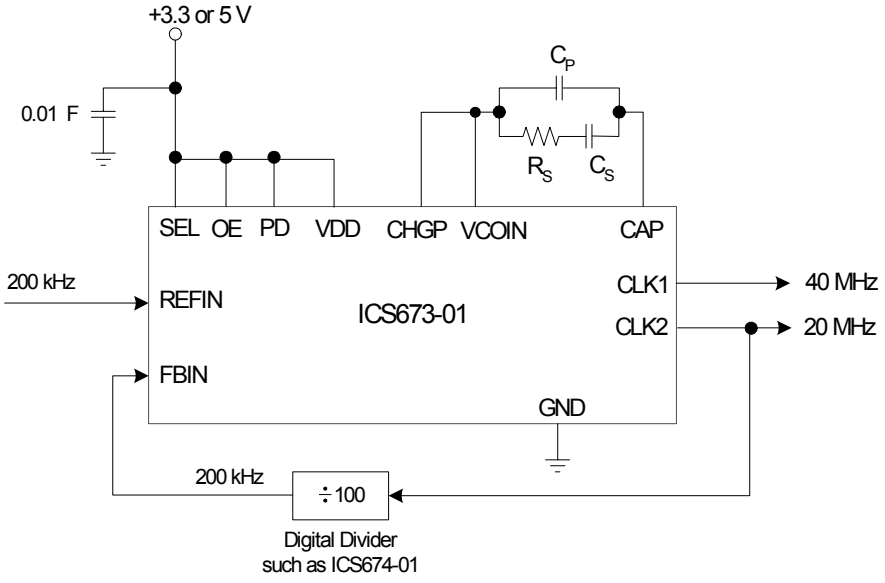
The CLK output frequency may be up to 2x the maximum Output Clock Frequency listed in the AC Electrical Characteristics above when the device is in an unlocked condition. Make sure that the external divider can operate up to this frequency.

Explanation of Operation

The ICS673-01 is a PLL building block circuit that includes an integrated VCO with a wide operating range. The device uses external PLL loop filter components which through proper configuration allow for low input clock reference frequencies, such as a 15.7 kHz Hsync input.

The phase/frequency detector compares the falling edges of the clocks inputted to FBIN and REFIN. It then generates an error signal to the charge pump, which produces a charge proportional to this error. The external loop filter integrates this charge, producing a voltage that then controls the frequency of the VCO. This process continues until the edges of FBIN are aligned with the edges of the REFIN clock, at which point the output frequency will be locked to the input frequency.

Figure 3. Example Configuration -- Generating a 20 MHz clock from a 200 kHz reference.



Determining the Loop Filter Values

The loop filter components consist of C_S, C_P, and R_S. Calculating these values is best illustrated by an example. Using the example in Figure 1, we can synthesize 20 MHz from a 200 kHz input.

The phase locked loop may be approximately described by the following equations:

$$\text{Bandwidth (BW)} = \frac{R_S \cdot K_O \cdot I_{CP}}{2\pi N}$$

$$\text{Damping factor, } \zeta = \frac{R_S}{2}\sqrt{\frac{K_O \cdot I_{CP} \cdot C_S}{N}}$$

where:

K_O = VCO gain (Hz/V)
I_{cp} = Charge pump current (A)
N = Total feedback divide from VCO, including the internal VCO post divider
C_S = Loop filter capacitor (Farads)
R_S = Loop filter resistor (Ohms)

As a general rule, the bandwidth should be at least 20 times less than the reference frequency, i.e.,

$BW \leq (REFIN) / 20$

In this example, using the above equation, bandwidth should be less than or equal to 10 kHz. By setting the bandwith to 10kHz and using the first equation, R_S can be determined since all other variables are known. In the example of Figure 1, N = 200, comprising the divide by 2 on the chip (VCO post divider) and the external divide by 100. Therefore, the bandwidth equation becomes:

$$10{,}000 = \frac{R_S \cdot 190 \cdot 10^{6} \cdot 2.5 \cdot 10^{-6}}{2\pi \cdot 200}$$

and R_S = 26 kΩ

Choosing a damping factor of 0.7 (a minimal damping factor than can be used to ensure fast lock time), damping factor equation becomes:

$$0.7 = \frac{25{,}000}{2}\sqrt{\frac{190 \cdot 10^{6} \cdot 2.5 \cdot 10^{-6} \cdot C_S}{200}}$$

and C_S = 1.32 nF (1.2 nF is the nearest standard value).

The capacitor C_P is used to damp transients from the charge pump and should be approximately 1/20th the size of C_S, i.e.,

$C_P \cong C_S / 20$

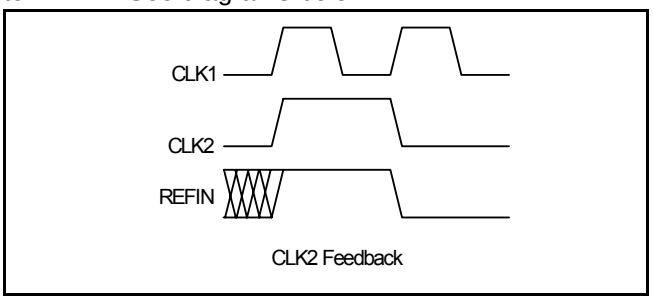
Therefore, C_P = 60 pF (56 pF nearest standard value).

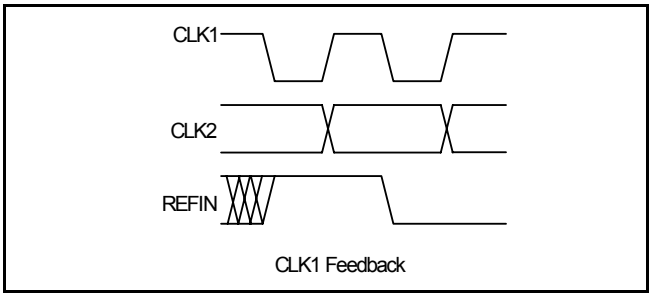
To summarize, the loop filter components are:

C_S = 1.2 nf
C_P = 56 pf
R_S = 26 kΩ

Output Clock Alignment to REFIN

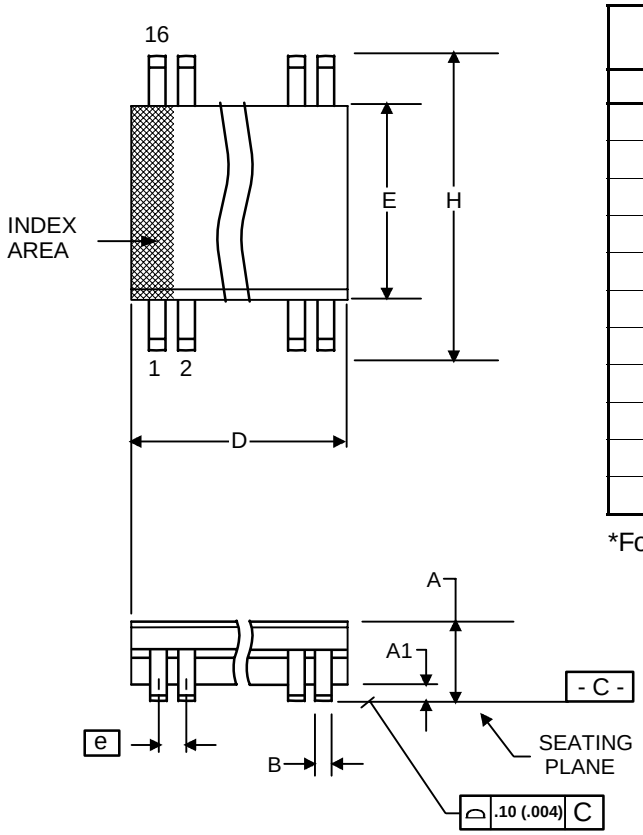
When choosing either CLK1 or CLK2 to drive the feedback divider, ICS recommends that CLK2 be used so that the falling edges of CLK2 and REFIN, and the rising edge of CLK1, are all synchronized. If CLK1 is used for feedback, CLK2 may be either a rising or falling edge when compared to REFIN. See diagrams below.





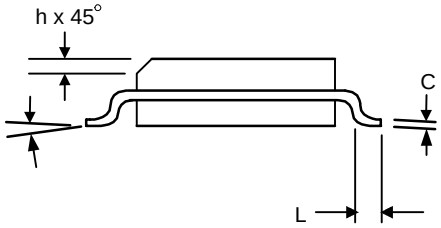
Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
673M-01I	ICS673M-01I	Tubes	16-pin SOIC	-40 to +85° C
673M-01IT	ICS673M-01I	Tape and Reel	16-pin SOIC	-40 to +85° C
673M-01ILF	673M-01ILF	Tubes	16-pin SOIC	-40 to +85° C
673M-01ILFT	673M-01ILF	Tape and Reel	16-pin SOIC	-40 to +85° C
673M-01	ICS673M-01	Tubes	16-pin SOIC	0 to +70° C
673M-01T	ICS673M-01	Tape and Reel	16-pin SOIC	0 to +70° C
673M-01LF	673M-01LF	Tubes	16-pin SOIC	0 to +70° C
673M-01LFT	673M-01LF	Tape and Reel	16-pin SOIC	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
<product line email>
<product line phone>

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339

www.IDT.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View ICS673M-01I on WIN SOURCE
- IDT, Integrated Device Technology Inc Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management