



THE DATASHEET OF ICS570ALFT



MULTIPLIER AND ZERO DELAY BUFFER

ICS570

Description

The ICS570 is a high-performance Zero Delay Buffer (ZDB) which integrates IDT's proprietary analog/digital Phase Locked Loop (PLL) techniques. The A version is recommended for 5 V designs and the B version for 3.3 V designs. The chip is part of IDT's ClockBlocks™ family, and was designed as a performance upgrade to meet today's higher speed and lower voltage requirements. The zero delay feature means that the rising edge of the input clock aligns with the rising edges of both output clocks, giving the appearance of no delay through the device. There are two outputs on the chip, one being a low-skew divide by two of the other output. The device incorporates an all-chip power down/tri-state mode that stops the internal PLL and puts both outputs into a high impedance state.

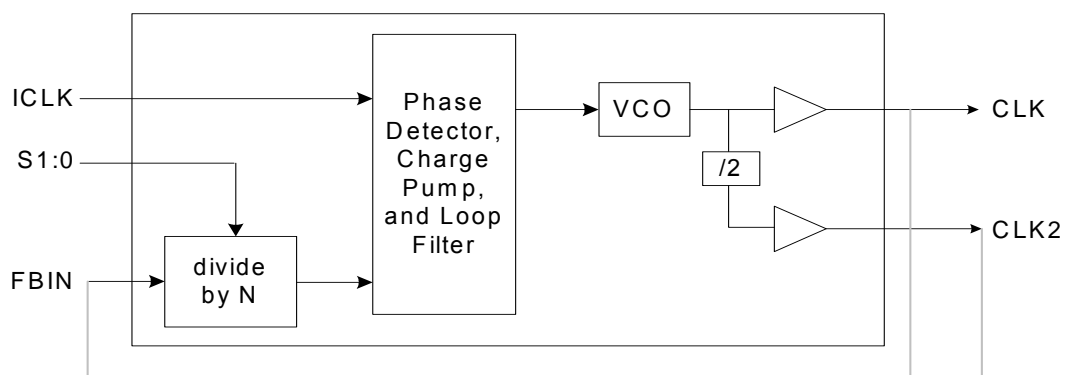
The ICS570 is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to graphics/video. By allowing off-chip feedback paths, the device can eliminate the delay through other devices.

The ICS570 A and B versions were designed to improve input to output jitter from the original ICS570M version, and are recommended for all new designs.

Features

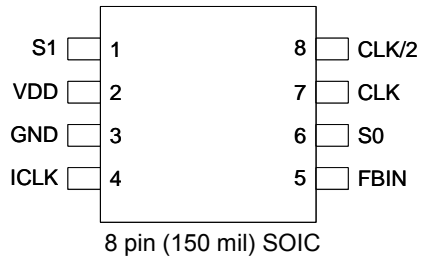
- 8-pin SOIC package
- Available in Pb (lead) free package
- Pin-for-pin replacement and upgrade to ICS570M
- Functional equivalent to AV9170 (not a pin-for-pin replacement)
- Low input to output skew of 300 ps max (>60 MHz outputs)
- Ability to choose between 14 different multipliers from 0.5x to 32x
- Output clock frequency up to 170 MHz at 3.3 V
- Can recover degraded input clock duty cycle
- Output clock duty cycle of 45/55
- Power Down and Tri-State Mode
- Passes spread spectrum clock modulation
- Full CMOS clock swings with 25 mA drive capability at TTL levels
- Advanced, low power CMOS process
- ICS570B has an operating voltage of 3.3 V (±5%)
- ICS570A has an operating voltage of 5.0 V (±5%)
- Industrial temperature version available

Block Diagram



External feedback can come from CLK or CLK/2 (see table on page 2)

Pin Assignment



Clock Multiplier Decoding Table

(Multiplies Input clock by amount shown)

| #1 | #0 | FBIN from CLK | | FBIN from CLK/2 | | ICS570B (3.3 V) | | ICS570A (5.0 V) | |
|----|----|--------------------------|--------|-----------------|--------|------------------|----------------|------------------|----------------|
| | | CLK | CLK/2 | CLK | CLK/2 | ICLK Input Range | FB from CLK/2* | ICLK Input Range | FB from CLK/2* |
| #1 | #0 | pin #7 | pin #8 | pin #7 | pin #8 | | | | |
| 0 | 0 | Power Down and Tri-State | | | | - | | - | |
| 0 | M | x3 | x1.5 | x6 | x3 | 3.75 to 28 | | 2.5 to 25 | |
| 0 | 1 | x4 | x2 | x8 | x4 | 2.75 to 19 | | 2.5 to 19 | |
| M | 0 | x8 | x4 | x16 | x8 | 2.5 to 9.5 | | 2.5 to 9.5 | |
| M | M | x6 | x3 | x12 | x6 | 2.5 to 12.5 | | 2.5 to 12.5 | |
| M | 1 | x10 | x5 | x20 | x10 | 2.5 to 7.5 | | 2.5 to 7.5 | |
| 1 | 0 | x1 | /2 | x2 | x1 | 11 to 85 | | 5 to 75 | |
| 1 | M | x16 | x8 | x32 | x16 | 1.5 to 5 | | 1.5 to 5 | |
| 1 | 1 | x2 | x1 | x4 | x2 | 5.5 to 37.5 | | 2.5 to 37.5 | |

0 = connect directly to ground

M = leave unconnected (self-biases to VDD/2)

1 = connect directly to VDD

*Input range with CLK feedback is double that for CLK/2

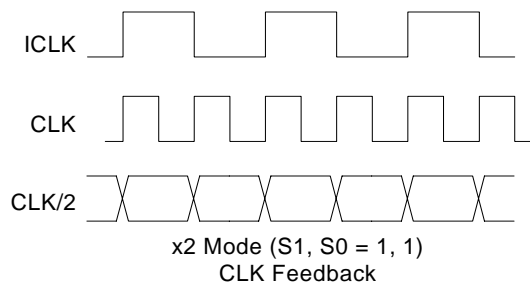
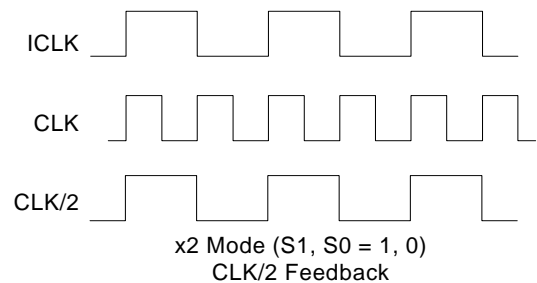
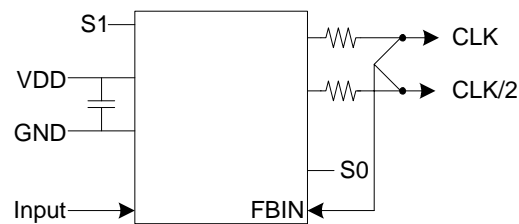
Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | S1 | Input | Select 1 for output clock. Connect to GND, VDD, or float per decoding |
| 2 | VDD | Power | Connect to +3.3 V (ICS570B). Connect to +5.0 V (ICS570A). |
| 3 | GND | Power | Connect to ground. |
| 4 | ICLK | Input | Reference clock input. |
| 5 | FBIN | Input | Feedback clock input. |
| 6 | S0 | Input | Select 0 for output clock. Connect to GND, VDD, or float per decoding |
| 7 | CLK | Output | Clock output per table above. |
| 8 | CLK/2 | Output | Clock output per table above. Low skew divide by two of pin 7 clock. |

External Components

The ICS570 requires a 0.01 μ F decoupling capacitor to be connected between VDD and GND. It must be connected close to the part to minimize lead inductance. No external power supply filtering is required for this device. A 33 Ω series terminating resistor can be used next to each output pin.

Recommended Circuit



Using CLK as the feedback will always result in synchronized rising edges between ICLK and CLK. However, the CLK/2 could be a falling edge compared with ICLK. IDT recommends using CLK/2 feedback whenever possible. This will synchronize the rising edges of all three clocks.

Clock Period Jitter Tables (ICS570A)

All jitter values are considered typical measured at 25° C with 27 Ω termination resistor and 15 pF loads on both CLK and CLK/2. The feedback is from CLK/2 to FBIN. Note that if an output is unused, it should be left unconnected to improve output jitter on the active output clocks.

Absolute and One Sigma Jitter (ps)

| S | S | CLKIN | CLK = 50M | | | CLK/2 = 25M | | |
|---|---|--------|------------|-----------|---------|-------------|----------|---------|
| | | | Multiplier | P to P | 1 sigma | Multiplier | P to P | 1 sigma |
| 0 | M | 8.333 | 6x | ± 115 | 80 | 3x | ± 65 | 20 |
| 0 | 1 | 6.25 | 8x | ± 115 | 80 | 4x | ± 60 | 20 |
| M | 0 | 3.125 | 16x | ± 120 | 80 | 8x | ± 55 | 20 |
| M | M | 4.167 | 12x | ± 120 | 90 | 6x | ± 60 | 20 |
| M | 1 | 2.5 | 20x | ± 120 | 80 | 10x | ± 60 | 20 |
| 1 | 0 | 25 | 2x | ± 120 | 70 | 1x | ± 55 | 20 |
| 1 | M | 1.5625 | 32x | ± 120 | 80 | 16x | ± 50 | 20 |
| 1 | 1 | 12.5 | 4x | ± 120 | 80 | 2x | ± 55 | 20 |

Absolute and One Sigma Jitter (ps)

| S | S | CLKIN | CLK = 100M | | | CLK/2 = 50M | | |
|---|---|--------|------------|-----------|---------|-------------|----------|---------|
| | | | Multiplier | P to P | 1 sigma | Multiplier | P to P | 1 sigma |
| 0 | M | 16.667 | 6x | ± 135 | 100 | 3x | ± 55 | 20 |
| 0 | 1 | 12.5 | 8x | ± 140 | 100 | 4x | ± 50 | 20 |
| M | 0 | 6.25 | 16x | ± 140 | 110 | 8x | ± 55 | 20 |
| M | M | 8.333 | 12x | ± 140 | 110 | 6x | ± 55 | 20 |
| M | 1 | 5 | 20x | ± 135 | 100 | 10x | ± 50 | 20 |
| 1 | 0 | 50 | 2x | ± 120 | 90 | 1x | ± 50 | 20 |
| 1 | M | 3.125 | 32x | ± 135 | 100 | 16x | ± 55 | 20 |
| 1 | 1 | 25 | 4x | ± 130 | 90 | 2x | ± 65 | 20 |

Absolute and One Sigma Jitter (ps)

| S | S | CLKIN | CLK = 150M | | | CLK/2 = 75M | | |
|---|---|--------|------------|-----------|---------|-------------|----------|---------|
| | | | Multiplier | P to P | 1 sigma | Multiplier | P to P | 1 sigma |
| 0 | M | 25 | 6x | ± 160 | 120 | 3x | ± 55 | 20 |
| 0 | 1 | 18.375 | 8x | ± 165 | 120 | 4x | ± 55 | 20 |
| M | 0 | 9.375 | 16x | ± 170 | 120 | 8x | ± 50 | 20 |
| M | M | 12.5 | 12x | ± 160 | 120 | 6x | ± 55 | 20 |
| M | 1 | 7.5 | 20x | ± 160 | 120 | 10x | ± 55 | 20 |

| | | | | | | | | |
|---|---|--------|-----|------|-----|-----|-----|----|
| 1 | 0 | 75 | 2x | ±155 | 110 | 1x | ±55 | 20 |
| 1 | M | 4.6875 | 32x | ±165 | 120 | 16x | ±55 | 20 |
| 1 | 1 | 37.5 | 4x | ±160 | 110 | 2x | ±50 | 20 |

Clock Period Jitter Tables (ICS570B)

All jitter values are considered typical measured at 25° C with 27Ω termination resistor and 15 pF loads on both CLK and CLK/2. The feedback is from CLK/2 to FBIN. Note that if an output is unused, it should be left unconnected to improve output jitter on the active output clocks.

Absolute and One Sigma Jitter (ps)

| S | S | CLKIN | CLK = 50M | | | CLK/2 = 25M | | |
|---|---|--------|------------|--------|---------|-------------|--------|---------|
| | | | Multiplier | P to P | 1 sigma | Multiplier | P to P | 1 sigma |
| 0 | M | 8.333 | 6x | ±110 | 80 | 3x | ±55 | 20 |
| 0 | 1 | 6.25 | 8x | ±125 | 90 | 4x | ±50 | 20 |
| M | 0 | 3.125 | 16x | ±130 | 90 | 8x | ±55 | 20 |
| M | M | 4.167 | 12x | ±120 | 90 | 6x | ±55 | 20 |
| M | 1 | 2.5 | 20x | ±115 | 90 | 10x | ±55 | 20 |
| 1 | 0 | 25 | 2x | ±130 | 50 | 1x | ±55 | 20 |
| 1 | M | 1.5625 | 32x | ±120 | 90 | 16x | ±55 | 20 |
| 1 | 1 | 12.5 | 4x | ±120 | 60 | 2x | ±55 | 20 |

Absolute and One Sigma Jitter (ps)

| S | S | CLKIN | CLK = 100M | | | CLK/2 = 50M | | |
|---|---|--------|------------|--------|---------|-------------|--------|---------|
| | | | Multiplier | P to P | 1 sigma | Multiplier | P to P | 1 sigma |
| 0 | M | 16.667 | 6x | ±100 | 70 | 3x | ±45 | 20 |
| 0 | 1 | 12.5 | 8x | ±100 | 70 | 4x | ±45 | 20 |
| M | 0 | 6.25 | 16x | ±110 | 80 | 8x | ±45 | 20 |
| M | M | 8.333 | 12x | ±100 | 70 | 6x | ±45 | 20 |
| M | 1 | 5 | 20x | ±105 | 70 | 10x | ±40 | 20 |
| 1 | 0 | 50 | 2x | ±90 | 60 | 1x | ±40 | 20 |
| 1 | M | 3.125 | 32x | ±95 | 70 | 16x | ±45 | 20 |
| 1 | 1 | 25 | 4x | ±105 | 70 | 2x | ±60 | 20 |

Absolute and One Sigma Jitter (ps)

| S | S | CLKIN | CLK = 150M | | | CLK/2 = 75M | | |
|---|---|--------|------------|--------|---------|-------------|--------|---------|
| | | | Multiplier | P to P | 1 sigma | Multiplier | P to P | 1 sigma |
| 0 | M | 25 | 6x | ±115 | 70 | 3x | ±50 | 20 |
| 0 | 1 | 18.375 | 8x | ±120 | 80 | 4x | ±50 | 20 |
| M | 0 | 9.375 | 16x | ±130 | 90 | 8x | ±50 | 20 |
| M | M | 12.5 | 12x | ±130 | 90 | 6x | ±45 | 20 |

| | | | | | | | | |
|---|---|--------|-----|------|----|-----|-----|----|
| M | 1 | 7.5 | 20x | ±130 | 90 | 10x | ±45 | 20 |
| 1 | 0 | 75 | 2x | ±115 | 90 | 1x | ±45 | 20 |
| 1 | M | 4.6875 | 32x | ±130 | 90 | 16x | ±50 | 20 |
| 1 | 1 | 37.5 | 4x | ±110 | 70 | 2x | ±60 | 20 |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS570. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature, Commercial version | 0 to +70° C |
| Ambient Operating Temperature, Industrial version | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|-------|-------|
| Ambient Operating Temperature, Commercial version | 0 | | 70 | ° C |
| Ambient Operating Temperature, Industrial version | -40 | | +85 | ° C |
| Power Supply Voltage (measured in respect to GND) | +3.15 | +3.3 | +3.45 | V |

DC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3\text{ V} \pm 5\%$, Ambient Temperature -40 to $+85^\circ\text{C}$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------------------|-----------------|---|---------|-------|------|-------|
| Operating Voltage | VDD | ICS570B, ICS570M | 3.15 | | 3.45 | V |
| | | ICS570A, ICS570M | 4.75 | | 5.25 | |
| Operating Current | IDD | ICS570B, ICS570M VDD=3.3 V, 50M input, S1:0 = 11 | | 16 | | mA |
| | | ICS570A, ICS570M VDD=5.0 V, 50M input, S1:0 = 11 | | 25 | | mA |
| Input High Voltage | V _{IH} | ICLK, FBIN | 2 | | | V |
| Input Low Voltage | V _{IL} | ICLK, FBIN | | | 0.8 | V |
| Input High Voltage | V _{IH} | S0, S1 | VDD-0.5 | | | V |
| Input Low Voltage (mid-level) | V _{IM} | S0, S1 | | VDD/2 | | V |
| Input Low Voltage | V _{IL} | S0, S1 | | | 0.5 | V |
| Output High Voltage (CMOS High) | V _{OH} | I _{OH} = -4 mA | VDD-0.4 | | | V |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 12mA | | | 0.4 | V |
| Short Circuit Current | I _{OS} | Each output | | ±100 | | mA |
| Input Capacitance | C _{IN} | S0, S1 | | 5 | | pF |

AC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3\text{ V} \pm 5\%$, Ambient Temperature -40 to $+85^{\circ}\text{C}$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|--------|------------------------------------|---------------------|---------|------|-------|
| Input Frequency, ICLK | | FBIN from CLK/2 | See table on page 2 | | | |
| Output Clock Frequency | | CLK | 10 | | 170 | MHz |
| Output to Output Skew | | ICS570B, ICS570M | | 100 | 175 | ps |
| Output to Output Skew | | $V_{DD}=5\text{ V}$, ICS570A | | 100 | 200 | ps |
| Input to Output Jitter | | 40 - 150 MHz | | 100-250 | | ps |
| | | ICS570M | | 600 | | ps |
| Input Skew, ICS570B , ICS570M | | ICLK to FBIN, CLK>30MHz, Note 1 | -300 | | 300 | ps |
| | | ICLK to FBIN, CLK<10MHz, Note 1 | -600 | | 600 | ps |
| Input Skew, ICS570A | | ICLK to FBIN CLK>30MHz, Note 1 | -1 | | 1 | ns |
| | | ICLK to FBIN, CLK<10MHz, Note 1 | -1.5 | | 1.5 | ns |
| Output Clock Rise Time | | 0.8 to 2.0V, Note 2 | | 0.75 | | ns |
| Output Clock Fall Time | | 2.0 to 0.8V, Note 2 | | 0.75 | | ns |
| Output Clock Duty Cycle | | at $V_{DD}/2$ | 45 | 49 - 51 | 55 | % |

Note 1: Assumes clocks with same rise time, measured from rising edges at $V_{DD}/2$

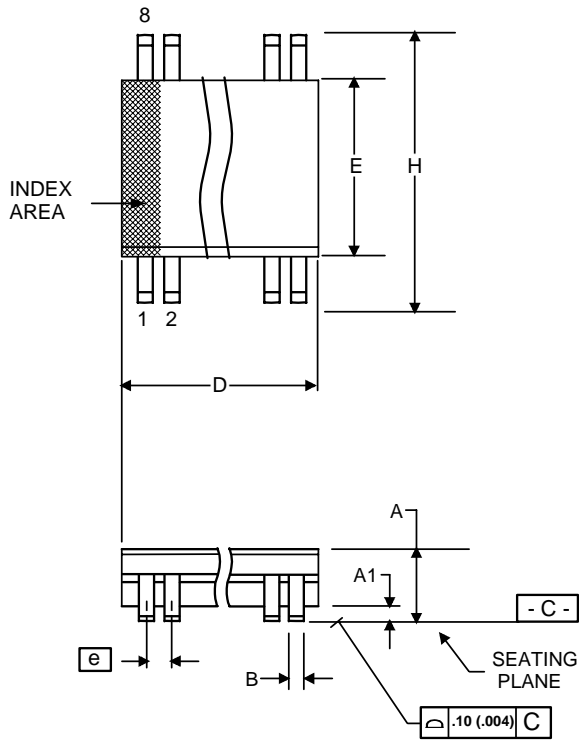
Note 2: Measured with 27Ω terminating resistor and 15 pF loads

Thermal Characteristics

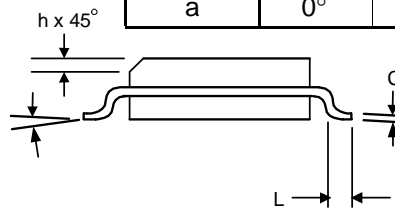
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-----------------------------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 150 | | $^{\circ}\text{C}/\text{W}$ |
| | θ_{JA} | 1 m/s air flow | | 140 | | $^{\circ}\text{C}/\text{W}$ |
| | θ_{JA} | 3 m/s air flow | | 120 | | $^{\circ}\text{C}/\text{W}$ |
| Thermal Resistance Junction to Case | θ_{JC} | | | 40 | | $^{\circ}\text{C}/\text{W}$ |

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches | |
|--------|-------------|------|-------------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | .0532 | .0688 |
| A1 | 0.10 | 0.25 | .0040 | .0098 |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.19 | 0.25 | .0075 | .0098 |
| D | 4.80 | 5.00 | .1890 | .1968 |
| E | 3.80 | 4.00 | .1497 | .1574 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 5.80 | 6.20 | .2284 | .2440 |
| h | 0.25 | 0.50 | .010 | .020 |
| L | 0.40 | 1.27 | .016 | .050 |
| a | 0° | 8° | 0° | 8° |



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|----------|--------------------|------------|--------------|
| 570A | ICS570A | Tubes | 8-pin SOIC | 0 to +70° C |
| 570AT | ICS570A | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| 570AI | ICS570AI | Tubes | 8-pin SOIC | -40 to 85° C |
| 570AIT | ICS570AI | Tape and Reel | 8-pin SOIC | -40 to 85° C |
| 570AILF | 570AILF | Tubes | 8-pin SOIC | -40 to 85° C |
| 570AILFT | 570AILF | Tape and Reel | 8-pin SOIC | -40 to 85° C |
| 570ALF | 570ALF | Tubes | 8-pin SOIC | 0 to +70° C |
| 570ALFT | 570ALF | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| 570B | ICS570B | Tubes | 8-pin SOIC | 0 to +70° C |
| 570BT | ICS570B | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| 570BLF | ICS570BL | Tubes | 8-pin SOIC | 0 to +70° C |
| 570BLFT | ICS570BL | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| 570BI | ICS570BI | Tubes | 8-pin SOIC | -40 to 85° C |
| 570BIT | ICS570BI | Tape and Reel | 8-pin SOIC | -40 to 85° C |
| 570BILF | 570BILF | Tubes | 8-pin SOIC | -40 to 85° C |
| 570BILFT | 570BILF | Tape and Reel | 8-pin SOIC | -40 to 85° C |
| 570M | ICS570M | Tubes | 8-pin SOIC | 0 to +70° C |
| 570MT | ICS570M | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| 570MLF | 570MLF | Tubes | 8-pin SOIC | 0 to +70° C |
| 570MLFT | 570MLF | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| 570MI | ICS570MI | Tubes | 8-pin SOIC | -40 to 85° C |
| 570MIT | ICS570MI | Tape and Reel | 8-pin SOIC | -40 to 85° C |

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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