



**THE DATASHEET OF  
HD3-4702-9**



## HD-4702

### CMOS Programmable Bit Rate Generator

FN2954  
 Rev 2.00  
 August 24, 2006

The HD-4702 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as a UART. It generates 13 commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal <sup>3</sup> 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the <sup>3</sup> 8 prescaler outputs Q0, Q1, Q2 available externally. All signals have a 50% duty cycle except 1800 Baud, which has less than 0.39% distortion.

The four rate select inputs (S0-S3) select which bit rate is at the output (Z). See Truth Table for Rate Select Inputs for select code and output bit rate. Two of the 16 select codes for the HD-4702 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single 5-position switch.

The HD-4702 has an initialization circuit which generates a master reset for the scan counter. This signal is derived from a digital differentiator that senses the first high level on the CP input after the ECP input goes low. When ECP is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset. See Clock Modes and Initialization below.

### Features

- HD-4702 Provides 13 Commonly Used Bit Rates
- Uses a 2.4576MHz Crystal/Input for Standard Frequency Output (16 Times Bit Rate)
- Low Power Dissipation
- Conforms to EIA RS-404
- One HD-4702 Controls up to Eight Transmission Channels
- Initialization Circuit Facilitates Diagnostic Fault Isolation
- On-Chip Input Pull-Up Circuit

### Ordering Information

PACKAGE	TEMP. RANGE (°C)	PART NUMBER	PART MARKING	PKG. NO.
PDIP	-40 to +85	HD3-4702-9	HD3-4702-9	E16.3
PDIP (Pb-free)	-40 to +85	HD3-4702-9Z*	HD3-4702-9Z	E16.3
CerDIP SMD#	-55 to +125	5962-9051801MEA		F16.3

\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

### Truth Table

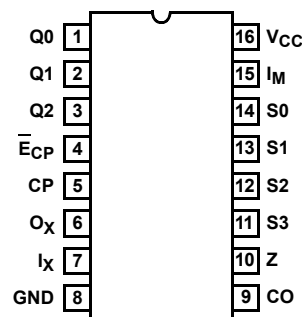
**TRUTH TABLE FOR RATE SELECT INPUTS**  
 (Using 2.4576MHz Crystal)

S3	S2	S1	S0	OUTPUT RATE (Z)
L	L	L	L	MUX Input (IM)
L	L	L	H	MUX Input (IM)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

NOTE: 19200 Baud by connecting Q2 to IM.

### Pinout




**HD-4702 (16 Ld PDIP)**  
 TOP VIEW



### Pin Description

PIN NUMBER	TYPE	SYMBOL	DESCRIPTION
16		V <sub>CC</sub>	V <sub>CC</sub> : Is the +5V power supply pin. A 0.1μF capacitor between pins 16 and 8 is recommended for decoupling.
8		GND	GROUND
5	I	CP	EXTERNAL CLOCK INPUT
4	I	$\bar{E}_{CP}$	EXTERNAL CLOCK ENABLE: A low signal on this input allows the baud rate to be generated from the CP input.
7	I	I <sub>X</sub>	CRYSTAL INPUT
6	O	O <sub>X</sub>	CRYSTAL DRIVE OUTPUT
15	I	I <sub>M</sub>	MULTIPLEXED INPUT
11, 12, 13, 14	I	S0 - S3	BAUD RATE SELECT INPUTS
9	O	CO	CLOCK OUTPUT
1, 2, 3	O	Q <sub>0</sub> - Q <sub>2</sub>	SCAN COUNTER OUTPUTS
10	O	Z	BIT RATE OUTPUT


#### CLOCK MODES AND INITIALIZATION

IX	$\bar{E}_{CP}$	CP	OPERATION
	H	L	Clocked from I <sub>X</sub>
X	L		Clocked from CP
X	H	H	Continuous Reset
X	L		Reset During 1st CP = High Time

H = HIGH Level

L = LOW Level

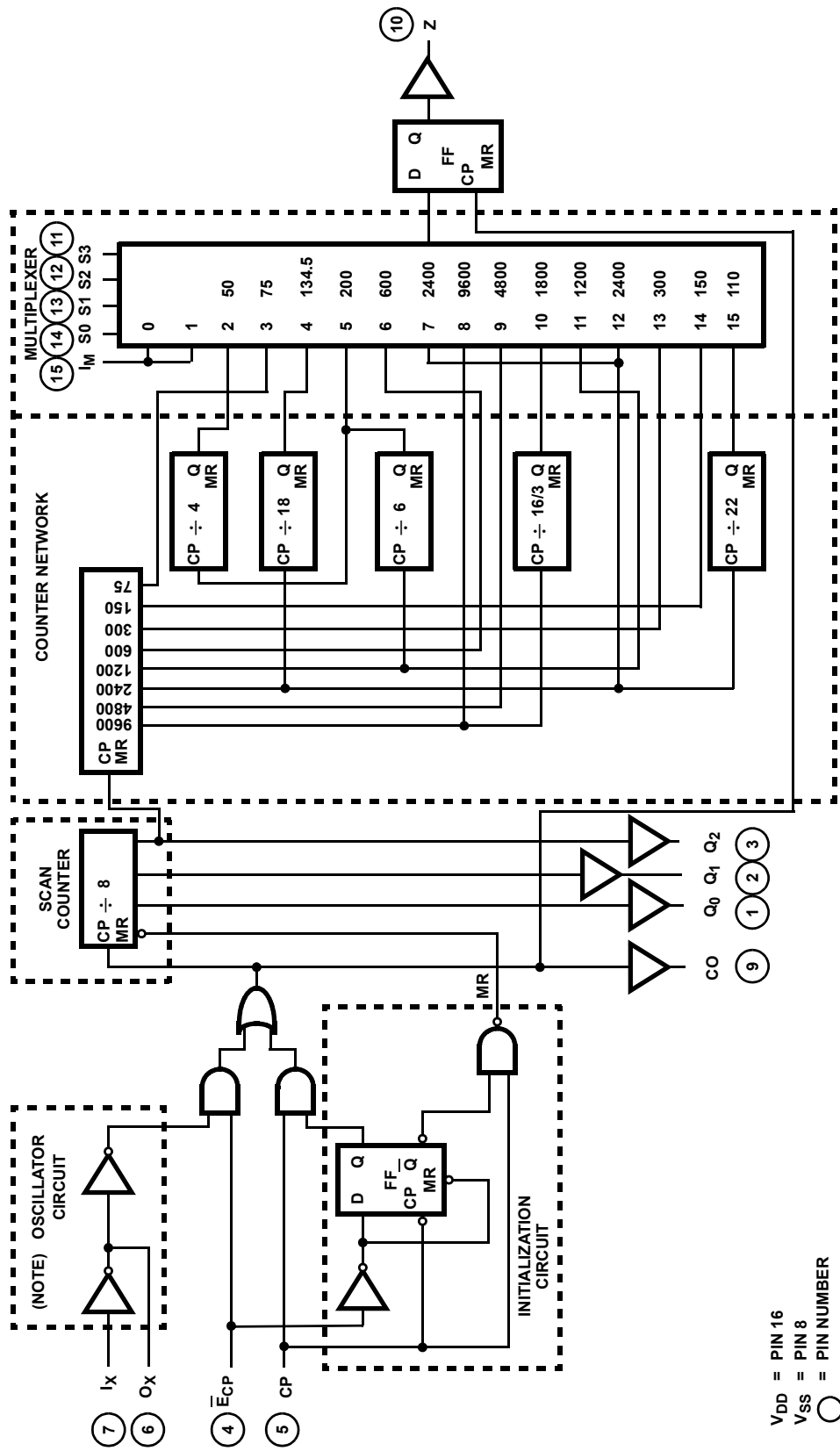
X = Don't Care

 = Clock Pulse

 = 1st HIGH Level Clock Pulse after  $\bar{E}_{CP}$  goes LOW

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

Block Diagram



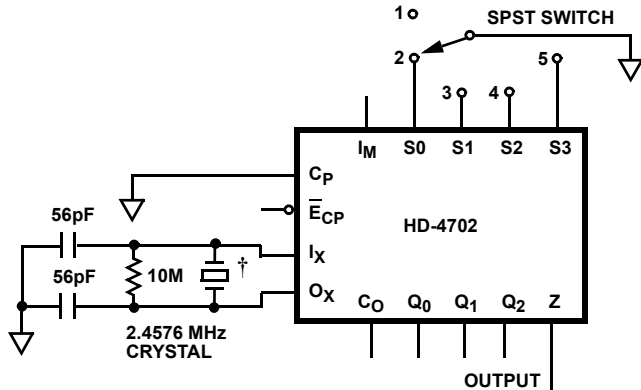
V<sub>DD</sub> = PIN 16  
 V<sub>SS</sub> = PIN 8  
 ○ = PIN NUMBER

NOTE: See Figure 4 in Design Information for Crystal Specifications.

## Application Information

### Single Channel Bit Rate Generator

Figure 1 shows the simplest application of the HD-4702. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 Baud. For many low cost terminals, these five bit rates are adequate.



† See Table 1.

SWITCH POSITION	HD-4702 BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

FIGURE 1. SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES

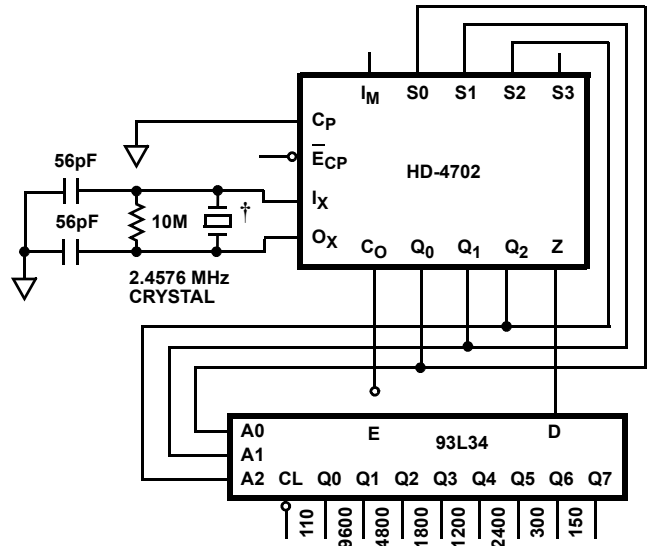
### Simultaneous Generation of Several Bit Rates

Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q<sub>0</sub> to Q<sub>2</sub>) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the HD-4702 to interrogate sequentially eight different frequency signals. The 93L34 8-bit addressable Latch, addressed by the same Scan Counter Outputs, re-converts the multiplexed single Output (Z) of the HD-4702 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S3 is left open (HIGH) and the following bit rates are generated:

- Q0: 110 Baud      Q1: 9600 Baud      Q2: 4800 Baud
- Q3: 1800 Baud    Q4: 1200 Baud      Q5: 2400 Baud
- Q6: 300 Baud      Q7: 150 Baud

Other bit rate combinations can be generated by changing the

Scan Counter to Selector interconnection or by inserting logic gates into this path.

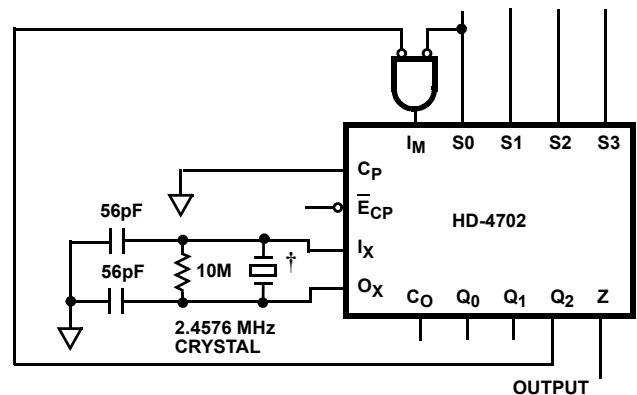


† See Table 1.

FIGURE 2. BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES

### 19200 Baud Operation

Though a 19200 Baud signal is not internally routed to the multiplexer, the HD-4702 can be used to generate this bit rate by connecting the Q<sub>2</sub> output to IM input and applying select code. An additional 2-input NOR gate can be used to retain the “Zero Baud” feature on select code 1 for the HD-4702 (See Figure 3).



† See Table 1.

FIGURE 3. 19200 BAUD OPERATION

TABLE 1. CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576MHz “AT” Cut
Series Resistance (Max)	250
Unwanted Modes	-6.0dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF +0.5



**Electrical Specifications**  $V_{CC} = 5V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  (HD-4702-9),  $T_A = -55^{\circ}C$  to  $+125^{\circ}C$  (HD-4702-8)

SYMBOL	AC PARAMETER	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
$t_{PLH}$	Propagation Delay, $I_X$ to CO	-	350	ns	$V_{CC} = 4.5V$ $C_L \leq 7pF$ on $O_X$ $C_L = 50pF$ (Note 1)
$t_{PHL}$		-	275	ns	
$t_{PLH}$	Propagation Delay, CP to CO	-	260	ns	
$t_{PHL}$		-	220	ns	
$t_{PLH}$	Propagation Delay, CO to Qn	-	(Note 2)	ns	
$t_{PHL}$		-	(Note 2)	ns	
$t_{PLH}$	Propagation Delay, CO to Z	-	85	ns	
$t_{PHL}$		-	75	ns	
$t_{TLH}$	Output Transition Time (Except $O_X$ )	-	160	ns	
$t_{THL}$		-	75	ns	
$t_s$	Set-Up Time, Select to CO	350	-	ns	
$t_h$	Hold Time, Select to CO	0	-	ns	
$t_s$	Set-Up Time, $I_M$ to CO	350	-	ns	
$t_h$	Hold Time, $I_M$ to CO	0	-	ns	
$t_{wCP(L)}$	Minimum Clock Pulse Width, Low (Notes 3, 4)	120	-	ns	
$t_{wCP(H)}$	Minimum Clock Pulse Width, High (Notes 3, 4)	120	-	ns	
$t_{wCP(L)}$	Minimum $I_X$ Pulse Width, Low (Note 4)	160	-	ns	
$t_{wCP(H)}$	Minimum $I_X$ Pulse Width, High (Note 4)	160	-	ns	
$t_{PLH}$	Propagation Delay $I_X$ to CO	-	300	ns	
$t_{PHL}$		-	250	ns	
$t_{PLH}$	Propagation Delay CP to CO	-	215	ns	
$t_{PHL}$		-	195	ns	
$t_{PLH}$	Propagation Delay CO to Qn	-	(Note 2)	ns	
$t_{PHL}$		-	(Note 2)	ns	
$t_{PLH}$	Propagation Delay CO to Z	-	75	ns	
$t_{PHL}$		-	65	ns	
$t_{TLH}$	Output Transition Time (Except $O_X$ )	-	80	ns	
$t_{THL}$		-	40	ns	

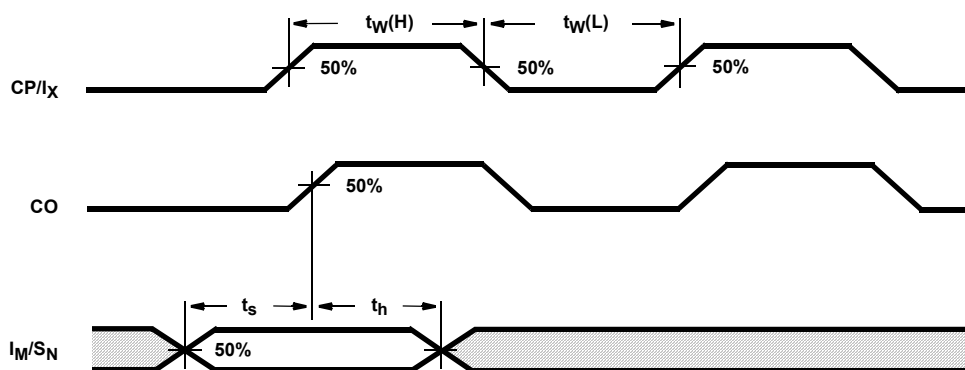
NOTES:

1. Propagation Delays ( $t_{PLH}$  and  $t_{PHL}$ ) and Output Transition Times ( $t_{TLH}$  and  $t_{THL}$ ) will change with Output Load Capacitance ( $C_L$ ). Setup Times ( $t_s$ ), Hold Times ( $t_h$ ), and Minimum Pulse Widths ( $t_w$ ) do not vary with load capacitance.
2. For multichannel operation, Propagation Delay (CO to Qn) plus Set-Up Time, Select to CO, is guaranteed to be  $\leq 367ns$ .
3. The first High Level Clock Pulse after  $\bar{E}_{CP}$  goes Low must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the clock inputs (CP,  $I_X$ ) be less than 15ns.

**Capacitance**  $T_A = +25^{\circ}\text{C}$ ; Frequency = 1MHz

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
$C_{IN}$	Input Capacitance	7	pF	All measurements are referenced the device GND
$C_{OUT}$	Output Capacitance	15	pF	

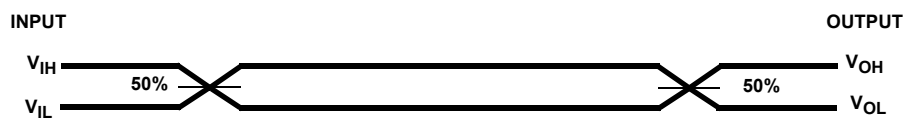
**Switching Waveforms**



NOTE:

1. Setup and Hold times are shown as positive values but may be specified as negative values.

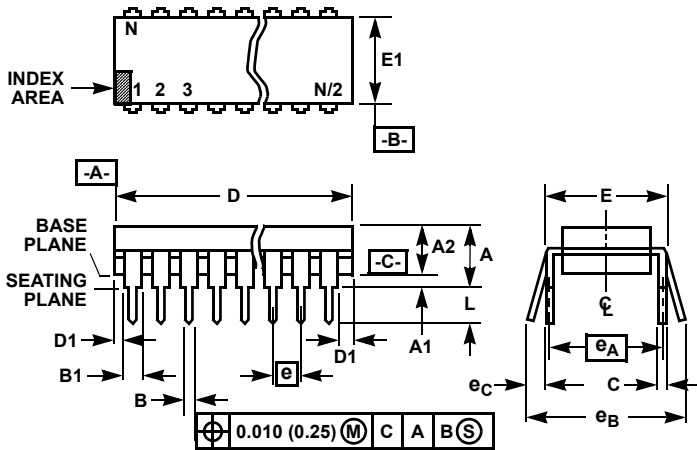
**AC Testing Input, Output Waveform**



NOTE:

1. AC Testing: All input signals must switch between  $V_{IL}$  and  $V_{IH}$ . Input rise and fall times are driven at 1 ns per volt.

**Dual-In-Line Plastic Packages (PDIP)**



**NOTES:**

2. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
5. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
6. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
7. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum [-C-].
8.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
9. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
10. N is the maximum number of terminal positions.
11. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E16.3 (JEDEC MS-001-BB ISSUE D)  
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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