THE DATASHEET OF

GDPXA255A0C300

Intel® PXA255 Processor

Electrical, Mechanical, and Thermal Specification

Data Sheet

Product Features

- High Performance Processor
  - —Intel® XScale™ Microarchitecture
  - —32 KB Instruction Cache
  - —32 KB Data Cache
  - —2 KB “mini” Data Cache
  - —Extensive Data Buffering
- Intel® Media Processing Technology
  - —Enhanced 16-bit Multiply
  - —40-bit Accumulator
- Flexible Clocking
  - —CPU clock from 100 to 400 MHz
  - —Flexible memory clock ratios
  - —Frequency change modes
- Rich Serial Peripheral Set
  - —AC97 Audio Port
  - —I^2S Audio Port
  - —USB Client Controller
  - —High Speed UART
  - —Second UART with flow control
  - —UART with hardware flow control
  - —FIR and SIR infrared comm ports
- Low Power
  - —Less than 500 mW Typical Internal Dissipation
  - —Supply Voltage may be Reduced to 1.00 V
  - —Low Power/Sleep Modes
- High Performance Memory Controller
  - —Four Banks of SDRAM - up to 100 MHz
  - —Five Static Chip Selects
  - —Support for PCMCIA or Compact Flash
  - —Companion Chip interface
- Additional Peripherals for system connectivity
  - —Multimedia Card Controller (MMC)
  - —SSP Controller
  - —Network SSP controller for baseband
  - —I2C Controller
  - —Two Pulse Width Modulators (PWMs)
  - —All peripheral pins double as GPIOs
- Hardware debug features
- Hardware Performance Monitoring features

Order Number: 278805-002

February, 2004

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Revision History

Date	Revision	Description
March 2003	-001	First public release of the EMTS
February 2004	-002	Updated 400 MHz Idle mode power.

1.0 About This Document

This is the electrical, mechanical, and thermal specification data sheet for the Intel® PXA255 Processor. This data sheet contains a functional overview, mechanical data, package signal locations, targeted electrical specifications (simulated), and bus functional waveforms. Detailed functional descriptions other than parametric performance is published in the *Intel® PXA255 Processor Developer's Manual*. Refer to Table 1, "Related Documentation" for a list of documents that support the PXA255 processor.

Table 1. Related Documentation

Document Title	Order / Contact
Intel® PXA255 Processor Developer's Manual	278693
Intel® XScale™ Microarchitecture for the PXA250 and PXA210 Applications Processors Developer's Manual	278525
Intel® PXA255 Processor Design Guide	278694

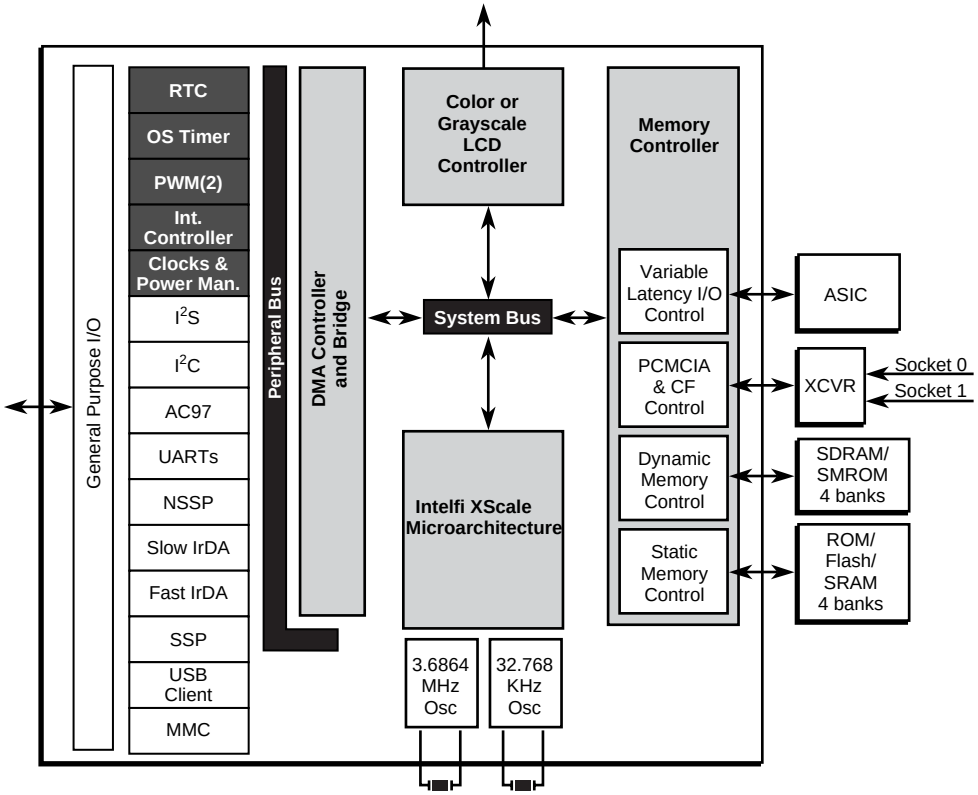
2.0 Functional Overview

The PXA255 processor provides high integration, high performance and low power consumption for portable handheld and handset devices. These processors incorporate the Intel® XScale™ Microarchitecture based on the ARM* V5TE architecture. Refer to the *Intel® XScale™ Microarchitecture for the Intel® PXA250 and PXA210 Applications Processors User's Manual* for implementation details, extensions, and options implemented by the XScale microarchitecture.

The processor memory interface supports a variety of memory types that allow flexible design requirements. Hooks for connection to two companion chips permit glueless connection to external devices. An integrated LCD display controller supports displays and permits 1, 2, and 4-bit grayscale, and 8- or 16-bit color pixels. A 256-byte palette RAM provides flexible color mapping capabilities.

A rich set of serial devices as well as general-system resources provide enough compute and connectivity capability for many applications. For details on the programming model and theory of operation of each of these units, refer to the *Intel® PXA255 Processor Developer's Manual*. For the processor block diagram, refer to Figure 1, "Processor Block Diagram" on page 8.

Figure 1. Processor Block Diagram



3.0 Package Information

3.1 Package Introduction

The PXA255 processor is offered in a 256-pin mBGA (refer to Figure 2, “PXA255 processor” on page 19).

3.1.1 Functional Signal Definitions

3.1.1.1 PXA255 Processor Signal Pin Descriptions

Table 3, “Pin and Signal Descriptions for the PXA255 Processor” on page 9 describes the signal definitions for the PXA255 processor. Figure 2, “PXA255 processor” on page 19 illustrates the physical characteristics of the PXA255 processor. Table 5, “PXA255 processor 256-Lead 17x17mm mBGA Pinout — Ballpad No. Order” on page 20 describes the pinout for the PXA255 processor.

Some of the processor pins can be connected to multiple signals. The GAFRn_m registers determine the signal connected to the pin. Some signals can go to multiple pins. The signal must be routed to one pin only by using the GAFRn_m registers. Because this is true, some pins are listed twice—once in each unit that can use the pin. Not all peripherals can be used simutaneously in one design because different peripherals share the same pins.

Table 2. Processor Pin Types

Type	Function
IC	CMOS input
OC	CMOS output
OCZ	CMOS output, Hi-Z
ICOCZ	CMOS bidirectional, Hi-Z
IA	Analog Input
OA	Analog output
IAOA	Analog bidirectional
SUP	Supply pin (either VCC or VSS)

Table 3. Pin and Signal Descriptions for the PXA255 Processor (Sheet 1 of 9)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
Memory Controller Pins				
MA[25:0]	OCZ	**Memory address bus.** (output) Signals the address requested for memory accesses.	Driven Low	Driven Low
MD[15:0]	ICOCZ	**Memory data bus.** (input/output) Lower 16 bits of the data bus.	Hi-Z	Driven Low
MD[31:16]	ICOCZ	**Memory data bus.** (input/output) Used for 32-bit memories.	Hi-Z	Driven Low
nOE	OCZ	**Memory output enable.** (output) Connect to the output enables of memory devices to control data bus drivers.	Driven High	Note [4]
nWE	OCZ	**Memory write enable.** (output) Connect to the write enables of memory devices.	Driven High	Note [4]
nSDCS[3:0]	OCZ	**SDRAM CS for banks 3 through 0.** (output) Connect to the chip select (CS) pins for SDRAM. For the PXA255 processor processor nSDCS0 can be Hi-Z, nSDCS1-3 cannot.	Driven High	Note [5]
DQM[3:0]	OCZ	**SDRAM DQM for data bytes 3 through 0.** (output) Connect to the data output mask enables (DQM) for SDRAM.	Driven Low	Driven Low
nSDRAS	OCZ	**SDRAM RAS.** (output) Connect to the row address strobe (RAS) pins for all banks of SDRAM.	Driven High	Driven High
nSDCAS	OCZ	**SDRAM CAS.** (output) Connect to the column address strobe (CAS) pins for all banks of SDRAM.	Driven High	Driven High
SDCKE[0]	OC	**Synchronous Static Memory clock enable.** (output) Connect to the CKE pins of SMROM. The memory controller provides control register bits for de-assertion.	Driven Low	Driven Low

Table 3. Pin and Signal Descriptions for the PXA255 Processor (Sheet 2 of 9)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
SDCKE[1]	OC	**SDRAM and/or Synchronous Static Memory clock enable.** (output) Connect to the clock enable pins of SDRAM. It is deasserted during sleep. SDCKE[1] is always de-asserted upon reset. The memory controller provides control register bits for de-assertion.	Driven low	Driven low
SDCLK[0]	OC	**Synchronous Static Memory clock.** (output) Connect to the clock (CLK) pins of SMROM. It is driven by either the internal memory controller clock, or the internal memory controller clock divided by 2. At reset, all clock pins are free running at the divide-by-2 clock speed and may be turned off via free-running control register bits in the memory controller. The memory controller also provides control register bits for clock division and deassertion of each SDCLK pin. SDCLK[0] control register assertion bit defaults to on if the boot-time static memory bank 0 is configured for SMROM.		
SDCLK[1]	OCZ	**SDRAM Clocks** (output) Connect SDCLK[1] and SDCLK[2] to the clock pins of SDRAM in bank pairs 0/1 and 2/3, respectively. They are driven by either the internal memory controller clock, or the internal memory controller clock divided by 2. At reset, all clock pins are free running at the divide-by-2 clock speed and may be turned off via free-running control register bits in the memory controller. The memory controller also provides control register bits for clock division and de-assertion of each SDCLK pin. SDCLK[2:1] control register assertion bits are always de-asserted upon reset.	Driven Low	Driven Low
SDCLK[2]	OC		Driven Low	Driven Low
nCS[5]/ GPIO[33]	ICOCZ	**Static chip selects.** (output) Chip selects to static memory devices such as ROM and Flash. Individually programmable in the memory configuration registers. nCS[5:0] can be used with variable latency I/O devices.	Pulled High - Note[1]	Note [4]
nCS[4]/ GPIO[80]	ICOCZ			
nCS[3]/ GPIO[79]	ICOCZ			
nCS[2]/ GPIO[78]	ICOCZ			
nCS[1]/ GPIO[15]	ICOCZ			
nCS[0]	ICOCZ	**Static chip select 0.** (output) Chip select for the boot memory. nCS[0] is a dedicated pin.	Driven High	Note [4]
RD/nWR	OCZ	**Read/Write for static interface.** (output) Signals that the current transaction is a read or write.	Driven Low	Holds last state
RDY/ GPIO[18]	ICOCZ	**Variable latency I/O ready pin.** (input) Notifies the memory controller when an external bus device is ready to transfer data.	Pulled High - Note[1]	Note [3]
L_DD[8]/ GPIO[66]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **Memory controller alternate bus master request.** (input) Allows an external device to request the system bus from the memory controller.	Pulled High - Note[1]	Note [3]

Table 3. Pin and Signal Descriptions for the PXA255 Processor (Sheet 3 of 9)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
L_DD[15]/ GPIO[73]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **Memory controller grant.** (output) Notifies an external device that it has been granted the system bus.	Pulled High - Note[1]	Note [3]
MBGNT/ GP[13]	ICOCZ	**Memory controller grant.** (output) Notifies an external device that it has been granted the system bus.	Pulled High - Note[1]	Note [3]
MBREQ/ GP[14]	ICOCZ	**Memory controller alternate bus master request.** (input) Allows an external device to request the system bus from the memory controller.	Pulled High - Note[1]	Note [3]
PCMCIA/CF Control Pins				
nPOE/ GPIO[48]	ICOCZ	**PCMCIA output enable.** (output) Reads from PCMCIA memory and to PCMCIA attribute space.	Pulled High - Note[1]	Note [5]
nPWE/ GPIO[49]	ICOCZ	**PCMCIA write enable.** (output) Performs writes to PCMCIA memory and to PCMCIA attribute space. Also used as the write enable signal for variable latency I/O.	Pulled High - Note[1]	Note [5]
nPIOW/ GPIO[51]	ICOCZ	**PCMCIA I/O write.** (output) Performs write transactions to PCMCIA I/O space.	Pulled High - Note[1]	Note [5]
nPIOR/ GPIO[50]	ICOCZ	**PCMCIA I/O read.** (output) Performs read transactions from PCMCIA I/O space.	Pulled High - Note[1]	Note [5]
nPCE[2]/ GPIO[53]	ICOCZ	**PCMCIA card enable 2.** (output) Selects a PCMCIA card. nPCE[2] enables the high byte lane and nPCE[1] enables the low byte lane. **MMC clock.** (output) Clock signal for the MMC controller.	Pulled High - Note[1]	Note [5]
nPCE[1]/ GPIO[52]	ICOCZ	**PCMCIA card enable 1.** (outputs) Selects a PCMCIA card. nPCE[2] enables the high byte lane and nPCE[1] enables the low byte lane.	Pulled High - Note[1]	Note [5]
nIOIS16/ GPIO[57]	ICOCZ	**IO Select 16**. (input) Acknowledge from the PCMCIA card that the current address is a valid 16 bit wide I/O address.	Pulled High - Note[1]	Note [5]
nPWAIT/ GPIO[56]	ICOCZ	**PCMCIA wait.** (input) Driven low by the PCMCIA card to extend the length of the transfers to/from the PXA255 processor processor.	Pulled High - Note[1]	Note [5]
PSKTSEL/ GPIO[54]	ICOCZ	**PCMCIA socket select.** (output) Used by external steering logic to route control, address, and data signals to one of the two PCMCIA sockets. When PSKTSEL is low, socket zero is selected. When PSKTSEL is high, socket one is selected. Has the same timing as the address bus.	Pulled High - Note[1]	Note [5]
nPREG/ GPIO[55]	ICOCZ	**PCMCIA register select.** (output) Indicates that the target address on a memory transaction is attribute space. Has the same timing as the address bus.	Pulled High - Note[1]	Note [5]
LCD Controller Pins				
L_DD(7:0)/ GPIO[65:58]	ICOCZ	**LCD display data.** (outputs) Transfers pixel information from the LCD Controller to the external LCD panel.	Pulled High - Note[1]	Note [3]
L_DD[8]/ GPIO[66]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **Memory controller alternate bus master request.** (input) Allows an external device to request the system bus from the Memory Controller.	Pulled High - Note[1]	Note [3]

Table 3. Pin and Signal Descriptions for the PXA255 Processor (Sheet 4 of 9)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
L_DD[9]/ GPIO[67]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **MMC chip select 0.** (output) Chip select 0 for the MMC controller.	Pulled High - Note[1]	Note [3]
L_DD[10]/ GPIO[68]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **MMC chip select 1.** (output) Chip select 1 for the MMC controller.	Pulled High - Note[1]	Note [3]
L_DD[11]/ GPIO[69]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **MMC clock.** (output) Clock for the MMC controller.	Pulled High - Note[1]	Note [3]
L_DD[12]/ GPIO[70]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **RTC clock.** (output) Real-time clock 1 Hz tick.	Pulled High - Note[1]	Note [3]
L_DD[13]/ GPIO[71]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **3.6864 MHz clock.** (output) Output from 3.6864 MHz oscillator.	Pulled High - Note[1]	Note [3]
L_DD[14]/ GPIO[72]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **32 kHz clock.** (output) Output from the 32 kHz oscillator.	Pulled High - Note[1]	Note [3]
L_DD[15]/ GPIO[73]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **Memory Controller grant.** (output) Notifies an external device it has been granted the system bus.	Pulled High - Note[1]	Note [3]
L_FCLK/ GPIO[74]	ICOCZ	**LCD frame clock.** (output) Indicates the start of a new frame. Also referred to as Vsync.	Pulled High - Note[1]	Note [3]
L_LCLK/ GPIO[75]	ICOCZ	**LCD line clock.** (output) Indicates the start of a new line. Also referred to as Hsync.	Pulled High - Note[1]	Note [3]
L_PCLK/ GPIO[76]	ICOCZ	**LCD pixel clock.** (output) Clocks valid pixel data into the LCD line-shift buffer.	Pulled High - Note[1]	Note [3]
L_BIAS/ GPIO[77]	ICOCZ	**AC bias drive.** (output) Notifies the panel to change the polarity for some passive LCD panel. For TFT panels, this signal indicates valid pixel data.	Pulled High - Note[1]	Note [3]
Full Function UART Pins				
FFRXD/ GPIO[34]	ICOCZ	**Full function UART receive.** (input) **MMC chip select 0.** (output) Chip select 0 for the MMC Controller.	Pulled High - Note[1]	Note [3]
FFTXD/ GPIO[39]	ICOCZ	**Full Function UART transmit.** (output) **MMC chip select 1.** (output) Chip select 1 for the MMC Controller.	Pulled High - Note[1]	Note [3]
FFCTS/ GPIO[35]	ICOCZ	**Full function UART clear-to-send.** (input)	Pulled High - Note[1]	Note [3]
FFDCD/ GPIO[36]	ICOCZ	**Full function UART data-carrier-detect.** (input)	Pulled High - Note[1]	Note [3]
FFDSR/ GPIO[37]	ICOCZ	**Full function UART data-set-ready.** (input)	Pulled High - Note[1]	Note [3]

Table 3. Pin and Signal Descriptions for the PXA255 Processor (Sheet 5 of 9)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
FFRI/ GPIO[38]	ICOCZ	**Full function UART ring indicator.** (input)	Pulled High - Note[1]	Note [3]
FFDTR/ GPIO[40]	ICOCZ	**Full function UART data-terminal-ready.** (output)	Pulled High - Note[1]	Note [3]
FFRTS/ GPIO[41]	ICOCZ	**Full function UART request-to-send.** (output)	Pulled High - Note[1]	Note [3]
Bluetooth UART Pins				
BTRXD/ GPIO[42]	ICOCZ	**Bluetooth UART receive.** (input)	Pulled High - Note[1]	Note [3]
BTTXD/ GPIO[43]	ICOCZ	**Bluetooth UART transmit.** (output)	Pulled High - Note[1]	Note [3]
BTCTS/ GPIO[44]	ICOCZ	**Bluetooth UART clear-to-send.** (input)	Pulled High - Note[1]	Note [3]
BTRTS/ GPIO[45]	ICOCZ	**Bluetooth UART request-to-send.** (output)	Pulled High - Note[1]	Note [3]
Standard UART and ICP Pins				
IRRXD/ GPIO[46]	ICOCZ	**IrDA receive signal.** (input) Receive pin for the FIR function. **Standard UART receive.** (input)	Pulled High - Note[1]	Note [3]
IRTXD/ GPIO[47]	ICOCZ	**IrDA transmit signal.** (output) Transmit pin for the Standard UART, SIR and FIR functions. **Standard UART transmit.** (output)	Pulled High - Note[1]	Note [3]
Hardware UART Pins				
HWRXD/ GPIO[42/49]	ICOCZ	**Hardware UART receive.** (input)	Pulled High - Note[1]	Note [3]
HWTXD/ GPIO[43/48]	ICOCZ	**Hardware UART transmit.** (output)	Pulled High - Note[1]	Note [3]
HWCTS/ GPIO[44/50]	ICOCZ	**Hardware UART clear-to-send.** (input)	Pulled High - Note[1]	Note [3]
HWRTS/ GPIO[45/51]	ICOCZ	**Hardware UART data-terminal-ready.** (output)	Pulled High - Note[1]	Note [3]
MMC Controller Pins				
MMCMD	ICOCZ	**Multimedia card command.** (bidirectional)	Hi-Z	Hi-Z
MMDAT	ICOCZ	**Multimedia card data.** (bidirectional)	Hi-Z	Hi-Z
nPCE[2]/ GPIO[53]	ICOCZ	**PCMCIA card enable 2.** (outputs) Selects a PCMCIA card. Bit one enables the high byte lane and bit zero enables the low byte lane. **MMC clock.** (output) Clock signal for the MMC controller.	Pulled High - Note[1]	Note [5]
L_DD[9]/ GPIO[67]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **MMC chip select 0.** (output) Chip select 0 for the MMC controller.	Pulled High - Note[1]	Note [3]

Table 3. Pin and Signal Descriptions for the PXA255 Processor (Sheet 6 of 9)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
L_DD[10]/ GPIO[68]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **MMC chip select 1.** (output) Chip select 1 for the MMC controller.	Pulled High - Note[1]	Note [3]
L_DD[11]/ GPIO[69]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **MMC clock.** (output) Clock for the MMC controller.	Pulled High - Note[1]	Note [3]
FFRXD/ GPIO[34]	ICOCZ	**Full function UART receive.** (input) **MMC chip select 0.** (output) Chip select 0 for the MMC controller.	Pulled High - Note[1]	Note [3]
FFTXD/ GPIO[39]	ICOCZ	**Full function UART transmit.** (output) **MMC chip select 1.** (output) Chip select 1 for the MMC controller.	Pulled High - Note[1]	Note [3]
MMCCLK/ GP[6]	ICOCZ	**MMC clock.** (output) Clock signal for the MMC controller.	Pulled High - Note[1]	Note [3]
MMCCS0/ GP[8]	ICOCZ	**MMC chip select 0.** (output) Chip select 0 for the MMC controller.	Pulled High - Note[1]	Note [3]
MMCCS1/ GP[9]	ICOCZ	**MMC chip select 1.** (output) Chip select 1 for the MMC controller.	Pulled High - Note[1]	Note [3]
SSP Pins				
SSPSCLK/ GPIO[23]	ICOCZ	**Synchronous serial port clock.** (output)	Pulled High - Note[1]	Note [3]
SSPSFRM/ GPIO[24]	ICOCZ	**Synchronous serial port frame.** (output)	Pulled High - Note[1]	Note [3]
SSPTXD/ GPIO[25]	ICOCZ	**Synchronous serial port transmit.** (output)	Pulled High - Note[1]	Note [3]
SSPRXD/ GPIO[26]	ICOCZ	**Synchronous serial port receive.** (input)	Pulled High - Note[1]	Note [3]
SSPEXTCLK/ GPIO[27]	ICOCZ	**Synchronous serial port external clock.** (input)	Pulled High - Note[1]	Note [3]
NSSP Pins				
NSSPSCLK/ GPIO[81]	ICOCZ	**Network synchronous serial port clock.** (output/input)	Pulled High - Note[1]	Note [3]
NSSPSFRM/ GPIO[82]	ICOCZ	**Network synchronous serial port frame.** (output/input)	Pulled High - Note[1]	Note [3]
NSSPTXD/ GPIO[83]	ICOCZ	**Network synchronous serial port transmit/recieve.** (output/input)	Pulled High - Note[1]	Note [3]
NSSPRXD/ GPIO[84]	ICOCZ	**Network synchronous serial port transmit/receive.** (output/input)	Pulled High - Note[1]	Note [3]
USB Client Pins				
USB_P	IAOAZ	**USB client positive.** (bidirectional)	Hi-Z	Hi-Z
USB_N	IAOAZ	**USB client negative pin.** (bidirectional)	Hi-Z	Hi-Z

Table 3. Pin and Signal Descriptions for the PXA255 Processor (Sheet 7 of 9)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
AC97 Controller and I^2S Controller Pins				
BITCLK/ GPIO[28]	ICOCZ	**AC97 audio port bit clock.** (input) AC97 clock is generated by Codec 0 and fed into the PXA255 processor processor and Codec 1. **AC97 Aaudio port bit clock.** (output) AC97 clock is generated by the PXA255 processor. **I^2S bit clock.** (input) I^2S clock is generated externally and fed into PXA255 processor. **I^2S bit clock.** (output) I^2S clock is generated by the PXA255 processor.	Pulled High - Note[1]	Note [3]
SDATA_IN0/ GPIO[29]	ICOCZ	**AC97 audio port data in.** (input) Input line for Codec 0. **I^2S data in.** (input) Input line for the I^2S controller.	Pulled High - Note[1]	Note [3]
SDATA_IN1/ GPIO[32]	ICOCZ	**AC97 audio port data in.** (input) Input line for Codec 1. **I^2S system clock.** (output) System clock from I^2S controller.	Pulled High - Note[1]	Note [3]
SDATA_OUT/ GPIO[30]	ICOCZ	**AC97 audio port data out.** (output) Output from the PXA255 processor to Codecs 0 and 1. **I^2S data out.** (output) Output line for the I^2S controller.	Pulled High - Note[1]	Note [3]
SYNC/ GPIO[31]	ICOCZ	**AC97 audio port sync signal.** (output) Frame sync signal for the AC97 controller. **I^2S sync.** (output) Frame sync signal for the I^2S controller.	Pulled High - Note[1]	Note [3]
nACRESET	OC	**AC97 audio port reset signal.** (output)	Driven Low	Driven Low
I^2C Controller Pins				
SCL	ICOCZ	**I^2C clock.** (bidirectional)	Hi-Z	Hi-Z
SDA	ICOCZ	**I^2C data.** (bidirectional).	Hi-Z	Hi-Z
PWM Pins				
PWM[1:0]/ GPIO[17:16]	ICOCZ	**Pulse width modulation channels 0 and 1.** (outputs)	Pulled High - Note[1]	Note [3]
DMA Pins				
DREQ[1:0]/ GPIO[19:20]	ICOCZ	**DMA request.** (input) Notifies the DMA Controller that an external device requires a DMA transaction. DREQ[1] is GPIO[19]. DREQ[0] is GPIO[20].	Pulled High - Note[1]	Note [3]
GPIO Pins				
GPIO[1:0]	ICOCZ	**General purpose I/O.** Wakeup sources on both rising and falling edges on nRESET.	Pulled High - Note[1]	Note [3]
GPIO[14:2]	ICOCZ	**General purpose I/O.** More wakeup sources for sleep mode.	Pulled High - Note[1]	Note [3]
GPIO[22:21]	ICOCZ	**General purpose I/O.** Additional General Purpose I/O pins.	Pulled High - Note[1]	Note [3]
Crystal and Clock Pins				
PXTAL	OA	**3.6864 MHz crystal input.** No external caps are required.	Note [2]	Note [2]
PEXTAL	IA	**3.6864 MHz crystal output.** No external caps are required.	Note [2]	Note [2]
TXTAL	OA	**32 KHz crystal input.** No external caps are required.	Note [2]	Note [2]

Table 3. Pin and Signal Descriptions for the PXA255 Processor (Sheet 8 of 9)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
TEXTAL	IA	**32 kHz crystal output.** No external caps are required.	Note [2]	Note [2]
L_DD[12]/ GPIO[70]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **RTC clock.** (output) Real time clock 1 Hz tick.	Pulled High - Note[1]	Note [3]
L_DD[13]/ GPIO[71]	ICOCZ	**LCD display data.** (output) Transfers the pixel information from the LCD controller to the external LCD panel. **3.6864 MHz clock.** (output) Output from 3.6864 MHz oscillator.	Pulled High - Note[1]	Note [3]
L_DD[14]/ GPIO[72]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD controller to the external LCD panel. **32 kHz clock.** (output) Output from the 32 kHz oscillator.	Pulled High - Note[1]	Note [3]
48MHz/GP[7]	ICOCZ	**48 MHz clock.** (output) Peripheral clock output derived from the PLL. **NOTE:** This clock is only generated when the USB unit clock enable is set.	Pulled High - Note[1]	Note [3]
RTCCLK/ GP[10]	ICOCZ	**Real time clock.** (output) 1 Hz output derived from the 32 kHz or 3.6864 MHz output.	Pulled High - Note[1]	Note [3]
3.6MHz/GP[11]	ICOCZ	**3.6864 MHz clock.** (output) Output from 3.6864 MHz oscillator.	Pulled High - Note[1]	Note [3]
32kHz/GP[12]	ICOCZ	**32 kHz clock.** (output) Output from the 32 kHz oscillator.	Pulled High - Note[1]	Note [3]
Miscellaneous Pins				
BOOT_SEL [2:0]	IC	**Boot select pins.** (input) Indicates type of boot device.	Input	Input
PWR_EN	OC	**Power Enable for the power supply.** (output) When negated, it signals the power supply to remove power to the core because the system is entering sleep mode.	Driven High	Driven low while entering sleep mode. Driven high when sleep exit sequence begins.
nBATT_FAULT	IC	**Main Battery Fault.** (input) Signals that main battery is low or removed. Assertion causes PXA255 processor processor to enter sleep mode or force an imprecise data exception, which cannot be masked. PXA255 processor will not recognize a wake-up event while this signal is asserted. Minimum assertion time for nBATT_FAULT is 1 ms.	Input	Input
nVDD_FAULT	IC	**VDD Fault.** (input) Signals that the main power source is going out of regulation. nVDD_FAULT causes the PXA255 processor to enter sleep mode or force an imprecise data exception, which cannot be masked. nVDD_FAULT is ignored after a wake-up event until the power supply timer completes (approximately 10 ms). Minimum assertion time for nVDD_FAULT is 1 ms.	Input	Input
nRESET	IC	**Hard reset.** (input) Level -sensitive input used to start the processor from a known address. Assertion terminates the current instruction abnormally and causes a reset. When nRESET is driven high, the processor starts execution from address 0. nRESET must remain low until the power supply is stable and the internal 3.6864 MHz oscillator has stabilized.	Input	Input. Driving low during sleep will cause normal reset sequence and exit from sleep mode.

Table 3. Pin and Signal Descriptions for the PXA255 Processor (Sheet 9 of 9)

Pin Name	Type	Signal Descriptions	Reset State	Sleep State
nRESET_OUT	OC	**Reset out.** (output) Asserted when nRESET is asserted and deasserts after nRESET is de-asserted but before the first instruction fetch. nRESET_OUT is also asserted for “soft” reset events: sleep, watchdog reset, or GPIO reset.	Driven low during any reset sequence - driven high prior to first fetch.	Driven Low
JTAG and Test Pins				
nTRST	IC	**JTAG test interface reset.** Resets the JTAG/debug port. If JTAG/debug is used, drive nTRST from low to high either before or at the same time as nRESET. If JTAG is not used, nTRST must be either tied to nRESET or tied low.	Input	Input
TDI	IC	**JTAG test data input.** (input) Data from the JTAG controller is sent to the PXA255 processor using this pin. This pin has an internal pull-up resistor.	Input	Input
TDO	OCZ	**JTAG test data output.** (output) Data from the PXA255 processor is returned to the JTAG controller using this pin.	Hi-Z	Hi-Z
TMS	IC	**JTAG test mode select.** (input) Selects the test mode required from the JTAG controller. This pin has an internal pull-up resistor.	Input	Input
TCK	IC	**JTAG test clock.** (input) Clock for all transfers on the JTAG test interface.	Input	Input
TEST	IC	**Test Mode.** (input) Reserved. Must be grounded.	Input	Input
TESTCLK	IC	**Test Clock.** (input) Reserved. Must be grounded.	Input	Input
Power and Ground Pins				
VCC	SUP	**Positive supply for internal logic.** Must be connected to the low voltage supply on the PCB.	Powered	Note [6]
VSS	SUP	**Ground supply for internal logic.** Must be connected to the common ground plane on the PCB.	Grounded	Grounded
PLL_VCC	SUP	**Positive supply for PLLs and oscillators.** Must be connected to the common low voltage supply.	Powered	Note [6]
PLL_VSS	SUP	**Ground supply for the PLL.** Must be connected to common ground plane on the PCB.	Grounded	Grounded
VCCQ	SUP	**Positive supply for all CMOS I/O except memory bus and PCMCIA pins.** Must be connected to the common 3.3v supply on the PCB.	Powered	Note [7]
VSSQ	SUP	**Ground supply for all CMOS I/O except memory bus and PCMCIA pins.** Must be connected to the common ground plane on the PCB.	Grounded	Grounded
VCCN	SUP	**Positive supply for memory bus and PCMCIA pins.** Must be connected to the common 3.3v or 2.5v supply on the PCB.	Powered	Note [7]
VSSN	SUP	**Ground supply for memory bus and PCMCIA pins.** Must be connected to the common ground plane on the PCB.	Grounded	Grounded

Table 4. Pin Description Notes

Note	Description
[1]	GPIO reset operation: Configured as GPIO inputs by default after any reset. The input buffers for these pins are disabled to prevent current drain and the pins are pulled high with 10K to 60K internal resistors. The input paths must be enabled and the pullups turned off by clearing the read-disable-hold (RDH) bit described in Section 3.5.7, “Power Manager Sleep Status Register (PSSR)” on page 3-27 in the *Intel® PXA255 Processor Developers Manual*. Even though sleep mode sets the RDH bit, the pull-up resistors are not re-enabled by sleep mode.
[2]	Crystal oscillator pins: These pins connect the external crystals to the on-chip oscillators. Refer to Section 3.3.1, “32.768 kHz Oscillator” on page 3-4 in the *Intel® PXA255 Processor Developers Manual* and Section 3.3.2, “3.6864 MHz Oscillator” on page 3-4 of the *Intel® PXA255 Processor Developers Manual* for details on sleep-mode operation.
[3]	GPIO sleep operation: The state of these pins is determined by the corresponding PGSRn during the transition into sleep mode. See Section 3.5.9, “Power Manager GPIO Sleep State Registers (PGSR0, PGSR1, PGSR2)” and Section 4.1.3.2, “GPIO Pin Direction Registers (GPDR0, GPDR1, GPDR2)” on page 4-8 in the *Intel® PXA255 Processor Developers Manual*. If selected as an input, this pin does not drive during sleep. If selected as an output, the value contained in the sleep-state register is driven out onto the pin and held there while the PXA255 processor is in sleep mode. GPIOs configured as inputs after exiting sleep mode cannot be used until PSSR[RDH] is cleared.
[4]	Static memory control pins: During sleep mode, these pins can be programmed to either drive the value in the sleep-state register or be placed in Hi-Z. To select the Hi-Z state, software must set the FS bit in the power-manager general-configuration register. If PCFR[FS] is not set, then during the transition to sleep these pins function as described in [3], above. For nWE, nOE, and nCS[0], if PCFR[FS] is not set, they are driven high by the memory controller before entering sleep. If PCFR[FS] is set, these pins are placed in Hi-Z.
[5]	PCMCIA control pins: During sleep mode: can be programmed either to drive the value in the sleep-state register or be placed in Hi-Z. To select the Hi-Z state, software must set PCFR[FP]. If it is not set, then during the transition to sleep these pins function as described in [3], above.
[6]	During sleep, this supply may be driven low. This supply must never be high impedance.
[7]	Remains powered in sleep mode.

Figure 2. PXA255 processor

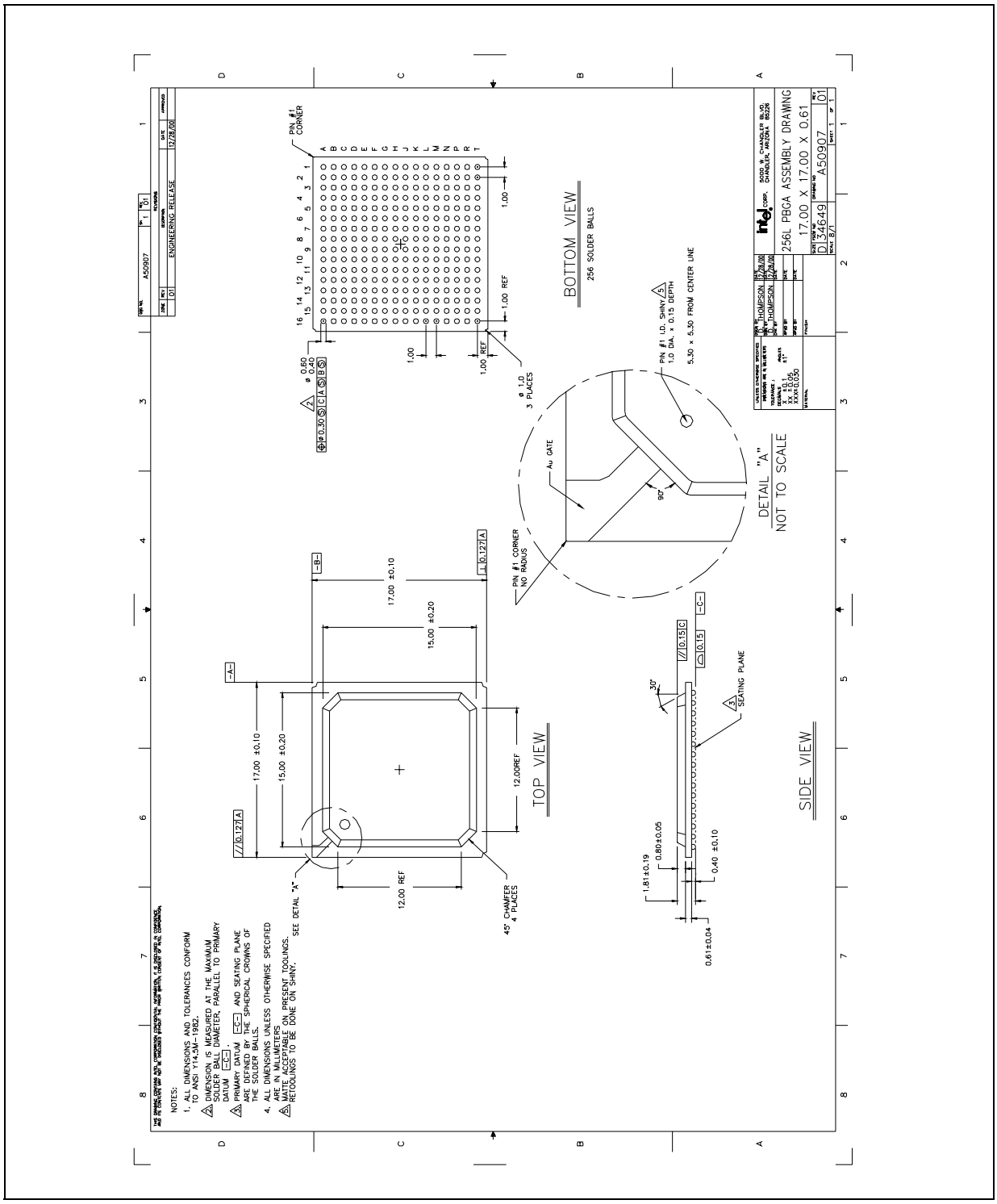


Table 5. PXA255 processor 256-Lead 17x17mm mBGA Pinout — Ballpad No. Order (Sheet 1 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	VCCN	C10	VCCQ	F3	nSDCAS
A2	L_DD[13]/GPIO[71]	C11	VSSQ	F4	VCCN
A3	L_DD[12]/GPIO[70]	C12	USB_P	F5	SDCLK[1]
A4	L_DD[11]/GPIO[69]	C13	VCCQ	F6	VSSQ
A5	L_DD[9]/GPIO[67]	C14	VSSQ	F7	GPIO[10]
A6	L_DD[7]/GPIO[65]	C15	IRTXD/GPIO[47]	F8	FFRTS/GPIO[41]
A7	GPIO[11]	C16	VSS	F9	SSPSCLK/GPIO[23]
A8	L_BIAS/GPIO[77]	D1	SDCLK[2]	F10	FFDTR/GPIO[40]
A9	SSPRXD/GPIO[26]	D2	SDCLK[0]	F11	VCC
A10	SDATA_OUT/GPIO[30]	D3	RDnWR	F12	GPIO[9]
A11	SDA	D4	VCCN	F13	BOOT_SEL[2]
A12	FFDCD/GPIO[36]	D5	L_DD[10]/GPIO[68]	F14	GPIO[8]
A13	FFRXD/GPIO[34]	D6	L_DD[5]/GPIO[63]	F15	VSSQ
A14	FFCTS/GPIO[35]	D7	L_DD[1]/GPIO[59]	F16	NSSPSCLK/GPIO[81]
A15	BTCTS/GPIO[44]	D8	L_LCLK/GPIO[75]	G1	MA[0]
A16	SDATA_IN1/GPIO[32]	D9	SSPTXD/GPIO[25]	G2	VSSN
B1	DQM[1]	D10	nACRESET	G3	nSDCS[2]
B2	DQM[2]	D11	SCL	G4	nWE
B3	L_DD[15]/GPIO[73]	D12	PWM[1]/GPIO[17]	G5	nOE
B4	GPIO[14]	D13	BTTXD/GPIO[43]	G6	nSDCS[1]
B5	GPIO[13]	D14	MMCMD	G7	VCC
B6	GPIO[12]	D15	VCCQ	G8	VSSQ
B7	L_DD[3]/GPIO[61]	D16	NSSPRXD/GPIO[84]	G9	VCC
B8	L_PCLK/GPIO[76]	E1	nSDRAS	G10	VSSQ
B9	SSPEXTCLK/GPIO[27]	E2	VSSN	G11	TESTCLK
B10	FFRI/GPIO[38]	E3	SDCKE[1]	G12	TEST
B11	FFDSR/GPIO[37]	E4	SDCKE[0]	G13	BOOT_SEL[1]
B12	USB_N	E5	L_DD[6]/GPIO[64]	G14	VCCQ
B13	BTRXD/GPIO[42]	E6	L_DD[4]/GPIO[62]	G15	GPIO[7]
B14	BTRTS/GPIO[45]	E7	L_DD[[0]/GPIO[58]	G16	BOOT_SEL[0]
B15	IRRXD/GPIO[46]	E8	L_FCLK/GPIO[74]	H1	MA[2]
B16	MMDAT	E9	SSPSFRM/GPIO[24]	H2	MA[1]
C1	RDY/GPIO[18]	E10	SDATA_IN0/GPIO[29]	H3	MD[16]
C2	VSSN	E11	SYNC/GPIO[31]	H4	VCCN
C3	L_DD[14]/GPIO[72]	E12	PWM[0]/GPIO[16]	H5	MD[17]
C4	VSSQ	E13	FFTXD/GPIO[39]	H6	MA[3]

Table 5. PXA255 processor 256-Lead 17x17mm mBGA Pinout — Ballpad No. Order (Sheet 2 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
C5	L_DD[8]/GPIO[66]	E14	VCCQ	H7	VSSQ
C6	VCCQ	E15	NSSPTXD/GPIO[83]	H8	VSS
C7	L_DD[2]/GPIO[60]	E16	NSSPSFRM/GPIO[82]	H9	VSS
C8	VSSQ	F1	nSDCS[0]	H10	VCC
C9	BITCLK/GPIO[28]	F2	nSDCS[3]	H11	nTRST
H12	TCK	L9	VCC	P6	MD[24]
H13	TMS	L10	GPIO[0]	P7	MD[26]
H14	GPIO[6]	L11	PWR_EN	P8	MD[27]
H15	TDI	L12	GPIO[1]	P9	nCS[2]/GPIO[78]
H16	TDO	L13	GPIO[2]	P10	MD[29]
J1	MA[7]	L14	VSSQ	P11	MD[12]
J2	VSSN	L15	TEXTAL	P12	MD[31]
J3	MA[6]	L16	TXTAL	P13	nPOE/GPIO[48]
J4	MD[18]	M1	MA[14]	P14	nPCE[1]/GPIO[52]
J5	MA[5]	M2	MD[21]	P15	VSSN
J6	MA[4]	M3	MA[15]	P16	nPSKTSEL/GPIO[54]
J7	VCC	M4	VCCN	R1	MA[18]
J8	VSS	M5	MD[1]	R2	VSSN
J9	VSS	M6	MD[6]	R3	MA[20]
J10	VSSQ	M7	MD[7]	R4	VSSN
J11	GPIO[5]	M8	DQM[0]	R5	MA[22]
J12	GPIO[4]	M9	MD[8]	R6	VSSN
J13	nRESET	M10	MD[15]	R7	MD[25]
J14	VSSQ	M11	VCCQ	R8	VSSN
J15	PLL_VCC	M12	GPIO[22]	R9	MD[10]
J16	PLL_VSS	M13	nPREG/GPIO[55]	R10	VSSN
K1	MA[8]	M14	VCCN	R11	MD[30]
K2	MA[9]	M15	VSSN	R12	VSSN
K3	MD[19]	M16	nIOIS16/GPIO[57]	R13	nCS[4]/GPIO[80]
K4	VCCN	N1	MD[22]	R14	VSSN
K5	MA[10]	N2	VSSN	R15	nPIOW/GPIO[51]
K6	MA[11]	N3	MA[16]	R16	nPCE[2]/GPIO[53]
K7	VSSQ	N4	MD[0]	T1	VSS
K8	VCC	N5	VCCN	T2	VCCN
K9	VSSQ	N6	MD[4]	T3	MD[23]
K10	VCC	N7	VCCN	T4	MA[21]
K11	nRESET_OUT	N8	nCS[0]	T5	MA[24]

Table 5. PXA255 processor 256-Lead 17x17mm mBGA Pinout — Ballpad No. Order (Sheet 3 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
K12	nBATT_FAULT	N9	VCCN	T6	MD[3]
K13	nVDD_FAULT	N10	MD[13]	T7	MD[5]
K14	GPIO[3]	N11	VCCN	T8	nCS[1]/GPIO[15]
K15	PXTAL	N12	DREQ[0]/GPIO[20]	T9	nCS[3]/GPIO[79]
K16	PEXTAL	N13	VCCN	T10	MD[9]
L1	MA[12]	N14	DREQ[1]/GPIO[19]	T11	MD[11]
L2	VSSN	N15	GPIO[21]	T12	MD[14]
L3	MA[13]	N16	nPWAIT/GPIO[56]	T13	nCS[5]/GPIO[33]
L4	MD[20]	P1	MA[17]	T14	nPWE/GPIO[49]
L5	MD[2]	P2	MA[19]	T15	nPIOR/GPIO[50]
L6	VCC	P3	VCCN	T16	VCCN
L7	DQM[3]	P4	MA[25]		
L8	MD[28]	P5	MA[23]		

3.2 Package Power Ratings

Table 6. θ_{JA} and Maximum Power Ratings

Processor	θ_{JA}	Max Power
PXA255	33 C°/w	1.4W

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

This section provides the absolute maximum ratings for the processors. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 7. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
TS	Storage Temperature	-40	125	°C
VSS_O	Offset Voltage between any two VSS pins (VSS, VSSQ, VSSN)	-0.3	0.3	V
VCC_O	Offset Voltage between any of the following pins: VCCQ and VCCN	-0.3	0.3	V
VCC_HV	Voltage Applied to High Voltage Supplies (VCCQ, VCCN)	VSS-0.3	VSS+4.0	V
VCC_LV	Voltage Applied to Low Voltage Supplies (VCC, PLL_VCC)	VSS-0.3	VSS+1.65	V
VIP	Voltage Applied to non-Supply pins except XTAL pins	VSS-0.3	max of VCCQ+0.3, VSS+4.0	V
VIP_X	Voltage Applied to XTAL pins (PXTAL, PEXTAL, TXTAL, TEXTAL)	VSS-0.3	max of VCC+0.3, VSS+1.65	V
VESD	Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V
IEOS	Maximum DC Input Current (Electrical Overstress) for any non-supply pin		5	mA

4.2 Power Consumption Specifications

Power consumption depends on the operating voltage, peripherals enabled, external switching activity, and external loading.

Specifying maximum power consumption requires all units to be run at their maximum performance, and at maximum voltage and loading conditions. The maximum power consumption of the PXA255 processor is calculated using these conditions:

- All peripheral units operating at maximum frequency and size configuration
- All I/O loads maximum (50 pF)
- Core operating at worst-case power scenario (hit rates adjusted for worst power)
- All voltages at maximum of range. Maximum range for the core voltage is set to maintain compatibility with the PXA250.
- Maximum case temperature

Do not exceed the maximum package power rating or T_{case} temperature.

Since few systems operate at maximum loading, performance, and voltage, a more optimal system design requires more typical power-consumption figures. These figures are important when considering battery size and optimizing regulator efficiency. Typical systems operate with fewer modules active and at nominal voltage and load. The typical power consumption for the PXA255 processor is calculated using these conditions:

- SSP, STUART, USB, PWM, Timer, I2S peripherals operating

- LCD enabled with 320x240x16-bit color
- MMC, AC97, BTUART, FFUART, ICP, I2C peripherals disabled
- I/O loads at nominal (35 pf for all pins)
- Core operating at 98% instruction hit rate, 95% data hit rate, run mode
- All voltages at nominal values
- Nominal case temperature

Table 8 contains power consumption numbers for the PXA255 processor.

Table 8. Power Consumption Specifications for PXA255 processor (Sheet 1 of 2)

Symbol	Description	Typical	Maximum	Units
400 MHz active mode, Maximum: V_{cc}=1.65V, V_{ccq}/V_{ccn}=3.6V, Temp=100° C Typical: V_{cc}=1.3V, V_{ccq}/V_{ccn}=3.3V, Temp=Room				
I_{ccc}	V_{cc} Current	245	800	mA
I_{ccp}	V_{ccq} and V_{ccn} Current	28	355	mA
P_{TOTAL}	Total Power	411	2598	mW
300 MHz active mode, Maximum: V_{cc}=1.43V, V_{ccq}/V_{ccn}=3.6V, Temp=100° C Typical: V_{cc}=1.1V, V_{ccq}/V_{ccn}=3.3V, Temp=Room				
I_{ccc}	V_{cc} Current	185	570	mA
I_{ccp}	V_{ccq} and V_{ccn} Current	24	345	mA
P_{TOTAL}	Total Power	283	2057	mW
200 MHz active mode, Maximum: V_{cc}=1.32V, V_{ccq}/V_{ccn}=3.6V, Temp=100° C Typical: V_{cc}=1.0V, V_{ccq}/V_{ccn}=3.3V, Temp=Room				
I_{ccc}	V_{cc} Current	115	340	mA
I_{ccp}	V_{ccq} and V_{ccn} Current	19	330	mA
P_{TOTAL}	Total Power	178	1637	mW
400 MHz idle mode, Maximum: V_{cc}=1.65V, V_{ccq}/V_{ccn}=3.6V, Temp=100° C Typical: V_{cc}=1.3V, V_{ccq}/V_{ccn}=3.3V, Temp=Room				
I_{ccc}	V_{cc} Current	95	460	mA
I_{ccp}	V_{ccq} and V_{ccn} Current	9	50	mA
P_{TOTAL}	Total Power	121	939	mW
300 MHz idle mode, Maximum: V_{cc}=1.43V, V_{ccq}/V_{ccn}=3.6V, Temp=100° C Typical: V_{cc}=1.1V, V_{ccq}/V_{ccn}=3.3V, Temp=Room				
I_{ccc}	V_{cc} Current	43	335	mA
I_{ccp}	V_{ccq} and V_{ccn} Current	9	50	mA
P_{TOTAL}	Total Power	77	659	mW
200 MHz idle mode, Maximum: V_{cc}=1.32V, V_{ccq}/V_{ccn}=3.6V, Temp=100° C Typical: V_{cc}=1.0V, V_{ccq}/V_{ccn}=3.3V, Temp=Room				
I_{ccc}	V_{cc} Current	33	205	mA
I_{ccp}	V_{ccq} and V_{ccn} Current	9	50	mA
P_{TOTAL}	Total Power	63	451	mW
33 MHz idle mode, Maximum: V_{cc}=1.32V, V_{ccq}/V_{ccn}=3.6V, Temp=100° C Typical: V_{cc}=1.0V, V_{ccq}/V_{ccn}=3.3V, Temp=Room				

Table 8. Power Consumption Specifications for PXA255 processor (Sheet 2 of 2)

Symbol	Description	Typical	Maximum	Units
I_{ccc}	V_{cc} Current	15	70	mA
I_{ccp}	V_{ccq} and V_{ccn} Current	9	50	mA
P_{TOTAL}	Total Power	45	272	mW
Sleep mode, Maximum: V_{cc}=0V, V_{ccq}/V_{ccn}=3.3V, Temp=Room				
I_{ccp}	V_{ccq} and V_{ccn} Current	45	75	µA
Fast sleep wakeup mode, Maximum: V_{cc}=1.0/1.1/1.3V, V_{ccq}/V_{ccn}=3.3V, Temp=Room				
I_{ccc}	V_{cc} Current	-	-	–
I_{ccp}	V_{ccq} and V_{ccn} Current	-	-	-

4.3 Operating Conditions

This section shows voltage, frequency, and temperature specifications for the processor for four different ranges (shown in Table 9, “Voltage, Temperature, and Frequency Electrical Specifications”.) The temperature specification for each range is constant; the frequency range depends on the operation voltage.

Note: The parameters in Table 9 are preliminary and subject to change.

Table 9. Voltage, Temperature, and Frequency Electrical Specifications (Sheet 1 of 2)

Symbol	Description	Min	Typical	Max	Units
T_{case}	Case Temperature - Extended Temp	-40	-	100	°C
T_{case}	Case Temperature - Nominal Temp	0	-	85	°C
VVSS	VSS, VSSN, VSSQ Voltage	-0.3	0	0.3	V
VVCCQ	VCCQ Voltage	3.0	3.3	3.6	V
VVCCN	VCCN Voltage	2.375	2.5/3.3	3.6	V
Low Voltage Range					
VVCC_L	VCC, PLL_VCC Voltage, Low Range	.95	1.00	1.155	V
fTURBO_L	Turbo Mode Frequency, Low Range	99.5		118	MHz
fSDRAM_L	External Synchronous Memory Frequency, Low Range	50		99.5	MHz
Medium Voltage Range					
VVCC_M	VCC, PLL_VCC Voltage, Mid Range	.95	1.00	1.32	V
fTURBO_M	Turbo Mode Frequency, Mid Range	99.5		199.1	MHz
fSDRAM_M	External Synchronous Memory Frequency, Mid Range	50		99.5	MHz
High Voltage Range					
VVCC_H	VCC, PLL_VCC Voltage, High Range	1.045	1.1	1.43	V
fTURBO_H	Turbo Mode Frequency, High Range	99.5		298.7	MHz
fSDRAM_H	External Synchronous Memory Frequency, High Range	50		99.5	MHz

Table 9. Voltage, Temperature, and Frequency Electrical Specifications (Sheet 2 of 2)

Symbol	Description	Min	Typical	Max	Units
Peak Voltage Range					
VVCC_P	VCC, PLL_VCC Voltage, Peak Range	1.235	1.30	1.65	V
fTURBO_P	Turbo Mode Frequency, Peak Range	99.5		398.2	MHz
fSDRAM_P	External Synchronous Memory Frequency, Peak Range	50		99.5	MHz

4.4 Targeted DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. Table 10, "Standard Input, Output, and I/O Pin DC Operating Conditions" shows the DC operating conditions for the high- and low-strength input, output, and I/O pins. All DC specification values are valid for the entire temperature range of the device.

Table 10. Standard Input, Output, and I/O Pin DC Operating Conditions

Symbol	Description	Min	Typical	Max	Units
Input DC Operating Conditions					
VIH	Input High Voltage, all standard input and I/O pins	0.8*VCCQ		VCCQ	V
VIL	Input Low Voltage, all standard input and I/O pins	VSS		0.2*VCCQ	V
IIN	Input Leakage, all standard input and IO pins			10	µA
Output DC Operating Conditions					
VOH	Output High Voltage, all standard output and I/O pins	VCCQ-0.1		VCCQ	V
VOL	Output Low Voltage, all standard output and I/O pins	VSS		VSS+0.4	V
IOH_H	Output High Current, all standard, high-strength output and I/O pins (VO=VOH)	-10			mA
IOH_L	Output High Current, all standard, low-strength output and I/O pins (VO=VOH)	-3			mA
IOL_H	Output Low Current, all standard, high-strength output and I/O pins (VO=VOH)	10			mA
IOL_L	Output Low Current, all standard, low-strength output and I/O pins (VO=VOH)	3			mA

Table 11. Standard Input, Output, I/O Pin DC Operating Conditions for 2.5-V Memory

Symbol	Description	Min	Typ	Max	Units
Input DC Operating Conditions					
Vih	Input High Voltage, all standard input and I/O pins	0.9*VCCN		VCCN	V
Vil	Input Low Voltage, all standard input and I/O pins	VSS		0.1*VCCN	V
Iin	Input Leakage, all standard input and I/O pins	-		10	uA
Output DC Operating Conditions					
Voh	Output High Voltage, all standard output and I/O pins	VCCN-0.3		VCCN	V
Vol	Output Low Voltage, all standard output and I/O pins	VSS		VSS+0.3	V

4.5 Targeted AC Specifications

All the non-analog input, output, and I/O pins on the processor can be divided into one of two categories:

1. High Strength Input, Output, and I/O pins:
   - nCS[5:1] (GP 33, 80, 79, 78, 15 respectively), nCS[0]
   - MD[31:0], MA[25:0]
   - DQM[3:0]
   - nOE, nWE, nSDRAS, nSDCAS, nSDCS[3:0]
   - SDCLK[2:0], SDCKE[1:0]
   - RDnWR, RDY (GP[18])
   - nPWE, nPOE pins (GP[49:48])
   - MMCLK (GP[53]), MMCMD, MMDAT
   - TDO
   - nACRESET
2. Low Strength Input, Output, and I/O pins - all remaining non-supply pins

A pin's AC characteristics include input and output capacitance, which determine loading for external drivers or other load analysis. The AC characteristics also include a de-rating factor, which indicates how much faster or slower the AC timings get with different loads. Table 12, "Standard Input, Output, and I/O Pin AC Operating Conditions" shows the AC operating conditions for the high- and low-strength input, output, and I/O pins. All AC specification values are valid for the entire temperature range of the device.

Table 12. Standard Input, Output, and I/O Pin AC Operating Conditions

Symbol	Description	Min	Typical	Max	Units
CIN	Input capacitance, all standard input and IO pins			10	pF
COUT_H	Output capacitance, all standard high-strength output and IO pins	25[1]		50[1]	pF
tdF_H	Output de-rating, falling edge on all standard, high-strength output and I/O pins, from 50pF load.				ns/pF
tdR_H	Output de-rating, rising edge on all standard, high-strength output and I/O pins, from 50pF load.				ns/pF

NOTE: [1]AC specifications guaranteed for loads in this range. All testing is done at 50pF

4.6 Oscillator Electrical Specifications

The processor contains two oscillators, each for a specific crystal: a 32.768-kHz oscillator and a 3.6864-MHz oscillator. When choosing a crystal, match the crystal parameters as closely as possible.

4.6.1 32.768-kHz Oscillator Specifications

The 32.768-kHz oscillator is connected between the TXTAL (amplifier input) and TEXTAL (amplified output). Table 13, “32.768-kHz Oscillator Specifications” shows the 32.768-kHz specifications.

Table 13. 32.768-kHz Oscillator Specifications

Symbol	Description	Min	Typical	Max	Units
Crystal Specifications - Typical is FOX NC38					
F_{XT}	Crystal Frequency, TXTAL/TEXTAL	—	32.768	—	kHz
ESR	Equivalent series resistance, TXTAL/TEXTAL	6	—	65	kΩ
P	Drive Level	—	—	1	uW
Amplifier Specifications					
VIH_X	Input High Voltage, TXTAL	0.8*VCC		VCC	V
VIL_X	Input Low Voltage, TXTAL	VSS		0.2*VCC	V
IIN_XT	Input Leakage, TXTAL			1	µA
CIN_XT	Input Capacitance, TXTAL/TEXTAL		18	25	pF
tS_XT	Stabilization Time	2	-	10	s
Board Specifications					
RP_XT	Parasitic Resistance, TXTAL/TEXTAL to any node	20			MΩ
CP_XT	Parasitic Capacitance, TXTAL/TEXTAL, total			5	pF
COP_XT	Parasitic Shunt Capacitance, TXTAL to TEXTAL			0.4	pF

To drive the 32.768-kHz crystal pins from an external source

- Drive the TEXTAL pin with a digital signal that has a low level near 0 volts and a high level near VCC. Do not exceed VCC or go below VSS by more than 100 mV. The minimum slew rate is 1 volt per 1 µs. The maximum current sourced by the external clock source when the clock is at its maximum positive voltage should be approximately 1 mA.
- Float the TXTAL pin or drive it complementary to the TEXTAL pin, with the same voltage level, slew rate, and input current restrictions.

4.6.2 3.6864 MHz Oscillator Specifications

The 3.6864-MHz oscillator is connected between the PXTAL (amplifier input) and PEXTAL (amplified output). Table 14 shows the 3.6864-MHz specifications.

Table 14. 3.6864-MHz Oscillator Specifications

Symbol	Description	Min	Typical	Max	Units
Crystal Specifications - Typical is FOX HC49S					
F_{XP}	Crystal Frequency, PXTAL/PEXTAL	—	3.6864	—	MHz
ESR	Equivalent series resistance, PXTAL/PEXTAL	50	-	300	Ω
P	Drive Level	—	—	100	uW
Amplifier Specifications					
VIH_X	Input High Voltage, PXTAL	0.8*VCC		VCC	V
VIL_X	Input Low Voltage, PXTAL	VSS		0.2*VCC	V
IIN_XP	Input Leakage, PXTAL			10	µA
CIN_XP	Input Capacitance, PXTAL/PEXTAL		40	50	pF
tS_XP	Stabilization Time	17.8		67.8	ms
Board Specifications					
RP_XP	Parasitic Resistance, PXTAL/PEXTAL to any node	20			MΩ
CP_XP	Parasitic Capacitance, PXTAL/PEXTAL, total			5	pF
COP_XP	Parasitic Shunt Capacitance, PXTAL to PEXTAL			0.4	pF

To drive the 3.6864-MHz crystal pins from an external source

- Drive the PEXTAL pin with a digital signal with a low level near 0 volts and a high level near VCC. Do not exceed VCC or go below VSS by more than 100 mV. The minimum slew rate is 1 volt / 100 ns. The maximum current sourced by the external clock source when the clock is at its maximum positive voltage should be approximately 1 mA.
- Float the PXTAL pin or drive it complementary to the PXTAL pin, with the same voltage level, slew rate, and input current restrictions. If floated, some degree of noise susceptibility will be introduced in the system; therefore, it is not recommended.

Note: The minimum duty cycle for an external signal driven into PEXTAL is 40/60.

4.7 Reset and Power AC Timing Specifications

The processor asserts the nRESET_OUT pin in one of several different modes:

- Power on
- Hardware reset
- Watchdog reset
- GPIO reset
- Sleep mode

The following sections provide the timing and specifications for the entry and exit of these modes.

4.7.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operation. Figure 3, “Power-On Reset Timing” on page 31, shows this sequence and is detailed in Table 15, “Power-On Timing Specifications” on page 31.

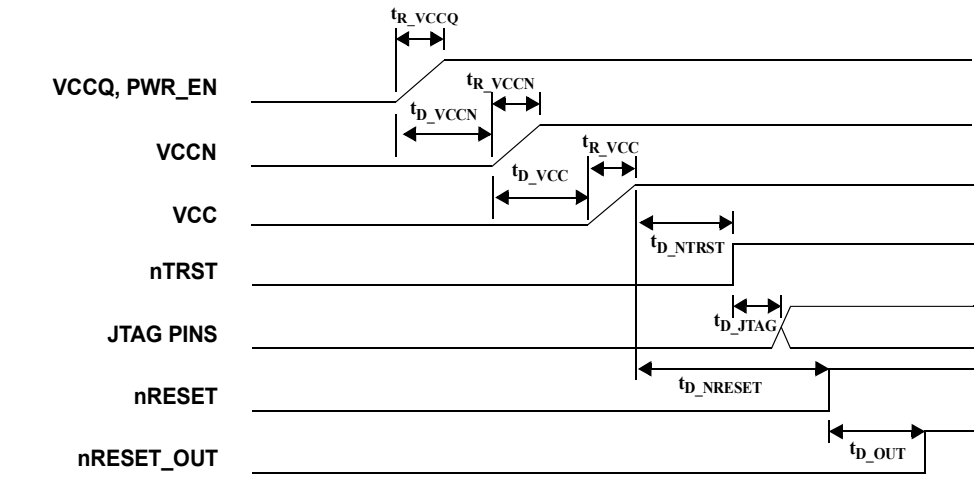
On the processor, it is important that the power supplies be powered up in a certain order to avoid high current situations. The required order is:

1. VCCQ
2. VCCN
3. VCC and PLL_VCC

On the processor, it is important that the VCCQ power supply be powered up before or at the same time as the VCCN power supply. The VCC and PLL_VCC power supplies may be powered up anytime within the specification shown in Figure 3 and Table 15.

Note: If hardware reset is entered during sleep mode, follow the proper power-supply stabilization times indicated in Figure 3 and nRESET timing requirements indicated in Table 15.

Figure 3. Power-On Reset Timing



NOTES:
1. nBATT_FAULT and nVDD_FAULT must be high before nRESET_OUT is deasserted or the processor enters sleep mode.
2. The inclusion of PWR_EN is for informational purposes only to show its relationship to VCCQ. The use of PWR_EN to bring up VCCN or VCC at power-on reset is optional depending on the system's power management requirements. VCCN and VCC are not dependant on the PWR_EN signal being asserted.

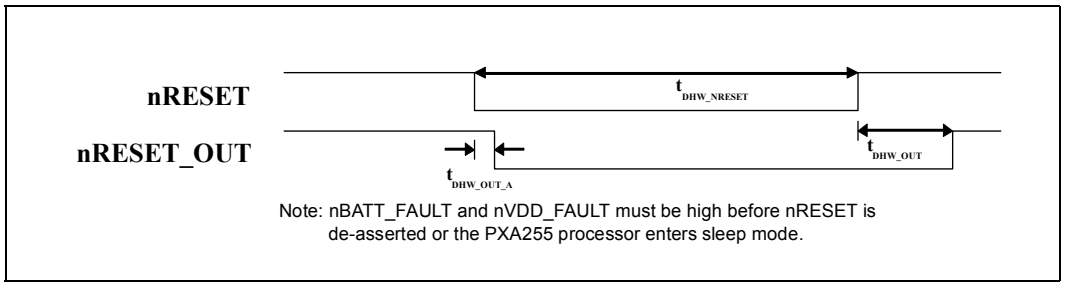
Table 15. Power-On Timing Specifications

Symbol	Description	Min	Typical	Max	Units
tR_VCCQ	VCCQ rise / stabilization time	0.01	—	100	ms
tR_VCCN	VCCN rise / stabilization time	0.01	—	100	ms
tR_VCC	VCC, PLL_VCC rise / stabilization time	0.01	—	10	ms
tD_VCCN	Delay between VCCQ applied and VCCN applied	0	—	—	ms
tD_VCC	Delay from VCCN applied and VCC, PLL_VCC applied	-10	—	—	ms
tD_NTRST	Delay between VCC, PLL_VCC stable and nTRST de-asserted	10	—	—	ms
tD_JTAG	Delay between nTRST de-asserted and JTAG pins active, with nRESET asserted	0.03	—	—	ms
tD_NRESET	Delay between VCC, PLL_VCC stable and nRESET de-asserted	10	—	—	ms
tD_OUT	Delay between nRESET de-asserted and nRESET_OUT de--asserted	18.1	—	18.2	ms
tD_NCS0	Delay between nRESET_OUT deasserted and nCS0 asserted	400	—	420	ns

4.7.2 Hardware Reset Timing

The timing sequences shown in hardware reset timing for hardware reset assumes stable power supplies at the assertion of nRESET. If the power supplies are unstable, follow the timings indicated in Section 4.7.1, “Power-On Timing” on page 30.

Figure 4. Hardware Reset Timing



Note: nBATT_FAULT and nVDD_FAULT must be high before nRESET is de-asserted or the PXA255 processor enters sleep mode.

Table 16. Hardware Reset Timing Specifications

Symbol	Description	Min	Typical	Max	Units
tDHW_NRESET	Minimum assertion time of nRESET	0.001			ms
tDHW_OUT_A	Delay between nRESET asserted and nRESET_OUT asserted	0		0.001	ms
tDHW_OUT	Delay between nRESET de-asserted and nRESET_OUT de-asserted	18.1		18.2	ms
tDHW_NCS0	Delay between nReset_Out de-asserted and nCS0 asserted	400	—	420	ns

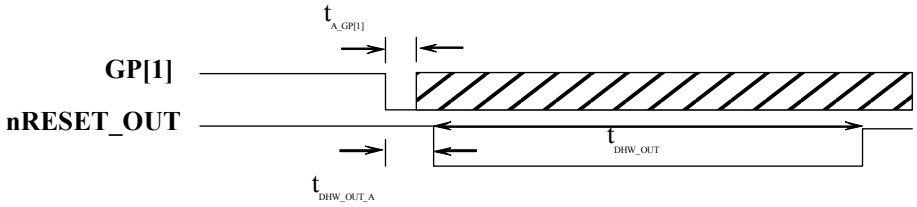
4.7.3 Watchdog Reset Timing

Watchdog reset is an internally generated reset and therefore has no external pin dependencies. The nRESET_OUT pin is the only indicator of watchdog reset, and it stays asserted for t_{DHW_OUT}. Refer to Figure 4, “Hardware Reset Timing” on page 32.

4.7.4 GPIO Reset Timing

GPIO reset is generated externally, and the source is reconfigured as a standard GPIO as soon as the reset propagates internally. The clocks module is not reset by GPIO reset, so the timing varies based on the frequency of clock selected, and if the clocks and power manager is in the frequency change sequence when GPIO reset is asserted (see Section 4.6.1, “32.768-kHz Oscillator Specifications” on page 28.) Figure 5, “GPIO Reset Timing” on page 33 shows the possible timing of GPIO reset.

Figure 5. GPIO Reset Timing



Note: nBATT_FAULT and nVDD_FAULT must be high before nRESET is deasserted or the application processor will enter Sleep Mode

Table 17. GPIO Reset Timing Specifications

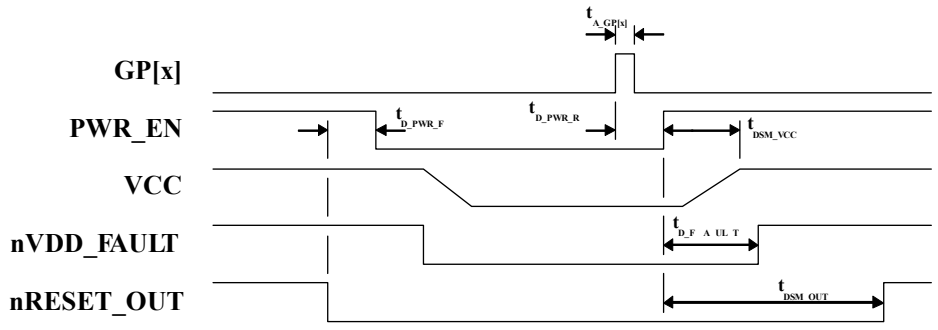
Symbol	Description	Min	Typical	Max	Units
tA_GP[1]	Minimum assert time of GP[1][1] in 3.6864MHz input clock cycles	4			cycles
tDHW_OUT_A	Delay between GP[1] asserted and nRESET_OUT asserted in 3.6864 MHz input clock cycles	3		8	cycles
tDHW_OUT	Delay between nRESET_OUT asserted and nRESET_OUT de-asserted, run or turbo mode[2]	1.28		6.5	µs
tDHW_OUT_F	Delay between nRESET_OUT asserted and nRESET_OUT de-asserted, during frequency change sequence[3]	1.28		360	µs
tDHW_NCS0	Delay between nReset_Out de-asserted and nCS0 asserted	150.69	—	390	ns

NOTES:
1. GP[1] is not recognized as a reset source again until configured to do so in software. Software should check the state of GP[1] before configuring as a reset to ensure no spurious reset is generated.
2. Time is 512*N processor clock cycles plus up to 4 cycles of the 3.6864-MHz input clock.
3. Time during the frequency change sequence depends on the state of the PLL lock detector at the assertion of GPIO reset. The lock detector has a maximum time of 350µs plus synchronization.

4.7.5 Sleep Mode Timing

Sleep mode is asserted internally; and asserts the nRESET_OUT and PWR_EN signals. The sequence indicated in Figure 6, “Sleep Mode Timing” on page 34 and detailed in Figure 18, “Sleep Mode Timing Specifications” on page 34 is the required timing parameters for sleep mode.

Figure 6. Sleep Mode Timing



Note: nBATT_FAULT must be high or the PXA255 processor will not exit sleep mode.

Table 18. Sleep Mode Timing Specifications

Symbol	Description	Min	Typical	Max	Units
tA_GP[x}	Assert time of GPIO wake-up source (x=[15:0])	91.6	—	—	µs
tD_PWR_F	Delay from nRESET_OUT asserted to PWR_EN de-asserted	61	—	91.6	µs
tD_PWR_R	Delay between GP[x] asserted to PWR_EN asserted	30.5	—	122.1	µs
tDSM_VCC	Delay between PWR_EN asserted and VCC stable		—	10	ms
tD_FAULT	Delay between PWR_EN asserted and nVDD_FAULT de-asserted		—	10	ms
tDSM_OUT	Delay between PWR_EN asserted and nRESET_OUT de-asserted, OPDE set	28.0	—	28.5	ms
tDSM_OUT_F	Delay between PWR_EN asserted and nRESET_OUT de-asserted, FWAKE set	—	—	650	µs
tDSM_OUT_O	Delay between PWR_EN asserted and nRESET_OUT de-asserted, OPDE clear	10.35	—	10.5	ms
t_{DSM_NCS0}	Delay between nReset_Out de-asserted and nCS0 asserted	180.84	—	332	ns

NOTE: For the parameter t_{DSM_VCC}, VCC refers to the VCC supply internal to the processor. The internal VCC regulator must be stable within the stated maximum for the processor to function correctly. Factors such as external voltage regulator ramp time and bulk capacitance will affect the ramp time of the internal regulator and must be taken into account when designing the system.

4.8 Memory Bus and PCMCIA AC Specifications

This section provides the timing information for these types of memory:

- SRAM / ROM / Flash / Synchronous Fast Flash Asynchronous writes (Table 19, "SRAM / ROM / Flash / Synchronous Fast Flash AC Specifications" on page 35)
- Variable latency I/O (Table 20, "Variable Latency I/O Interface AC Specifications" on page 35)
- Card interface (PCMCIA or Compact Flash) (Table 21, "Card Interface (PCMCIA or Compact Flash) AC Specifications" on page 36)
- Synchronous memories (Table 22, "Synchronous Memory Interface AC Specifications 1" on page 36)

Table 19. SRAM / ROM / Flash / Synchronous Fast Flash AC Specifications

Symbol	Description	MEMCLKs
tromAS	MA(25:0) setup to nCS, nOE, nSDCAS (as nADV) asserted	1
tromAH	MA(25:0) hold after nCS, nOE, nSDCAS (as nADV) de-asserted	1
tromASW	MA(25:0) setup to nWE asserted	3
tromAHW	MA(25:0) hold after nWE de-asserted	1
tromCES	nCS setup to nWE asserted	2
tromCEH	nCS hold after nWE de-asserted	1
tromDS	MD(31:0), DQM(3:0) write data setup to nWE asserted	1
tromDSWH	MD(31:0), DQM(3:0) write data setup to nWE de-asserted	2
tromDH	MD(31:0), DQM(3:0) write data hold after nWE de-asserted	1
tromNWE	nWE high time between beats of write data	2

Table 20. Variable Latency I/O Interface AC Specifications

Symbol	Description	MEMCLKs
tvlioAS	MA(25:0) setubp to nCS asserted	1
tvlioASRW	MA(25:0) setup to nOE or nPWE asserted	1
tvlioAH	MA(25:0) hold after nOE or nPWE de-asserted	1
tvlioCES	nCS setup to nOE or nPWE asserted	2
tvlioCEH	nCS hold after nOE or nPWE de-asserted	1
tvlioDSW	MD(31:0), DQM(3:0) write data setup to nPWE asserted	1
tvlioDSWH	MD(31:0), DQM(3:0) write data setup to nPWE de-asserted	2
tvlioDHW	MD(31:0), DQM(3:0) hold after nPWE de-asserted	1
tvlioDHR	MD(31:0) read data hold after nOE de-asserted	0
tvlioRDYH	RDY hold after nOE, nPWE de-asserted	0
tvlioNPWE	nPWE, nOE high time between beats of write or read data	2

Table 21. Card Interface (PCMCIA or Compact Flash) AC Specifications

Symbol	Description	MEMCLKs
tcardAS	MA(25:0), nPREG, PSKTSEL, nPCE setup to nPWE, nPOE, nPIOW, or nPIOR asserted	2
tcardAH	MA(25:0), nPREG, PSKTSEL, nPCE hold after nPWE, nPOE, nPIOW, or nPIOR de-asserted	2
tcardDS	MD(31:0) setup to nPWE, nPOE, nPIOW, or nPIOR asserted	2
tcardDH	MD(31:0) hold after nPWE, nPOE, nPIOW, or nPIOR de-asserted	2
tcardCMD	nPWE, nPOE, nPIOW, or nPIOR command assertion	2

NOTE: These numbers are minimums. They can be much longer based on the programmable card interface timing registers.

Table 22. Synchronous Memory Interface AC Specifications [1]

Symbol	Description	MIN	MAX	Units, Notes
SDRAM / SMROM / SDRAM-Timing Synchronous Flash (Synchronous)				
tsynCLK	SDCLK period	10	20	ns, 2
tsynCMD	nSDCAS, nSDRAS, nWE, nSDCS assert time	1		sdclk
tsynRCD	nSDRAS to nSDCAS assert time	1		sdclk
tsynCAS	nSDCAS to nSDCAS assert time	2		sdclk
tsynSDOS	MA(25:0), MD(31:0), DQM(3:0), nSDCS(3:0), nSDRAS, nSDCAS, nWE, nOE, SDCKE(1:0), RDnWR output setup time to SDCLK(2:0) rise	3.8		ns, 3
tsynSDOH	MA(25:0), MD(31:0), DQM(3:0), nSDCS(3:0), nSDRAS, nSDCAS, nWE, nOE, SDCKE(1:0), RDnWR output hold time from SDCLK(2:0) rise	3.6		ns, 3
tsynSDIS	MD(31:0) read data input setup time from SDCLK(2:0) rise	0.5		ns
tsynDIH	MD(31:0) read data input hold time from SDCLK(2:0) rise	1.5		ns
Fast Flash (Synchronous READS only)				
tffCLK	SDCLK period	15	20	ns, 4
tffAS	MA(25:0) setup to nSDCAS (as nADV) asserted	0.5		sdclk
tffCES	nCS setup to nSDCAS (as nADV) asserted	0.5		sdclk
tffADV	nSDCAS (as nADV) pulse width	1		sdclk
tffOS	nSDCAS (as nADV) de-assertion to nOE assertion	3		sdclk
tffCEH	nOE deassertion to nCS de-assertion	4		sdclk

NOTES:
1. These numbers are for a maximum 99.5 MHz MEMCLK and 99.5 MHz output SDCLK.
2. SDCLK for SDRAM, SMROM, and SDRAM-timing Synchronous Flash can be at the slowest, divide-by-2 of the 99.5 MHz MEMCLK. It can be 99.5 MHz at the fastest.
3. This number represents 1/2 SDCLK period.
4. SDCLK for Fast Flash can be at the slowest, divide-by-2 of the 99.5 MHz MEMCLK. It can be divide-by-2 of the 132.7 MHz MEMCLK at its fastest.

4.9 Peripheral Module AC Specifications

This section describes the AC specifications for the LCD and SSP peripheral units.

4.9.1 LCD Module AC Timing

Figure 7 describes the LCD timing parameters. The LCD pin timing specifications are referenced to the pixel clock (L_PCLK). Values for the parameters are given in Table 23.

Figure 7. LCD AC Timing Definitions

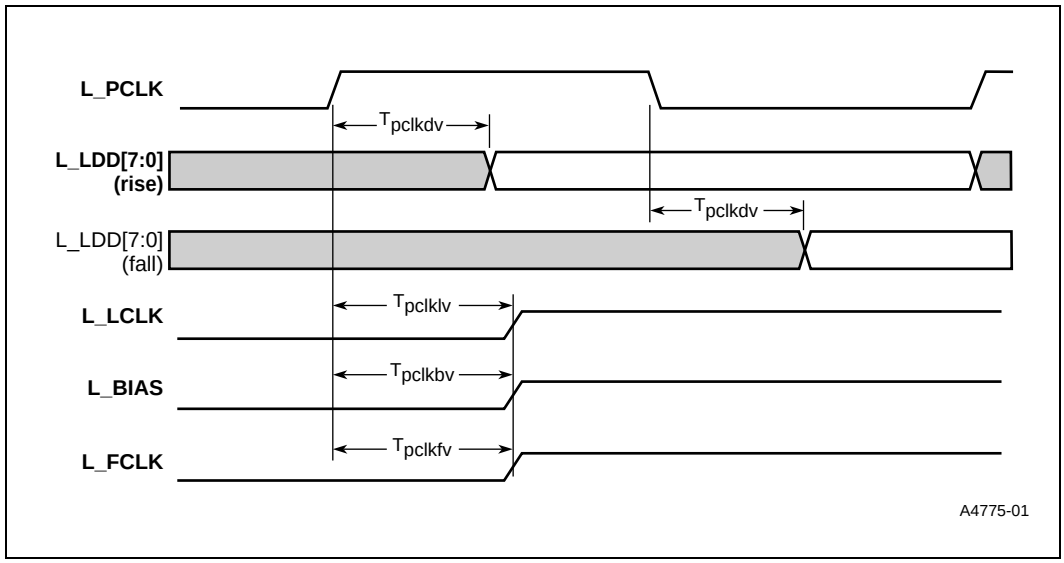


Table 23. LCD AC Timing Specifications

Symbol	Description	Min	Max	Units	Notes
Tpclkdv	Tpclkdv L_PCLK rise/fall to L_LDD<7:0> driven valid	0	3.5	ns	1
Tpclklv	L_PCLK fall to L_LCLK driven valid	-0.5	2.0	ns	2
Tpclkfv	L_PCLK fall to L_FCLK driven valid	-0.5	2.0	ns	2
Tpclkbv	L_PCLK rise to L_BIAS driven valid	5.524	12	ns	2

NOTES:
1. Program the LCD data pins to be driven on either the rising or falling edge of the pixel clock (L_PCLK).
2. These LCD signals can, at times, transition when L_PCLK is not clocking (between frames). At this time, they are clocked with the internal version of the pixel clock before it is driven out onto the L_PCLK pin.

4.9.2 SSP Module AC Timing

Figure 8, “SSP AC Timing Definitions” on page 38 describes the SSP timing parameters. The SSP pin timing specifications are referenced to SCLK_C. Values for the parameters are given in Table 24, “SSP AC Timing Specifications” on page 38.

Figure 8. SSP AC Timing Definitions

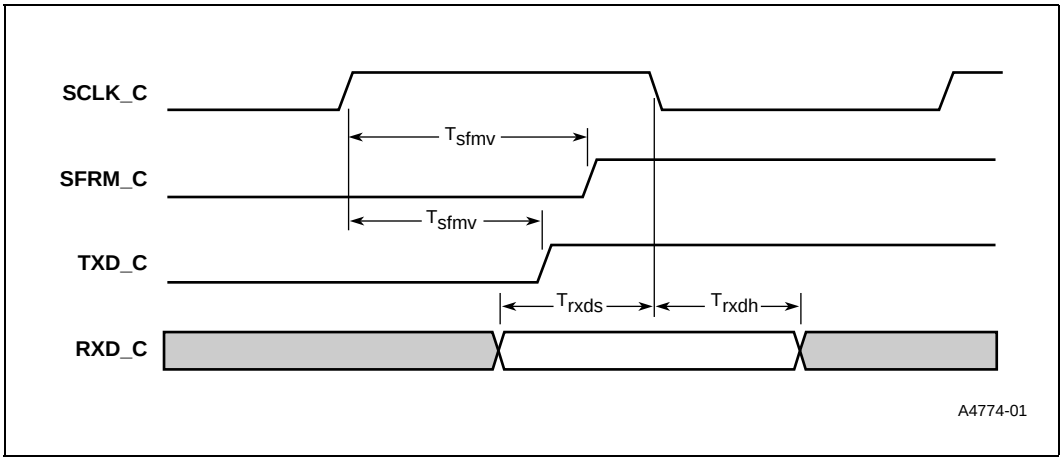


Table 24. SSP AC Timing Specifications

Symbol	Description	Min	Max	Units	Notes
Tsfmv	SCLK_C rise to SFRM_C driven valid		21	ns	
Trxds	RXD_C valid to SCLK_C fall (input setup)	11		ns	
Trxdh	SCLK_C fall to RXD_C invalid (input hold)	0		ns	
Tsfmv	SCLK_C rise to TXD_C valid		22	ns	

4.9.3 Boundary Scan Test Signal Timings

Table 25, “Boundary Scan Test Signal Timing” shows the boundary scan test signal timing.

Table 25. Boundary Scan Test Signal Timing (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
TBSF	TCK frequency	0.0	33.33	MHz	
TBSCH	TCK high time	15.0		ns	Measured at 1.5 V
TBSCL	TCK low time	15.0		ns	Measured at 1.5 V
TBSCR	TCK rise time		5.0	ns	0.8 V to 2.0 V
TBSCF	TCK fall time		5.0	ns	2.0 V to 0.8 V
TBSIS1	Input setup to TCK TDI, TMS	4.0		ns	
TBSIH1	Input hold from TCK TDI, TMS	6.0		ns	
TBSIS2	Input setup to TCK nTRST	25.0		ns	
TBSIH2	Input hold from TCK nTRST	3.0		ns	
TBSOV1	TDO valid delay	1.5	6.9	ns	Relative to falling edge of TCK
TOF1	TDO float delay	1.1	5.4	ns	Relative to falling edge of TCK
TOV12	All outputs (non-test) valid delay	1.5	6.9	ns	Relative to falling edge of TCK

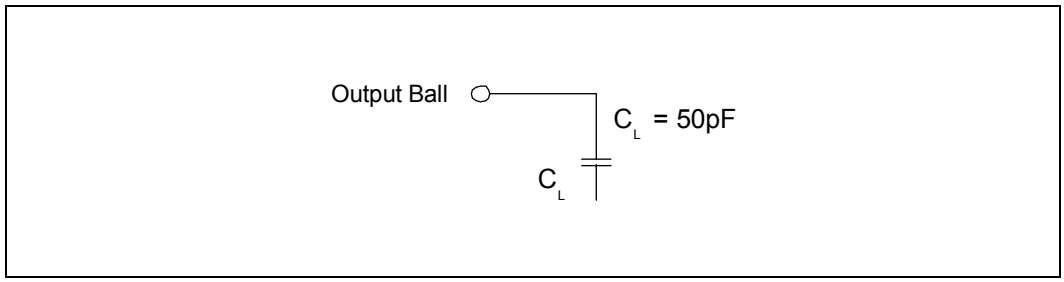
Table 25. Boundary Scan Test Signal Timing (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
TOF2	All outputs (non-test) float delay	1.1	5.4	ns	Relative to falling edge of TCK
TIS10	Input setup to TCK all inputs (non-test)	4.0		ns	
TIH8	Input hold from TCK all inputs (non-test)	6.0		ns	

4.10 AC Test Conditions

The AC specifications in Section 4.5, "Targeted AC Specifications" on page 27 are tested with a 50 pF load indicated in Figure 9.

Figure 9. AC Test Load

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