THE DATASHEET OF

GC80303-SL57T

Intel® 80303 I/O Processor

- *66 MHz PCI-to-PCI Bridge*
- *100 MHz SDRAM and Internal Bus*
- *Complies with PCI Local Bus Specification, Revision 2.2*
- *Universal (5 V and 3.3 V) PCI Signaling Environment*

Datasheet

Product Features

- High Performance 100 MHz Intel® 80960JT Core
  - — Sustained One Instruction/Clock Execution
  - — 16 Kbyte, 2-Way Set-Associative Instruction Cache
  - — 4 Kbyte, Direct-Mapped Data Cache
  - — Sixteen 32-Bit Global Registers
  - — Sixteen 32-Bit Local Registers
  - — 1 Kbyte, Internal Data RAM
  - — Local Register Cache (Eight Available Stack Frames)
  - — Two 32-Bit On-Chip Timer Units
- PCI-to-PCI Bridge Unit
  - — Primary and Secondary 66 MHz/64-bit PCI Interfaces
  - — Eight Delayed Read/Write Buffers and Two Posting Buffers
  - — Six Secondary PCI Output Clocks
  - — Forwards Memory, I/O, Configuration Commands from PCI Bus to PCI Bus
- Memory Controller
  - — 100 MHz SDRAM Support
  - — 512 Mbytes of 64-Bit SDRAM
  - — Four SDRAM Output Clocks
  - — ECC Single-Bit error correction, Double-Bit error detection
  - — Two Independent Banks for SRAM / ROM / Flash (8 Mbyte/Bank; 8-Bit)
- Two Address Translation Units
  - — Connects Internal Bus to 64-bit PCI Buses
  - — I/O Address Translation Support
  - — Direct Outbound Addressing Support
- DMA Controller
  - — Three Independent Channels
  - — PCI Memory Controller Interface
  - — 64-Bit Internal and PCI Bus Addressing
  - — Independent Interface to 66 MHz/64-bit Primary and Secondary PCI Buses
  - — 528 Mbyte/sec Burst Transfers to PCI and SDRAM Memory
  - — Direct Addressing to/from PCI Buses
  - — Unaligned Transfers Supported in Hardware
  - — Two Channels Dedicated to Primary PCI Bus
  - — One Channel Dedicated to Secondary PCI Bus
- I^2C Bus Interface Unit
  - — Serial Bus
  - — Master/Slave Capabilities
  - — System Management Functions
- Secondary PCI Arbitration Unit
  - — Supports Six Secondary PCI Devices
  - — Multi-priority Arbitration Algorithm
- Private PCI Device Support
- 540 Ball - Plastic Ball Grid Array (H-PBGA)
- I_2O Messaging Unit
- Application Accelerator
  - — Built-in hardware XOR engine
  - — 512 or 1 Kbyte Queue
- Performance Monitoring
  - — Ninety-eight Events Monitored On-Chip
- Eight General Purpose I/O Pins

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June, 2002

Datasheet

Contents

Figures

Tables

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1.0 About This Document

This is the datasheet for the Intel® 80303 I/O processor. This datasheet contains a functional overview, mechanical data (package signal locations and simulated thermal characteristics), targeted electrical specifications (simulated), and bus functional waveforms. Detailed functional descriptions other than parametric performance is published in the *Intel® 80303 I/O Processor Developer's Manual* .

1.1 Intel® Solutions960® Program

The Intel® Solutions960® program features a wide variety of development tools which support the Intel® i960® processor family. Many of these tools are developed by partner companies; some are developed by Intel, such as profile-driven optimizing compilers. For more information on these products, contact your local Intel representative.

1.2 Terminology

In this document, the following terms are used:

- Primary and Secondary PCI buses are the 80303 I/O processor external PCI buses, which conform to PCI SIG specifications.
- Intel® 80960 core refers to the Intel® 80960JT processor which is integrated into the 80303 I/O processor.

1.3 Additional Information Sources

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

Intel Corporation
Literature Sales
P.O. Box 5937
Denver, CO 80217-9808
1-800-548-4725

Table 1. Related Documentation

Document Title	Order / Contact
Intel® 80303 I/O Processor Developer's Manual	Intel Order #273353
80303 Specification Updates	Intel Order #273355
i960® Jx Microprocessor Developer's Manual	Intel Order #272483
PCI Local Bus Specification Revision 2.2	PCI Special Interest Group 1-800-433-5177 www.pcisig.com
PCI-to-PCI Bridge Architecture Specification, Revision 1.1	PCI Special Interest Group 1-800-433-5177 www.pcisig.com
PCI System Design Guide Revision 1.0	PCI Special Interest Group 1-800-433-5177 www.pcisig.com
PCI Hot-Plug Specification Revision 1.0	PCI Special Interest Group 1-800-433-5177 www.pcisig.com
PCI Bus Power Management Interface Specification, Revision 1.1	PCI Special Interest Group 1-800-433-5177 www.pcisig.com
I^2C Peripherals for Microcontrollers	Philips Semiconductor
Advanced Configuration and Power Interface Specification, Revision 1.0 (ACPI)	www.teleport.com/~acpi

NOTE: Also see our product website at: developer.intel.com/design/iio.

2.0 Functional Overview

As indicated in Figure 1, the 80303 I/O processor combines many features with the 80960JT to create an intelligent I/O processor. Subsections following the figure briefly describe the main features; for detailed functional descriptions, refer to the *Intel® 80303 I/O Processor Developer's Manual* .

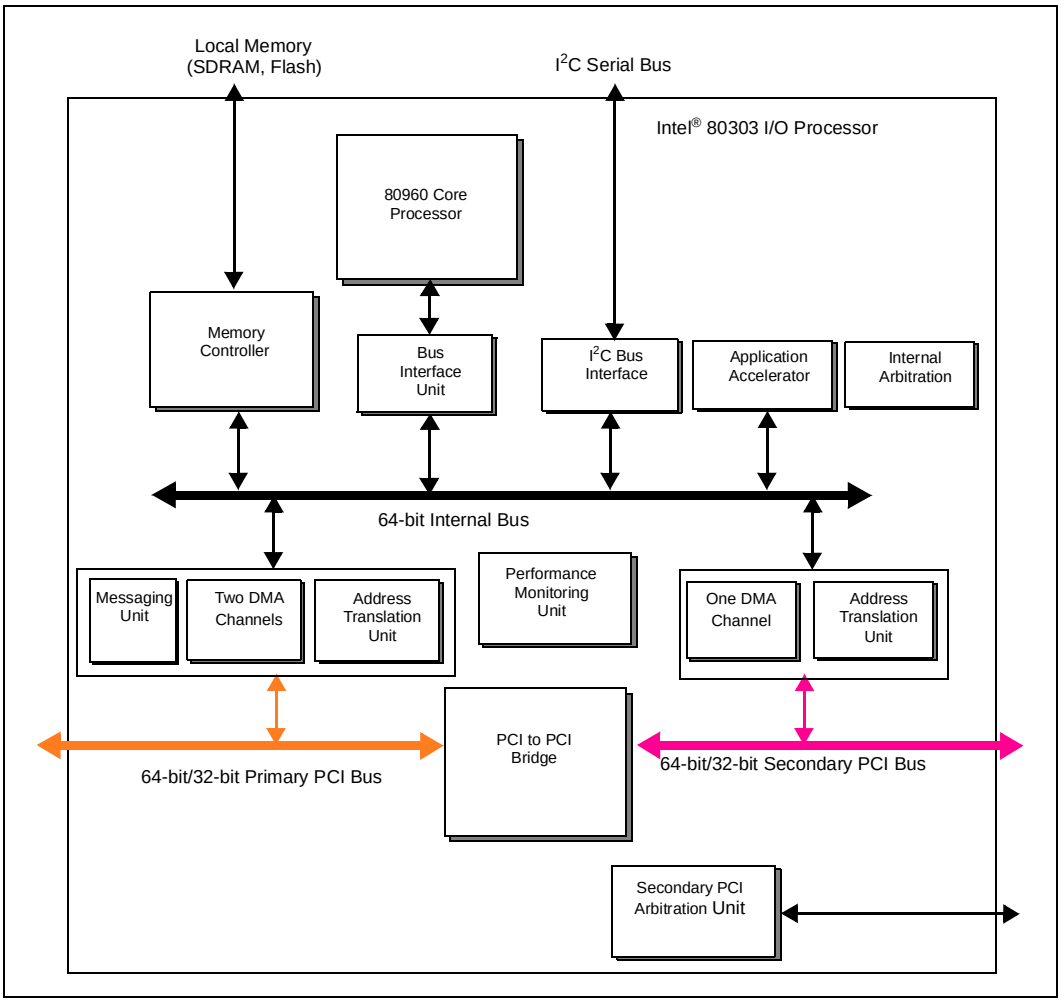
The PCI bus is an industry standard, high performance, low latency system bus that operates up to 528 Mbyte/s. The 80303 I/O processor, a multi-function PCI device, is fully compliant with the *PCI Local Bus Specification* Revision 2.2. Function 0 is the PCI-to-PCI bridge unit; Function 1 is the address translation unit.

The PCI-to-PCI bridge unit is the path between two independent 64-bit PCI buses and provides the ability to overcome PCI electrical load limits. The addition of the Intel® i960® core processor brings intelligence to the bridge.

The 80303 I/O processor, object code compatible with the i960 core processor, is capable of sustained execution at the rate of one instruction per clock.

The internal bus, a 64-bit PCI-like bus, is a high-speed interface to local memory and I/O. Physical and logical memory attributes are programmed via memory-mapped control registers (MMRs); an extension not found on the Intel® i960® Kx, Sx or Cx processors.

Figure 1. Functional Block Diagram



2.1 Key Functional Units

2.1.1 PCI-to-PCI Bridge Unit

The PCI-to-PCI bridge unit (referred to as “bridge”) connects two independent PCI buses. Each PCI bus may be 32 or 64 bits wide. The bridge is fully compliant with the *PCI-to-PCI Bridge Architecture Specification*, Revision 1.1 published by the PCI Special Interest Group. The bridge forwards bus transactions on one PCI bus to the other PCI bus. Dedicated data queues support high performance bandwidth on the PCI buses. The Intel® 80303 I/O Processor supports PCI 64-bit Dual Address Cycle (DAC) addressing.

The bridge has dedicated PCI configuration space accessible through the primary PCI bus. The bridge also supports the power management extended capability configuration header as defined by the *PCI Bus Power Management Interface Specification*, Revision 1.1. Compliance to this specification provides the hardware support required by the software initiative defined by the *Advanced Configuration and Power Interface Specification*, Revision 1.0 (ACPI).

2.1.2 Private PCI Device Support

The 80303 I/O processor explicitly supports private PCI devices on the secondary PCI bus. The bridge and Address Translation Unit work together to hide private PCI devices from PCI configuration cycles and allow these hidden devices to use a private PCI address space. The Address Translation Unit issues PCI configuration cycles to configure hidden devices.

2.1.3 DMA Controller

The DMA Controller supports low-latency, high-throughput data transfers between PCI bus agents and local memory. Three separate DMA channels accommodate data transfers: two for primary PCI bus, one for the secondary PCI bus. The DMA Controller supports chaining and unaligned data transfers. The DMA Controller is programmable only through the i960 core processor.

2.1.4 Address Translation Unit

The Address Translation Unit (ATU) allows PCI transactions direct access to the 80303 I/O processor local memory. The ATU supports transactions between PCI address space and 80303 I/O processor address space. Address translation is controlled through programmable registers accessible from both the PCI interface and the i960 core processor. Dual access to registers allows flexibility in mapping the two address spaces. The ATU also supports the power management extended capability configuration header that is defined by the *PCI Bus Power Management Interface Specification*, Revision 1.1.

2.1.5 Messaging Unit

The Messaging Unit (MU) provides data transfer between the PCI system and the 80303 I/O processor. The Messaging Unit uses interrupts to notify the PCI system or the 80303 I/O processor when new data arrives. The MU has four messaging mechanisms: Message Registers, Doorbell Registers, Circular Queues, and Index Registers. Each mechanism allows a host processor or external PCI device and the 80303 I/O processor to communicate through message passing and interrupt generation.

2.1.6 Memory Controller Unit

The Memory Controller Unit (MCU) allows direct control of a local SDRAM and Flash subsystem. The MCU features programmable chip selects, a wait state generator and Error Correction and Detection. With the ATU configuration registers, local memory can be configured as PCI addressable memory or private processor memory.

2.1.7 I^2C Bus Interface Unit

The I^2C (Inter-Integrated Circuit) Bus Interface Unit allows the 80960 core to serve as a master and slave device residing on the I^2C bus. The I^2C bus is a serial bus developed by Philips Semiconductor comprising a two pin interface. The bus allows the 80303 I/O processor to interface to other I^2C peripherals and microcontrollers for system management functions. It requires a minimum of hardware for an economical system to relay status and reliability information on the I/O subsystem to an external device. For more information, see *I^2C Peripherals for Microcontrollers* (Philips Semiconductor).

2.1.8 Secondary PCI Arbitration Unit

The Secondary PCI Arbitration Unit provides PCI arbitration for the secondary PCI bus. The arbitration includes a fairness algorithm with programmable priorities and six external PCI Request and Grant signal pairs.

2.1.9 Application Accelerator Unit

The Application Accelerator Unit (AAU) provides hardware acceleration of XOR functions commonly used in RAID algorithms. Additionally; the AAU provides block moves within local memory, interfaces the internal bus and operates on data within local memory and, is programmable through the i960 core processor and supports chaining and unaligned data transfers.

2.1.10 Performance Monitor Unit

The Performance Monitor Unit (PMU) allows software to monitor the performance of the different buses: Primary PCI, Secondary PCI, and Internal. Multiple performance characteristics are captured with 14 mode registers and a global time stamp register.

2.1.11 Bus Interface Unit

The Bus Interface Unit (BIU) provides an interface between the 100 MHz 80960JT core and the 100 MHz internal bus. To optimize performance, the BIU implements prefetching and write merging.

2.2 Intel® i960® Core Features (Intel® 80960JT)

The processing power of the 80303 I/O processor comes from the 100 MHz 80960JT processor core. The 80960JT is a scalar implementation of the 80960 Core Architecture. Figure 2 shows a block diagram of the 80960JT Core processor.

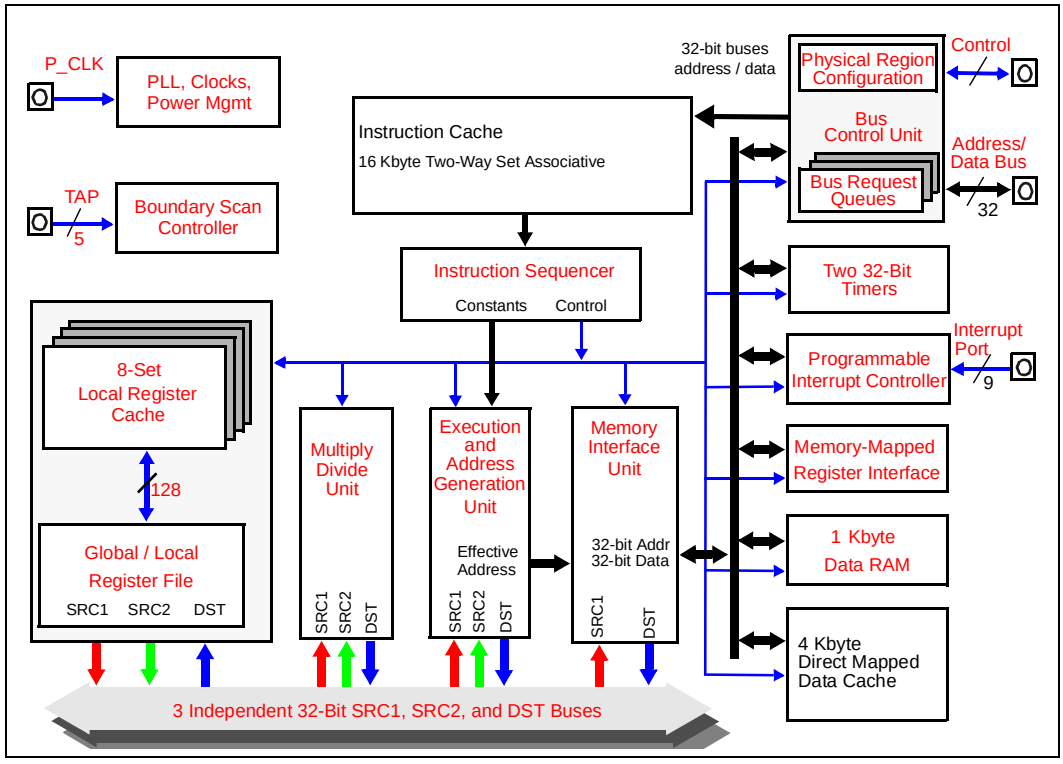
Factors that contribute to the 80960JT core's performance include:

- 100 MHz Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- Efficient instruction pipeline minimizes pipeline break latency
- Register and resource scoreboarding allow overlapped instruction execution
- 128-bit register bus speeds local register caching
- 16 Kbyte two-way set-associative, integrated instruction cache
- 4 Kbyte direct-mapped, integrated data cache
- 1 Kbyte integrated data RAM delivers zero wait state program data

The 80960 core operates out of its own 32-bit address space, which is independent of the PCI address space. Local memory can be:

- Made visible to the PCI address space
- Kept private to the 80960JT core
- Allocated as a combination of the two

Figure 2. Intel® 80960JT Core Block Diagram



2.2.1 Burst Bus

A 32-bit high-performance bus controller interfaces the 80303 I/O processor to the Bus Interface Unit. The Bus Control Unit fetches instructions and transfers data on the internal bus at the rate of up to four 32-bit words per six clock cycles. The external address/data bus is multiplexed.

Data caching is programmed through a group of logical memory templates and a defaults register. The Bus Control Unit's features include:

- Multiplexed external bus minimizes pin count.
- External ready control for address-to-data, data-to-data and data-to-next-address wait state types.
- Little endian byte ordering.
- Unaligned bus accesses performed transparently.
- Three-deep load/store queue decouples the bus from the 80960 core.

Upon reset, the 80960JT conducts an internal self test. Before executing its first instruction, it performs an external bus confidence test by performing a checksum on the first words of the Initialization Boot Record.

2.2.2 Timer Unit

The Timer Unit (TU) contains two independent 32-bit timers that are capable of counting at several clock rates and generating interrupts. Each is programmed through the Timer Unit registers. These memory-mapped registers are addressable on 32-bit boundaries. The timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the 80960JT interrupt controller. The TU can generate a fault when unauthorized writes from user mode are detected.

2.2.3 Priority Interrupt Controller

Low interrupt latency is critical to many embedded applications. As part of its highly flexible interrupt mechanism, the 80960JT exploits several techniques to minimize latency:

- Interrupt vectors and interrupt handler routines can be reserved on-chip
- Register frames for high-priority interrupt handlers can be cached on-chip
- The interrupt stack can be placed in cacheable memory space

2.2.4 Faults and Debugging

The 80960JT employs a comprehensive fault model. The processor responds to faults by making implicit calls to a fault handling routine. Specific information collected for each fault allows the fault handler to diagnose exceptions and recover appropriately.

The processor also has built-in debug capabilities. With software, the 80960JT may be configured to detect as many as seven different trace event types. Alternatively, **mark** and **fmark** instructions can generate trace events explicitly in the instruction stream. Hardware breakpoint registers are also available to trap on execution and data addresses.

2.2.5 On-Chip Cache and Data RAM

Memory subsystems often impose substantial wait state penalties. The 80960JT integrates considerable storage resources on-chip to decouple CPU execution from the external bus. The 80960JT includes a 16 Kbyte instruction cache, a 4 Kbyte data cache and 1 Kbyte data RAM.

2.2.6 Local Register Cache

The 80960JT rapidly allocates and deallocates local register sets during context switches. The processor needs to flush a register set to the stack only when it saves more than seven sets to its local register cache.

2.2.7 Test Features

The 80303 I/O processor incorporates numerous features that enhance the user's ability to test both the processor and the system to which it is attached. These features include ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG).

The 80960JT provides testability features compatible with IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std. 1149.1).

One of the boundary scan instructions, HIGHZ, forces the processor to float all its output pins (ONCE mode). ONCE mode can also be initiated at reset without using the boundary scan mechanism.

ONCE mode is useful for board-level testing. This feature allows a mounted 80303 I/O processor to electrically "remove" itself from a circuit board allowing system-level testing where a remote tester can exercise the processor system.

The test logic does not interfere with component or system behavior and ensures that components function correctly and the connections between various components are correct.

The JTAG Boundary Scan feature is an alternative to conventional "bed-of-nails" testing. Boundary Scan can examine connections that might otherwise be inaccessible to a test system.

2.2.8 Memory-Mapped Control Registers

The 80960JT is compliant with 80960 family architecture. Each memory-mapped, 32-bit register is accessed via memory-format instructions. The processor ensures that these accesses do not generate external bus cycles.

2.2.9 Instructions, Data Types and Memory Addressing Modes

As with 80960 family processors, the instruction set supports several different data types and formats:

- Bit
- Bit fields
- Integer (8-, 16-, 32-, 64-bit)
- Ordinal (8-, 16-, 32-, 64-bit unsigned integers)
- Triple word (96 bits)
- Quad word (128 bits)

The 80960JT provides a full set of addressing modes for C and assembly:

- Two Absolute modes
- Five Register Indirect modes
- Index with displacement mode
- IP with displacement mode

Table 2 shows the available 80960JT instructions.

Table 2. Instruction Set

Processor Management	Arithmetic	Logical	Bit, Bit Field and Byte
Flush Local Registers Modify Arithmetic Controls Modify Process Controls Halt System Control Cache Control Interrupt Control	Add Subtract Multiply Divide Remainder Modulo Shift Extended Shift Extended Multiply Extended Divide Add with Carry Subtract with Carry Conditional Add Conditional Subtract Rotate	And Not And And Not Or Exclusive Or Not Or Or Not Nor Exclusive Nor Not Nand	Set Bit Clear Bit Not Bit Alter Bit Scan For Bit Span Over Bit Extract Modify Scan Byte for Equal Byte Swap
Comparison	**Branch**	**Call/Return**	**Fault**
Compare Conditional Compare Compare and Increment Compare and Decrement Test Condition Code Check Bit	Unconditional Branch Conditional Branch Compare and Branch	Call Call Extended Call System Return Branch and Link	Conditional Fault Synchronize Faults
Debug	**Data Movement**	**Atomic**	
Modify Trace Controls Mark Force Mark	Load Store Move Conditional Select Load Address	Atomic Add Atomic Modify	

3.0 Package Information

3.1 Package Introduction

The 80303 I/O processor is offered in a Plastic Ball Grid Array (PBGA) package. This is a perimeter array package with five rows of ball connections in the outer area of the package. See Figure 3 “540-Lead H-PBGA Package Diagram (Top and Side View)” on page 28.

3.1.1 Functional Signal Definitions

This section defines the pins and signals in the following tables:

- Table 3 “Pin Description Nomenclature” on page 18
- Table 4 “Memory Controller Signals” on page 19
- Table 5 “Primary PCI Bus Signals” on page 22
- Table 6 “Secondary PCI Bus Signals” on page 24
- Table 7 “Miscellaneous Signals” on page 26

3.1.1.1 Signal Pin Descriptions

Table 3. Pin Description Nomenclature

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or output
OD	Open Drain pin
-	Pin must be connected as described
N/C	NO CONNECT. Do not make electrical connections to these balls.
5V	Input pin is 5 volt tolerant
Sync(...)	Synchronous. Signal meets timings relative to an input clock. Sync(P) Synchronous to **P_CLK** Sync(S) Synchronous to **R_CLKIN** Sync(D) Synchronous to **DCLKIN** Sync(T) Synchronous to **TCK**
Async	Asynchronous. Inputs may be asynchronous relative to **P_CLK**, **R_CLKIN**, **DCLKIN** or **TCK**. All asynchronous signals are level-sensitive.
Prst(...)	While the **P_RST#** pin is asserted, the pin: Prst(1) Is driven to Vcc Prst(0) Is driven to Vss Prst(X) Is driven to unknown state Prst(H) Is pulled up to Vcc Prst(L) Is pulled down to Vss Prst(Z) Floats Since **P_RST#** is asynchronous, these are asynchronous events.
Srst(...)	While the **S_RST#** pin is asserted, the pin: Srst(1) Is driven to Vcc Srst(0) Is driven to Vss Srst(X) Is driven to unknown state Srst(H) Is pulled up to Vcc Srst(L) Is pulled down to Vss Srst(Z) Floats Note that **S_RST#** is asserted when **P_RST#** is asserted or BCR[6] is set with software.
Irst(...)	While the **I_RST#** pin is asserted, the pin: Irst(1) Is driven to Vcc Irst(0) Is driven to Vss Irst(X) Is driven to unknown state Irst(H) Is pulled up to Vcc Irst(L) Is pulled down to Vss Irst(Z) Floats Note that **I_RST#** is asserted when **P_RST#** is asserted or EBCR[5] is set with software.
Trst(...)	While the **TRST#** pin is asserted, the pin: Trst(Z) Floats
P32(...)	While the Primary PCI Bus is configured as a 32-bit PCI bus by the Primary central resource: P32(H) is pulled up internally to Vcc
S32(...)	While the Secondary PCI Bus is configured as a 32-bit PCI bus with **32BITPCI_EN#**: S32(H) is pulled up internally to Vcc

Table 4. Memory Controller Signals (Sheet 1 of 3)

Name	Count	Type	Description
DCLK[3:0]	4	O	**SDRAM OUTPUT CLOCKS** are used to provide clocks to the external SDRAM memory subsystem.
DCLKOUT	1	O	**SDRAM FEEDBACK CLOCK** must be connected to **DCLKIN** of the 80303 I/O processor and be trace length matched to **DCLK[3:0]**. **DCLKOUT** may not appear to be in sync with **DCLK[3:0]**.
DCLKIN	1	I	**SDRAM INPUT CLOCK** provides feedback for the internal SDRAM memory subsystem PLL and must be connected to **DCLKOUT** of the 80303 I/O processor.
SA[13:0]	14	O Irst(0) Sync(D)	**SDRAM MULTIPLEXED ADDRESS BUS** carries the multiplexed row and column addresses to the SDRAM memory banks. For SA[10], see note 1. SA[13] is for memory configurations that use 256Mbx16 SDRAM devices. Refer to the Memory Controller Unit chapter of the 80303 I/O Processor Developer's Manual for details.
SBA[1:0]	2	O Irst(0) Sync(D)	**SDRAM INTERNAL BANK SELECT** indicates which of the SDRAM internal banks are read or written during the current transaction. See note 1.
SRAS#	1	O Irst(1) Sync(D)	**SDRAM ROW ADDRESS STROBE** indicates the presence of a valid row address on the Multiplexed Address Bus **SA[13:0]**. See note 1.
SCAS#	1	O Irst(1) Sync(D)	**SDRAM COLUMN ADDRESS STROBE** indicates the presence of a valid column address on the Multiplexed Address Bus **SA[13:0]**. See note 1.
SDQM[7:0]	8	O Irst(X) Sync(D)	**SDRAM DATA MASK** controls which of the eight bytes on the data bus should be written or read. When **SDQM[7:0]** asserted, the SDRAM devices do not accept/drive valid data from/to the byte lanes. When **SDQM[7:0]** deasserted, the SDRAM devices accept/drive valid data from/to the byte lanes. See note 1. By convention, **SDQM[1]** masks two x8 SDRAM devices. Functionally, all **SDQM[7:0]** signals are equivalent.
SWE#	1	O Irst(1) Sync(D)	**SDRAM WRITE ENABLE** indicates that the current memory transaction is a write operation. See note 1.
SCE[1:0]#	2	O Irst(1) Sync(D)	**SDRAM CHIP ENABLE** enables the SDRAM devices for a memory access (1 per bank supported). See note 1.
SCKE[1:0]	2	O Irst(0) Sync(D)	**SCKE[1:0]** are the clock enables for the SDRAM memory. Deasserting will place the SDRAM in self-refresh mode. See note 1.
DQ[63:0]	64	I/O Irst(X) Sync(D)	**DATA BUS** carries 64-bit data to and from memory. During a data (T_d) cycle, read or write data is present on one or more contiguous bytes, comprising **DQ[63:56]**, **DQ[55:48]**, **DQ[47:40]**, **DQ[39:32]**, **DQ[31:24]**, **DQ[23:16]**, **DQ[15:8]** and **DQ[7:0]**. During write operations, unused pins are driven to determinate values. See note 1.
SCB[7:0]	8	I/O Irst(X) Sync(D)	**ERROR CORRECTION CODE** carries the 8-bit ECC code to and from memory during data cycles. See note 1.
ROE#	1	O Irst(1) Sync(D)	**ROM OUTPUT ENABLE** specifies, during a T_a cycle, whether the operation is a write (1) or read (0) to the ROM interface. It remains valid during T_d cycles. When **ROE#** is asserted, the data is transferred from the memory on **RAD[16:9]**.

Table 4. Memory Controller Signals (Sheet 2 of 3)

Name	Count	Type	Description
RWE#	1	O Irst(1) Sync(D)	**ROM WRITE ENABLE** indicates the direction data is to be transferred to/from ROM and controls the $\overline{WE}$ input on the ROM device. When **RWE#** is asserted, the data is transferred to the memory on **DQ[7:0]**.
RCE[1:0]#	2	O Irst(1) Sync(D)	**FLASH CHIP ENABLE** enables the Flash devices for a memory access.
RALE	1	O Irst(0) Sync(D)	**ROM ADDRESS LATCH ENABLE** indicates the cycle in which the address on **RAD[16:3]** should be externally latched for the Flash subsystem.
RAD[16:9]	8	I/O 5V Irst(1) Sync(D)	**FLASH ADDRESS/DATA BUS**: During an address (T_a) cycle, **RAD[16:9]** contain Flash address bits [16:9]. During a data cycle (Td), **RAD[16:9]** contain Flash data bits [7:0].
RAD[8]	1	5V Prst(H) Sync(D)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 8 contains a physical word address. **RAD[8]** multiplexes physical address bits [22] with [8]. Refer to the MCU chapter of the *Intel® 80303 I/O Processor Developer's Manual* for details.
RAD[7]	1	5V Prst(H) Sync(D)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 7 contains a physical word address. **RAD[7]** multiplexes physical address bits [21] with [7]. Refer to the MCU chapter of the *Intel® 80303 I/O Processor Developer's Manual* for details.
RAD[6]/ **RST_MODE#** (Config. Pin)	1	I/O 5V Prst(H) Sync(D)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 6 contains a physical word address. **RAD[6]** multiplexes physical address bits [20] with [6]. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *Intel® 80303 I/O Processor Developer's Manual* for details. **RESET MODE** is sampled at Primary PCI bus reset to determine if the 80303 I/O processor is to be held in reset. If asserted, the 80303 I/O processor will be held in reset until the 80960 Processor Reset bit is cleared in the Extended Bridge Control Register.
RAD[5]/ **ONCE#** (Config. Pin)	1	I/O 5V Prst(H) Sync(D)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 5 contains a physical word address. **RAD[5]** multiplexes physical address bits [19] with [5]. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *Intel® 80303 I/O Processor Developer's Manual* for details. **ONCE MODE**: The processor samples this pin during reset. If it is asserted low at the end of reset, the processor enters ONCE Mode. In ONCE mode, the processor stops all clocks and floats all output pins except the TDO and RAD[8:0] pins. The **ONCE#** pin has a weak internal pullup which is active during reset to ensure normal operation if the pin is left unconnected.
RAD[4]/ **STEST** (Config. Pin)	1	I/O 5V Prst(H) Sync(D)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 4 contains a physical word address. **RAD[4]** multiplexes physical address bits [18] with [4]. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *Intel® 80303 I/O Processor Developer's Manual* for details. **SELF TEST** enables or disables the processor's internal self-test feature at initialization. **STEST** is examined at the end of **P_RST#**. When **STEST** is asserted, the processor performs its internal self-test and the external bus confidence test. When **STEST** is deasserted, the processor performs only the external bus confidence test. 0 = Self Test Disabled 1 = Self Test Enabled

Table 4. Memory Controller Signals (Sheet 3 of 3)

Name	Count	Type	Description
RAD[3]/ RETRY (Config. Pin)	1	I/O 5V Prst(H) Sync(D)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 3 contains a physical word address. **RAD[3]** multiplexes physical address bits [17] with [3]. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *Intel® 80303 I/O Processor Developer's Manual* for details. **RETRY** is sampled at Primary PCI bus reset to determine if the Primary PCI interface will be disabled. If high, the Primary PCI interface will disable PCI configuration cycles by signaling a Retry until the Configuration Cycle Retry bit is cleared in the Extended Bridge Control Register. If low, the Primary PCI interface allow configuration cycles to occur.
RAD[2]/ SPMEM# (Config. Pin)	1	I/O 5V Prst(H) Sync(D)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 2 contains a physical word address. Refer to the MCU chapter of the *Intel® 80303 I/O Processor Developer's Manual* for details. **SPECIAL DOWNSTREAM WINDOW ENABLE** If **SPMEM#** is sampled low at the end of reset then a special downstream memory window FEC0_0000h through FECF_FFFFh is opened. This supports an alternate address mechanism to an external Hot-Plug controller.
RAD[1]/ 32BITPCI_EN# (Config. Pin)	1	I/O 5V Prst(H) Sync(D)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 1 contains a physical word address. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *Intel® 80303 I/O Processor Developer's Manual* for details. **32-BIT Secondary PCI Enable** The **32BITPCI_EN#** signal is sampled at Primary PCI Reset to notify the secondary PCI arbiter NOT to generate the 64-bit protocol of the rising edge of the secondary reset for the secondary PCI bus. If **32BITPCI_EN#** is high, the secondary PCI arbiter asserts **S_REQ64#** during **S_RST#**, indicating the secondary PCI bus is a 64-bit bus. If **32BITPCI_EN#** is low, the secondary PCI arbiter does not assert **S_REQ64#** during **S_RST#**, indicating the secondary PCI bus is NOT a 64-bit bus.
RAD[0]	1	5V Prst(H) Sync(D)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 0 contains a physical word address. Refer to the MCU chapter of the *Intel® 80303 I/O Processor Developer's Manual* for details.

NOTE: These pins remain functional for 20 **DCLKIN** periods after **I_RST#** is asserted for a warm boot. The designated Irst() state applies after 20 **DCLKIN** periods after **I_RST#** is asserted. For more details, refer to the MCU Chapter.

Table 5. Primary PCI Bus Signals (Sheet 1 of 2)

Name	Count	Type	Description
P_AD[31:0]	32	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI ADDRESS/DATA** is the multiplexed PCI address and bottom 32 bits of the data bus.
P_AD[63:32]	32	I/O 5V Sync(P) Prst(Z) P32(H)	**PRIMARY PCI DATA** is the upper 32 bits of the primary PCI data bus driven during the data phase.
P_PAR	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS PARITY** is even parity across **P_AD[31:0]** and **P_C/BE[3:0]#**.
P_PAR64	1	I/O 5V Sync(P) Prst(Z) P32(H)	**PRIMARY PCI BUS UPPER DWORD PARITY** is even parity across **P_AD[63:32]** and **P_C/BE[7:4]#**.
P_C/BE[3:0]#	4	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS COMMAND and BYTE ENABLES** are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables for **P_AD[31:0]**.
P_C/BE[7:4]#	4	I/O 5V Sync(P) Prst(Z) P32(H)	**PRIMARY PCI BUS BYTE ENABLES** are as byte enables for **P_AD[63:32]** during the data phase.
P_REQ#	1	O Prst(Z)	**PRIMARY PCI BUS REQUEST** indicates to the primary PCI bus arbiter that the 80303 I/O processor processor desires use of the PCI bus.
P_REQ64#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS REQUEST 64-BIT TRANSFER** indicates the attempt of a 64-bit transaction on the primary PCI bus. If the target is 64-bit capable, the target acknowledges the attempt with the assertion of **P_ACK64#**.
P_GNT#	1	I 5V Sync(P)	**PRIMARY PCI BUS GRANT** indicates that access to the primary PCI bus has been granted.
P_ACK64#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS ACKNOWLEDGE 64-BIT TRANSFER** indicates that the device has positively decoded its address as the target of the current access and the target is willing to transfer data using the full 64-bit data bus.
P_FRAME#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS CYCLE FRAME** is asserted to indicate the beginning and duration of an access.
P_IRDY#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS INITIATOR READY** indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the Address/Data bus. During a read, it indicates the processor is ready to accept the data.
P_TRDY#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS TARGET READY** indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the Address/Data bus. During a write, it indicates the target is ready to accept the data.

Table 5. Primary PCI Bus Signals (Sheet 2 of 2)

Name	Count	Type	Description
P_STOP#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS STOP** indicates a request to stop the current transaction on the primary PCI bus.
P_DEVSEL#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS DEVICE SELECT** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
P_SERR#	1	I/O 5V OD Sync(P) Prst(Z)	**PRIMARY PCI BUS SYSTEM ERROR** is driven for address parity errors on the primary PCI bus.
P_CLK	1	I 5V	**PRIMARY PCI BUS INPUT CLOCK** provides the timing for all primary PCI transactions and is the clock source for most internal 80303 I/O processor units.
P_RST#	1	I 5V Async	**PRIMARY RESET** brings PCI-specific registers, sequencers, and signals to a consistent state. When **P_RST#** is asserted: PCI output signals are driven to a known consistent state. PCI bus interface output signals are three-stated. open drain signals such as **P_SERR#** are floated. **P_RST#** may be asynchronous to **P_CLK** when asserted or deasserted. Although asynchronous, deassertion must be guaranteed to be a clean, bounce-free edge.
P_PERR#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS PARITY ERROR** is asserted when a data parity error occurs during a primary PCI bus transaction.
P_LOCK#	1	I 5V Sync(P)	**PRIMARY PCI BUS LOCK** indicates the need to perform an atomic operation on the primary PCI bus.
P_IDSEL	1	I 5V Sync(P)	**PRIMARY PCI BUS INITIALIZATION DEVICE SELECT** is used to select the 80303 I/O processor during a Configuration Read or Write command on the primary PCI bus.
P_INT[A:D]#	4	O OD Async Prst(Z)	**PRIMARY PCI BUS INTERRUPT** requests an interrupt. The assertion and deassertion of **P_INT[A:D]#** is asynchronous to **P_CLK**. A device asserts its **P_INT[A:D]#** line when requesting attention from its device driver. Once the **P_INT[A:D]#** signal is asserted, it remains asserted until the device driver clears the pending request. **P_INT[A:D]#** Interrupts are level sensitive.
P_M66EN	1	I 5V	**PRIMARY PCI BUS 66 MHz ENABLE** indicates the speed of the primary PCI bus. If this signal is sampled high the PCI bus speed is 66 MHz, if low the bus speed is 33 MHz.

Table 6. Secondary PCI Bus Signals (Sheet 1 of 2)

Name	Count	Type	Description
S_AD[31:0]	32	I/O 5V Sync(S) Srst(0)	**SECONDARY PCI ADDRESS/DATA** is the multiplexed secondary PCI address and lower 32 bits of the data bus.
S_AD[63:32]	32	I/O 5V Sync(S) Srst(Z) S32(H)	**SECONDARY PCI DATA** is the upper 32 bits of the secondary PCI data bus.
S_PAR	1	I/O 5V Sync(S) Srst(0)	**SECONDARY PCI BUS PARITY** is even parity across **S_AD[31:0]** and **S_C/BE[3:0]#**.
S_PAR64	1	I/O 5V Sync(S) Srst(Z) S32(H)	**SECONDARY PCI BUS UPPER DWORD PARITY** is even parity across **S_AD[63:32]** and **S_C/BE[7:4]#**.
S_C/BE[3:0]#	4	I/O 5V Sync(S) Srst(0)	**SECONDARY PCI BUS COMMAND and BYTE ENABLES** are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as the byte enables for **S_AD[31:0]**.
S_C/BE[7:4]#	4	I/O 5V Sync(S) Srst(Z) S32(H)	**SECONDARY PCI BYTE ENABLES** are used as byte enables for **S_AD[63:32]** during secondary PCI data phases.
S_REQ64#	1	I/O 5V Sync(S) Srst(X)	**SECONDARY PCI BUS REQUEST 64-BIT TRANSFER** indicates the attempt of a 64-bit transaction on the secondary PCI bus. If the target is 64-bit capable, the target acknowledges the attempt with the assertion of **S_ACK64#**. Srst(0) when in 64-bit mode Srst(1) when in 32-bit mode
S_ACK64#	1	I/O 5V Sync(S) Srst(Z)	**SECONDARY PCI BUS ACKNOWLEDGE 64-BIT TRANSFER** indicates device has positively decoded its address as target of current access, indicates the target is willing to transfer data using 64 bits.
S_FRAME#	1	I/O 5V Sync(S) Srst(Z)	**SECONDARY PCI BUS CYCLE FRAME** is asserted to indicate the beginning and duration of an access.
S_IRDY#	1	I/O 5V Sync(S) Srst(Z)	**SECONDARY PCI BUS INITIATOR READY** indicates initiating agent ability to complete current data phase of the transaction. During a write, it indicates that valid data is present on the secondary Address/Data bus. During a read, it indicates the processor is ready to accept the data.
S_TRDY#	1	I/O 5V Sync(S) Srst(Z)	**SECONDARY PCI BUS TARGET READY** indicates target agent ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the secondary Address/Data bus. During a write, it indicates the target is ready to accept the data.
S_STOP#	1	I/O 5V Sync(S) Srst(Z)	**SECONDARY PCI BUS STOP** indicates a request to stop the current transaction on the secondary PCI bus.

Table 6. Secondary PCI Bus Signals (Sheet 2 of 2)

Name	Count	Type	Description
S_DEVSEL#	1	I/O 5V Sync(S) Srst(Z)	**SECONDARY PCI BUS DEVICE SELECT** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
S_SERR#	1	I/O 5V OD Sync(S) Srst(Z)	**SECONDARY PCI BUS SYSTEM ERROR** is driven for address parity errors on the secondary PCI bus.
S_RST#	1	O Async Prst(0)	**SECONDARY PCI BUS RESET** is an output based on **P_RST#**. It brings PCI-specific registers, sequencers, and signals to a consistent state. When **P_RST#** is asserted or BCR[6] is set, it causes **S_RST#** to assert and: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • open drain signals such as **S_SERR#** are floated **S_RST#** may be asynchronous to **R_CLKIN** when asserted or deasserted. Although asynchronous, deassertion must be guaranteed to be a clean, bounce-free edge.
S_PERR#	1	I/O 5V Sync(S) Srst(Z)	**SECONDARY PCI BUS PARITY ERROR** is asserted when a data parity error during a secondary PCI bus transaction.
S_LOCK#	1	I/O 5V Sync(S) Srst(Z)	**SECONDARY PCI BUS LOCK** indicates the need to perform an atomic operation on the secondary PCI bus.
S_CLK[5:0]	6	O	**SECONDARY PCI BUS OUTPUT CLOCKS** are used to drive external logic on the secondary PCI bus.
S_M66EN	1	I/O 5V Srst(X)	**SECONDARY PCI BUS 66 MHz ENABLE** indicates the speed of the secondary PCI bus. If this signal is high the bus speed is 66 MHz and if it is low the bus speed is 33 MHz. Srst(0) when P_M66EN is low Srst(1) when P_M66EN is high
S_HOLDA#	1	O OD Prst(Z)	**SECONDARY PCI BUS HOLD ACKNOWLEDGE.** This output pin, indicates to an external secondary PCI device, that it can now acquire the bus. It will function similar to a secondary PCI bus grant pin, except when S_HOLDA# is asserted all other secondary PCI bus activity is halted.
S_HOLD#	1	I 5V	**SECONDARY PCI BUS HOLD.** This input pin will handle requests from an external secondary PCI device to acquire the bus. It will function similar to a secondary PCI bus request pin, except when S_HOLDA# is asserted all other secondary PCI bus activity is halted.
S_REQ[5:0]#	6	I 5V Sync(S)	**SECONDARY PCI BUS REQUESTS** are the request signals from devices 0 through 5 on the secondary PCI bus.
S_GNT[5:0]#	6	O Sync(S) Srst(Z)	**SECONDARY PCI BUS GRANT** are grant signals sent to devices 5-0 on the secondary PCI bus

Table 7. Miscellaneous Signals (Sheet 1 of 2)

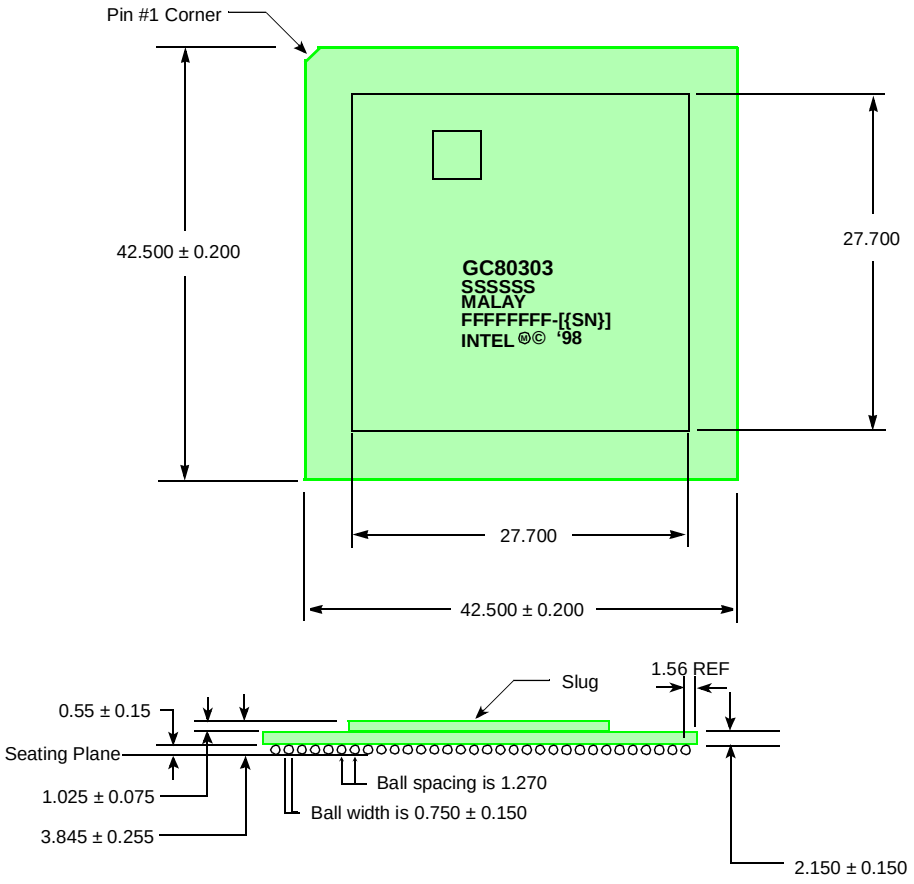
Name	Count	Type	Description
GPIO[7:0] (Config. Pin)	8	I/O 5V Async Prst(H)	**GENERAL PURPOSE INPUT/OUTPUT**. These pins can be selected on a per pin basis as general purpose inputs or outputs. If the pin is sampled low at the end of reset it will become a general purpose output.
FAIL#	1	O Irst(0)	**FAIL** indicates a failure of the processor's built-in self-test performed during initialization. **FAIL#** is asserted immediately upon reset and toggles during self-test to indicate the status of individual tests: When self-test passes, the processor deasserts **FAIL#** and commences operation from user code. When self-test fails, the processor asserts **FAIL#** and then stops executing. Self-test failing does not cause the bridge to stop execution. 0 = Self Test Failed 1 = Self Test Passed
I_RST#	1	O Async	**INTERNAL BUS RESET** indicates when the internal bus has been reset with **P_RST#** or a software reset.
XINT[3:0]#/ S_INT[D:A]#	4	I 5V Async	**SECONDARY PCI BUS INTERRUPT REQUESTS. S_INT[D:A]#** assertion and deassertion is asynchronous to **R_CLKIN**. A device asserts **S_INT[D:A]#** when requesting attention from it device driver. When **S_INT[D:A]#** is asserted, it remains asserted until the device driver clears the pending request. **S_INT[D:A]#** interrupts are level low sensitive. **EXTERNAL INTERRUPT REQUEST**. External devices use these signals to request interrupt service from the i960 Core Processor. These signals operate in dedicated mode, where each signal is assigned a dedicated interrupt level. These interrupt requests can be directed to either the Primary PCI signals (**P_INT[A:D]#**) or the i960 Core Processor pins (**XINT[3:0]#**) as shown below. **S_INT[A]#** ⇒ **P_INT[A]#** or **XINT[0]#** **S_INT[B]#** ⇒ **P_INT[B]#** or **XINT[1]#** **S_INT[C]#** ⇒ **P_INT[C]#** or **XINT[2]#** **S_INT[D]#**⇒ **P_INT[D]#** or **XINT[3]#**
XINT4#	1	I 5V Async	**EXTERNAL INTERRUPT REQUEST**. External devices use these signals to request interrupt service from the i960 Core Processor. These signals operate in dedicated mode, where each signal is assigned a dedicated interrupt level. This interrupt request is directed to the i960 Core Processor **XINT[4]#**.
XINT5#	1	I 5V Async	**EXTERNAL INTERRUPT REQUEST**. External devices use these signals to request interrupt service from the i960 Core Processor. These signals operate in dedicated mode, where each signal is assigned a dedicated interrupt level. This interrupt request is directed to the i960 Core Processor **XINT[5]#**.
LCDINIT#	1	I 5V Sync(P)	**LCD INITIALIZATION** is a static signal used to initialize the internal logic for the LCD960 debugger. This signal has an internal pullup for normal operation.
N/C	20	N/C	**NO CONNECT** pins have no usable function and must not be connected to any signal, power or ground. However they are in the boundary scan chain.
NMI#	1	I 5V Async	**NON-MASKABLE INTERRUPT** causes an i960 core processor non-maskable interrupt event to occur. **NMI#** is the highest priority interrupt source.

Table 7. Miscellaneous Signals (Sheet 2 of 2)

Name	Count	Type	Description
PWRDELAY	1	I Async	**POWER FAIL DELAY** is used with external circuitry to enable a reset of the memory controller's power fail state machine during power up initialization.
R_CLKIN	1	I 5V	**REFERENCE INPUT CLOCK** is the input clock to the 80303 I/O processor which drives the internal secondary PCI clocks. This pin must be connected to **R_CLKOUT** of the 80303 I/O processor, even if the secondary PCI bus is not used.
R_CLKOUT	1	O	**REFERENCE FEEDBACK CLOCK** must be connected to **R_CLKIN** of the 80303 I/O processor and be trace length matched to **S_CLK[5:0]**. **R_CLKOUT** may not appear to be in sync with **S_CLK[5:0]**.
SCL	1	I/O 5V OD Irst(Z)	**I^2C CLOCK** provides synchronous operation of the I^2C bus.
SDA	1	I/O 5V OD Irst(Z)	**I^2C DATA** is used for data transfer and arbitration on the I^2C bus.
TCK	1	I 5V Trst(H)	**TEST CLOCK** is an input which provides the clocking function for the IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the component on the rising edge and data is clocked out of the component on the falling edge.
TDI	1	I 5V Sync(T) Trst(H)	**TEST DATA INPUT** is the serial input pin for the JTAG feature. TDI is sampled on the rising edge of **TCK**, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pullup to ensure proper operation when this signal is unconnected.
TDO	1	O Sync(T) Trst(Z)	**TEST DATA OUTPUT** is the serial output pin for the JTAG feature. **TDO** is driven on the falling edge of **TCK** during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, **TDO** floats. The behavior of **TDO** is independent of **P_RST#**.
TMS	1	I 5V Sync(T) Trst(H)	**TEST MODE SELECT** is sampled at the rising edge of **TCK** to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing. This signal has a weak internal pullup to ensure proper operation when this signal is unconnected.
TRST#	1	I 5V Async Trst(H)	**TEST RESET** asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan Testing (JTAG). This signal has a weak internal pullup.
V_{CC}	77	-	POWER. Connect to a 3.3 volt power board plane.
V_{CC5REF}	1	I	**INPUT REFERENCE VOLTAGE** is strapped to 5V. This reference voltage allows the input pins (not including PCI and SDRAM pins) to be 5V tolerant.
VREF_P	1	I	**PRIMARY PCI INPUT VOLTAGE REFERENCE** is strapped to primary PCI power rail. It is used to clamp the inputs to either 5V or 3.3V.
VREF_S	1	I	**SECONDARY PCI INPUT VOLTAGE REFERENCE** is strapped to secondary PCI power rail. It is used to clamp inputs to either 5V or 3.3V.
V_{SS}	78	-	GROUND. Connect to a **V_{SS}** board plane.
V_{CCPLL1} **V_{CCPLL2}** **V_{CCPLL3}**	3	POWER	**PLL POWER** is a separate **V_{CC}** supply pin for the phase lock loop clock generator. It is intended for external connection to the V_{CC} board plane. In noisy environments, add to each V_{CCPLL} pin a simple bypass filter circuit (see Section 4.3) to reduce noise-induced clock jitter and its effects on timing relationships.

3.1.2 540-Lead H-PBGA Package

Figure 3. 540-Lead H-PBGA Package Diagram (Top and Side View)



NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M 1982.
2. Dimensions are measured at the maximum solder ball diameter parallel to primary datum.
3. Primary datum and seating plane are defined by the spherical crowns of the solder balls.
4. All dimensions are in millimeters.

Figure 4. 540-Lead H-PBGA Package Diagram (Bottom View)

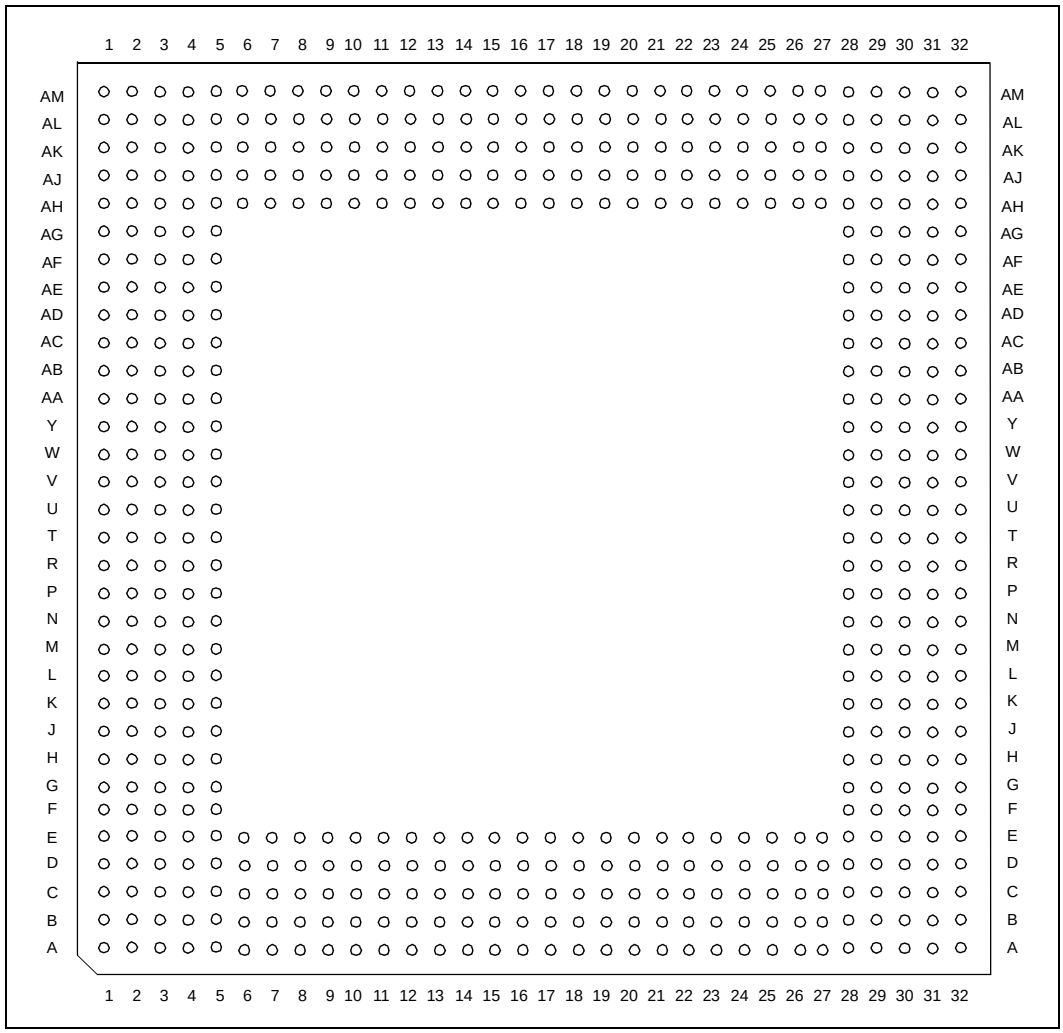


Table 8. 540-Lead H-PBGA - Ballpad Order (Sheet 1 of 5)

Ball#	Signal	Ball#	Signal	Ball#	Signal
A1	VSS	B7	VSS	C13	DQ16
A2	VSS	B8	DQ24	C14	VCC
A3	DQ31	B9	VSS	C15	SDQM2
A4	DQ30	B10	DQ21	C16	VCC
A5	DQ29	B11	VSS	C17	SA11
A6	DQ27	B12	DQ18	C18	VCC
A7	DQ25	B13	VCC	C19	SA0
A8	DQ23	B14	SCB2	C20	VCC
A9	DQ22	B15	VSS	C21	SRAS#
A10	SCKE1	B16	SA10	C22	VCC
A11	DQ19	B17	VSS	C23	DQ15
A12	DQ17	B18	SA4	C24	VCC
A13	SCB3	B19	VSS	C25	DQ46
A14	SDQM3	B20	SDQM1	C26	VCC
A15	SBA1	B21	VSS	C27	DQ8
A16	SA8	B22	SCB1	C28	VCC
A17	SA6	B23	VSS	C29	DQ39
A18	SA2	B24	DQ13	C30	VCC
A19	SCE0#	B25	VCC	C31	VCC
A20	SDQM0	B26	DQ10	C32	DQ2
A21	SWE#	B27	VSS	D1	S_AD37
A22	SCB0	B28	DQ6	D2	S_AD39
A23	DQ14	B29	DQ38	D3	S_AD32
A24	DQ12	B30	DQ37	D4	S_AD34
A25	DQ11	B31	VSS	D5	VSS
A26	DQ9	B32	VSS	D6	DQ59
A27	DQ7	C1	S_AD33	D7	VCC
A28	DQ5	C2	S_AD35	D8	DQ56
A29	DQ4	C3	VCC	D9	VSS
A30	DQ3	C4	VCC	D10	DQ52
A31	VSS	C5	DQ62	D11	DQ50
A32	VSS	C6	VCC	D12	DQ48
B1	VSS	C7	DQ26	D13	VSS
B2	VSS	C8	VCC	D14	SA13
B3	DQ63	C9	DQ54	D15	SDQM6
B4	VSS	C10	VCC	D16	SA12
B5	DQ61	C11	DQ20	D17	VSS
B6	DQ28	C12	VCC	D18	SA9

Table 8. 540-Lead H-PBGA - Ballpad Order (Sheet 2 of 5)

Ball#	Signal	Ball#	Signal	Ball#	Signal
D19	VCC	E25	DQ47	J1	S_AD57
D20	SA3	E26	DQ45	J2	S_AD59
D21	VSS	E27	DQ43	J3	VCC
D22	SDQM5	E28	DQ41	J4	S_AD52
D23	SCAS#	E29	DQ34	J5	S_AD54
D24	SCB4	E30	VCC	J28	N/C
D25	VSS	E31	DQ36	J29	N/C
D26	DQ44	E32	DQ35	J30	VCC
D27	DQ42	F1	S_AD45	J31	VCC
D28	DQ40	F2	VSS	J32	N/C
D29	VSS	F3	S_AD47	K1	S_AD61
D30	DQ1	F4	S_AD40	K2	VSS
D31	VSS	F5	S_AD42	K3	S_AD63
D32	DQ0	F28	VCCPLL1	K4	S_AD56
E1	S_AD41	F29	DQ33	K5	S_AD58
E2	S_AD43	F30	DCLK1	K28	N/C
E3	VCC	F31	VSS	K29	N/C
E4	S_AD36	F32	DCLK0	K30	PWRDELAY
E5	S_AD38	G1	S_AD49	K31	VSS
E6	DQ60	G2	S_AD51	K32	N/C
E7	DQ58	G3	VCC	L1	S_CBE4#
E8	DQ57	G4	S_AD44	L2	S_CBE6#
E9	DQ55	G5	S_AD46	L3	VCC
E10	DQ53	G28	N/C	L4	S_AD60
E11	DQ51	G29	DQ32	L5	S_AD62
E12	DQ49	G30	VCC	L28	N/C
E13	SCB7	G31	DCLK3	L29	N/C
E14	SCB6	G32	DCLK2	L30	VCC
E15	SDQM7	H1	S_AD53	L31	N/C
E16	SCKE0	H2	S_AD55	L32	N/C
E17	DCLKIN	H3	S_AD48	M1	S_ACK64#
E18	SBA0	H4	VSS	M2	S_AD1
E19	SA7	H5	S_AD50	M3	S_PAR64
E20	SA5	H28	DCLKOUT	M4	VSS
E21	SA1	H29	VSS	M5	S_CBE5#
E22	SCE1#	H30	N/C	M28	VCC
E23	SDQM4	H31	VSS	M29	VSS
E24	SCB5	H32	N/C	M30	N/C

Table 8. 540-Lead H-PBGA - Ballpad Order (Sheet 3 of 5)

Ball#	Signal	Ball#	Signal	Ball#	Signal
M31	VSS	T29	VSS	Y5	S_FRAME#
M32	N/C	T30	XINT2#	Y28	RAD8
N1	S_AD3	T31	VSS	Y29	VSS
N2	S_AD5	T32	XINT1#	Y30	VCC
N3	VCC	U1	S_CBE1#	Y31	VSS
N4	S_CBE7#	U2	S_SERR#	Y32	VCCPLL2
N5	S_REQ64#	U3	VCC	AA1	S_AD19
N28	N/C	U4	S_AD9	AA2	S_AD21
N29	N/C	U5	S_AD11	AA3	VCC
N30	VCC	U28	XINT0#	AA4	S_AD16
N31	N/C	U29	GPIO7	AA5	S_AD18
N32	NMI#	U30	VCC	AA28	VCC
P1	S_AD7	U31	GPIO6	AA29	VCC
P2	VSS	U32	GPIO5	AA30	VCC
P3	S_AD8	V1	S_PERR#	AA31	VCC5REF
P4	VREF_S	V2	VSS	AA32	RAD7
P5	S_AD0	V3	S_LOCK#	AB1	S_AD23
P28	VCC	V4	S_AD13	AB2	VSS
P29	FAIL#	V5	S_AD15	AB3	S_CBE3#
P30	VCC	V28	VCC	AB4	S_AD20
P31	VSS	V29	GPIO4	AB5	S_AD22
P32	LCDINIT#	V30	GPIO3	AB28	RAD6
R1	S_M66EN	V31	VSS	AB29	RAD5
R2	S_AD10	V32	N/C	AB30	RAD4
R3	VCC	W1	S_DEVSEL#	AB31	VSS
R4	S_AD2	W2	S_IRDY#	AB32	RAD3
R5	S_AD4	W3	VCC	AC1	S_AD25
R28	N/C	W4	S_PAR	AC2	S_AD27
R29	XINT5#	W5	S_STOP#	AC3	VCC
R30	VCC	W28	VCC	AC4	S_AD24
R31	XINT4#	W29	GPIO2	AC5	S_AD26
R32	XINT3#	W30	VCC	AC28	RAD2
T1	S_AD12	W31	GPIO1	AC29	RAD1
T2	S_AD14	W32	GPIO0	AC30	VCC
T3	S_AD6	Y1	S_CBE2#	AC31	RAD0
T4	VSS	Y2	S_AD17	AC32	RAD16
T5	S_CBE0#	Y3	S_TRDY#	AD1	S_AD29
T28	I_RST#	Y4	VSS	AD2	S_AD31

Table 8. 540-Lead H-PBGA - Ballpad Order (Sheet 4 of 5)

Ball#	Signal	Ball#	Signal	Ball#	Signal
AD3	S_AD28	AH1	S_CLK5	AJ7	P_GNT#
AD4	VSS	AH2	R_CLKIN	AJ8	VCC
AD5	S_AD30	AH3	S_GNT2#	AJ9	P_AD24
AD28	RAD15	AH4	VSS	AJ10	VSS
AD29	VSS	AH5	S_GNT3#	AJ11	P_AD18
AD30	RAD14	AH6	S_REQ5#	AJ12	P_FRAME#
AD31	VSS	AH7	P_AD30	AJ13	P_STOP#
AD32	RAD13	AH8	P_AD26	AJ14	VSS
AE1	S_HOLDA#	AH9	P_IDSEL	AJ15	P_AD11
AE2	S_GNT0#	AH10	P_AD20	AJ16	P_CBE0#
AE3	VCC	AH11	P_AD16	AJ17	P_AD4
AE4	S_RST#	AH12	P_TRDY#	AJ18	VSS
AE5	S_HOLD#	AH13	P_PAR	AJ19	P_REQ64#
AE28	RAD12	AH14	P_AD13	AJ20	VCC
AE29	VCC	AH15	P_AD9	AJ21	P_AD62
AE30	VCC	AH16	P_AD6	AJ22	VSS
AE31	RAD11	AH17	P_CLK	AJ23	P_AD54
AE32	RAD10	AH18	P_AD0	AJ24	P_AD50
AF1	S_CLK1	AH19	P_CBE7#	AJ25	P_AD46
AF2	VSS	AH20	P_PAR64	AJ26	VSS
AF3	S_CLK0	AH21	P_AD60	AJ27	P_AD38
AF4	S_CLK2	AH22	P_AD56	AJ28	P_AD34
AF5	S_CLK4	AH23	P_AD52	AJ29	SCL
AF28	VCC	AH24	P_AD48	AJ30	VCC
AF29	RAD9	AH25	P_AD44	AJ31	VSS
AF30	RWE#	AH26	P_AD40	AJ32	TDI
AF31	VSS	AH27	P_AD36	AK1	VCCPLL3
AF32	RALE	AH28	P_AD32	AK2	S_REQ0#
AG1	S_CLK3	AH29	VSS	AK3	VCC
AG2	R_CLKOUT	AH30	TRST#	AK4	S_REQ4#
AG3	VCC	AH31	TMS	AK5	VCC
AG4	S_REQ2#	AH32	TDO	AK6	P_RST#
AG5	S_GNT1#	AJ1	S_REQ1#	AK7	VCC
AG28	ROE#	AJ2	VSS	AK8	P_AD28
AG29	VCC	AJ3	VCC	AK9	VCC
AG30	VCC	AJ4	S_REQ3#	AK10	P_AD22
AG31	RCE1#	AJ5	S_GNT4#	AK11	VCC
AG32	RCE0#	AJ6	VSS	AK12	P_DEVSEL#

Table 8. 540-Lead H-PBGA - Ballpad Order (Sheet 5 of 5)

Ball#	Signal	Ball#	Signal	Ball#	Signal
AK13	VCC	AL9	P_AD23	AM5	P_REQ#
AK14	P_AD15	AL10	P_AD19	AM6	P_AD31
AK15	VCC	AL11	P_CBE2#	AM7	P_AD29
AK16	P_AD10	AL12	VSS	AM8	P_AD25
AK17	VCC	AL13	P_PERR#	AM9	P_CBE3#
AK18	P_AD2	AL14	VCC	AM10	P_AD21
AK19	VCC	AL15	P_AD14	AM11	P_AD17
AK20	P_CBE5#	AL16	VSS	AM12	P_IRDY#
AK21	VCC	AL17	P_AD8	AM13	P_LOCK#
AK22	P_AD58	AL18	P_AD5	AM14	P_SERR#
AK23	VCC	AL19	P_AD1	AM15	P_CBE1#
AK24	P_AD55	AL20	VSS	AM16	P_AD12
AK25	VCC	AL21	P_CBE6#	AM17	P_M66EN
AK26	P_AD42	AL22	P_AD63	AM18	P_AD7
AK27	VCC	AL23	P_AD59	AM19	P_AD3
AK28	P_AD41	AL24	VSS	AM20	VREF_P
AK29	VCC	AL25	P_AD51	AM21	P_ACK64#
AK30	VCC	AL26	VCC	AM22	P_CBE4#
AK31	SDA	AL27	P_AD45	AM23	P_AD61
AK32	TCK	AL28	VSS	AM24	P_AD57
AL1	VSS	AL29	P_AD37	AM25	P_AD53
AL2	VSS	AL30	P_AD33	AM26	P_AD49
AL3	S_GNT5#	AL31	VSS	AM27	P_AD47
AL4	VSS	AL32	VSS	AM28	P_AD43
AL5	P_INTA#	AM1	VSS	AM29	P_AD39
AL6	P_INTC#	AM2	VSS	AM30	P_AD35
AL7	P_AD27	AM3	P_INTB#	AM31	VSS
AL8	VSS	AM4	P_INTD#	AM32	VSS

Table 9. 540-Lead H-PBGA - Signal Name Order (Sheet 1 of 5)

Signal	Ball#	Signal	Ball#	Signal	Ball#
DCLK0	F32	DQ32	G29	GPIO5	U32
DCLK1	F30	DQ33	F29	GPIO6	U31
DCLK2	G32	DQ34	E29	GPIO7	U29
DCLK3	G31	DQ35	E32	I_RST#	T28
DCLKIN	E17	DQ36	E31	LCDINIT#	P32
DCLKOUT	H28	DQ37	B30	N/C	G28
DQ0	D32	DQ38	B29	N/C	H30
DQ1	D30	DQ39	C29	N/C	H32
DQ2	C32	DQ40	D28	N/C	J28
DQ3	A30	DQ41	E28	N/C	J29
DQ4	A29	DQ42	D27	N/C	J32
DQ5	A28	DQ43	E27	N/C	K28
DQ6	B28	DQ44	D26	N/C	K29
DQ7	A27	DQ45	E26	N/C	K32
DQ8	C27	DQ46	C25	N/C	L28
DQ9	A26	DQ47	E25	N/C	L29
DQ10	B26	DQ48	D12	N/C	L31
DQ11	A25	DQ49	E12	N/C	L32
DQ12	A24	DQ50	D11	N/C	M30
DQ13	B24	DQ51	E11	N/C	M32
DQ14	A23	DQ52	D10	N/C	N28
DQ15	C23	DQ53	E10	N/C	N29
DQ16	C13	DQ54	C9	N/C	N31
DQ17	A12	DQ55	E9	N/C	R28
DQ18	B12	DQ56	D8	N/C	V32
DQ19	A11	DQ57	E8	NMI#	N32
DQ20	C11	DQ58	E7	P_ACK64#	AM21
DQ21	B10	DQ59	D6	P_AD0	AH18
DQ22	A9	DQ60	E6	P_AD1	AL19
DQ23	A8	DQ61	B5	P_AD2	AK18
DQ24	B8	DQ62	C5	P_AD3	AM19
DQ25	A7	DQ63	B3	P_AD4	AJ17
DQ26	C7	FAIL#	P29	P_AD5	AL18
DQ27	A6	GPIO0	W32	P_AD6	AH16
DQ28	B6	GPIO1	W31	P_AD7	AM18
DQ29	A5	GPIO2	W29	P_AD8	AL17
DQ30	A4	GPIO3	V30	P_AD9	AH15
DQ31	A3	GPIO4	V29	P_AD10	AK16

Table 9. 540-Lead H-PBGA - Signal Name Order (Sheet 2 of 5)

Signal	Ball#	Signal	Ball#	Signal	Ball#
P_AD11	AJ15	P_AD49	AM26	P_REQ#	AM5
P_AD12	AM16	P_AD50	AJ24	P_REQ64#	AJ19
P_AD13	AH14	P_AD51	AL25	P_RST#	AK6
P_AD14	AL15	P_AD52	AH23	P_SERR#	AM14
P_AD15	AK14	P_AD53	AM25	P_STOP#	AJ13
P_AD16	AH11	P_AD54	AJ23	P_TRDY#	AH12
P_AD17	AM11	P_AD55	AK24	PWRDELAY	K30
P_AD18	AJ11	P_AD56	AH22	R_CLKIN	AH2
P_AD19	AL10	P_AD57	AM24	R_CLKOUT	AG2
P_AD20	AH10	P_AD58	AK22	RAD0	AC31
P_AD21	AM10	P_AD59	AL23	RAD1	AC29
P_AD22	AK10	P_AD60	AH21	RAD2	AC28
P_AD23	AL9	P_AD61	AM23	RAD3	AB32
P_AD24	AJ9	P_AD62	AJ21	RAD4	AB30
P_AD25	AM8	P_AD63	AL22	RAD5	AB29
P_AD26	AH8	P_CBE0#	AJ16	RAD6	AB28
P_AD27	AL7	P_CBE1#	AM15	RAD7	AA32
P_AD28	AK8	P_CBE2#	AL11	RAD8	Y28
P_AD29	AM7	P_CBE3#	AM9	RAD9	AF29
P_AD30	AH7	P_CBE4#	AM22	RAD10	AE32
P_AD31	AM6	P_CBE5#	AK20	RAD11	AE31
P_AD32	AH28	P_CBE6#	AL21	RAD12	AE28
P_AD33	AL30	P_CBE7#	AH19	RAD13	AD32
P_AD34	AJ28	P_CLK	AH17	RAD14	AD30
P_AD35	AM30	P_DEVSEL#	AK12	RAD15	AD28
P_AD36	AH27	P_FRAME#	AJ12	RAD16	AC32
P_AD37	AL29	P_GNT#	AJ7	RALE	AF32
P_AD38	AJ27	P_IDSEL	AH9	RCE0#	AG32
P_AD39	AM29	P_INTA#	AL5	RCE1#	AG31
P_AD40	AH26	P_INTB#	AM3	ROE#	AG28
P_AD41	AK28	P_INTC#	AL6	RWE#	AF30
P_AD42	AK26	P_INTD#	AM4	S_ACK64#	M1
P_AD43	AM28	P_IRDY#	AM12	S_AD0	P5
P_AD44	AH25	P_LOCK#	AM13	S_AD1	M2
P_AD45	AL27	P_M66EN	AM17	S_AD2	R4
P_AD46	AJ25	P_PAR	AH13	S_AD3	N1
P_AD47	AM27	P_PAR64	AH20	S_AD4	R5
P_AD48	AH24	P_PERR#	AL13	S_AD5	N2

Table 9. 540-Lead H-PBGA - Signal Name Order (Sheet 3 of 5)

Signal	Ball#	Signal	Ball#	Signal	Ball#
S_AD6	T3	S_AD44	G4	S_GNT2#	AH3
S_AD7	P1	S_AD45	F1	S_GNT3#	AH5
S_AD8	P3	S_AD46	G5	S_GNT4#	AJ5
S_AD9	U4	S_AD47	F3	S_GNT5#	AL3
S_AD10	R2	S_AD48	H3	S_HOLD#	AE5
S_AD11	U5	S_AD49	G1	S_HOLDA#	AE1
S_AD12	T1	S_AD50	H5	S_IRDY#	W2
S_AD13	V4	S_AD51	G2	S_LOCK#	V3
S_AD14	T2	S_AD52	J4	S_M66EN	R1
S_AD15	V5	S_AD53	H1	S_PAR	W4
S_AD16	AA4	S_AD54	J5	S_PAR64	M3
S_AD17	Y2	S_AD55	H2	S_PERR#	V1
S_AD18	AA5	S_AD56	K4	S_REQ0#	AK2
S_AD19	AA1	S_AD57	J1	S_REQ1#	AJ1
S_AD20	AB4	S_AD58	K5	S_REQ2#	AG4
S_AD21	AA2	S_AD59	J2	S_REQ3#	AJ4
S_AD22	AB5	S_AD60	L4	S_REQ4#	AK4
S_AD23	AB1	S_AD61	K1	S_REQ5#	AH6
S_AD24	AC4	S_AD62	L5	S_REQ64#	N5
S_AD25	AC1	S_AD63	K3	S_RST#	AE4
S_AD26	AC5	S_CBE0#	T5	S_SERR#	U2
S_AD27	AC2	S_CBE1#	U1	S_STOP#	W5
S_AD28	AD3	S_CBE2#	Y1	S_TRDY#	Y3
S_AD29	AD1	S_CBE3#	AB3	SA0	C19
S_AD30	AD5	S_CBE4#	L1	SA1	E21
S_AD31	AD2	S_CBE5#	M5	SA2	A18
S_AD32	D3	S_CBE6#	L2	SA3	D20
S_AD33	C1	S_CBE7#	N4	SA4	B18
S_AD34	D4	S_CLK0	AF3	SA5	E20
S_AD35	C2	S_CLK1	AF1	SA6	A17
S_AD36	E4	S_CLK2	AF4	SA7	E19
S_AD37	D1	S_CLK3	AG1	SA8	A16
S_AD38	E5	S_CLK4	AF5	SA9	D18
S_AD39	D2	S_CLK5	AH1	SA10	B16
S_AD40	F4	S_DEVSEL#	W1	SA11	C17
S_AD41	E1	S_FRAME#	Y5	SA12	D16
S_AD42	F5	S_GNT0#	AE2	SA13	D14
S_AD43	E2	S_GNT1#	AG5	SBA0	E18

Table 9. 540-Lead H-PBGA - Signal Name Order (Sheet 4 of 5)

Signal	Ball#	Signal	Ball#	Signal	Ball#
SBA1	A15	VCC	AE29	VCC	C20
SCAS#	D23	VCC	AE30	VCC	C22
SCB0	A22	VCC	AF28	VCC	C24
SCB1	B22	VCC	AG3	VCC	C26
SCB2	B14	VCC	AG29	VCC	C28
SCB3	A13	VCC	AG30	VCC	C30
SCB4	D24	VCC	AJ3	VCC	C31
SCB5	E24	VCC	AJ8	VCC	D7
SCB6	E14	VCC	AJ20	VCC	D19
SCB7	E13	VCC	AJ30	VCC	E3
SCE0#	A19	VCC	AK3	VCC	E30
SCE1#	E22	VCC	AK5	VCC	G3
SCKE0	E16	VCC	AK7	VCC	G30
SCKE1	A10	VCC	AK9	VCC	J3
SCL	AJ29	VCC	AK11	VCC	J30
SDA	AK31	VCC	AK13	VCC	J31
SDQM0	A20	VCC	AK15	VCC	L3
SDQM1	B20	VCC	AK17	VCC	L30
SDQM2	C15	VCC	AK19	VCC	M28
SDQM3	A14	VCC	AK21	VCC	N3
SDQM4	E23	VCC	AK23	VCC	N30
SDQM5	D22	VCC	AK25	VCC	P28
SDQM6	D15	VCC	AK27	VCC	P30
SDQM7	E15	VCC	AK29	VCC	R3
SRAS#	C21	VCC	AK30	VCC	R30
SWE#	A21	VCC	AL14	VCC	U3
TCK	AK32	VCC	AL26	VCC	U30
TDI	AJ32	VCC	B13	VCC	V28
TDO	AH32	VCC	B25	VCC	W3
TMS	AH31	VCC	C3	VCC	W28
TRST#	AH30	VCC	C4	VCC	W30
VCC	AA3	VCC	C6	VCC	Y30
VCC	AA28	VCC	C8	VCC5REF	AA31
VCC	AA29	VCC	C10	VCCPLL1	F28
VCC	AA30	VCC	C12	VCCPLL2	Y32
VCC	AC3	VCC	C14	VCCPLL3	AK1
VCC	AC30	VCC	C16	VREF_P	AM20
VCC	AE3	VCC	C18	VREF_S	P4

Table 9. 540-Lead H-PBGA - Signal Name Order (Sheet 5 of 5)

Signal	Ball#	Signal	Ball#	Signal	Ball#
VSS	H4	VSS	AL12	VSS	D17
VSS	H29	VSS	AL16	VSS	D21
VSS	H31	VSS	AL20	VSS	D25
VSS	A1	VSS	AL24	VSS	D29
VSS	A2	VSS	AL28	VSS	D31
VSS	A31	VSS	AL31	VSS	F2
VSS	A32	VSS	AL32	VSS	F31
VSS	AB2	VSS	AM1	VSS	K2
VSS	AB31	VSS	AM2	VSS	K31
VSS	AD4	VSS	AM31	VSS	M4
VSS	AD29	VSS	AM32	VSS	M29
VSS	AD31	VSS	B1	VSS	M31
VSS	AF2	VSS	B2	VSS	P2
VSS	AF31	VSS	B4	VSS	P31
VSS	AH4	VSS	B7	VSS	T4
VSS	AH29	VSS	B9	VSS	T29
VSS	AJ2	VSS	B11	VSS	T31
VSS	AJ6	VSS	B15	VSS	V2
VSS	AJ10	VSS	B17	VSS	V31
VSS	AJ14	VSS	B19	VSS	Y4
VSS	AJ18	VSS	B21	VSS	Y29
VSS	AJ22	VSS	B23	VSS	Y31
VSS	AJ26	VSS	B27	XINT0#	U28
VSS	AJ31	VSS	B31	XINT1#	T32
VSS	AL1	VSS	B32	XINT2#	T30
VSS	AL2	VSS	D5	XINT3#	R32
VSS	AL4	VSS	D9	XINT4#	R31
VSS	AL8	VSS	D13	XINT5#	R29

3.2 Package Thermal Specifications

The device is specified for operation when T_C (case temperature) is within the range of 0°C to 90°C, depending on operating conditions. Refer to the “Thermal Data for the 540-lead PBGA package” application note for more information regarding maximum case temperatures on the 540-lead PBGA package. Case temperature may be measured in any environment to determine whether the processor is within specified operating range. Measure the case temperature at the center of the top surface, opposite the ballpad.

3.2.1 Thermal Specifications

This section defines the terms used for thermal analysis.

3.2.1.1 Ambient Temperature

Ambient temperature, T_A, is the temperature of the ambient air surrounding the package. In a system environment, ambient temperature is the temperature of the air upstream from the package.

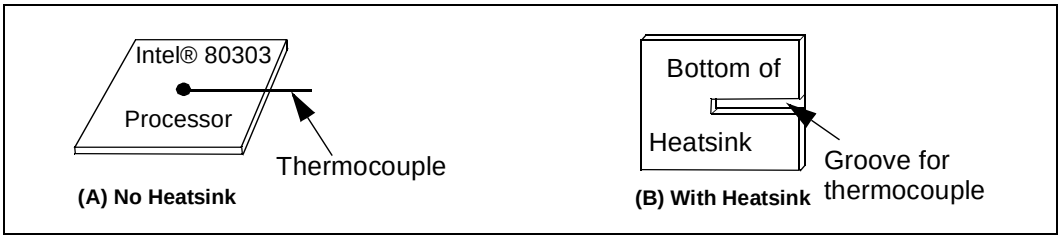
3.2.1.2 Case Temperature

When measuring case temperature, attention to detail is required to ensure accuracy. If a thermocouple is used, calibrate it before taking measurements. Errors may result when the measured surface temperature is affected by the surrounding ambient air temperature. Such errors may be due to a poor thermal contact between thermocouple junction and the surface, heat loss by radiation, or conduction through thermocouple leads.

To minimize measurement errors:

- Use a 35 gauge K-type thermocouple or equivalent.
- Attach the thermocouple bead or junction to the package top surface at a location corresponding to the center of the die (Figure 5A). The center of the die gives a more accurate measurement and less variation as the boundary condition changes.
- Attach the thermocouple bead at a 0° angle with respect to the package as shown in Figure 5A, when no heatsink is attached.
- When a passive heat sink is attached, a groove is made on the bottom surface of the heatsink and the thermocouple is attached at a 0° angle, as shown in Figure 5B.

Figure 5. Thermocouple Attachment - (A) No Heatsink / (B) With Heatsink



3.2.1.3 Thermal Resistance

The thermal resistance value for the case-to-ambient, θ_{CA}, is used as a measure of the cooling solution’s thermal performance.

3.2.2 Thermal Analysis

Table 10 lists the case-to-ambient thermal resistances of the 80303 for different air flow rates with and without a heat sink.

To calculate T_A, the maximum ambient temperature to conform to a particular case temperature:

$$T_A = T_C - P (\theta_{CA})$$

Compute P by multiplying I_{CC} and V_{CC}. Values for θ_{JC} and θ_{CA} are given in Table 6.

Junction temperature (T_J) is commonly used in reliability calculations. T_J can be calculated from θ_{JC} (thermal resistance from junction to case) using the following equation:

$$T_J = T_C + P (\theta_{JC})$$

Similarly, when T_A is known, the corresponding case temperature (T_C) can be calculated as follows:

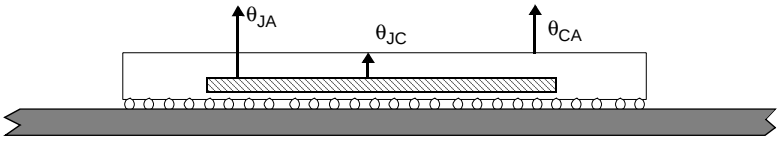
$$T_C = T_A + P (\theta_{CA})$$

The θ_{JA} (Junction to Ambient) for this package is currently estimated at 13.10° C/Watt with no airflow and no heatsink. The θ_{JA} (Junction to Ambient) for this package is currently estimated at 8.30° C/Watt with no airflow and a passive heatsink.

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

Table 10. 540-Lead H-PBGA Package Thermal Characteristics

Thermal Resistance — °C/Watt								
Parameter	Airflow — ft/min (m/sec)							
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	300 (1.52)	400 (2.03)	600 (3.04)	800 (4.06)
θ_{JC} (Junction-to-Case)	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
θ_{CA} (Case-to-Ambient) Without Heatsink	12.66	11.61	10.66	9.26	8.26	7.61	6.57	5.78
θ_{CA} (Case-to-Ambient) With Passive 0.25 in. Heatsink[2]	9.0	8.2	7.5	6.1	5.1	4.7	3.8	3.2
θ_{CA} (Case-to-Ambient) With 0.35 in. Passive Heatsink[2]	7.86	6.96	6.06	4.56	3.66	3.16	2.56	2.16



NOTES:
1. This table applies to a H-PBGA device soldered directly onto a board.
2. See Table 11 for heatsink information.
3. Estimated value.

3.3 Heat Sink Information

Table 11 provides a list of suggested sources for heat sinks. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

Table 11. Heat Sink Vendors and Contacts

Company	Factory Representative	Phone #	Fax #	Heatsink Part #
				Passive
AAVID Thermalloy, Inc 80 Commercial Street Concord, NH 03301 USA info@aavid.com http://www.aavidthermalloy.com/atp/atp.html	Attention: Sales	(603) 224-9988	(603) 223-1790	21933B withoou thermal grease (uses pins) 21935B withoou thermal grease (uses pins)

3.3.1 Socket Information

Table 12 and Table 13 provide vendor details for socket-headers and burn-in sockets for the Intel® 80310 I/O processor. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

3.3.2 Socket-Header Vendor

Table 12. Socket-Header Vendor

Company	Factory Representative	Phone/Fax #	Part #	
			BGA 540 Pin Header	BGA 540 Pin Socket Carrier
Adapter Technologies, Inc. 214-218 South 4th St. Perkasie, PA 18944	John Miller	215-258-5750/ 215-258-5760	BGAH-540-0-01-3201-0277-1	BGA-540-0-02-3201-0275P-130

3.3.3 Burn-in Socket Vendor

Table 13. Burn-in Socket Vendor

Company	Factory Representative	Phone #	Burn-in Socket Part #
Texas Instruments 111 Forbes Blvd. Mansfield, MA 02048	W. Ray Johnson	508-236-5375	ULGA540-005

3.3.4 Shipping Tray Vendor

Table 14. Shipping Tray Vendor

Company	Factory Representative	Phone #	Shipping Tray Part #
3M	Ron Goth	602-465-5381	7-0000-21001-184-167

3.3.5 Logic Analyzer Interposer Vendor

Table 15. Logic Analyzer Interposer Vendor

Company	Factory Representative	Phone/Fax #	Part #
Packard-Hughes Interconnect 17150 Von Karman Ave Irvine, CA 92614-0968	Karen May	949-660-5773 949-660-5825	1126898

3.3.6 JTAG Emulator Vendor

Table 16. JTAG Emulator Vendor

Company	Factory Representative	Phone/ Fax #	Part #
Corelis	Mike Winters	562-926-6727 562-484-6196	TBD

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–55° C to + 125° C
Case Temperature Under Bias	0° C to + 90° C
Supply Voltage wrt. V_{SS}	–0.5 V to + 4.6 V
Supply Voltage wrt. V_{SS} on V_{CC5}	–0.5 V to + 6.5 V
Voltage on Any Ball wrt. V_{SS}	–0.5 V to V_{CC} + 0.5 V

NOTICE: This data sheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 17. Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.6	V	
V_{CC5}	Input Protection Bias	V_{CC}	V_{CC}+2.25	V	
F_{P_CLK}	Input Clock Frequency	16	66.66	MHz	
T_C	Case Temperature Under Bias GC (540 H-PBGA)	0	90	°C	

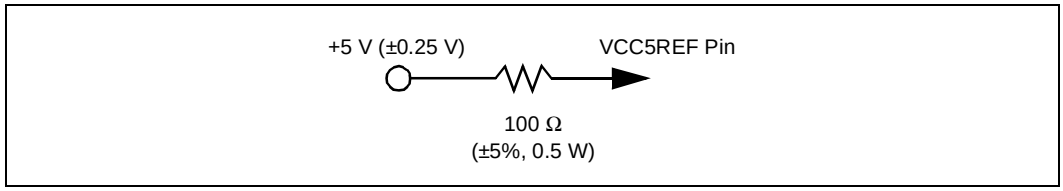
4.2 V_{CC5REF} Pin Requirements (V_{DIFF})

In mixed voltage systems that drive 80303 I/O processor inputs in excess of 3.3 V, the **V_{CC5REF}** pin must be connected to the system's 5 V supply. To limit current flow into the **V_{CC5REF}** pin, there is a limit to the voltage differential between the **V_{CC5REF}** pin and the other V_{CC} pins. The voltage differential between the **V_{CC5REF}** pin and its 3.3 V V_{CC} pins should never exceed 2.25 V. This limit applies to power-up, power-down, and steady-state operation. Table 18 outlines this requirement.

Note: This requirement also applies to the VREF_P and VREF_S pins.

If the voltage difference requirements cannot be met due to system design limitations, an alternate solution may be employed. As shown in Figure 6, a minimum of 100 Ω series resistor may be used to limit the current into the **V_{CC5REF}** pin. This resistor ensures that current drawn by the **V_{CC5REF}** pin does not exceed the maximum rating for this pin.

Figure 6. V_{CC5REF} Current-Limiting Resistor



This resistor is not necessary in systems that can guarantee the V_{DIFF} specification.

In 3.3 V-only systems and systems that drive pins from 3.3 V logic, connect the **V_{CC5REF}** pin directly to the 3.3 V V_{CC} plane.

Table 18. V_{DIFF} Specification for Dual Power Supply Requirements (3.3 V, 5 V)

Sym	Parameter	Min	Max	Units	Notes
V_{DIFF}	V_{CC5}-V_{CC} Difference		2.25	V	**V_{CC5REF}** input should not exceed V_{CC} by more than 2.25 V during power-up and power-down, or during steady-state operation.

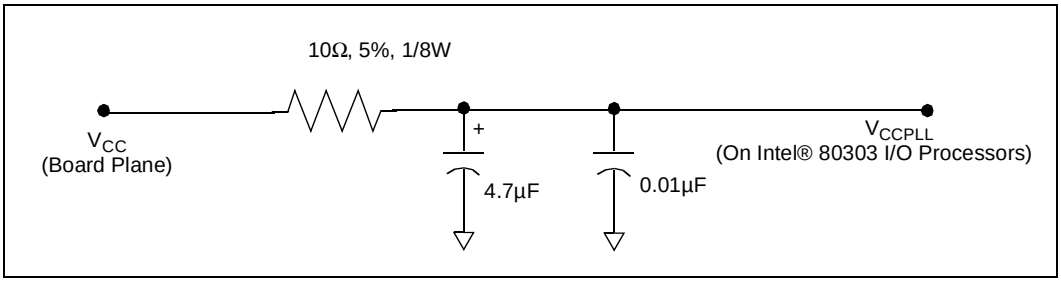
4.3 V_{CCPLL} Pin Requirements

To reduce clock skew on the Intel® 80303 I/O Processor, the V_{CCPLL} pin for the Phase Lock Loop (PLL) circuit is isolated on the pinout. The lowpass filter, as shown in Figure 7, reduces noise induced clock jitter and its effects on timing relationships in system designs.

The trace lengths between the 4.7µF capacitor, the 0.01uF capacitor, and VCCPLL must be as short as possible.

Note: There are three VCCPLL pins on the Intel® 80303 I/O Processor: VCCPLL1, VCCPLL2, and VCCPLL3. Each pin requires a lowpass filter. Providing just one lowpass filter and tying it to all three VCCPLL inputs is not recommended.

Figure 7. V_{CCPLL} Lowpass Filter



4.4 Targeted DC Specifications

Table 19. DC Characteristics

Sym	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage (SDRAM)	-2.0	0.8	V	(4)
V_{IH1}	Input High Voltage (SDRAM)	2.0 V	V_{CC} + 2.0	V	(4)
V_{IL2}	Input Low Voltage (5V PCI, Flash, Misc.)	-0.5	0.8	V	(1,3,5)
V_{IH2}	Input High Voltage (5V PCI, Flash, Misc.)	2.0 V	Vcc + 0.5	V	(1,3,5)
V_{IL3}	Input Low Voltage (3.3V PCI)	-0.5	0.3Vcc	V	(1,3,5)
V_{IH3}	Input High Voltage (3.3V PCI)	0.5Vcc	Vcc + 0.5	V	(1,3,5)
V_{OL1}	Output Low Voltage (5V PCI, Flash, Misc.)		0.4	V	I_{OL} = 6 mA (1,3,5)
V_{OH1}	Output High Voltage (5V PCI, Flash, Misc.)	2.4		V	I_{OH} = -2 mA (1,3,5)
V_{OL2}	Output Low Voltage (SDRAM)		0.4	V	I_{OL} = 4 mA (4)
V_{OH2}	Output High Voltage (SDRAM)	2.4		V	I_{OH} = -4 mA (4)
V_{OL3}	Output Low Voltage (3.3V PCI)		0.1Vcc	V	I_{OL} = 1.5mA(1)
V_{OH3}	Output HIGH Voltage (3.3V PCI)	0.9Vcc		V	I_{OH} = -0.5mA(1)
C_{IN}	Input Capacitance - PBGA		10	pF	F_{S_CLK} = T_F Min (1, 2)
C_{OUT}	I/O or Output Capacitance - PBGA		10	pF	F_{S_CLK} = T_F Min (1, 2)
C_{CLK}	S_CLK Capacitance - PBGA	5	10	pF	F_{S_CLK} = T_F Min (1, 2)
C_{IDSEL}	IDSEL Ball Capacitance		8	pF	(1,2)
L_{PIN}	Ball Inductance		25	nH	(1,2)

NOTES:
1. As required by the *PCI Local Bus Specification* Revision 2.2.
2. Not tested.
3. Flash signals include **RAD[16:0]**, **RALE**, **RCE[1:0]#**, **ROE#**, **RWE#**.
4. SDRAM signals include **SA[13:0]**, **SBA[1:0]**, **SCAS#**, **SCE[1:0]#**, **SCKE[1:0]**, **SDQM[7:0]**, **SRAS#**, **SWE#**, **DCLKIN**, **DCLKOUT**, **DQ[63:0]**, and **SCB[7:0]**.
5. Miscellaneous signals include all signals that are not PCI, SDRAM or Flash signals.

Table 20. I_{CC} Characteristics

Symbol	Parameter	Typ	Max	Units	Notes
I_{LI1}	Input Leakage Current for each signal except **TCK**, **TMS**, **TRST#**, **TDI**, **RAD[8:0]**, **LCDINIT#**		± 5	µA	$0 \le V_{IN} \le V_{CC}$ (5)
I_{LI2}	Input Leakage Current for **TCK**, **TMS**, **TRST#**, **TDI**, **RAD[8:0]**, **LCDINIT#**	-140	-250	µA	V_{IN} = 0.45 V (1,5)
I_{CC} Active (Power Supply)	Power Supply Current		2.15	A	(1,2)
I_{CC} Active (Thermal)	Thermal Current	1.5		A	(1,3)
I_{CC} Active (Power Modes)	Reset Mode		0.95	A	(4)

NOTES:
1. Measured with device operating and outputs loaded to the test condition in Figure 13.
2. I_{CC} Active (Power Supply) value is provided for selecting your system's power supply. It is measured using one of the worst case instruction mixes with V_{CC} = 3.6 V and ambient temperature = 55 ° C.
3. I_{CC} Active (Thermal) value is provided for your system's thermal management. Typical I_{CC} is measured with V_{CC} = 3.3 V and ambient temperature = 55 ° C.
4. I_{CC} Test (Power modes) refers to the I_{CC} values that are tested when the device is in Reset mode or ONCE mode with V_{CC} = 3.6 V and ambient temperature = 55 ° C.
5. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.

4.5 Targeted AC Specifications

4.5.1 Clock Signal Timings

Table 21. Clock Timings

Symbol	Parameter	Min	Max	Units	Notes
T_F	PCI clocks Frequency	16	66	MHz	
T_C	PCI clocks Period	15	62.5	ns	(1)
T_{CS}	PCI clocks Period Stability		±250	ps	Adjacent Clocks (2)
T_{CH1}	PCI clocks High Time (33MHz)	11		ns	Measured at 2.0V for 5V clock Measured at 0.5 V_{CC} for 3.3V clock (2)
T_{CL1}	PCI clocks Low Time (33MHz)	11		ns	Measured at 0.8V for 5V clock Measured at 0.3 V_{CC} for 3.3 V clock (2)
T_{CH2}	PCI clocks High Time (66MHz)	6		ns	Measured at 0.5 V_{CC} (2)
T_{CL2}	PCI clocks Low Time (66MHz)	6		ns	Measured at 0.3 V_{CC} (2)
T_{SR1}	PCI clocks Slew Rate (33MHz)	1	4	V/ns	0.4V to 2.4V for 5V clock (2) 0.2 V_{CC} to 0.6 V_{CC} for 3.3V clock
T_{SR2}	PCI clocks Slew Rate (66MHz)	1.5	4	V/ns	0.2 V_{CC} to 0.6 V_{CC} (2)
T_{skew1}	Clock skew between **R_CLKOUT** and **S_CLK[5:0]**	2.7	4.5	ns	(2, 4)
T_{skew2}	Clock skew for **S_CLK[5:0]**	0	300	ps	(2)
T_{DIF}	SDRAM clocks Frequency		100	MHz	
T_{DIC}	SDRAM clocks Period	10		ns	(1)
T_{DICS}	SDRAM clocks Period Stability		±250	ps	Adjacent Clocks (2)
T_{DICH1}	SDRAM clocks High Time	3		ns	Measured at 1.5V (100MHz) (2)
T_{DICL1}	SDRAM clocks Low Time	3		ns	Measured at 1.5V (100MHz) (2)
T_{skew3}	Clock skew between **DCLKOUT** and **DCLK[3:0]**	1.1	2.2	ns	(2, 3)
T_{skew4}	Clock skew for **DCLK[3:0]**		200	ps	(2)

NOTES:
1. See Figure 8 “P_CLK, TCK, DCLKIN, DCLKOUT Waveform” on page 53.
2. Not tested.
3. DCLKOUT is earlier than **DCLK[3:0]** .
4. **R_CLKOUT** is earlier than **S_CLK[5:0]**.

4.5.2 PCI Interface Signal Timings

Table 22. PCI Signal Timings

Sym	Parameter	66MHz		33MHz			
		Min	Max	Min	Max	Unit	Notes
T_{OV1}	Output Valid Delay from clock to signal except for **P_REQ#**, **P_INT[A:D]#, S_HOLDA#** and **S_GNT[5:0]#**	1	6	2	11	ns	(1,2,9)
T_{OV2}	Output Valid Delay from clock to **S_REQ64#**	0		0		ns	(1,2,7, 9)
T_{OV3}	Output Valid Delay from clock to **P_REQ#**, **S_HOLDA#** and **S_GNT[5:0]#**	2	6	2	12	ns	(1,2,9)
T_{OF}	Output Float Delay from clock		14		28	ns	(4,5,6, 9)
T_{IS1}	Input Setup to clock for signals except for **P_GNT#**, **S_HOLD#** and **S_REQ[5:0]#**	3		7		ns	(3,9)
T_{IS2}	Input Setup to clock for **P_GNT#**	5		10		ns	(3,9)
T_{IS3}	Input Setup to clock for **S_REQ[5:0]#** and **S_HOLD#**	5		12		ns	(3,9)
T_{IH1}	Input Hold from clock to PCI Signals	0		0		ns	(3,9)
T_{IS4}	Input Setup to **P_RST#** for **P_REQ64#**	$10T_c$		$10T_c$			(3)
T_{IH2}	Input Hold from **P_RST#** to **P_REQ64#**	0	50	0	50	ns	(3)

NOTES:
1. 5V PCI AC timings use 0 pF for minimum timings and 50 pF for maximum timings. 3.3V PCI AC timings use 10pF for minimum and maximum timings.
2. See Figure 9 "T_{OV} Output Delay Waveform" on page 53.
3. See Figure 11 "T_{IS} and T_{IH} Input Setup and Hold Waveform" on page 54
4. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested. See Figure 10 "T_{OF} Output Float Waveform" on page 53.
5. See Figure 10 "T_{OF} Output Float Waveform" on page 53.
6. Outputs precharged to V_{CC5}.
7. **S_REQ64#** is asserted asynchronously with respect to **P_RST#**. **S_REQ64#** is deasserted one **P_CLK** after the deassertion of **S_RST#**.
8. **IRQ[3:0]#** must be asserted for a minimum of two **P_CLK** periods to guarantee recognition.
9. All primary PCI clock references are to **P_CLK** and all secondary PCI clock references are to **S_CLK[5:0]**.

4.5.3 Core Signal Interface Timings

Table 23. Core Signal Timings

Sym	Parameter	Min	Max	Units	Notes
T_{OV4}	Output Valid Delay from **P_CLK** - **FAIL#**	4	12	ns	(1,4)
T_{IS5}	Input Setup to **DCLKIN** - **XINT[5:0]#**, **NMI#**	0		ns	(2,3)
T_{IH3}	Input Hold from **DCLKIN** - **XINT[5:0]#**, **NMI#**	3		ns	(2,3)
T_{OV5}	Output Valid Delay from **DCLKIN** - **XINT[5:4]#**	3	8	ns	
T_{IS6}	Input Setup to **DCLKIN** - **GPIO[7:0]**	0.8		ns	
T_{IH4}	Input Hold from **DCLKIN** - **GPIO[7:0]**	3		ns	
T_{OV6}	Output Valid Delay from **DCLKIN** - **GPIO[7:0]**	2.7	10	ns	
T_{OV7}	Output Valid Delay from **DCLKIN** - **I_RST#**	2	8	ns	

NOTES:
1. See Figure 9 "T_{OV} Output Delay Waveform" on page 53.
2. See Figure 11 "T_{IS} and T_{IH} Input Setup and Hold Waveform" on page 54.
3. Setup and hold times must be met for proper processor operation. **XINT[5:0]#** may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge. For asynchronous operation, **XINT[5:0]#** must be asserted for a minimum of two **P_CLK** periods to guarantee recognition.
4. The processor asserts **FAIL#** during built-in self-test. If self-test passes, **FAIL#** is deasserted. The processor asserts **FAIL#** during the bus confidence test. If the test passes, **FAIL#** is deasserted and user program execution begins.

4.5.4 SDRAM/Flash Interface Signal Timings

Table 24. SDRAM / Flash Signal Timings

Sym	Parameter	Min	Max	Units	Notes
T_{OV8}	Output Valid Delay from **DCLK[3:0]** - **SA[13:0]**, **SBA[1:0]**, **SCAS#**, **SRAS#**, and **SWE#**.	1.0	4.6	ns	(1,5)
T_{OV9}	Output Valid Delay from **DCLK[3:0]** - **DQ[63:0]**, and **SCB[7:0]**.	1.0	4.6	ns	(1,5)
T_{OV10}	Output Valid Delay from **DCLK[3:0]** - **SDQM[7:0]**	1.0	4.6	ns	(1,5)
T_{OV11}	Output Valid Delay from **DCLK[3:0]** - **SCKE[1:0]** and **SCE[1:0]#**	0.3	2.2	ns	(1,5)
T_{IS7}	Input Setup to **DCLK[3:0]** - **DQ[63:0]**, and **SCB[7:0]**	1.7		ns	(2)
T_{IH5}	Input Hold from **DCLK[3:0]** - **DQ[63:0]**, and **SCB[7:0]**	0.7		ns	(2)
T_{OV12}	Output Valid Delay from **DCLKIN** - **RAD[16:0]**, **RALE**, **RCE[1:0]#**, **ROE#**, and **RWE#**.	2.0	10.0	ns	(1,5)
T_{IS8}	Input Setup to **DCLKIN** - **RAD[16:0]**	3.5		ns	(2)
T_{IH6}	Input Hold from **DCLKIN** - **RAD[16:0]**	1.0		ns	(2)

NOTES:
1. See Figure 9 "T_{OV} Output Delay Waveform" on page 53.
2. See Figure 11 "T_{IS} and T_{IH} Input Setup and Hold Waveform" on page 54.
3. SDRAM signals include **SA[13:0]**, **SBA[1:0]**, **SCAS#**, **SCE[1:0]#**, **SCKE[1:0]**, **SDQM[7:0]**, **SRAS#**, **SWE#**, **DQ[63:0]**, and **SCB[7:0]**. Timings are for 3.3V signalling environment.
4. Flash signals include **RAD[16:0]**, **RALE**, **RCE[1:0]#**, **ROE#**, and **RWE#**. Timings are for 5V signalling environment.
5. These output valid times are specified with a 0 pF loading.

4.5.5 Boundary Scan Test Signal Timings

Table 25. Boundary Scan Test Signal Timings

Sym	Parameter	Min	Max	Units	Notes
T_{BSF}	**TCK** Frequency	0	$0.5T_F$	MHz	
T_{BSCH}	**TCK** High Time	15		ns	Measured at 1.5 V (1)
T_{BSCL}	**TCK** Low Time	15		ns	Measured at 1.5 V (1)
T_{BSCR}	**TCK** Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{BSCF}	**TCK** Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to **TCK** — **TDI**, **TMS**	3		ns	(4)
T_{BSIH1}	Input Hold from **TCK** — **TDI**, **TMS**	5		ns	(4)
T_{BSOV1}	**TDO** Valid Delay	5	15	ns	Relative to falling edge of **TCK** (2, 3)
T_{OF1}	**TDO** Float Delay	5	15	ns	Relative to falling edge of **TCK** (2, 5)

NOTES:
1. Not tested.
2. Outputs precharged to V_{CC5}.
3. See Figure 9 "T_{OV} Output Delay Waveform" on page 53.
4. See Figure 11 "T_{IS} and T_{IH} Input Setup and Hold Waveform" on page 54.
5. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested. See Figure 10 "T_{OF} Output Float Waveform" on page 53.

4.5.6 I²C Interface Signal Timings

Table 26. I²C Interface Signal Timings

Symbol	Parameter	Std. Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCL}	**SCL** Clock Frequency	0	100	0	400	KHz	
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7		1.3		µs	(1)
T_{HDSTA}	Hold Time (repeated) START Condition	4		0.6		µs	(1,3)
T_{LOW}	**SCL** Clock Low Time	4.7		1.3		µs	(1,2)
T_{HIGH}	**SCL** Clock High Time	4		0.6		µs	(1,2)
T_{SUSTA}	Setup Time for a Repeated START Condition	4.7		0.6		µs	(1)
T_{HDDAT}	Data Hold Time	0		0	0.9	µs	(1)
T_{SUDAT}	Data Setup Time	250		100		ns	(1)
T_{SR}	**SCL** and **SDA** Rise Time		1000	$20+0.1C_b$	300	ns	(1,4)
T_{SF}	**SCL** and **SDA** Fall Time		300	$20+0.1C_b$	300	ns	(1,4)
T_{SUSTO}	Setup Time for STOP Condition	4		0.6		µs	(1)

NOTES:
1. See Figure 12.
2. Not tested.
3. After this period, the first clock pulse is generated.
4. C_b = the total capacitance of one bus line, in pF.

4.6 AC Timing Waveforms

Figure 8. P_CLK, TCK, DCLKIN, DCLKOUT Waveform

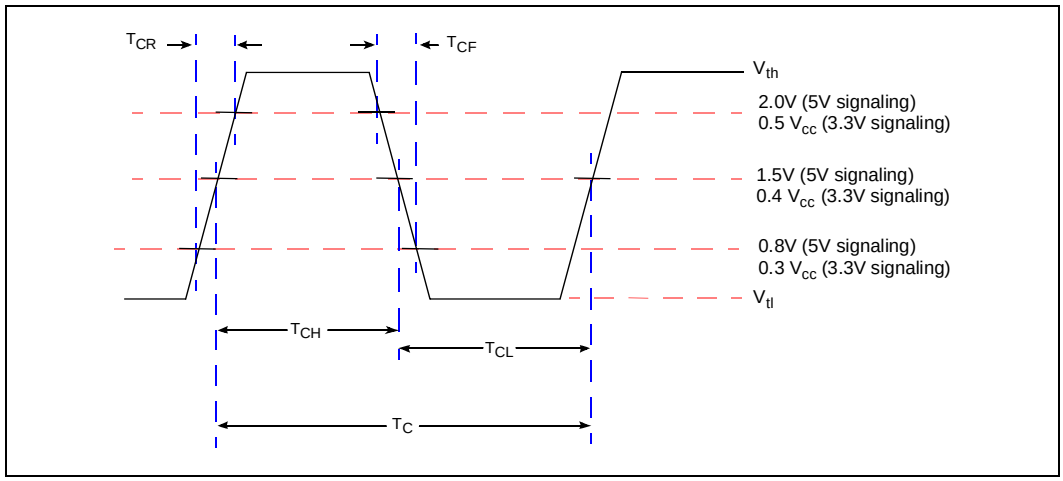


Figure 9. T_{OV} Output Delay Waveform

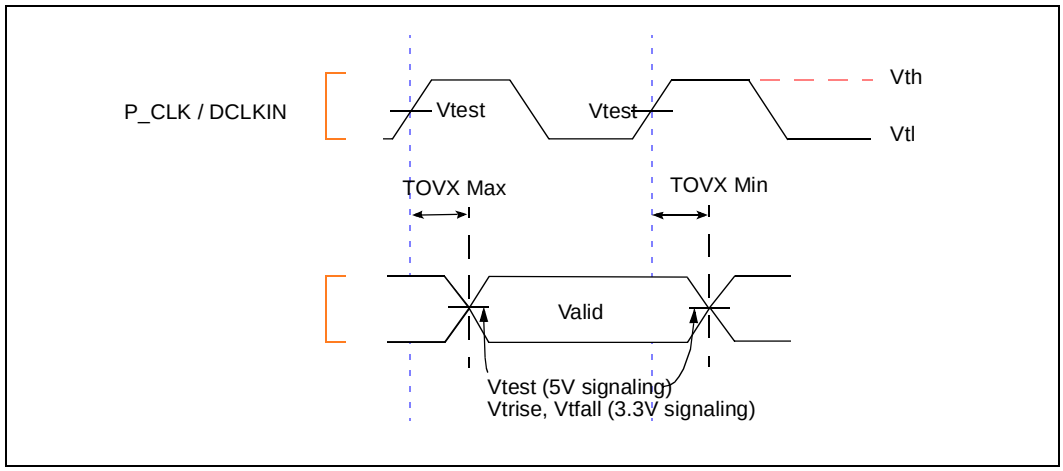


Figure 10. T_{OF} Output Float Waveform

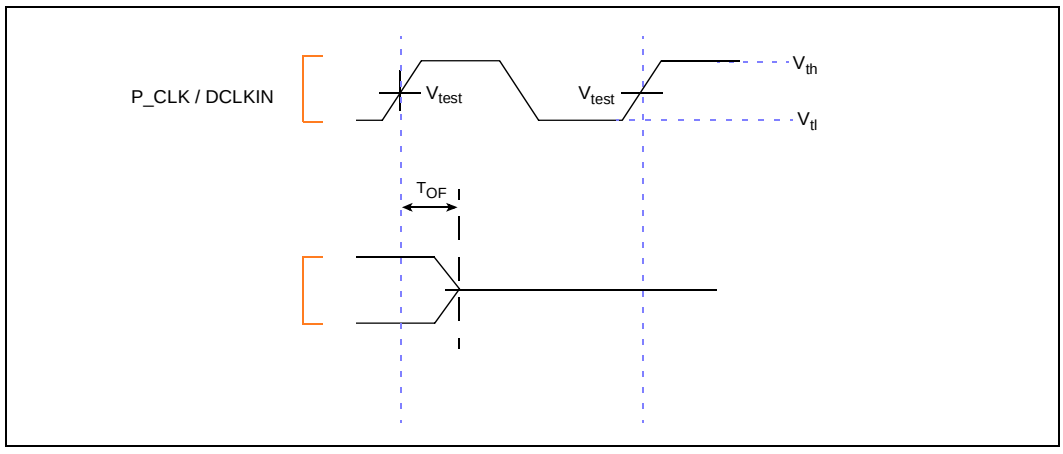


Figure 11. T_{IS} and T_{IH} Input Setup and Hold Waveform

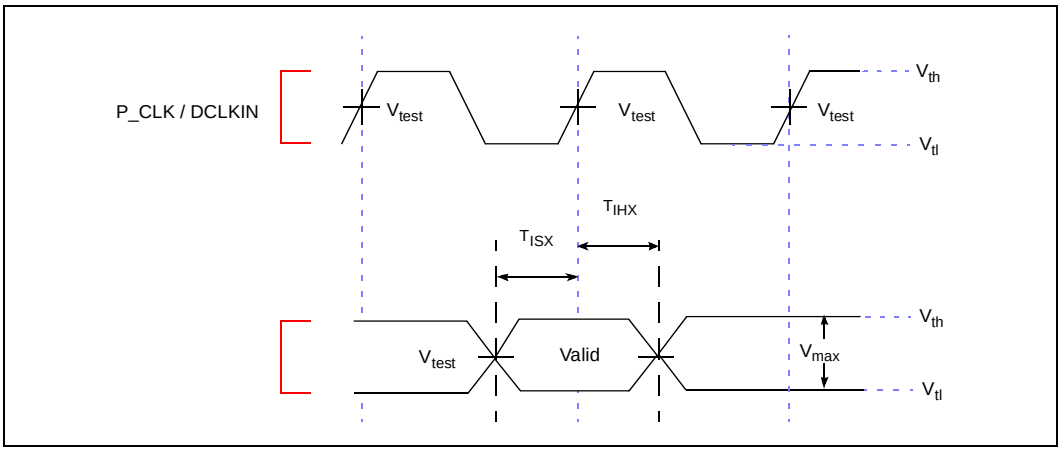
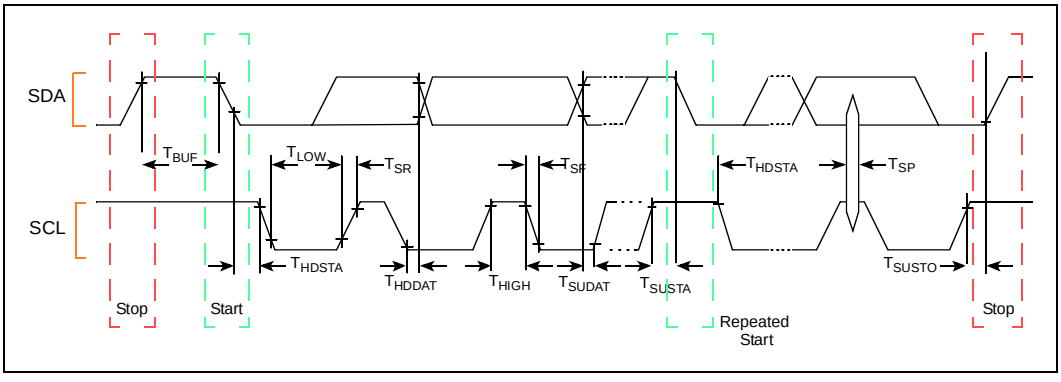


Table 27. Measure Condition Parameters

Symbol	5V Signaling	3.3V Signaling	SDRAM	Units
V_{th}	2.4	$0.6V_{cc}$	0	V (Note)
V_{tl}	0.4	$0.2V_{cc}$	3	V (Note)
V_{test}	1.5	$0.4V_{cc}$	1.5	V
V_{trise}	n/a	$0.285V_{cc}$	1.5	V
V_{tfall}	n/a	$0.615V_{cc}$	1.5	V
V_{max}	2.0	$0.4V_{cc}$	N/A	V (Note)
Input Signal Edge Rate	1.0 V / ns @ 33 MHz 1.5 V / ns @ 66 MHz		1.0 V / ns	

NOTE: The input test for the 5V environment is done with 400 mV of overdrive (over V_{ih} and V_{il}); the test for the 3.3V environment is done with $0.1V_{cc}$ of overdrive. V_{max} specifies the maximum peak-to-peak waveform allowed for measuring input timing.

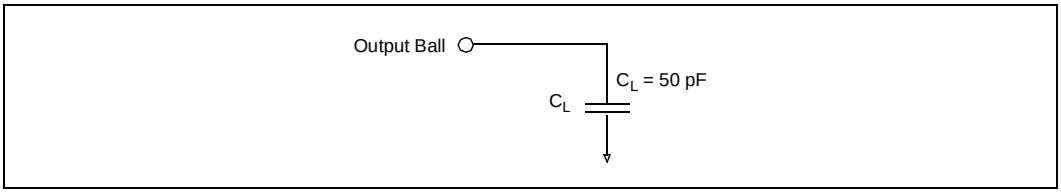
Figure 12. I^2C Interface Signal Timings



4.7 AC Test Conditions

The AC specifications in Section 4.5, “Targeted AC Specifications” on page 49 are tested with a 50 pF load indicated in Figure 13.

Figure 13. AC Test Load (all signals except SDRAM and Flash signals)



The PCI maximum AC specifications are tested with the 50 pF load indicated in Figure 13. The PCI minimum AC specifications are tested with a 0 pF load. All of the SDRAM and Flash timings are specified for a 0 pF load.

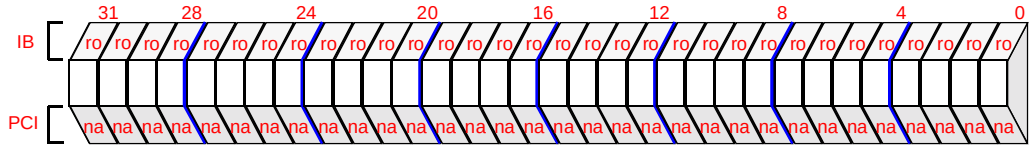
5.0 Device Identification on Reset

During the manufacturing process, values characterizing the i960 Rx I/O processor type and stepping are programmed into memory-mapped registers. The i960 Rx I/O processor contains two, read-only device ID MMRs. One holds the Processor Device ID (PDIDR MMR Location - 0000 1710H) and the other holds the i960 Core Processor Device ID (DEVICEID MMR Location - FF00 8710H). During initialization, the DEVICEID is placed in g0.

The device identification values are compliant with the IEEE 1149.1 specification and Intel standards. Table 28 describes the fields of the two Device IDs.

Note: The value programmed into these registers varies with stepping. Refer to the Specification Update for the correct value.

Table 28. Device ID Registers



IB: 0000 1710H
FF00 8710H
PCI: NA

Legend:
NA = Not Accessible
RO = Read Only
RV = Reserved
PR = Preserved
RW = Read/Write
RS = Read/Set
RC = Read Clear
IB = Internal Bus Address
PCI = PCI Configuration Address Offset

Bit	Default	Description
31:28	X	Version - Indicates stepping changes.
27	X	V_{CC} - Indicates device voltage type. 0 = 5.0 V 1 = 3.3 V
26:21	X	Product Type - Indicates the generation or “family member”.
20:17	X	Generation Type - Indicates the generation of the device.
16:12	X	Model Type - Indicates member within a series and specific model information.
11:01	X	Manufacturer ID - Indicates manufacturer ID assigned by IEEE. 0000 0001 001 = Intel Corporation
0	1	Constant

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