



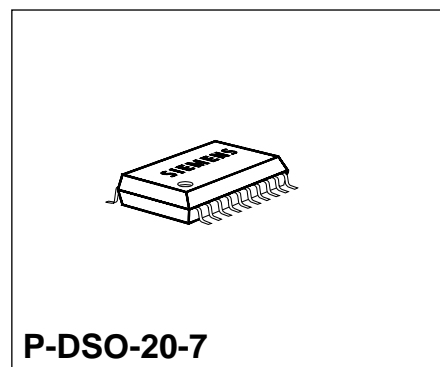
**THE DATASHEET OF  
FZL4146G**



### Bipolar IC

#### Features

- Short-circuit signaling
- Four driver circuits for driving power transistors
- Turn-ON threshold setting from 1.5 to 7 V



Type	Ordering Code	Package
FZL 4146 G	Q67000-H8743	P-DSO-20-7 (SMD)

#### General Description

The IC comprises four driver circuits capable of driving power transistors (PNP or PMOS). The output transistors are protected against short-circuit to ground and supply voltage. The turn-ON threshold can be set from 1.5 V to 7 V. Overload at one or several outputs will be indicated at pin SQ (signaling output). The corresponding power transistors are then protected by changeover to clock-governed operation.

#### Circuit Description

Each driver circuit has one active high driver input DI and a common enable input ENA (active high) is provided for all stages. The Q output is designed to drive the output transistors. The load current is sampled and, if necessary, limited via pin W. If the load current exceeds the preset value, the output stage switches off. Switching-ON again is provided by the built-in clock generator T. Its operation requires an external capacitor  $C_e$  at pin CE. If  $C_e$  is bridged by a break-key, switching-ON can only be carried out by operating this key. The duty cycle of the clock generator is 1:47 (e.g. 45  $\mu$ s/2.1 ms with  $C_e = 10$  nF). The clock generator is privileged versus the current sensor shut down. When the supply is connected, the internal RS-FF goes into the state corresponding to the released output.

The turn-ON threshold at input DI and ENA can be set via pin TS from 1.5 to 7 V.

$V_{TS} = 0 \text{ V} \dots 1.5 \text{ V}$	Turn-ON threshold = 1.5 V
$V_{TS} = 1.5 \text{ V} \dots 7 \text{ V}$	Turn-ON threshold = $V_{TS}$
$V_{TS} = V_S$	Turn-ON threshold = 7 V

Inputs DI, ENA and W are proof against line break, i.e. an open input at DI or ENA corresponds to input L, open input W corresponds to overcurrent. If input TS is open, the highest turn-ON threshold is provided.

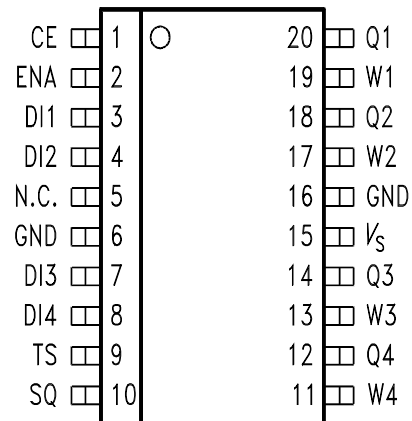
The internal current supply B and the undervoltage monitor UV ensure that in case of a supply voltage that is below the  $V_S$  turn-OFF threshold, outputs Q and SQ are disabled and the inputs go high-impedance. Basic functioning is possible within the range from  $V_S$  turn-OFF threshold to 4.5 V.

In case of overcurrent or short-circuit to ground at any output stage the signaling output (SQ) will go low. In clock-governed operation (i.e. when there is automatic switching-ON by the clock and not by a key), SQ goes high and low at the clock rate as long as a short-circuit or overload is present. SQ is an open-collector output.

Any input and output is ESD proof within the limit values.

## Pin Configuration (top view)

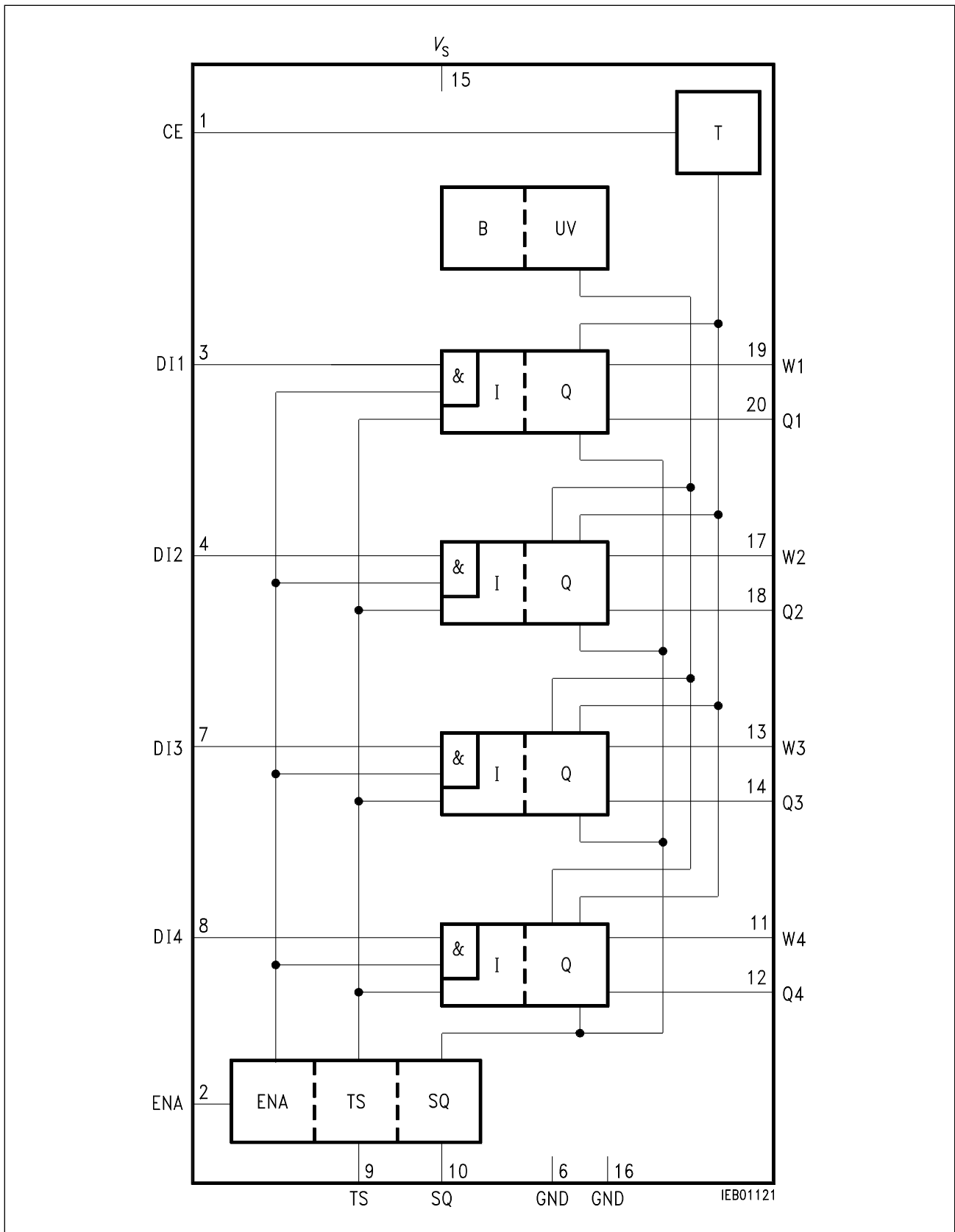
### P-DSO-20-7



IEP01120

## Pin Definitions and Functions

Pin	Symbol	Function
1	CE	Pin for $C_e$
2	ENA	Enable input for drivers 1 to 4
3	DI1	Input driver 1
4	DI2	Input driver 2
5	N.C.	Not connected
6	GND	Ground
7	DI3	Input driver 3
8	DI4	Input driver 4
9	TS	Threshold changeover for all inputs
10	SQ	Short-circuit signaling output for drivers 1 to 4
11	W4	Output current sensor driver 4
12	Q4	Output driver 4
13	W3	Output current sensor driver 3
14	Q3	Output driver 3
15	$V_s$	Supply voltage
16	GND	Ground
17	W2	Output current sensor driver 2
18	Q2	Output driver 2
19	W1	Output current sensor driver 1
20	Q1	Output driver 1



Block Diagram

## Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_S$	- 0.3	40	V	
Supply voltage	$V_S$	- 0.3	45	V	100 ms, 5 s interval
Supply voltage	$V_S$	- 0.3	48	V	120 $\mu$ s
Reverse supply current in GND	$I_{GND}$		0.5	A	<sup>1) 4)</sup>
Input voltage at DI, ENA, TS	$V_{DI, ENA, TS}$	- 5	40	V	
Input voltage at DI, ENA, TS	$V_{DI, ENA, TS}$	- 5	45	V	100 ms, 5 s interval
Output voltage Q	$V_Q$	$V_S - 8$	$V_S$	V	min. - 0.3 V
Current in Q	$I_Q$	- 10	3	mA	<sup>18)</sup>
Voltage at W	$V_W$	$V_S - 6.5$	$V_S + 5$	V	min. - 0.3 V, max. 45
Voltage at W	$V_W$	$V_S - 12$	$V_S + 5$	V	min. - 0.3 V, max. 45 V <sup>2)</sup>
Voltage at CE	$V_C$	- 0.3	$V_S$	V	min. - 0.3 V, max. 45 V <sup>3)</sup>
Voltage at SQ	$V_{SQ}$	- 0.5	45	V	Output high
Input current DI, ENA, TS	$V_{DI, ENA, TS}$	- 3	3	mA	<sup>4)</sup>
Input current DI, ENA, TS	$V_{DI, ENA, TS}$	- 5	5	mA	100 ms, 5 s interval
Input current DI, ENA, TS	$V_{DI, ENA, TS}$	- 10	10	mA	10 $\mu$ s, 500 $\mu$ s interval

**Notes:** <sup>1)</sup> An adequate resistor in the GND line can provide protection in case of wrong polarization of  $V_S$ . It should be noted, however, that in this case all pins may become conductive across GND.

<sup>2)</sup> Loading may lead to degradation and thus to a shift of the switching threshold at W. (Characteristics: switching threshold at W).

Short loading may lead to a deviation of approx. 20 mV.

<sup>3)</sup> In case of short-circuit of  $V_S$ , the capacitance stored in  $C_e$  during previous operation will not damage the IC.

<sup>4)</sup> Note the power loss.

## Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Current in SQ	$I_{SQ}$	- 3	8	mA	Output low 1 ms, 50 ms interval <sup>5)</sup> 10 μs, 500 μs interval <sup>5)</sup>
Current in W	$I_W$	- 5	5	mA	
Current in W	$I_W$	- 10	10	mA	
Junction temperature	$T_j$	- 40	150	°C	6)
Storage temperature	$T_{stg}$	- 50	150	°C	
Therm. resistance, system-ambient	$R_{th SA}$		95	K/W	
Therm. resistance, system-packag.	$R_{th SP}$		25	K/W	
ESD strength acc. to MIL - hrs. 883 Meth. 3015 (100 pF/1.5 kΩ, 5 discharges/polarity)	$V_{ESD}$	- 2	2	kV	
Burst strength of the inputs/ outputs Q and W connected to the power transistors (in acc. with IEC publ. 801-4)	$V_{Burst}$	300		V	7)
Junction temperature in normal operation during 15 years with 100 % ED	$T_{j15}$		125	°C	8)

**Notes:** <sup>5)</sup> Loading may lead to degradation and thus to a shift of the switching threshold at W. Unfrequent loading leads to a deviation of approx. 20 mV.

<sup>6)</sup> Related to GND; the GND pins are connected with the chip carrier via the leadframe.

<sup>7)</sup> If it can be proved with samples.

<sup>8)</sup> During normal operation, the failure rate is  $\leq 100$  fit acc. to SN 29500 at a junction temperature of 75 °C.

## Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage <sup>11)</sup>	$V_S$	4.5	40	V	$V_{TS} = 0 \dots 1.5 \text{ V}$
Supply voltage <sup>12)</sup>	$V_S$	$V_{TS} + 3$	40	V	$V_{TS} = 1.5 \dots 7 \text{ V}$
Supply voltage <sup>13)</sup>	$V_S$	10	40	V	$V_{TS} = V_S$
Supply voltage rise	$dV_S/dt$	- 1	1	V/ $\mu$ s	<sup>20)</sup>
Junction temperature	$T_j$	- 25	150	$^{\circ}\text{C}$	
Time-determining capacitor of the clock generator	$C_e$	1	100	nF	<sup>10)</sup>
Input voltage	$V_{DI, ENA, TS}$	- 2	40	V	<sup>14) 15) 16) 17) 19)</sup>
Current at output SQ	$I_{SQ}$	- 1	6	mA	

- Notes:**
- <sup>9)</sup> W pins that remain open, must be connected to  $V_S$ .
  - <sup>10)</sup> The  $C_e$  value depends on the desired pulse width  $t_p$  during short circuit. It applies:  $C_e = 0.25 \text{ mS} \times t_p$ .
  - <sup>11)</sup> At an input threshold = 1.5 V
  - <sup>12)</sup> At an input threshold = 1.5 V to 7 V
  - <sup>13)</sup> At an input threshold = 7 V
  - <sup>14)</sup> This function is also ensured for  $40 \text{ V} \leq V_S \leq 45 \text{ V}$  and  $-40 \text{ }^{\circ}\text{C} \leq T_j \leq -25 \text{ }^{\circ}\text{C}$  as long as  $0 \text{ V} \leq V_{DI, ENA, TS} \leq 40 \text{ V}$ .
  - <sup>15)</sup> The outputs Q are disabled even if  $-3 \text{ V} \leq V_{DI, ENA} \leq -2 \text{ V}$  or  $-1 \text{ mA} \leq I_{DI, ENA} \leq 50 \text{ } \mu\text{A}$  and  $V_S - 5 \text{ V} \leq V_W \leq V_S + 5 \text{ V}$ , max. 45 V.
  - <sup>16)</sup> The outputs Q are enabled even if  $40 \text{ V} \leq V_{DI, ENA} \leq 45 \text{ V}$  and  $V_S - 0.2 \text{ V} \leq V_W \leq V_S + 5 \text{ V}$ , max. 45 V.
  - <sup>17)</sup> Current limiting and disabling of outputs Q are ensured even if  $40 \text{ V} \leq V_{DI, ENA} \leq 45 \text{ V}$  and  $V_S - 5 \text{ V} \leq V_W \leq V_S - 0.4 \text{ V}$ .
  - <sup>18)</sup> Dynamic charge reversal of a 2-nF capacitor as in **figure 1** is permissible (corresponds to short circuit to conducting output in P-channel MOSFET)
  - <sup>19)</sup> Proper working of the IC is also ensured if, before  $V_S$  is turned-On, an input voltage  $V_{DI, ENA}$  is present in the permissible range (footnote 15).
  - <sup>20)</sup> At 10 V/ $\mu$ s short-term malfunction is possible, but never a latch-up.

## Characteristics

Supply voltage  $4.5\text{ V} \leq V_S \leq 40\text{ V}$ , junction temperature  $-25\text{ °C} \leq T_j \leq 125\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	$I_{s, OFF}$			5	mA	$V_{ENA} = 0\text{ V}$ , $V_W = V_S$ <sup>4)</sup>
Current consumption	$I_{s, ON}$			13.5	mA	$V_{ENA} = V_{DI} = V_W = V_Q = V_S$ ; $V_{TS} = 0\text{ V}$ <sup>3)</sup>
H-input voltage at DI, ENA	$V_{IH}$	2			V	$V_{TS} = 0\text{ V}$
H-input voltage at DI, ENA	$V_{IH}$	6.8			V	$V_{TS} = V_S$
L-input voltage at DI, ENA	$V_{IL}$			0.7	V	$V_{TS} = 0\text{ V}$
L-input voltage at DI, ENA	$V_{IL}$			4.8	V	$V_{TS} = V_S$
Input hysteresis	$V_{HI}$	30	100	300	mV	$0\text{ V} \leq V_{TS} \leq V_S \leq 30\text{ V}$
	$V_{HI}$	30	100	300	mV	$2\text{ V} \leq V_{TS} \leq V_S$
Input current DI, ENA <sup>1), 7)</sup>	$I_{DI, ENA}$	50		200	$\mu\text{A}$	$1.5\text{ V} \leq V_{DI, ENA} \leq 30\text{ V}$
Input current DI, ENA	$I_{DIO, ENA0}$			100	$\mu\text{A}$	$0\text{ V} \leq V_{DI, ENA} \leq 30\text{ V}$ $V_S = 0\text{ V}$
L-output voltage at SQ	$V_{SQ, L}$			0.5	V	$I_{SQ} = 5\text{ mA}$ , $V_W = V_S - 2\text{ V}$
Leakage current output SQ	$I_{SQ, H}$			10	$\mu\text{A}$	$V_W = V_S$
Output current Q	$I_{Q0}$	0.6		1.6	mA	$V_S - 2\text{ V} \leq V_Q \leq V_S$
Current from TS	$-I_{TS}$	2	5	10	$\mu\text{A}$	$V_{TS} = 0.7\text{ V}$
Current in W	$I_W$			100	$\mu\text{A}$	$V_S - 2\text{ V} \leq V_W \leq V_S$
Switching threshold at W <sup>2)</sup>	$V_W$	$V_S - 0.25$	$V_S - 0.3$	$V_S - 0.35$	V	

Notes see page 11.

## Characteristics (cont'd)

Supply voltage  $4.5 \text{ V} \leq V_S \leq 40 \text{ V}$ , junction temperature  $-25 \text{ °C} \leq T_j \leq 125 \text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current in W	$I_W$			100	$\mu\text{A}$	$V_S - 2 \text{ V} \leq V_W \leq V_S$
Charge current from CE	$-I_{Ce}$		5		$\mu\text{A}$	
Discharge current from CE	$I_{Ce}$		235		$\mu\text{A}$	
Upper switching threshold at CE	$V_{CU}$			2.4	V	
Lower switching threshold at CE	$V_{CL}$			1.4	V	
$V_Q$ at overcurrent	$V_{QR}^{6)}$	$V_S - 0.4 \text{ V}$			V	$V_W = V_S - 2 \text{ V}$ , $I_Q = -20 \mu\text{A}$
$V_Q$ at output disable	$V_{QL}^{6)}$	$V_S - 0.4 \text{ V}$			V	$V_{ENA} = 0 \text{ V}$ , $I_Q = -20 \mu\text{A}$ , $0 \text{ V} \leq V_S \leq 40 \text{ V}$
Signal run time LH	$t_{PLH}$			50	$\mu\text{s}$	
Signal run time HL	$t_{PHL}$			50	$\mu\text{s}$	
Pulse width	$t_P$	33	45	65	$\mu\text{s}$	$C_e = 10 \text{ nF}$
Duty cycle	$t_P/t_0$	1:55	1:47	1:40		$C_e = 10 \text{ nF}$
Delay time of the short-circuit signaling	$t_{PWM}^{5)}$			10	$\mu\text{s}$	$V_C = 0 \text{ V}$
Duration of the negative spikes at input W, which do not result in switching off	$t_{VZ}$	1			$\mu\text{s}$	

Notes see page 11.

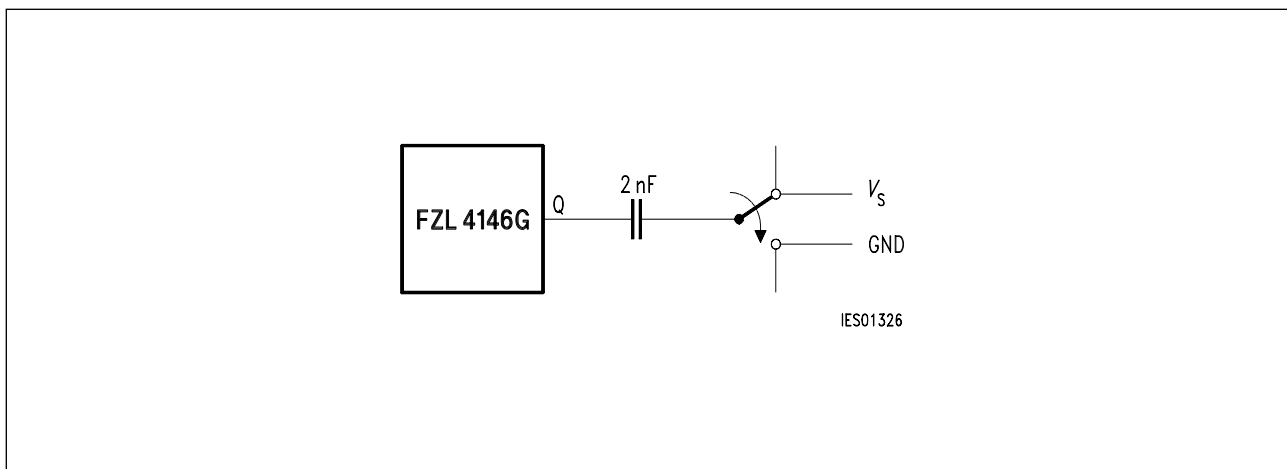
**Characteristics (cont'd)**

Supply voltage  $4.5\text{ V} \leq V_S \leq 40\text{ V}$ , junction temperature  $-25\text{ °C} \leq T_j \leq 125\text{ °C}$

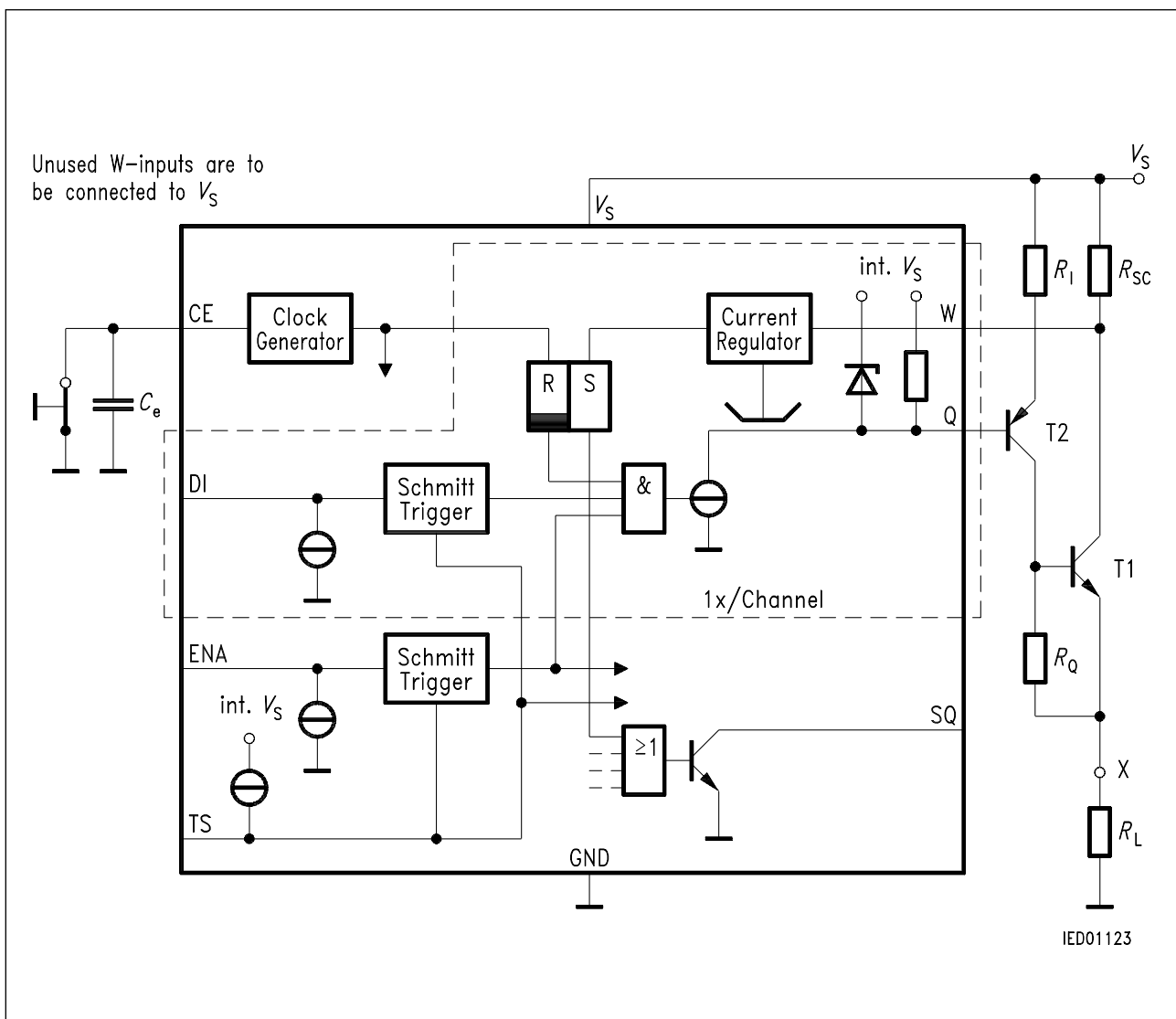
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Difference between $V_{TS}$ and input switching threshold ENA, DI during transition from L to H	$V_{DIH} - V_{TS}$	-0.2		0.2	V	$2\text{ V} \leq V_{TS} \leq 4.8\text{ V}$
Idling voltage at output Q	$V_{QH}$	$V_S - 13$	$V_S - 11.5$	$V_S - 10$	V	$V_S \geq 18\text{ V}$
$V_S$ turn-Off threshold	$V_{TSV}$	2.5		4.5	V	$V_Q > V_{QL};$ $I_Q = -20\text{ }\mu\text{A}$
Resistance across Q and $V_S$	$R_Q$	8	13	19	k $\Omega$	$V_{ENA} = 0\text{ V};$ $I_Q = -100\text{ }\mu\text{A}$ $R_Q = (V_S - V_Q)/0.1\text{ mA}$
Z-diode internal resistance	$R_Z$		20	50	$\Omega$	$V_{ENA} = 0\text{ V};$ $I_{Q1} = -3\text{ mA}$ $I_{Q2} = -8\text{ mA},$ $R_Q = \Delta V_Q/5\text{ mA}$

**Footnotes for the Characteristics**

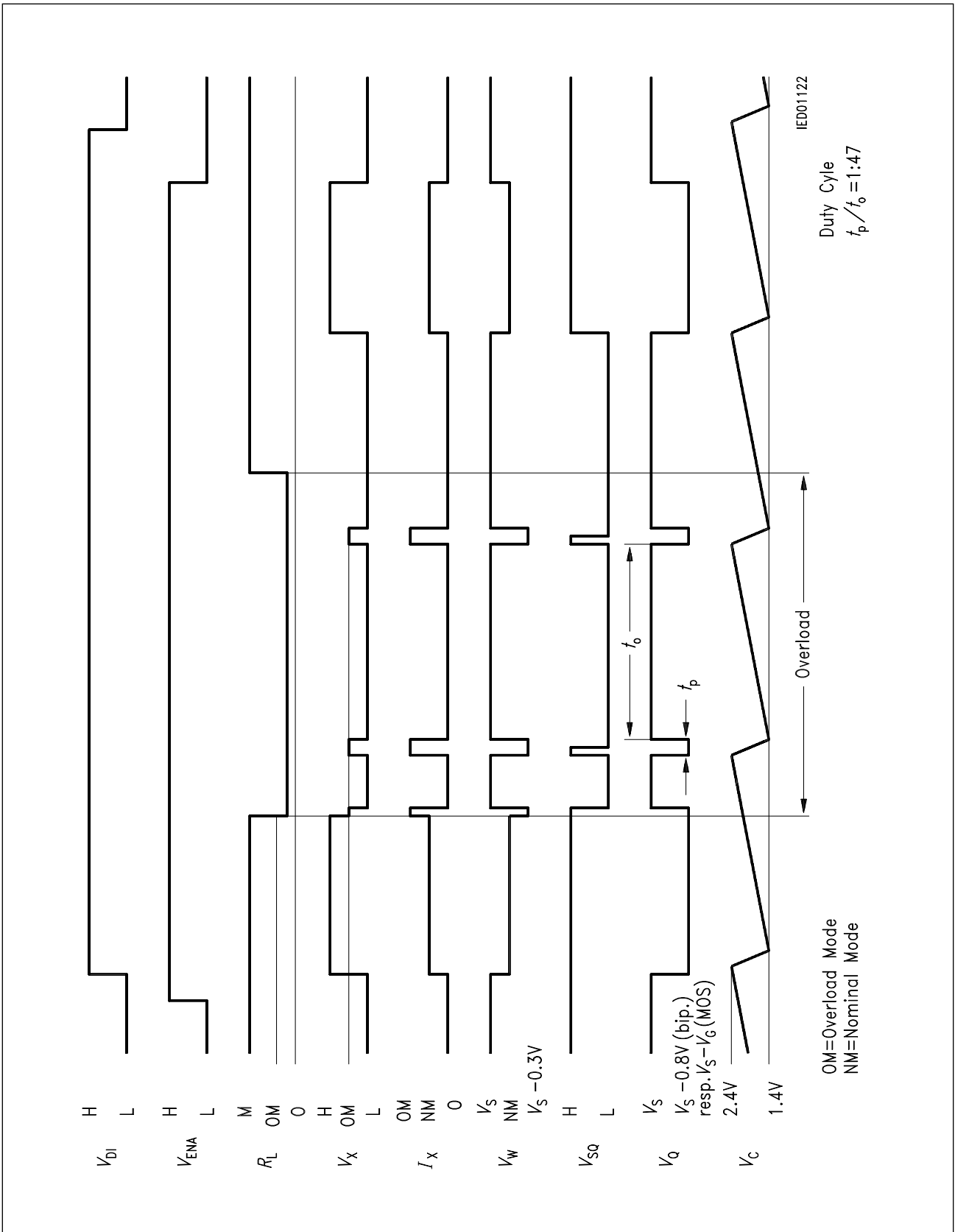
- 1) The given limit values apply to inputs DI, ENA, if they are not measured, from 0 to 40 V.
- 2) The layout provides an adaption of  $V_{wtyp.}$  from  $V_S - 0.3\text{ V}$  to  $V_S - 0.4\text{ V}$  or  $V_S - 0.48\text{ V}$  by simply changing of the ALU mask.
- 3) All inputs DI1 to DI4 and W1 to W4 as well as Q1 to Q4  
 $I_{SON}$  means the sum of all currents flowing from the voltage source  $V_S$  into the IC, i.e.  
 $I_{SON} = I_S + \sum I_{DI} + \sum I_{ENA} + \sum I_W + \sum I_Q.$
- 4) All other pins are open.
- 5) The delay time of loop  $W \rightarrow I$  regulator  $\rightarrow$  RS-FF  $\rightarrow$  AND  $\rightarrow$  current source  $\rightarrow$  Q is unaccessible for measurement without external wiring due to fast reaction of the current regulator. For this reason, in case of overload, the above mentioned switch-OFF delay time is replaced by the delay time for input  $W \rightarrow$  output SQ.  
 Measurement: jump function at W from  $V_W = V_S$  to  $V_W = V_S - 1\text{ V}$
- 6)  $I_Q$  = leakage current  $I_{CBO}$  of the external PNP-driver transistor
- 7) For  $V_{DI, TS} < 1.5\text{ V}$ ,  $I_{DI, ENA}$  remains below its minimum value; it is however ensured that in case of open inputs the corresponding outputs will be safely disabled.



**Figure 1**



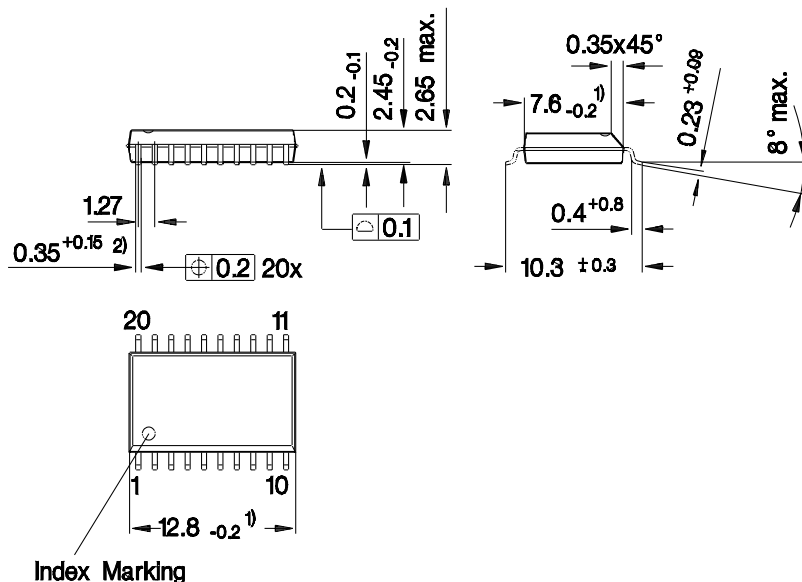
**Figure 2**  
**Application Circuit**



**Figure 3**  
**Operating Mode: Automatic Turn-ON after Overload**

## Package Outlines

### P-DSO-20-7 (Plastic Dual Small Outline Package)



- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion

GPS05094

### Sorts of Packing



Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

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