



# FXM2IC102

## 2-Bit I<sup>2</sup>C Bus Interface Voltage Translator / Repeater

### Features

- Bi-Directional Interface between any Two Levels from 1.65V to 5.5V
- Auto-Direction Sensing, Direction Control not Needed
- Buffer Isolates Capacitance and Allows 400pF on Each Port
- Open-Drain Inputs/Outputs
- Schmitt Trigger Data Inputs
- Accommodates Standard-Mode and Fast-Mode I<sup>2</sup>C-bus Devices
- Fully Configurable: Inputs and Outputs Track V<sub>CC</sub> Level
- Non-Preferential Power-up; Either V<sub>CC</sub> May be Powered Up First
- Outputs Remain in 3-State until Active V<sub>CC</sub> Level is Reached
- Power-Off High Impedance
- Active HIGH Output Enable Referenced to V<sub>CCA</sub>
- 5V-Tolerant Output Enable
- Packaged in 8-Terminal Leadless MicroPak™ (1.6mm x 1.6mm)
- ESD Protection Exceeds:
  - 8kV HBM ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 15kV HBM I/O to GND ESD (per JESD22-A114 & Mil Std 883e 3015.7)

### Description

The FXM2IC102 is a configurable dual-voltage-supply translator designed for bi-directional voltage translation over a wide range of input and output voltage levels.

The FXM2IC102 is intended for use as a voltage translator in applications using the I<sup>2</sup>C bus interface. Input and output voltage levels are compatible with I<sup>2</sup>C device specification voltage levels.

The device is designed so that the A port tracks the V<sub>CCA</sub> level and the B port tracks the V<sub>CCB</sub> level. This allows for bi-directional voltage translation over voltage ranges: 1.8V, 2.5V, 3.3V, and 5.0V.

The device remains in 3-state until both V<sub>CCS</sub> reach active levels, allowing either V<sub>CC</sub> to be powered up first. Internal power-down control circuits place the device in 3-state if either V<sub>CC</sub> is removed.


The two ports of the device have auto-direction sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

Schmitt triggers are used on data inputs for signal noise suppression. Typically the inputs have 100 millivolts of hysteresis over the full V<sub>CC</sub> range.

The FXM2IC102 typically consumes only 230nA during “no I<sup>2</sup>C data transactions” when V<sub>CCA</sub> = 1.8V and V<sub>CCB</sub> = 3.3V. See Figure 4 and Figure 5 for more details.

FXM2IC102 exhibits robust I<sup>2</sup>C repeater performance due to strong current sinking capability in > 400pf bus segments. See Figure 6 and Figure 7 for details.

### Ordering Information

Part Number	Operating Temperature Range	Top Mark	 Eco Status	Package	Packing Method
FXM2IC102L8X	-40 to +85°C	XG	Green	8-Lead MicroPak, 1.6mm Wide	3000 Units on Tape and Reel

 For Fairchild's definition of Eco Status, please visit: [http://www.fairchildsemi.com/company/green/rohs\\_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html).

## Pin Configuration

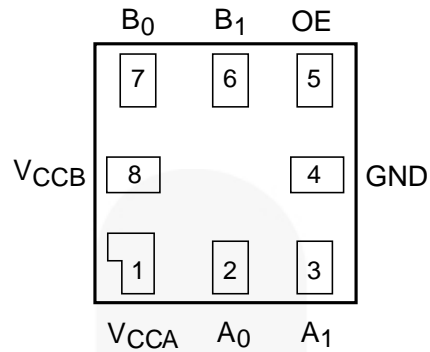


Figure 1. Pin Configuration (Top-Through View)

## Pin Definitions

Pin #	Name	Description
1	$V_{CCA}$	A-Side Power Supply
2, 3	$A_0, A_1$	A-Side Inputs or 3-State Outputs
4	GND	Ground
5	OE	Output Enable Input
6, 7	$B_1, B_0$	B-Side Inputs or 3-State Outputs
8	$V_{CCB}$	B-Side Power Supply

## Functional Diagram

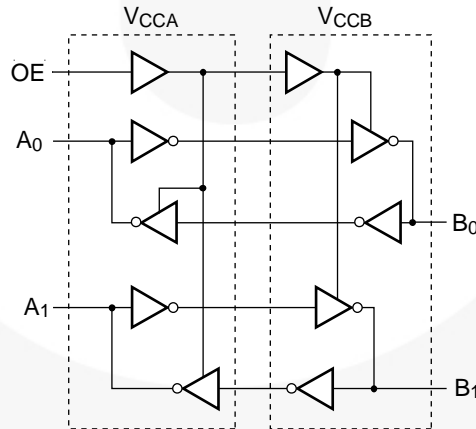


Figure 2. Functional Diagram

## Truth Table

Control	Outputs
OE	
LOW Logic Level	3-State
HIGH Logic Level	Normal Operation

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
$V_{CCA}, V_{CCB}$	Supply Voltage		-0.5	7.0	V
$V_{IN}$	DC Input Voltage	A Port	-0.5	7.0	
		B Port	-0.5	7.0	
		Control Input (OE)	-0.5	7.0	
$V_O$	Output Voltage <sup>(1)</sup>	$A_n$ Outputs 3-State	-0.5	7.0	V
		$B_n$ Outputs 3-State	-0.5	7.0	
		$A_n$ Outputs Active	-0.5	$V_{CCA} + 0.5V$	
		$B_n$ Outputs Active	-0.5	$V_{CCB} + 0.5V$	
$I_{IK}$	DC Input Diode Current	At $V_{IN} < 0V$		-50	mA
$I_{OK}$	DC Output Diode Current	At $V_O < 0V$		-50	mA
		At $V_O > V_{CC}$		+50	
$I_{OH} / I_{OL}$	DC Output Source/Sink Current		-50	+50	mA
$I_{CC}$	DC $V_{CC}$ or Ground Current per Supply Pin			±100	mA
$T_{STG}$	Storage Temperature Range		-65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		8000	V
		Charged Device Model, JESD22-C101		2000	

**Note:**

- $I_O$  absolute maximum rating must be observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Units
$V_{CCA}, V_{CCB}$	Power Supply Operating		1.65	5.50	V
$V_{IN}$	Input Voltage	A Port	0	5.5	V
		B Port	0	5.5	
		Control Input (OE)	0	$V_{CCA}$	
$\Delta_t / \Delta_V$	Maximum Input Edge Rate	$V_{CCA/B} = 1.65V$ to $5.5V$		200	ns/V
$T_A$	Free Air Operating Temperature		-40	+85	°C

**Note:**

- All unused inputs and I/O pins must be held at  $V_{CCI}$  or GND.  $V_{CCI}$  is the  $V_{CC}$  associated with the input side.

## Power-Up/Power-Down Sequencing

FXM translators offer an advantage in that either  $V_{CC}$  may be powered up first. This benefit derives from the chip design. When either  $V_{CC}$  is at 0V, outputs are in a high-impedance state. The control input (OE) is designed to track the  $V_{CCA}$  supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

The recommended power-up sequence is:

1. Apply power to the first  $V_{CC}$ .
2. Apply power to the second  $V_{CC}$ .
3. Drive the OE input HIGH to enable the device.

The recommended power-down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either  $V_{CC}$ .
3. Remove power from other  $V_{CC}$ .

## Application Circuit

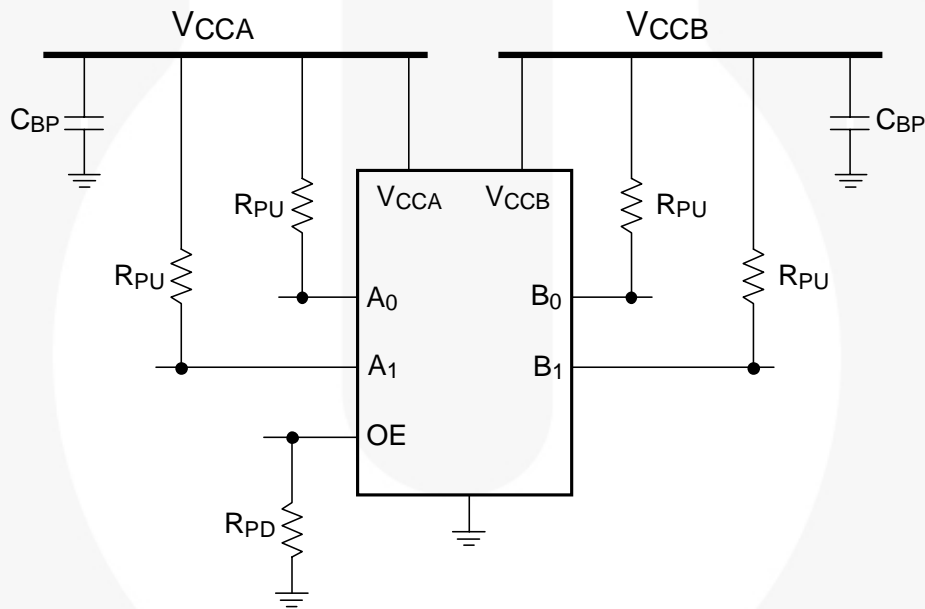


Figure 3. Application Circuit

## Application Notes

The FXM2IC102 has open-drain outputs and requires pull-up resistors on the four data I/O pins, as shown in Figure 3. If a pair of data I/O pins ( $A_n/B_n$ ) is not used, both pins should be tied to GND (or both to  $V_{CC}$ ). In this case, pull-down or pull-up resistors are not required.

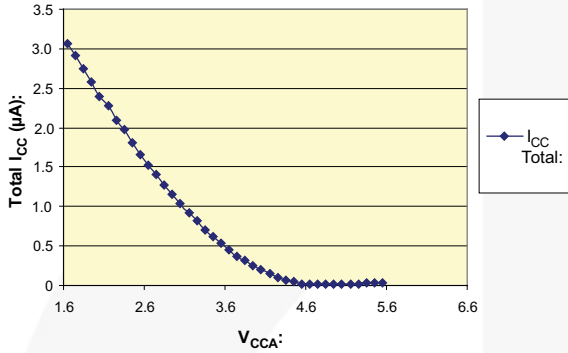
The recommended values for the pull-up resistors ( $R_{PU}$ ) are 1k $\Omega$  minimum to 10k $\Omega$  maximum. The recommended value for the bypass capacitors ( $C_{BP}$ ) is 0.1 $\mu$ F. The recommended value for the pull-down resistor ( $R_{PD}$ ) on OE is 1k $\Omega$  or higher and may depend upon the current-sinking capability of the device driving the OE pin.

### Low I<sub>CC</sub> During I<sup>2</sup>C Idle

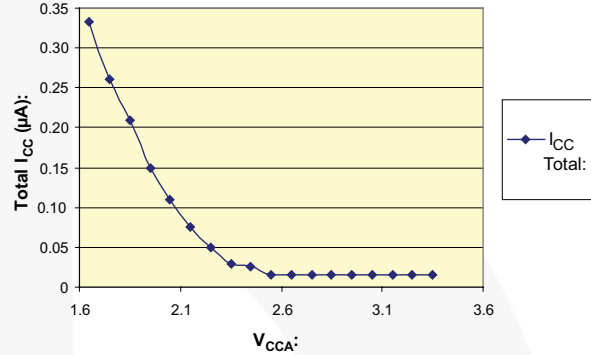
In a typical Mobile Internet Device (MID) application, I<sup>2</sup>C data transactions are idle the vast majority of the time. Therefore, it is critical that the I<sup>2</sup>C translator burns as little current as possible when no data transactions are passing across the I<sup>2</sup>C bus. Figure 4 and Figure 5 plot the typical FXM2IC102 I<sub>CC</sub> performance across the entire voltage translation range during no I<sup>2</sup>C data

transactions. In Figure 4, V<sub>CCB</sub> = 5.5V and in Figure 5, V<sub>CCB</sub> = 3.3V.

For example, to translate from 1.8V to 3.3V (Figure 5), with no I<sup>2</sup>C data transactions present, the total I<sub>CC</sub> of the FXM2IC102 is typically only 230nA. In effect, the FXM2IC102 virtually powers itself down when the I<sup>2</sup>C bus is idle.



**Figure 4. FXM2IC102 I<sub>CC</sub> vs. V<sub>CCA</sub> Sweep During no I<sup>2</sup>C Data Transactions (V<sub>CCB</sub> = 5.5V. T<sub>A</sub> = +25°C)**



**Figure 5. FXM2IC102 I<sub>CC</sub> vs. V<sub>CCA</sub> Sweep During no I<sup>2</sup>C Data Transactions (V<sub>CCB</sub> = 3.3V. T<sub>A</sub> = +25°C)**

**Note:**

3. Figure 4 depicts the typical I<sub>CC</sub> of the FXM2IC102 when translating from 5.5V on the V<sub>CCB</sub> supply to a range of 1.65V – 5.5V on the V<sub>CCA</sub> supply.

**Note:**

4. Figure 5 depicts the typical I<sub>CC</sub> of the FXM2IC102 when translating from 3.3V on the V<sub>CCB</sub> supply to a range of 1.65V – 3.3V on the V<sub>CCA</sub> supply.

## What Makes a Good I<sup>2</sup>C Repeater?

The I<sup>2</sup>C specification identifies the maximum number of devices allowed on an I<sup>2</sup>C segment as 400pf. Therefore, when an I<sup>2</sup>C segment exceeds 400pf, a repeater is required to split the segment into two, whereby each of the individual I<sup>2</sup>C segments does not exceed 400pf.

The question then arises, “What makes a good I<sup>2</sup>C repeater?” The question becomes complicated when considering the following factors:

- Current sinking capability of the outputs
- Output edge rates
- Distributed and lumped capacitances of the I<sup>2</sup>C segment
- Speed of the I<sup>2</sup>C bus: standard mode (100kbits/s), fast mode (400kbit/s), or fast-mode plus (1000kbit/s)
- Pull-up resistor sizing
- System signal delays, including device propagation delay and time of flight vs. meeting critical data setup/hold times
- Multiple master / slave topologies
- Clock stretching

It is possible to simplify this by focusing on the output current sinking capability relative to the bus impedance.

The DC electrical tables of the I<sup>2</sup>C specification, for fast mode, require a maximum V<sub>OL</sub> of 0.4V while sinking 3mA of current when V<sub>DD</sub> > 2V, and a maximum V<sub>OL</sub> of 0.2 \* V<sub>DD</sub>, while sinking 3mA when V<sub>DD</sub> < 2V. The

minimum I<sub>OL</sub> is 3mA for a V<sub>OL</sub> of 0.4V and 6mA for a V<sub>OL</sub> of 0.6V.

In short, the more a repeater can sink current while maintaining the maximum V<sub>OL</sub>, the more capacitance it can drive at a given data rate. The I<sup>2</sup>C specifically benchmarks this by stating: “to drive a full bus load at 400kHz, 6mA I<sub>OL</sub> is required at 0.6V V<sub>OL</sub>. Parts not meeting this specification can still function, but not at 400kHz and 400pF”.

As shown in Figure 6, the FXM2IC102 can typically sink 11mA – 13mA, depending on temperature, while maintaining a V<sub>OL</sub> of 0.33V when V<sub>DD</sub> is only 1.65V. This says the FXM2IC102 delivers conservatively twice the current sinking capability for a 400pF, 1.65V segment running at 400kHz.

If V<sub>DD</sub> = 1.95V, (Figure 7) the FXM2IC102 can sink 18mA – 21mA, depending on temperature, while maintaining a V<sub>OL</sub> of 0.39V. This says the FXM2IC102 delivers conservatively 3 times the current sinking capability for a 400pF, 1.95V segment running at 400kHz.

If V<sub>DD</sub> = 3.0V, the FXM2IC102 can sink 25mA – 30mA, depending on temperature, while maintaining a V<sub>OL</sub> of 0.4V. This says the FXM2IC102 delivers conservatively 4x the current sinking capability for a 400pF, 3.0V segment running at 400kHz.

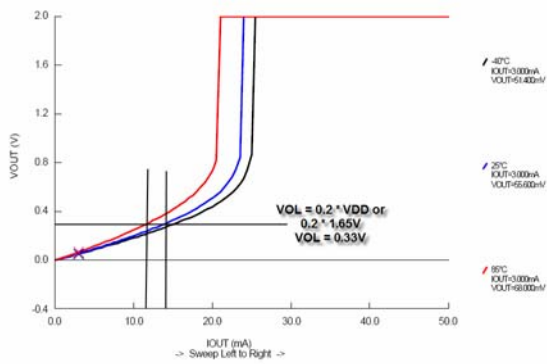


Figure 6. V<sub>OL</sub> vs. I<sub>OL</sub> (V<sub>DD</sub> = 1.65V)

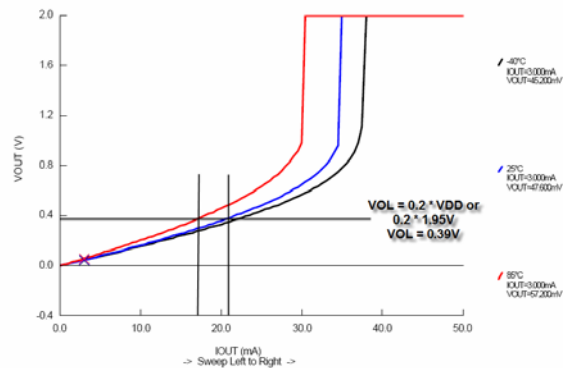


Figure 7. V<sub>OL</sub> vs. I<sub>OL</sub> (V<sub>DD</sub> = 1.95V)

## DC Electrical Characteristics

T<sub>A</sub> = -40°C to +85°C.

Symbol	Parameter	Conditions		V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Min.	Max.	Units
V <sub>IHA</sub>	High Level Input Voltage A	Data Inputs A <sub>n</sub>		1.65–5.50	1.65–5.50	0.7 x V <sub>CCA</sub>		V
		Control Input OE		1.65–5.50	1.65–5.50	0.9 x V <sub>CCA</sub>		
V <sub>IHB</sub>	High Level Input Voltage B	Data Inputs B <sub>n</sub>		1.65–5.50	1.65–5.50	0.7 x V <sub>CCB</sub>		V
V <sub>ILA</sub>	Low Level Input Voltage A	Data Inputs A <sub>n</sub>		1.65–5.50	1.65–5.50		0.3 x V <sub>CCA</sub>	V
		Control Input OE		1.65–5.50	1.65–5.50		0.1 x V <sub>CCA</sub>	
V <sub>ILB</sub>	Low Level Input Voltage B	Data Inputs B <sub>n</sub>		1.65–5.50	1.65–5.50		0.3 x V <sub>CCB</sub>	V
V <sub>OLA</sub>	Low Level Output Voltage A <sup>(5)</sup>	A Port	I <sub>OL</sub> = 3mA	1.65–2.30	1.65–5.50		0.1 x V <sub>CCA</sub>	V
			I <sub>OL</sub> = 6mA	3.00–5.50	1.65–5.50		0.2	
V <sub>OLB</sub>	Low Level Output Voltage B <sup>(5)</sup>	B Port	I <sub>OL</sub> = 3mA	1.65–5.50	1.65–2.30		0.1 x V <sub>CCB</sub>	V
			I <sub>OL</sub> = 6mA	1.65–5.50	3.00–5.50		0.2	
I <sub>L</sub>	Input Leakage Current	Control Input OE, V <sub>IN</sub> = V <sub>CCA</sub> or GND		1.65–5.50	1.65–5.50		±1.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	A <sub>n</sub>	V <sub>IN</sub> or V <sub>O</sub> = 0V to 5.5V	0	5.50		±2.0	μA
		B <sub>n</sub>	V <sub>IN</sub> or V <sub>O</sub> = 0V to 5.5V	5.50	0		±2.0	
I <sub>OZ</sub>	3-State Output Leakage <sup>(6)</sup>	A <sub>n</sub> , B <sub>n</sub>	V <sub>O</sub> = 0V to 5.5V, OE = V <sub>IL</sub>	5.50	5.50		±2.0	μA
		A <sub>n</sub>	V <sub>O</sub> = 0V to 5.5V, OE = Don't Care	5.50	0		±2.0	
		B <sub>n</sub>	V <sub>O</sub> = 0V to 5.5V, OE = Don't Care	0	5.50		±2.0	
I <sub>CCA/B</sub>	Quiescent Supply Current <sup>(7,8)</sup>	V <sub>IN</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0		1.65–5.50	1.65–5.50		5.0	μA
I <sub>CCZ</sub>	Quiescent Supply Current <sup>(7)</sup>	V <sub>IN</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0, OE = V <sub>IL</sub>		1.65–5.50	1.65–5.50		5.0	μA
I <sub>CCA</sub>	Quiescent Supply Current <sup>(6)</sup>	V <sub>IN</sub> = 5.5V or GND, I <sub>O</sub> = 0, OE = Don't Care, B <sub>n</sub> to A <sub>n</sub>		0	1.65–5.50		-2.0	μA
				1.65–5.50	0		2.0	
I <sub>CCB</sub>	Quiescent Supply Current <sup>(6)</sup>	V <sub>IN</sub> = 5.5V or GND, I <sub>O</sub> = 0, OE = Don't Care, A <sub>n</sub> to B <sub>n</sub>		1.65–5.50	0		-2.0	μA
				0	1.65–5.50		2.0	

### Notes:

- This is the output voltage for static conditions. Dynamic drive specifications are given in the Dynamic Output Electrical Characteristics table.
- “Don't Care” indicates any valid logic level.
- V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input side.
- Reflects current per supply, V<sub>CCA</sub> or V<sub>CCB</sub>.

## Dynamic Output Electrical Characteristics

Output rise / fall time and dynamic output current<sup>(9)</sup>. Output load:  $C_L = 50\text{pF}$ ,  $R_L = 1\text{k}\Omega$ .  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

Symbol	Parameter	$V_{CCO}$ <sup>(10)</sup>								Units
		4.5 to 5.5V		3.0 to 3.6V		2.3 to 2.7V		1.65 to 1.95V		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
$t_{\text{rise}}$	Output Rise Time, A Port, B Port <sup>(11)</sup>		4		5		6		8	ns
$t_{\text{fall}}$	Output Fall Time, A Port, B Port <sup>(12)</sup>		4		5		6		8	ns
$I_{\text{OHD}}$	Dynamic Output Current HIGH <sup>(11)</sup>	-45		-24		-15		-8		mA
$I_{\text{OLD}}$	Dynamic Output Current LOW <sup>(12)</sup>	+45		+24		+15		+8		mA

### Notes:

9. Dynamic output characteristics are guaranteed, but not tested.
10.  $V_{CCO}$  is the  $V_{CC}$  associated with the output side.
11. See Figure 12.
12. See Figure 13.

## Maximum Data Rate<sup>(13)</sup>

Output Load:  $C_L = 50\text{pF}$ ,  $R_L = 1\text{k}\Omega$ .  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

$V_{CCA}$	$V_{CCB}$ :				Units
	4.5 to 5.5V	3.0 to 3.6V	2.3 to 2.7V	1.65 to 1.95V	
	Min.	Min.	Min.	Min.	
4.5V to 5.5V	40	35	30	20	MHz
3.0V to 3.6V	35	35	30	20	MHz
2.3V to 2.7V	30	30	25	20	MHz
1.65V to 1.95V	20	20	20	20	MHz

### Notes:

13. Maximum data rate is guaranteed, but not tested.

## Capacitance

$T_A = +25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Typical	Units
$C_{\text{IN}}$	Input Capacitance Control Pin (OE)	$V_{CCA} = V_{CCB} = \text{GND}$	4	pF
$C_{\text{I/O}}$	Input/Output Capacitance, $A_n$ , $B_n$	$V_{CCA} = V_{CCB} = 5.0\text{V}$ , $\text{OE} = V_{CCA}$	6	pF
$C_{\text{pd}}$	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 5.0\text{V}$ , $V_{\text{IN}} = 0\text{V}$ or $V_{\text{CC}}$ , $f = 10\text{MHz}$	40	pF

## AC Characteristics

Output Load:  $C_L = 50\text{pF}$ ,  $R_L = 1\text{k}\Omega$ .  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

Symbol	Parameter	$V_{CCB}$ :								Units
		4.5 to 5.5V		3.0 to 3.6V		2.3 to 2.7V		1.65 to 1.95V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b><math>V_{CCA} = 4.5</math> to <math>5.5\text{V}</math></b>										
$t_{PLH}$	A to B	1.0	4.5	1.5	5.5	2.0	7.0	3.0	11.5	ns
	B to A	1.0	4.5	1.5	5.5	1.5	6.5	2.5	9.5	
$t_{PHL}$	A to B	2.0	6.0	2.5	6.5	3.0	8.0	4.0	12.5	ns
	B to A	2.0	6.0	2.5	7.0	3.0	8.0	3.5	12.0	
$t_{PZL}$	OE to A		9.5		10.0		11.5		18.0	ns
	OE to B		9.0		11.0		13.5		22.0	
$t_{PLZ}$	OE to A		26.5		26.5		26.5		26.5	ns
	OE to B		26.0		26.5		20.5		15.5	
$t_{skew}$	A Port, B Port <sup>(14)</sup>		0.5		0.5		0.5		0.5	ns
<b><math>V_{CCA} = 3.0</math> to <math>3.6\text{V}</math></b>										
$t_{PLH}$	A to B	1.5	5.5	1.5	6.5	2.0	8.0	3.0	12.0	ns
	B to A	1.5	5.5	1.5	6.5	2.0	7.5	2.5	10.5	
$t_{PHL}$	A to B	2.5	7.0	2.5	7.5	3.0	9.0	4.0	13.0	ns
	B to A	2.5	6.5	2.5	7.5	3.0	9.5	4.0	13.0	
$t_{PZL}$	OE to A		12.5		13.0		15.5		21.0	ns
	OE to B		10.0		12.5		14.5		22.5	
$t_{PLZ}$	OE to A		27.5		28.0		28.0		28.0	ns
	OE to B		27.5		28.0		28.5		22.5	
$t_{skew}$	A Port, B Port <sup>(14)</sup>		0.5		0.5		0.5		0.5	ns
<b><math>V_{CCA} = 2.3</math> to <math>2.7\text{V}</math></b>										
$t_{PLH}$	A to B	1.5	6.5	2.0	7.5	2.5	8.5	3.5	12.5	ns
	B to A	2.0	7.5	2.0	8.0	2.5	8.5	3.0	11.5	
$t_{PHL}$	A to B	3.0	8.5	3.0	9.5	3.0	10.0	4.0	13.5	ns
	B to A	3.0	8.0	3.0	9.0	3.0	10.0	4.5	14.0	
$t_{PZL}$	OE to A		16.0		16.5		18.0		23.5	ns
	OE to B		11.0		14.0		15.5		23.5	
$t_{PLZ}$	OE to A		29.0		29.0		29.5		29.5	ns
	OE to B		29.0		29.0		29.5		29.5	
$t_{skew}$	A Port, B Port <sup>(14)</sup>		0.5		0.5		0.5		0.5	ns
<b><math>V_{CCA} = 1.65</math> to <math>1.95\text{V}</math></b>										
$t_{PLH}$	A to B	2.5	9.5	2.5	10.5	3.0	11.5	4.0	15.0	ns
	B to A	3.0	11.5	3.0	12.0	3.5	12.5	4.0	15.0	
$t_{PHL}$	A to B	3.5	11.5	4.0	12.5	4.5	14.0	5.0	15.5	ns
	B to A	4.0	12.5	4.0	13.0	4.0	13.5	5.0	15.5	
$t_{PZL}$	OE to A		27.0		27.0		27.0		30.0	ns
	OE to B		18.0		19.5		22.5		29.0	
$t_{PLZ}$	OE to A		34.0		34.0		34.5		35.0	ns
	OE to B		31.5		32.5		33.5		36.5	
$t_{skew}$	A Port, B Port <sup>(14)</sup>		0.5		0.5		0.5		0.5	ns

### Note:

14. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port ( $A_n$  or  $B_n$ ) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) (see Figure 15). Skew is guaranteed, but not tested.

## Applications Test Circuit

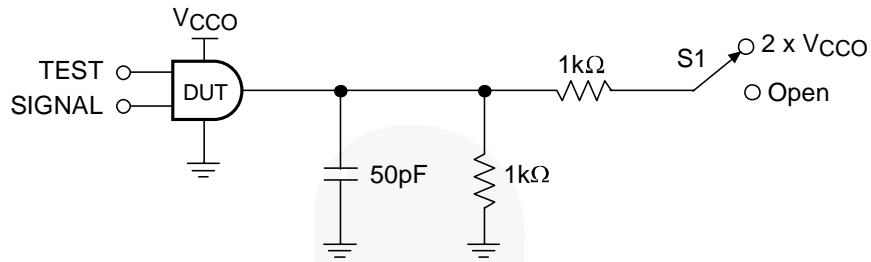


Figure 8. AC Test Circuit

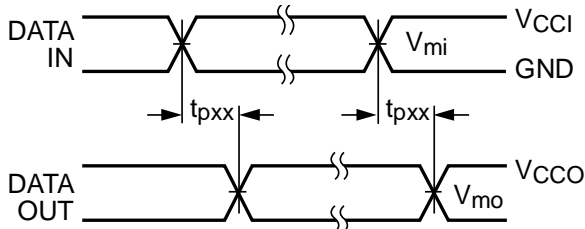
Table 1. Propagation Delay Table

Test	Input Signal	Output Enable Control	S1 Position
$t_{PLH}$ , $t_{PHL}$	Data Pulses	$V_{CCA}$	Open
$t_{PZL}$ (OE to $A_n$ , $B_n$ )	0V	LOW to HIGH Switch	$2 \times V_{CCO}$
$t_{PLZ}$ (OE to $A_n$ , $B_n$ )	0V	HIGH to LOW Switch	$2 \times V_{CCO}$

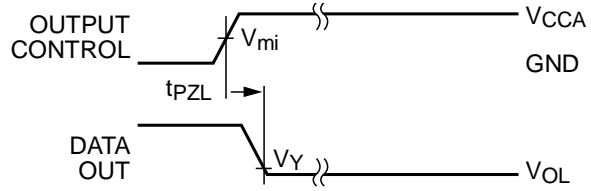
Table 2. AC Load Table

$V_{CCO}$	$C_L$	$R_L$
$1.8 \pm 0.15V$	50pF	1kΩ
$2.5 \pm 0.2V$	50pF	1kΩ
$3.3 \pm 0.3V$	50pF	1kΩ
$5.0 \pm 0.5V$	50pF	1kΩ

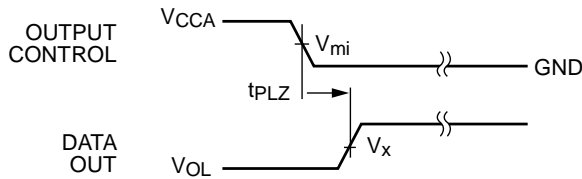
## Timing Diagrams



**Figure 9. Waveform for Inverting and Non-Inverting Functions<sup>(15)</sup>**

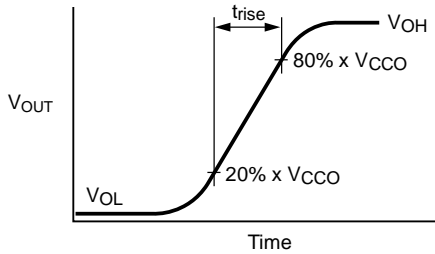


**Figure 10. 3-STATE Output Low Enable Time<sup>(15)</sup>**



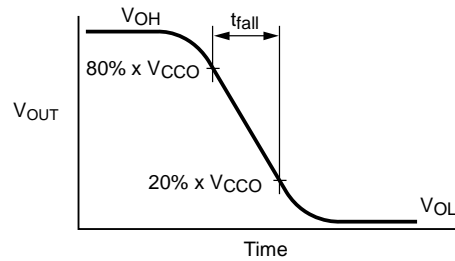
**Figure 11. 3-STATE Output High Enable Time<sup>(15)</sup>**

Symbol	V <sub>CC</sub>
V <sub>mi</sub> <sup>(16)</sup>	V <sub>CC1</sub> / 2
V <sub>mo</sub>	V <sub>CC0</sub> / 2
V <sub>X</sub>	0.5 x V <sub>CC0</sub>
V <sub>Y</sub>	0.1 x V <sub>CC0</sub>



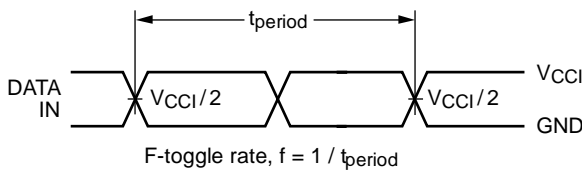
$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \times V_{CC0}}{t_{RISE}}$$

**Figure 12. Active Output Rise Time and Dynamic Output Current High**

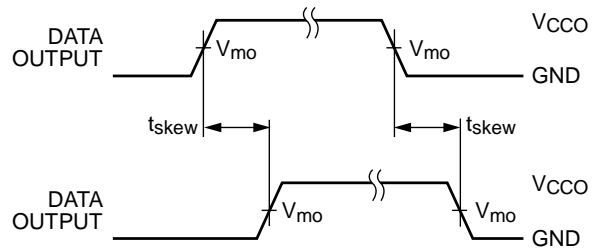


$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \times V_{CC0}}{t_{FALL}}$$

**Figure 13. Active Output Fall Time and Dynamic Output Current Low**



**Figure 14. Maximum Data Rate (or F-Toggle) in MHz**



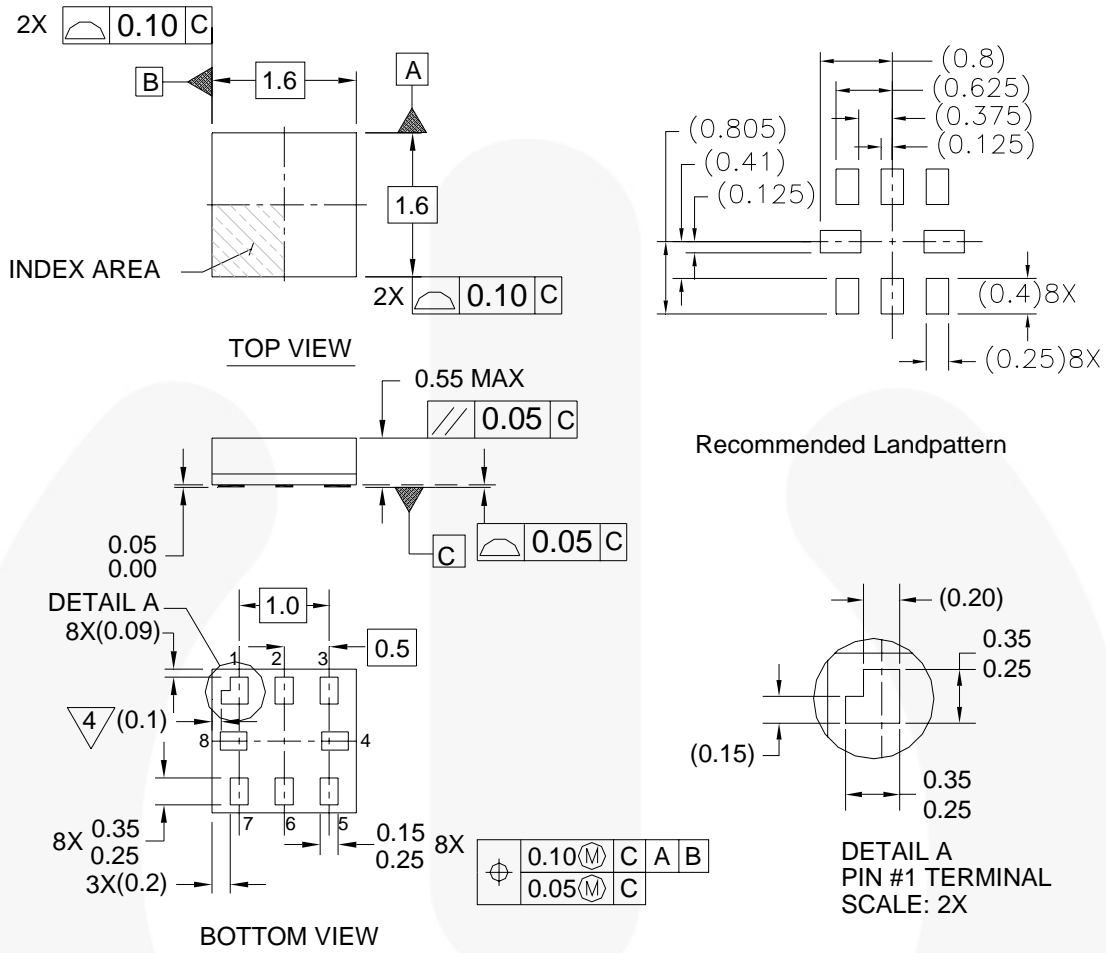
$$t_{skew} = (t_{pHLmax} - t_{pHLmin}) \text{ or } (t_{pLHmax} - t_{pLHmin})$$

**Figure 15. Output Skew Time**

### Notes:

15. Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90% at  $V_{IN} = 1.65\text{V}$  to  $1.95\text{V}$ ;  
 Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90% at  $V_{IN} = 2.3$  to  $2.7\text{V}$ ;  
 Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, at  $V_{IN} = 3.0\text{V}$  to  $3.6\text{V}$  only;  
 Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, at  $V_{IN} = 4.5\text{V}$  to  $5.5\text{V}$  only.
16.  $V_{CC1} = V_{CCA}$  for control pin OE or  $V_{mi} = (V_{CCA} / 2)$ .

## Physical Dimensions



### Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

**Figure 16. 8-Lead MicroPak™, 1.6mm Wide**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>.







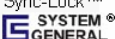
### Tape & Reel Format for MicroPak™

Always visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:  
[http://www.fairchildsemi.com/products/logic/pdf/micropak\\_tr.pdf](http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf).



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |   |   |   |   |
|---|---|---|---|
| AccuPower™  | FPST™   | PowerTrench®  | The Power Franchise®  |
| Auto-SPM™   | F-PFST™   | PowerXS™  |  |
| Build it Now™   | FRFET®  | Programmable Active Droop™  | TinyBoost™  |
| CorePLUS™   | Global Power Resource <sup>SM</sup>   | QFET®   | TinyBuck™   |
| CorePOWER™  | Green FPS™  | QST™  | TinyCalc™   |
| CROSSVOL7™  | Green FPS™ e-Series™  | Quiet Series™   | TinyLogic®  |
| CTL™  | Gmax™   | RapidConfigure™   | TINYOPTO™   |
| Current Transfer Logic™   | GTO™  |  | TinyPower™  |
| EcoSPARK®   | IntelliMAX™   | Saving our world, 1mW/Wk at a time™   | TinyPWM™  |
| EfficientMax™   | ISOPLANAR™  | SignalWise™   | TinyWire™   |
| EZSWITCH™   | MegaBuck™   | SmartMax™   | TriFault Detect™  |
|  | MICROCOUPLER™   | SMART START™  | TRUECURRENT™  |
|  | MicroFET™   | SPM®  | μSerDes™  |
| Fairchild®  | MicroPak™   | STEALTH™  |  |
| Fairchild Semiconductor®  | MillerDrive™  | SuperFET™   | UHC®  |
| FACT Quiet Series™  | MotionMax™  | SuperSOT™.3   | Ultra FRFET™  |
| FACT®   | Motion-SPM™   | SuperSOT™.6   | UniFET™   |
| FAST®   | OPTOLOGIC®  | SuperSOT™.8   | VCC™  |
| FastvCore™  | OPTOPLANAR®   | SupreMOS™   | VisualMax™  |
| FETBench™   |  | SyncFET™  | XST™  |
| FlashWriter <sup>®*</sup>   | PDP SPM™  | Sync-Lock™  |   |
|   | Power-SPM™  |  |   |

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 142

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View FXM2IC102L8X\\_F113 on WIN SOURCE](#)
- ⊖ [Fairchild/ON Semiconductor Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management