THE DATASHEET OF

FSUSB43L10X

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ON Semiconductor®

FSUSB43 — Low-Power, Two-Port, High-Speed, USB2.0 (480Mbps) Switch

Features

- Over-Voltage Tolerance (OVT) on all USB Ports up to 5.25V without External Components
- Low On Capacitance: 3.7pF Typical
- Low On Resistance: 3.9Ω Typical
- Low Power Consumption: 1μA Maximum
  - 20μA Maximum I_{CCT} over an Expanded Voltage Range (V_{IN}=1.8V, V_{CC}=4.3V)
- Wide -3db Bandwidth: > 720MHz
- Packaged in 10-Lead MicroPak™ (1.6 x 2.1mm)
- 8kV ESD Rating, >16kV Power/GND ESD Rating
- Power-Off Protection on All Ports when V_{CC}=0V
  - D+/D- Pins Tolerate up to 5.25V

Applications

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSUSB43 is a bi-directional, low-power, two-port, high-speed, USB2.0 switch. Configured as a double-pole, double-throw (DPDT) switch, it is optimized for switching between two high-speed (480Mbps) sources or a high-speed and full-speed (12Mbps) source.

The FSUSB43 is compatible with the requirements of USB2.0 and features an extremely low on capacitance (C_{ON}) of 3.7pF. The wide bandwidth of this device (720MHz) exceeds the bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

The FSUSB43 contains special circuitry on the switch I/O pins for applications where the V_{CC} supply is powered-off (V_{CC}=0), which allows the device to withstand an over-voltage condition. This minimizes current consumption even when the control voltage applied to the SEL pin is lower than the supply voltage (V_{CC}). This feature is especially valuable to mobile applications, such as cell phones, allowing for direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

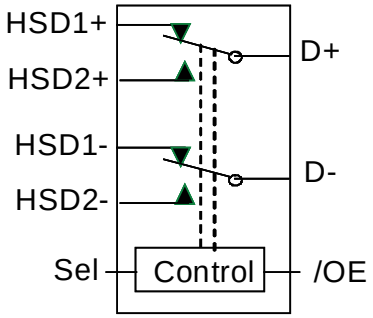

Figure 1. Analog Symbol

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Eco Status	Package
FSUSB43L10X	JH	-40 to +85°C	Green	10-Lead MicroPak™ 1.6 x 2.1mm, JEDEC MO-255B

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Publication Order Number:
FSUSB43/D

Pin Configuration

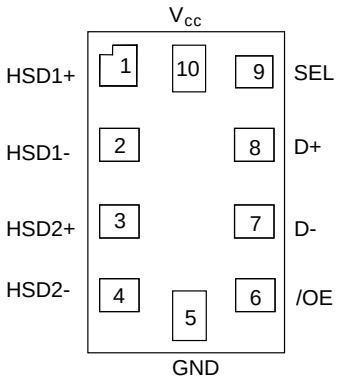


Figure 2. Pin Assignment (Top Through View)

Pin Definitions

Pin #	Name	Description
1	HSD1+	Multiplexed Source Inputs
2	HSD1-	Multiplexed Source Inputs
3	HSD2+	Multiplexed Source Inputs
4	HSD2-	Multiplexed Source Inputs
5	GND	Ground
6	/OE	Switch Enable
7	D-	USB Data Bus
8	D+	USB Data Bus
9	SEL	Switch Select
10	V_{CC}	Supply Voltage

Truth Table

SEL	/OE	Function
X	HIGH	Disconnect
LOW	LOW	D+, D-=HSD1+, HSD1-
HIGH	LOW	D+, D-=HSD2+, HSD2-

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	+5.5	V
V_{CNTRL}	DC Input Voltage (Sel, /OE)[1]		-0.5	V_{CC}	V
V_{SW}	ALL PINS for V_{CC} 0 to 5.5V		-0.5	5.5	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	DC Output Current			100	mA
T_{STG}	Storage Temperature		-65	+150	°C
ESD	Human Body Model: JEDEC JESD22-A114	All Pins		8	kV
		I/O to GND		9	
		Power to GND		16	
	Charged Device Model: JEDEC JESD22-C101			2	

Note:
1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.4	4.4	V
V_{CNTRL}	Control Input Voltage[2] (Sel, /OE)	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	4.5	V
T_A	Operating Temperature	-40	+85	°C

Note:
2. The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18mA	3.0			-1.2	V
V_{IH}	Input Voltage High		2.4 to 3.6	1.3			V
			4.3	1.7			V
V_{IL}	Input Voltage Low		2.4 to 3.6			0.5	V
			4.3			0.7	V
I_{IN}	Control Input Leakage	V_{SW}=0 to V_{CC}	4.3	-1.0		1.0	µA
I_{OZ}	Off State Leakage	0 ≤ Dn, HSD1n, HSD2n ≤ 3.6V	4.3	-2.0		2.0	µA
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW}=0V to 4.3V, V_{CC}=0V Figure 4	0	-2		2	µA
R_{ON}	HS Switch On Resistance(3)	V_{SW}=0.4V, I_{ON}=-8mA Figure 3	2.4		4.5	7.5	Ω
			3.0		3.9	6.5	
ΔR_{ON}	HS Delta R_{ON}(4)	V_{SW}=0.4V, I_{ON}=-8mA	3.0		0.65		Ω
I_Q	Quiescent Supply Current	V_{CNTRL}=0 or V_{CC}, I_{OUT}=0	4.3			1.0	µA
I_{CCT}	Increase in I_Q Current per Control Voltage and V_{CC}	V_{CNTRL}=2.6V, V_{CC}=4.3V	4.3			10.0	µA
		V_{CNTRL}=1.8V, V_{CC}=4.3V	4.3			20.0	µA

Notes:

3. Measured by the voltage drop between HSDn and Dn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSDn or Dn ports).
4. Guaranteed by characterization.

AC Electrical Characteristics

All typical values are for V_{CC}=3.3V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time SEL, /OE to Output	R_L=50Ω, C_L=5pF, V_{SW}=0.8V Figure 5, Figure 6	2.4		24	40	ns
			3.0 to 3.6		13	30	
t_{OFF}	Turn-Off Time SEL, /OE to Output	R_L=50Ω, C_L=5pF, V_{SW}=0.8V Figure 5, Figure 6	2.4		15	35	ns
			3.0 to 3.6		12	25	
t_{PD}	Propagation Delay(5)	R_L=50Ω, C_L=5 pF Figure 5, Figure 7	3.3		0.25		ns
t_{BBM}	Break-Before-Make Time(5)	R_L=50Ω, C_L=5pF V_{SW1}=V_{SW2}=0.8V Figure 9	2.4	2.0		10	ns
			3.0 to 3.6	2.0		6.5	
OIRR	Off Isolation(5)	R_L=50Ω, f=240MHz Figure 11	3.0 to 3.6		-30		dB
Xtalk	Non-Adjacent Channel Crosstalk(5)	R_L=50Ω, f=240MHz Figure 12	3.0 to 3.6		-45		dB
BW	-3db Bandwidth(5)	R_L=50Ω, C_L=0pF Figure 10	3.0 to 3.6		720		MHz
		R_L=50Ω, C_L=5pF Figure 10			550		MHz

Note:
5. Guaranteed by characterization.

USB High-Speed-Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output(6)	R_L=50Ω, C_L=5pF Figure 8	3.0 to 3.6		20		ps
t_J	Total Jitter(6)	R_L=50Ω, C_L=5pf, t_r=t_f=500ps (10-90%) at 480Mbps, (PRBS=2^{15} – 1)	3.0 to 3.6		200		ps

Note:
6. Guaranteed by characterization.

Capacitance

Symbol	Parameter	Conditions	T_A=- 40ºC to +85ºC			Units
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance(7)	V_{CC}=0V		1.5		pF
C_{ON}	D+/D- On Capacitance(7)	V_{CC}=3.3V, /OE=0V, f=240MHz Figure 14		3.7		
C_{OFF}	D1n, D2n Off Capacitance(7)	V_{CC} and /OE=3.3V Figure 13		2.0		

Note:
7. Guaranteed by characterization.

Test Diagrams

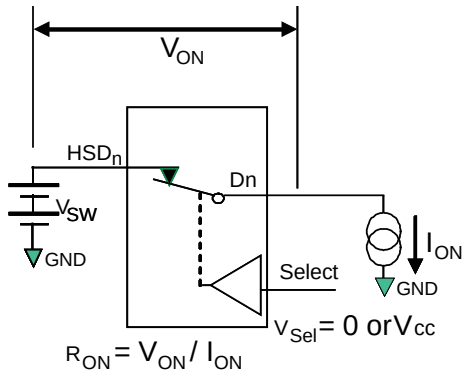
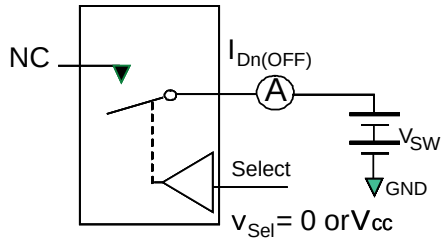
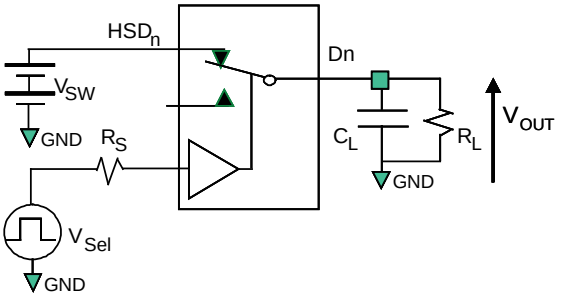


Figure 3. On Resistance



**Each switch port is tested separately

Figure 4. Off Leakage



R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 5. AC Test Circuit Load

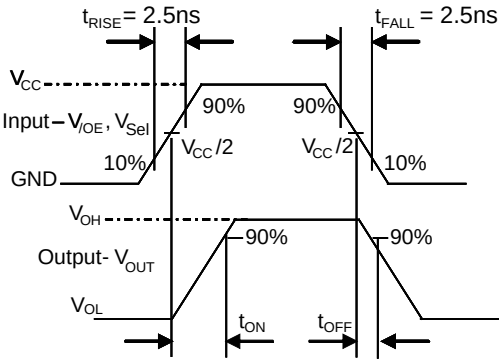


Figure 6. Turn-On / Turn-Off Waveforms

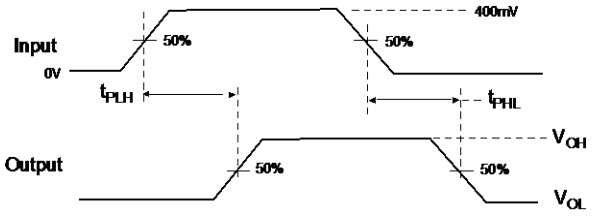


Figure 7. Propagation Delay ($t_r t_f$ – 500ps)

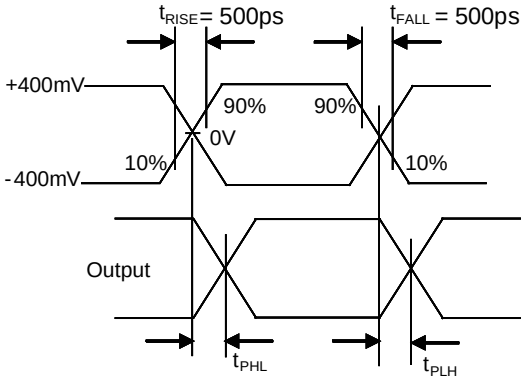
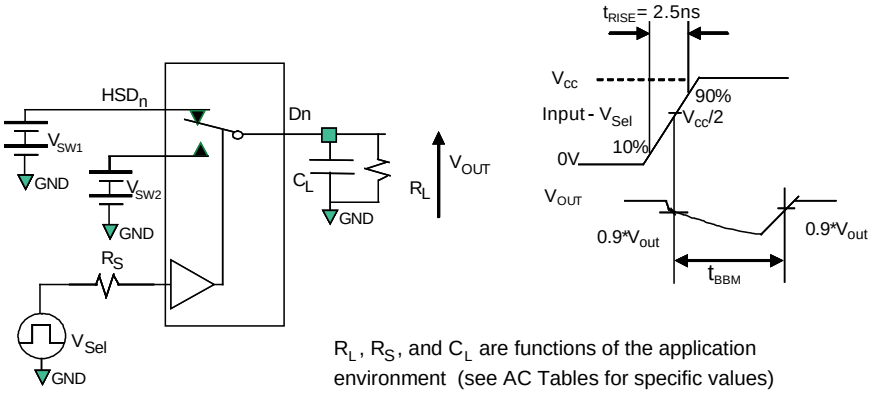


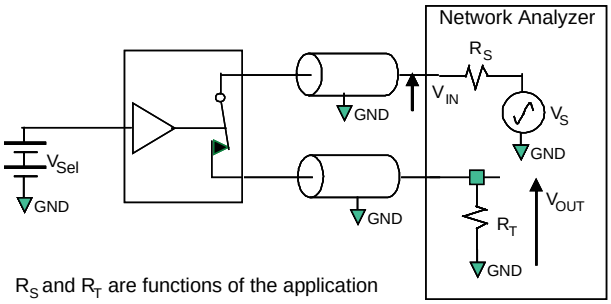
Figure 8. Intra-Pair Skew Test $t_{SK(P)}$

Test Diagrams (Continued)



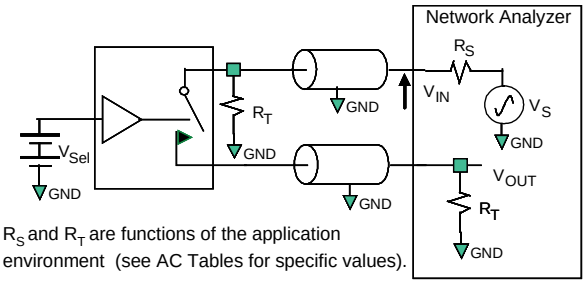
R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 9. Break-Before-Make Interval Timing



R_S and R_T are functions of the application environment (see AC Tables for specific values).

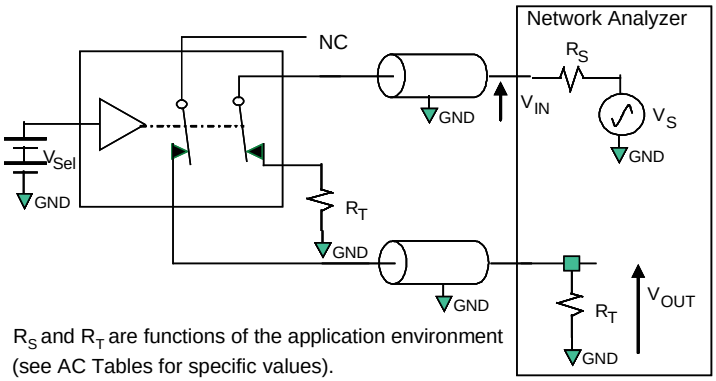
Figure 10. Bandwidth



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Off isolation = 20 Log (V_{OUT} / V_{IN})

Figure 11. Channel Off Isolation



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Crosstalk = 20 Log (V_{OUT} / V_{IN})

Figure 12. Non-Adjacent Channel-to-Channel Crosstalk

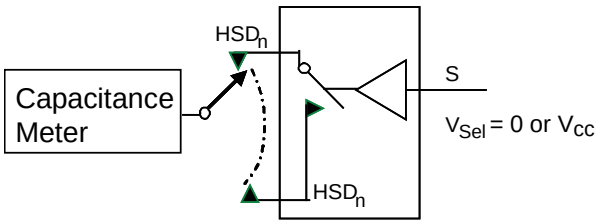


Figure 13. Channel Off Capacitance

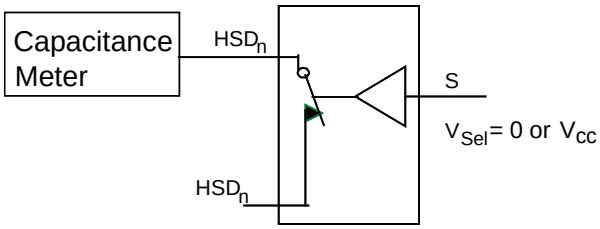


Figure 14. Channel On Capacitance

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