THE DATASHEET OF

S32K311NHT0VPAST

S32K3XX

S32K3xx Data Sheet

Rev. 13 — 12 November 2025 Product data sheet

Supports S32K344, S32K324, S32K314, S32K312, S32K311, S32K310, S32K341, S32K342, S32K322, S32K328, S32K338, S32K348, S32K356, S32K358, S32K388 and S32K389. Data is preliminary for S32K312 and S32K344 100LQFP only.

This document includes key information in the file attached to it. See the attachment icon in the PDF window to see the list of attachments.

- Operating characteristics
  - Voltage range: 2.97 V to 5.5 V
  - Ambient temperature range: -40 °C to 125 °C for all power modes
- Arm™ Cortex-M7 core, 32-bit CPU
  - M7 supports up to 320 MHz frequency
  - Arm Core based on the Armv7 and Thumb®-2 ISA
  - Integrated Digital Signal Processor (DSP)
  - Configurable Nested Vectored Interrupt Controller (NVIC)
  - Single Precision Floating Point Unit (FPU)
- Clock interfaces
  - 8 - 40 MHz Fast External Oscillator (FXOSC)
  - 48 MHz Fast Internal RC oscillator (FIRC)
  - 32 kHz Low Power Oscillator (SIRC)
  - 32 kHz Slow External Oscillator (SXOSC)
  - System Phased Lock Loop (SPLL)
- I/O and package
  - MAPBGA437 , LQFP48, HDQFP100, HDQFP172, MAPBGA257, MAPBGA289, HDQFP172 with Exposed pad (EP) package options
- Up to 32-channel DMA with up to 128 request sources using DMAMUX
- Memory and memory interfaces
  - Up to 12 MB program flash memory with ECC
  - Up to 256 KB of flexible program or data flash memory
  - Up to 2304 KB SRAM with ECC, includes 384 KB of TCM RAM ensuring maximum CPU performance of fast control loops with minimal latency
  - Data and instruction cache for each core to minimize performance impact of memory access latencies
  - QuadSPI support
- Mixed-signal analog
  - Up to three 12-bit Analog-to-Digital Converters (ADC) with up to 24 channel analog inputs per module
  - One Temperature Sensor (TempSense)
  - Up to three Analog Comparators (CMP), with each comparator having an internal 8-bit DAC
- Human-Machine Interface (HMI)
  - Up to 320 GPIO pins
  - Non-Maskable Interrupt (NMI)
  - Up to 60 pins with wakeup capability
  - Up to 32 pins with interrupt support

- Power management
  - Low-power Arm Cortex-M7 core with excellent energy efficiency, balanced with performance
  - Power Management Controller (PMC) with simplified mode management (RUN and STANDBY)
  - Supports peripheral specific clock gating. Only specific peripherals remain working in low power modes.
- Communications interfaces
  - Up to 16 serial communication interface (LPUART) modules, with LIN, UART and DMA support
  - Up to six Low Power Serial Peripheral Interface (LPSPI) modules with DMA support
  - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support
  - Up to twelve FlexCAN modules (with optional CAN-FD support)
  - FlexIO module for flexible and high performance serial interfaces
  - Up to two Ethernet modules
  - Up to two Synchronous Audio Interface (SAI) modules
- Reliability, safety and security
  - Hardware Security Engine (HSE_B) - Supports AES accelerator(for K388 and K389 only)
  - Up to two Internal Software Watchdog Timers (SWT)
  - Error-Correcting Code (ECC) on all memories
  - Error Detection Code (EDC) on data path
  - Cyclic Redundancy Check (CRC) module
  - 64-bit Unique Identification (ID) number
  - Extended Cross domain Domain Controller (XRDC), providing protection for master core access rights
  - Virtualization Wrapper (VIRT_WRAPPER), providing I/O protection
- Debug functionality
  - Serial Wire JTAG debug Port (SWJ-DP), with 2 pin Serial Wire Debug (SWD) for external debugger
  - Debug Watchpoint and Trace (DWT), with four configurable comparators as hardware watchpoints
  - Serial Wire Output (SWO)-synchronous trace data support
  - Instrumentation Trace Macrocell (ITM) with software and hardware trace, plus time stamping
  - CoreSight AHB Trace Macrocell (HTM)
  - Flash Patch and Breakpoints (FPB) with ability to patch code and data from code space to system space
  - Serial Wire Viewer (SWV): A trace capability providing displays of reads, writes, exceptions, PC Samples and print
  - Full data trace for up to 16 output wide
  - Embedded Cross Trigger (ECT) is used for multicore run-control and trace cross triggering, using CoreSight Cross Trigger Interface (CTI)
- Timing and control
  - Up to three enhanced modular I/O system (eMIOS), offering up to 72 timer channels (IC/OC/PWM)
  - Up to two System Timer Modules (STM)
  - Up to two Logic Control Units (LCU)
  - Full cross triggering support for ADC / timer (BCTU)
  - One Trigger MUX Control (TRGMUX) module
  - Up to three Periodic Interrupt Timer (PIT) modules
  - 32-bit Real Time Counter (RTC) with autonomous periodic interrupt (API) function

1 Overview

The S32K3xx product series further extends the highly-scalable portfolio of Arm ® Cortex ® - M0+/M4F S32K1xx chips in the automotive industry with the Arm Cortex-M7 core at higher frequency, more memory, ASIL-B and D rating and advanced security module. With a focus on automotive environment robustness, the S32K3xx product series devices are well suited to a wide range of applications in electrical harsh environments, and are optimized for cost-sensitive applications offering new, space saving package options. The S32K3xx series offers a broad range of memory, peripherals and performance options. Devices in this series share common peripherals and pin-out, allowing developers to migrate easily within a chip series or among other chip series to take advantage of more memory or feature integration.

2 Block diagram

The following figures show the S32K3xx product series block diagrams:

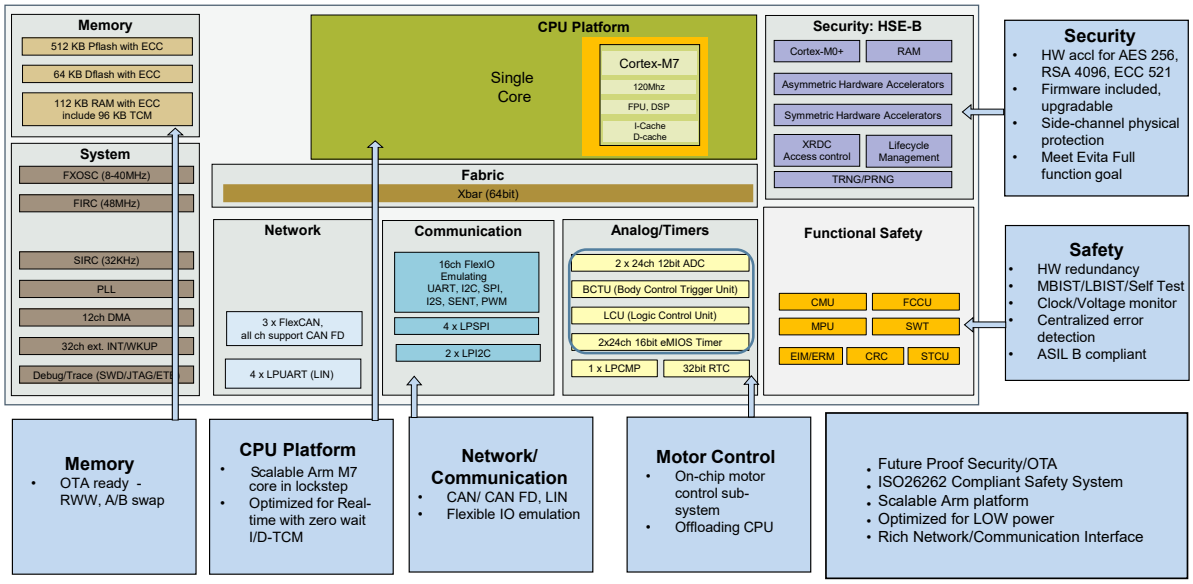


Figure 1. S32K310: ASIL B Single Core 512 KB General Purpose MCU

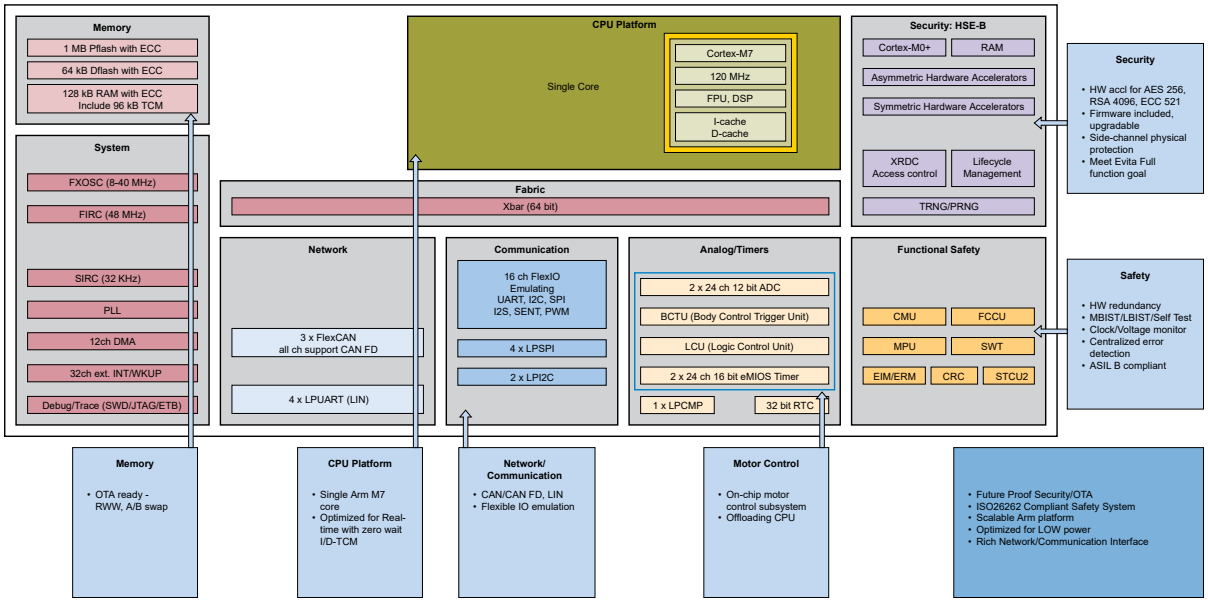


Figure 2. S32K311: ASIL B Single Core 1MB General Purpose MCU

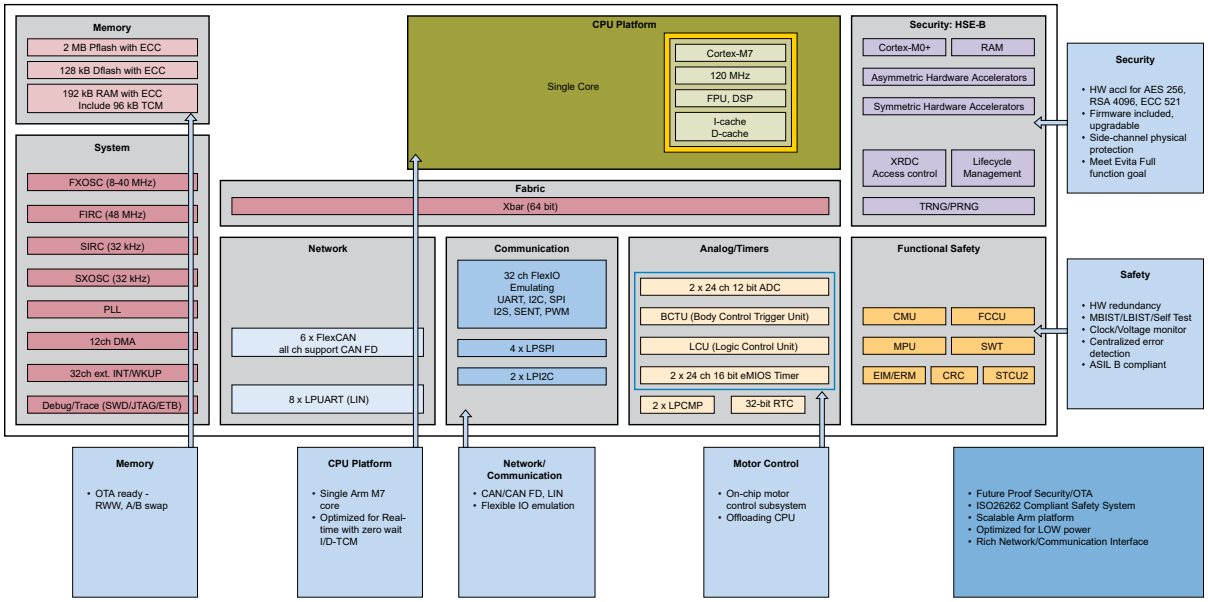


Figure 3. S32K312: ASIL B Single Core 2MB General Purpose MCU

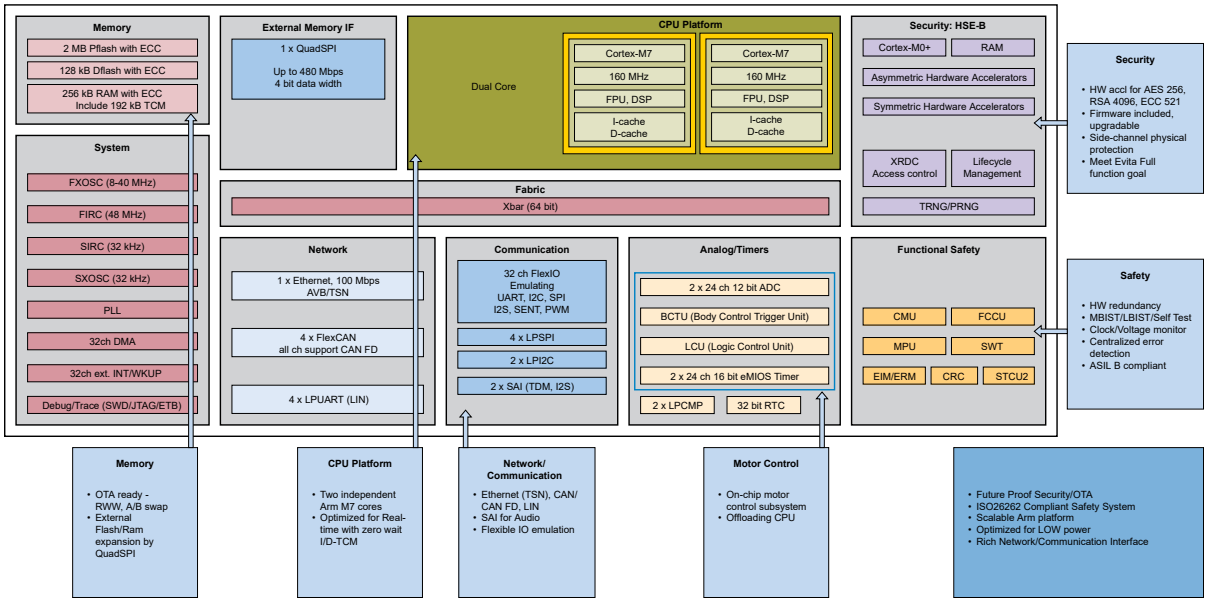


Figure 4. S32K322: ASIL B Dual Core 2MB General Purpose MCU

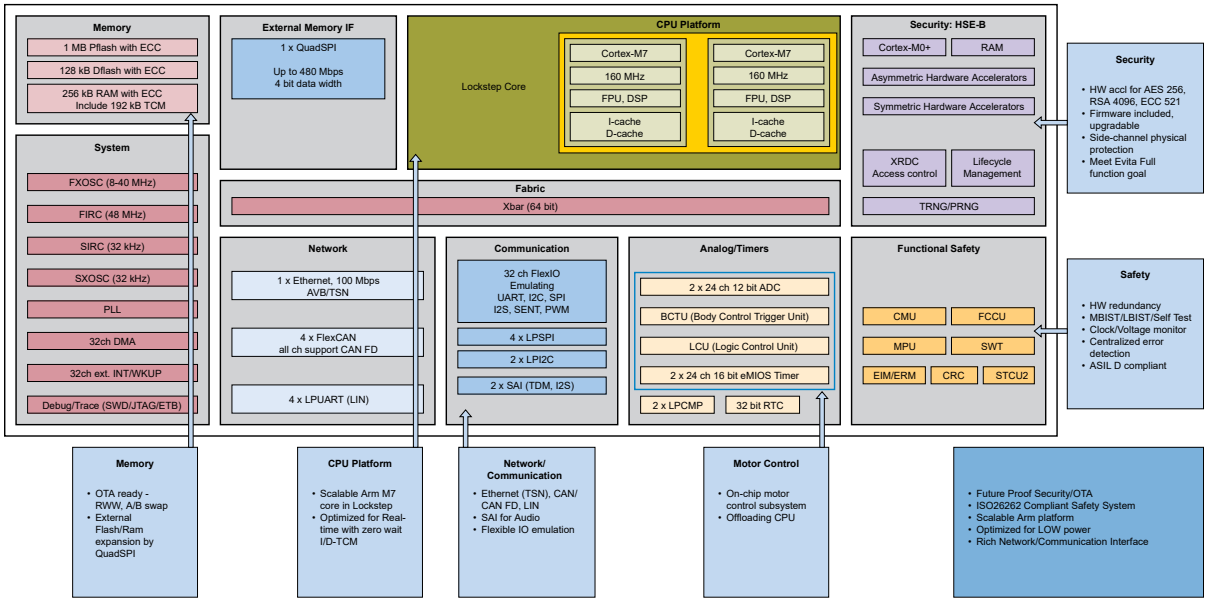


Figure 5. S32K341: ASIL D Lockstep Core 1MB General Purpose MCU

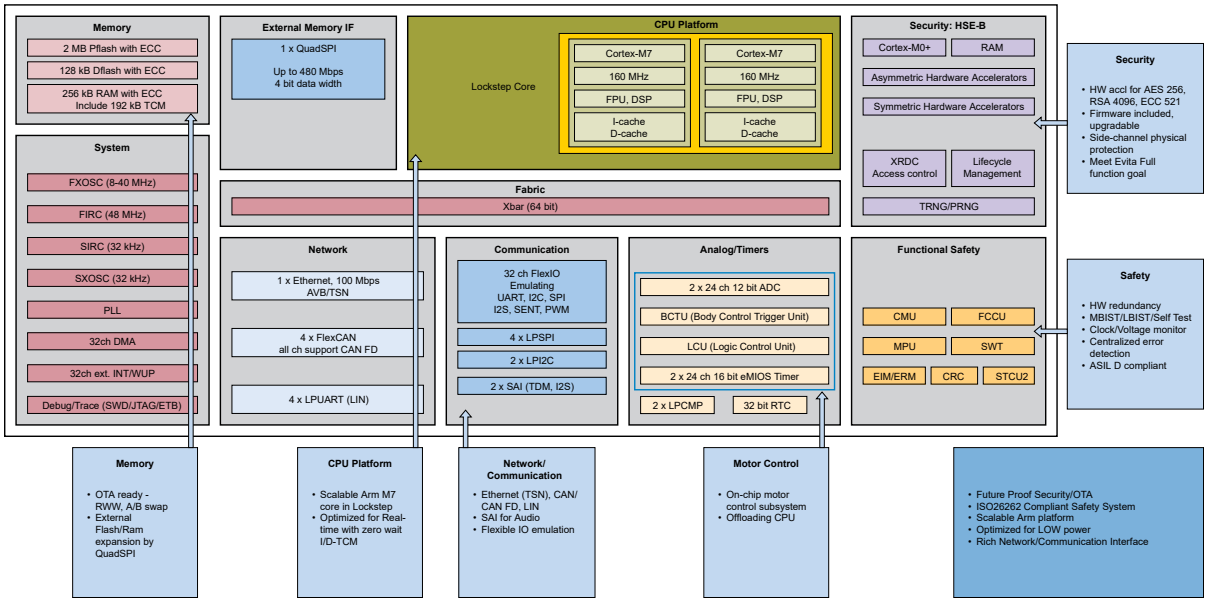


Figure 6. S32K342: ASIL D Lockstep Core 2MB General Purpose MCU

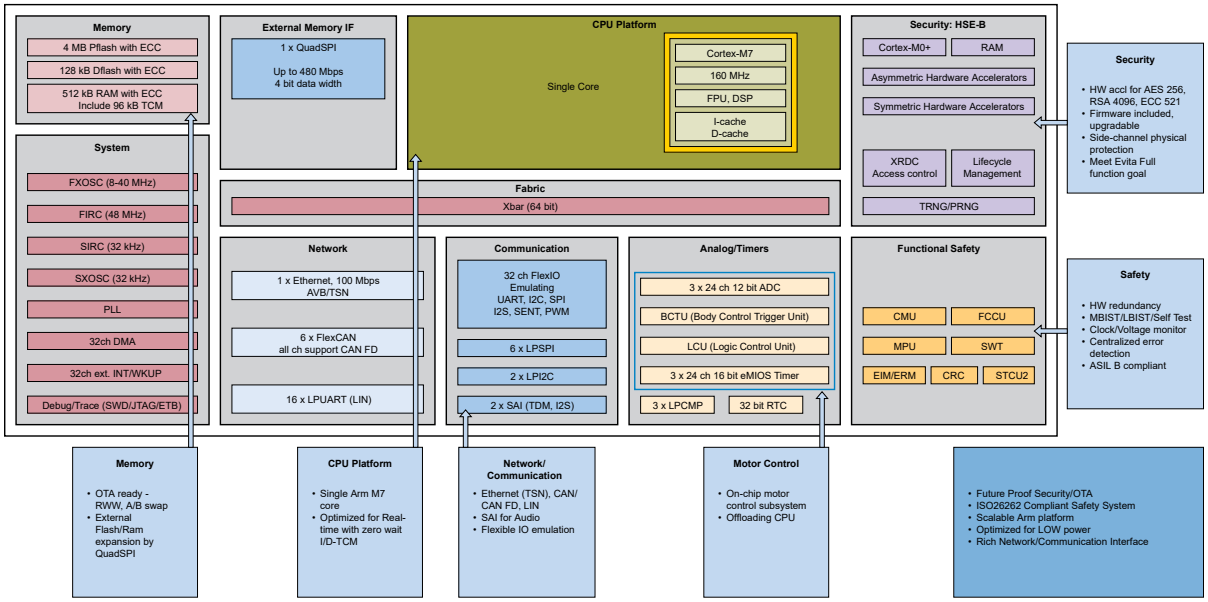


Figure 7. S32K314: ASIL B Single Core 4MB General Purpose MCU

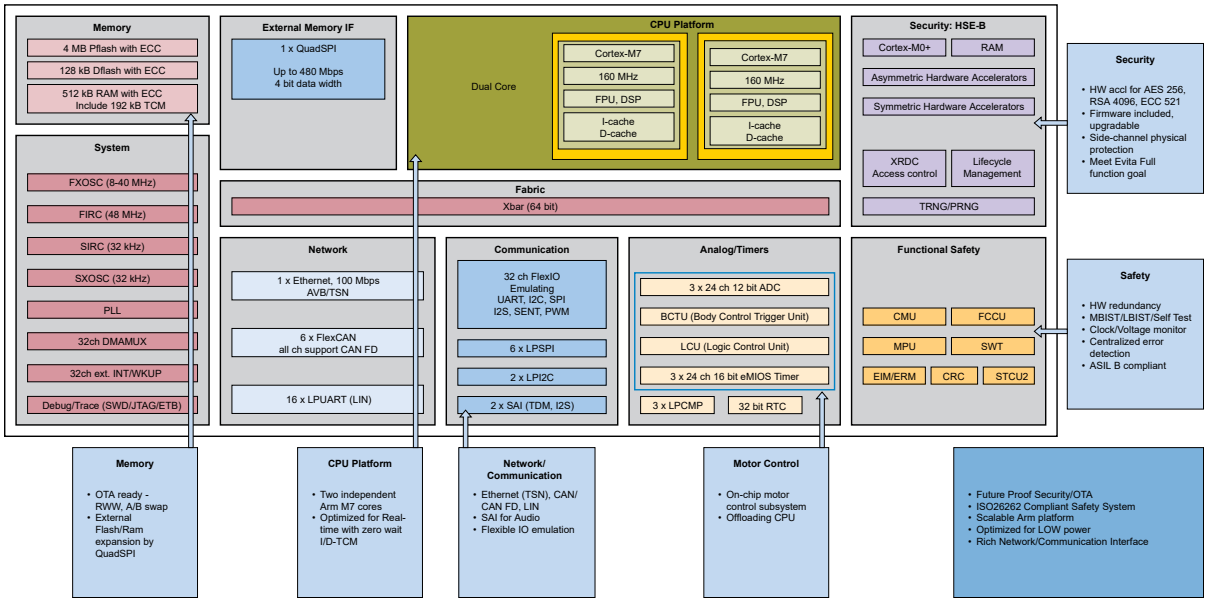


Figure 8. S32K324: ASIL B Dual Core 4MB General Purpose MCU

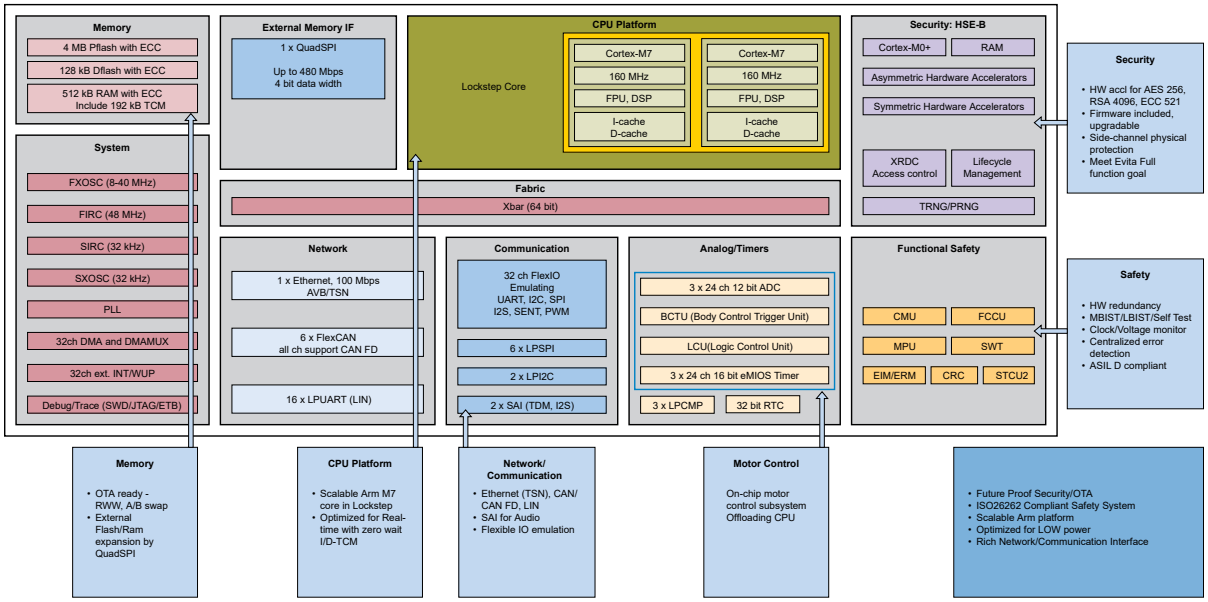


Figure 9. S32K344: ASIL D Lockstep Core 4MB General Purpose MCU

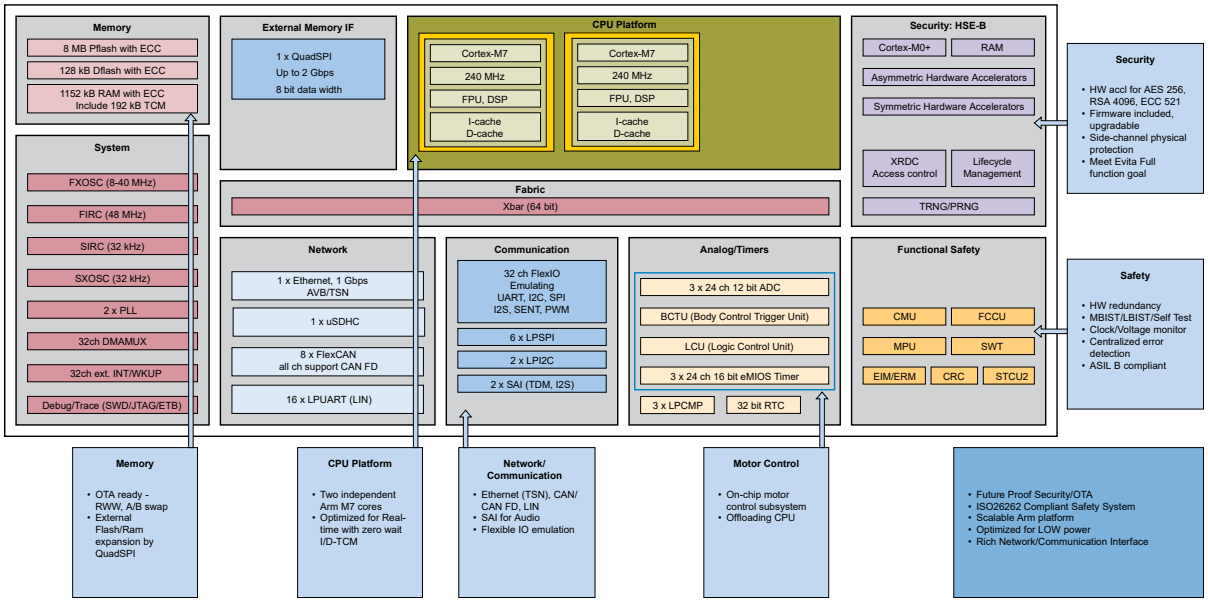


Figure 10. S32K328: ASIL B Dual Core 8MB General Purpose MCU

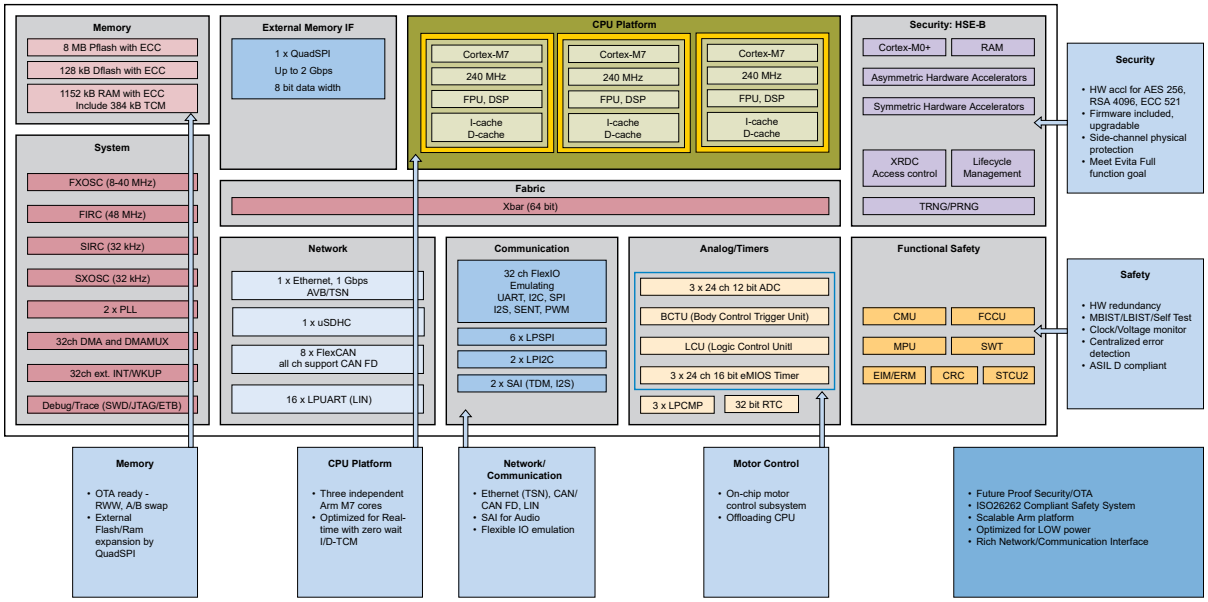


Figure 11. S32K338: ASIL B Three Core 8MB General Purpose MCU

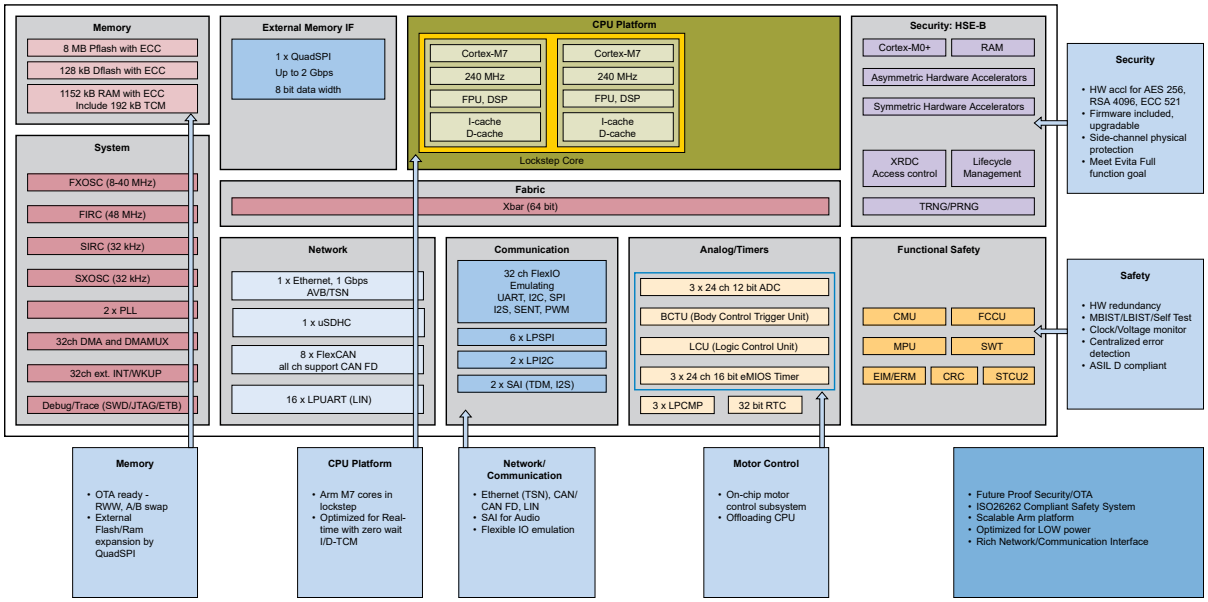


Figure 12. S32K348: ASIL D Lockstep Core 8MB General Purpose MCU

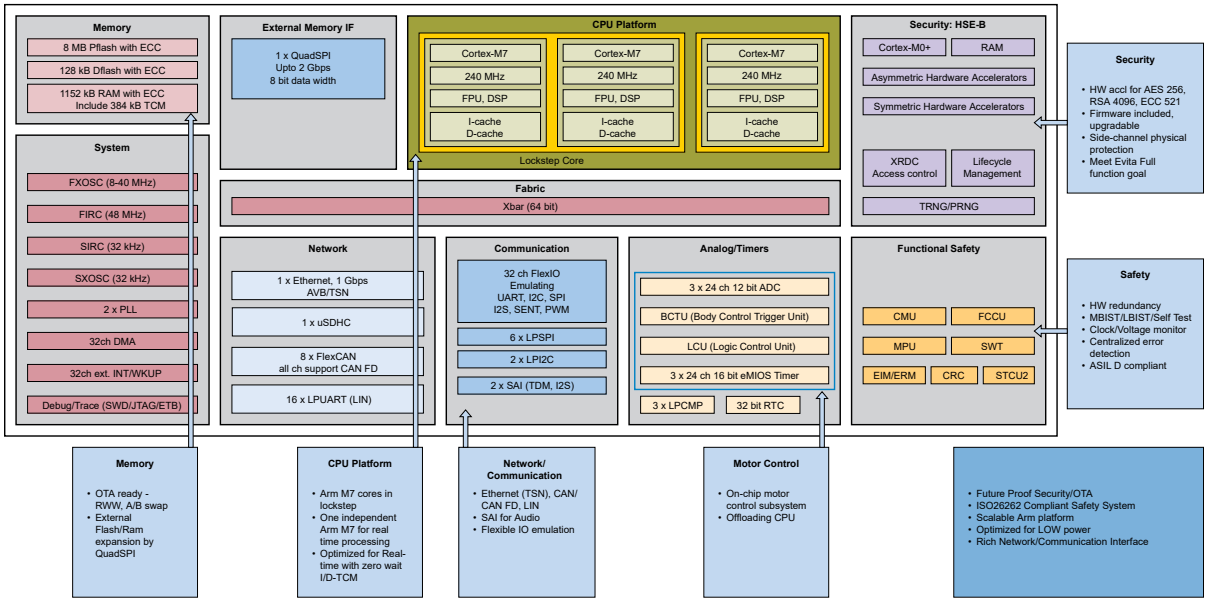


Figure 13. S32K358: ASIL D Lockstep Core + One, 8MB General Purpose MCU

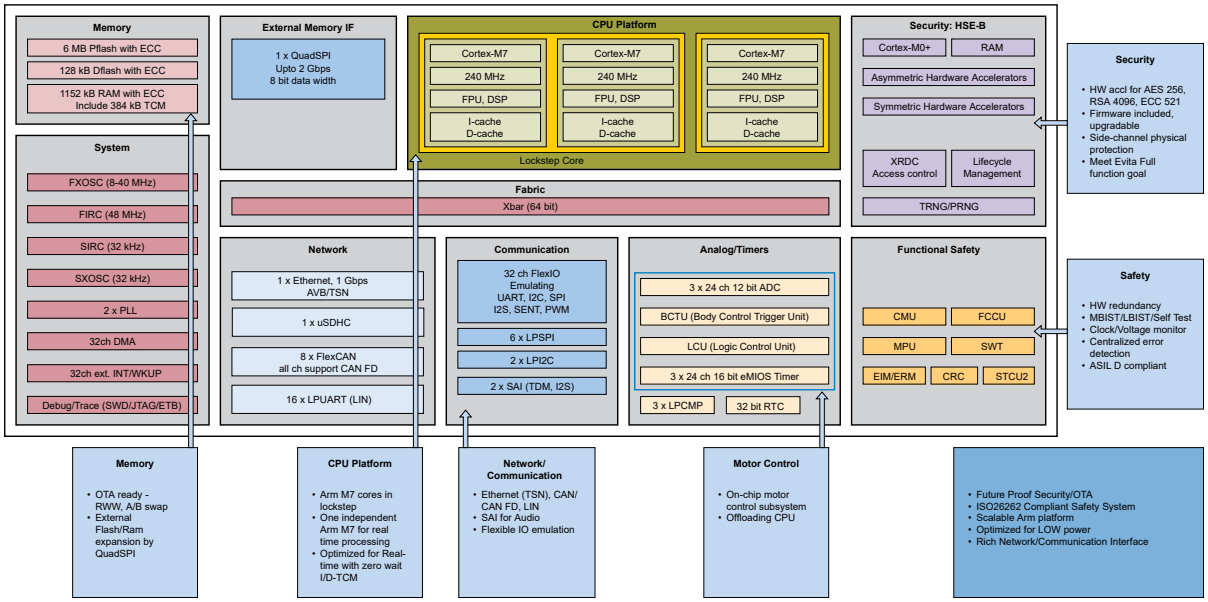


Figure 14. S32K356: ASIL D Lockstep Core + One, 6MB General Purpose MCU

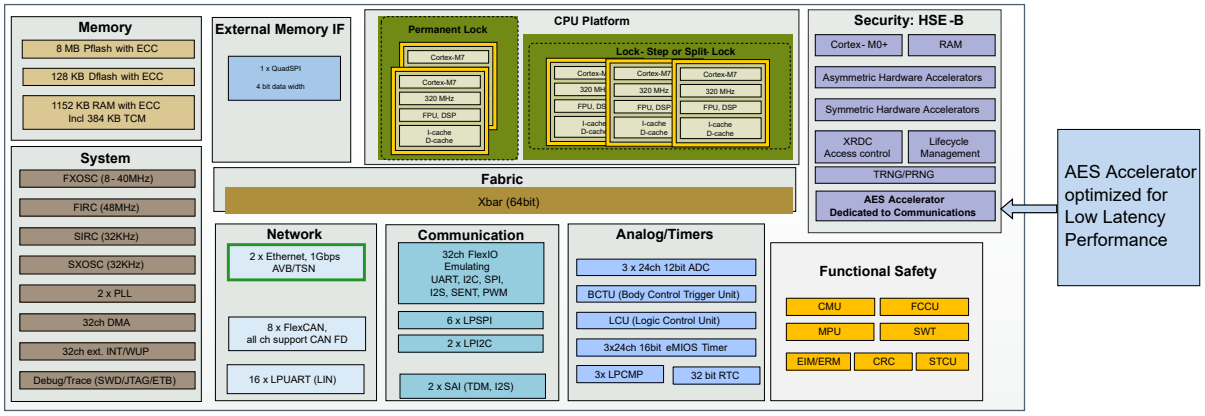


Figure 15. S32K388: ASIL D 8MB MCU

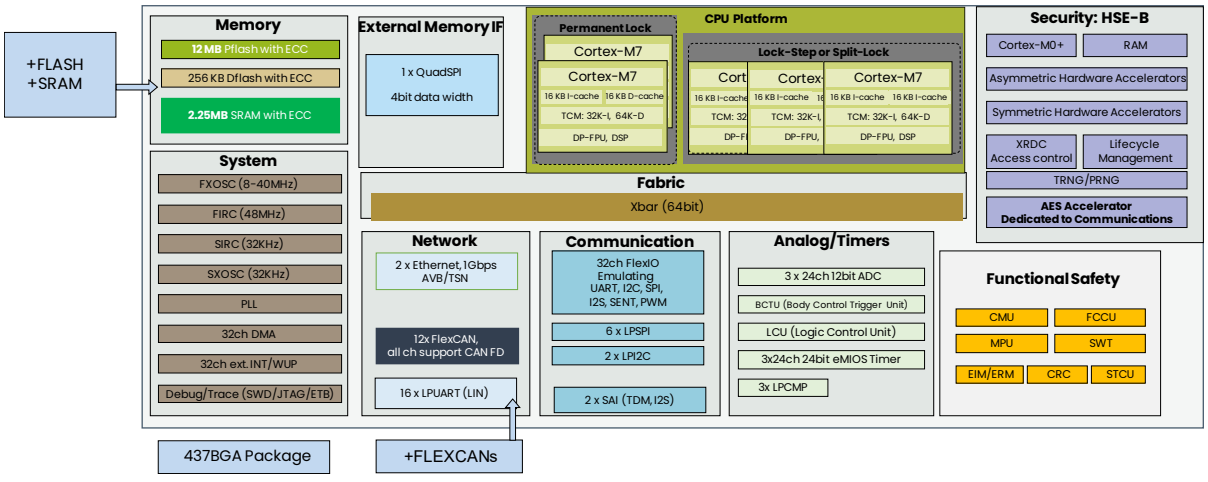


Figure 16. S32K389: ASIL D 12MB MCU

3 Feature comparison

The following table compares some of the prominent features related to memory and package options of these chips from the S32K3xx family/product series:

- S32K310
- S32K311
- S32K312
- S32K322
- S32K341
- S32K342
- S32K314
- S32K324
- S32K344
- S32K328
- S32K338
- S32K348
- S32K356
- S32K358
- S32K388
- S32K389

Table 1. S32K3xx chip's feature comparison

Feature	Chip															
	S32K310	S32K311	S32K312	S32K322	S32K341	S32K342	S32K314	S32K324	S32K344	S32K328	S32K338	S32K348	S32K356	S32K358	S32K388	S32K389
Safety/ ASIL	B				D		B		D	B		D				
Program flash memory	512 KB	1 MB	2 MB		1 MB	2 MB	4 MB			8 MB			6 MB	8 MB		12 MB
Data flash memory (KB)	64		128							128						256
Total RAM (KB)	112KB (incl. 96KB TCM)	128KB (incl. 96KB TCM)	192KB (incl. 96KB TCM)	256KB (incl. 192KB TCM)			512KB (including 96KB TCM)	512KB (incl. 192KB TCM)		1152KB (incl. 192KB TCM)	1152KB (incl. 384KB TCM)	1152KB (incl. 192KB TCM)	1152KB (incl. 384KB TCM)			2304KB (incl. 384KB TCM)
Standby RAM	16 KB	32 KB								64 KB						
Security	HSE_B														HSE B + AES_ACCEL	
Core quantity	1 x M7			2 x M7	1 x M7 LS		1 x M7	2 x M7	1 x M7 LS	2 x M7	3 x M7	1 x M7 LS	1xM7 LS + 1xM7		1xM7 LS+3xM7 or 2xM7 LS+1xM7	1xM7 LS + 3xM7 or 2xM7 LS +1xM7
Frequency (MHz)	120			160						240					320	

Table continues on the next page...

Table 1. S32K3xx chip's feature comparison...*continued*

Feature	Chip															
	S32K310	S32K311	S32K312	S32K322	S32K341	S32K342	S32K314	S32K324	S32K344	S32K328	S32K338	S32K348	S32K356	S32K358	S32K388	S32K389
DMA channels	12			32												
ASIL-B DMIPS [1] [2]	277-387-813			738-1032-2168	—		369-516-1084	738-1032-2168	—	1108-1550-3254	1662-2325-4881	—	554-775-1627		739-1033-2169 [3] 2217-3099-6507 [4]	
ASIL-D DMIPS [1] [2]	—			369-516-1084			—		369-516-1084	—			554-775-1627		1478-2066-4338 [3] 739-1033-2169 [4]	
ASIL-B CoreMark score [1] [5]	634			1692	—		846	1692	—	2538	3807	—	1269		1692 [3] 5078 [4]	
ASIL-D CoreMark score [1] [5]	—			846			—		846	—			1269		3384 [3] 1692 [4]	
FlexCAN instances	3		6	4			6			8						12

Table continues on the next page...

Table 1. S32K3xx chip's feature comparison...*continued*

Feature	Chip															
	S32K310	S32K311	S32K312	S32K322	S32K341	S32K342	S32K314	S32K324	S32K344	S32K328	S32K338	S32K348	S32K356	S32K358	S32K388	S32K389
EMAC instances	—			1						—						
GMAC instances	—									1					2	
SAI instances	—			2												
LPUART instances	4		8	4			16									
LPSPI instances	4						6									
I^2C instances	2															
FlexIO (incl. SENT support) channels	16		32													
QuadSPI instances	—			1[6]						1[7]					1[6]	
uSDHC instances	—									1					—	
ADC instances	2						3									
LPCMP instances	1		2				3									

Table continues on the next page...

Table 1. S32K3xx chip's feature comparison...*continued*

Feature	Chip															
	S32K310	S32K311	S32K312	S32K322	S32K341	S32K342	S32K314	S32K324	S32K344	S32K328	S32K338	S32K348	S32K356	S32K358	S32K388	S32K389
PIT instances	2			3											4	
SWT instances	1			2	1			2	1	2	3	1	2		4	
STM instances	1			2						3					4	
LCU instances	2															
BCTU instances	1															
TRGMUX instances	1															
eMIOS instances	2						3									
RTC instances	1															
437-ball MAPBGA package	No															Yes
289-ball MAPBGA package	No									Yes						No
257-ball MAPBGA package	No						Yes			No						

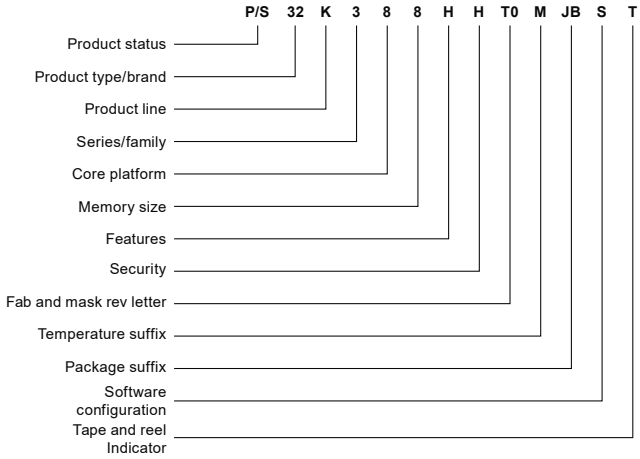
Table continues on the next page...

Table 1. S32K3xx chip's feature comparison...*continued*

Feature	Chip															
	S32K310	S32K311	S32K312	S32K322	S32K341	S32K342	S32K314	S32K324	S32K344	S32K328	S32K338	S32K348	S32K356	S32K358	S32K388	S32K389
172-HDQFP package	No		Yes							No						
172-HDQFP - EP package	No									Yes					No	
100-HDQFP package	Yes						No									
100-LQFP package	No		Yes	No			Yes			No						
48-pin LQFP package	Yes		No													

[1] ASIL-B and ASIL-D performance is available simultaneously. ASIL-D performance can also be used for ASIL-B performance.
[2] The first result abides by all of the "ground rules" out in Dhrystone documentation, the second permits inlining of functions, not just permitted C strings libraries, while the third additionally permits simultaneous ("multi-file") compilation. All are with the original (K and R) v2.1 of Dhrystone. Arm Compiler 6.17. See https://developer.arm.com/Processors/Cortex-M7 for details.
[3] Core configuration is 2xLS + 1 independent core
[4] Core configuration is 1xLS + 3 independent cores
[5] Results depends on specific compiler version, contact NXP sales representative for more details.
[6] 4-bit data width, SDR mode only
[7] 8-bit data width, SDR and DDR mode

4 Ordering information



Product status for ordering and marking

P: Prototype
S: Qualified ordering P/N
N: Non-China manufacturing qualified part number

Product type/brand

32: Automotive 32 bit MCU/MPU

Product line

K: General purpose MCU

Series/family

3: K3 product family/Arm CortexM7 based

Core platform

1: 1 x M7 core
2: 2 x M7 cores
3: 3 x M7 cores
4: 1 x M7 lockstep core
5: 1 x M7 lockstep core plus 1 x M7 core
6: 1 x M7 LS core + 1 x M7 core + DSP + 2 x eTPU
7: 1 x M7 LS core + 2 x M7 split-lock cores + DSP
8: 2 x M7 lockstep + 1 x M7 core or 1 x M7 lockstep + 3 x M7 cores
9: 1 x M7 LS core + 2 x M7 split-lock cores + 1 x DSP + 2 x eTPU

Memory size

	0	1	2	4	6	8	9
P-Flash	512 kB	1 MB	2 MB	4 MB	6 MB	8 MB	12 MB

Extra feature

No ethernet MAC, No SAI	100 Mbps ethernet MAC + SAI	1 Gbps ethernet MAC + SAI	2 x 1 Gbps ethernet MAC+ SAI
N	E	G	H

Security *

HSE B standard security	OEM specific security
H	V

Fab and mask rev letter

Tx: Global foundry
x0: 1st mask revision
x1: 2nd mask revision

Ambient temperature (Ta)

V: -40 °C to 105 °C
M: -40 °C to 125 °C

Package suffix

pins	BGA	HDQFP	HDQFP-EP	LQFP
48				LF
100		PA		LL
172		PB	PC	
176				KU
257	MM			
289	JB			
437	JG			

Software configuration

S: Standard family SW package, including:

- Real time driver including Autosar MCAL and non Autosar driver package (ISO26262 compliant, crypto driver included)
- Standard security firmware
- Safety peripheral driver (SPD)
- Inter-core communication framework (IPCF)

I: ISELED SW licensed + standard family SW package

Tape and reel

T: Trays/tubes
R: Tape and reel

*9th character = G is not offered as standard part number nomenclature. Contact NXP sales representative for more details.

Figure 17. Ordering information

4.1 Determining valid orderable parts

To determine the orderable part numbers for this device, please contact NXP sales representative.

5 General

5.1 Absolute maximum ratings

Caution: *When the MCU is in an unpowered state, current injected through the chip pins may bias internal chip structures (for example, ESD diodes) and incorrectly power up these internal structures through inadvertent paths. The presence of such residual voltage may influence different chip-internal blocks in an unpredictable manner and may ultimately result in*

unpredictable chip behavior (for example, POR flag not set). Once in the illegal state, powering up the chip further and then applying reset will clear the illegal state. Injection current specified for the chip under the aspect of absolute maximum ratings represent the capability of the internal circuitry to withstand such condition without causing physical damage. Functional operation of the chip under conditions - specified as absolute maximum ratings - is not implied.

Note: *Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in the following table for specific conditions. Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device. All the limits defined in the datasheet specification must be honored together and any violation to any one or more will not guarantee desired operation. Unless otherwise specified, all maximum and minimum values in the datasheet are across process, voltage, and temperature.*

The VDD_HV_B and V15 voltage supply domains are only present in certain devices and packages (S32K388, S32K389, S32K358, S32K356, S32K348, S32K338, S32K328, S32K344, S32K324, S32K314, S32K342, S32K341, S32K322).

The VDD_DCDC supply voltage is only present in certain devices and packages (S32K358, S32K356, S32K348, S32K338, S32K328, S32K388 and S32K389).

Table 2. Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_A	Main I/O and analog supply voltage [1][2]	-0.3	—	6.0	V	—	—
VDD_HV_B	Secondary I/O supply voltage [1][2]	-0.3	—	6.0	V	—	—
VDD_DCDC	Supply voltage for the SMPS gate driver [1][2][3]	-0.3	—	6.0	V	—	—
V15	Voltage sensing input [1]	-0.3	—	2.75	V	For S32K388 and S32K389	—
V15	High-current logic supply voltage [1]	-0.3	—	2.75	V	For S32K358, S32K356, S32K348, S32K338 and S32K328	—
V15	High-current logic supply voltage [1][2]	-0.3	—	6.0	V	For all S32K3xx variants except S32K388, S32K389, S32K358, S32K356, S32K348, S32K338 and S32K328	—
V25	Flash memory supply (2.5 V), internally regulated [1]	-0.3	—	2.9	V	—	—
V11	High-current core logic supply input [1]	-0.3	—	1.26	V	For S32K388 and S32K389	—
V11	Core logic voltage supply	-0.3	—	1.26	V	For all S32K3xx variants except S32K388 and S32K389	—

Table continues on the next page...

Table 2. Absolute maximum ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	(1.1 V), internally regulated [1]						
VREFH	ADC high reference voltage [1][2]	-0.3	—	6.0	V	—	—
VREFL	ADC low reference voltage [1]	-0.3	—	0.3	V	—	—
VGPIO_trans	Transient overshoot voltage allowed on I/O pin [1][2][4]	-	—	6.0	V	—	—
I_INJPAD_DC_ABS	Continuous DC input current (positive/negative) that can be injected into an I/O pin [5]	-3	—	3	mA	—	—
I_INJSUM_DC_ABS	Sum of absolute value of injected currents on all the I/O pins (continuous DC limit) [5][6]	—	—	30	mA	—	—
TSTG	Storage ambient temperature [7]	-55	—	150	°C	—	—
TSDR	Maximum solder temperature[8]			260	°C	Pb free	

[1] All voltages are referred to VSS unless otherwise specified.
[2] 6.0 V maximum for 10 hours over lifetime; 7.0 V maximum for 60 seconds over lifetime.
[3] Voltage at VDD_DCDC cannot be higher than VDD_HV_A.
[4] When a low impedance voltage source, without current limitation, is connected to one or more I/O pins, the VGPIO_trans absolute max rating must be honored. During current injection, the voltage at the I/O pin or pins could go beyond this limit if (and ONLY IF) the injected current is being limited (I_INJPAD_DC_ABS is respected).
[5] When the input pad voltage levels are close to VDD_HV_A (respectively to VDD_HV_B) or VSS, plus /minus the forward voltage of ESD diodes, practically, no current is being injected. When these limits are exceeded, the maximum input current spec must be honored. See S32K3 Hardware Design Guidelines for more details and recommendations for protecting the devices against injection current.
[6] If a positive injection current is present in one or more I/O pins, and the device is in Low-Speed RUN or STANDBY mode, the VDD_HV_A (or respectively, VDD_HV_B) may lift and cause unexpected behavior. Therefore, it is recommended to add external protection hardware, to safely cover this scenario.
[7] TSTG specifies the storage temperature range. It is not the operating temperature range. Please refer to the Thermal operating characteristics table.
[8] Solder profile per IPC/JEDEC J-STD-020D.

5.2 Operating Conditions

Note: *Device functionality is guaranteed down to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics will be degraded when voltage drops below 2.97 V.*

The VDD_HV_B and V15 voltage supply domains are only present in certain devices and packages (S32K388, S32K389, S32K358, S32K356, S32K348, S32K338, S32K328, S32K344, S32K324, S32K314, S32K342, S32K341, S32K322).

The VDD_DCDC supply voltage is only present in certain devices and packages (S32K358, S32K356, S32K348, S32K338, S32K328, S32K388 and S32K389).

Table 3. Operating Conditions

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_A	Main I/O and analog supply voltage [1]	2.97	3.3 or 5.0	5.5	V	—	—
VDD_HV_B	Secondary I/O supply voltage [1]	2.97	3.3 or 5.0	5.5	V	—	—
VDD_DCDC	Supply voltage for the SMPS gate driver [1][2]	2.97	3.3 or 5.0	5.5	V	—	—
V15	Voltage sensing input [1][3]	1.425	1.5	1.65	V	For S32K388 and S32K389	—
I_V15	Current consumption of V15 pin	-2	180	400	uA	Applies to S32K388 and S32K389 in RUN mode	—
I_V15	Current consumption of V15 pin	-2	—	-2	uA	Applies to S32K388 and S32K389 in Standby mode with trickle regulator disabled	—
V15	High-current logic supply input voltage [1][3]	1.425	1.5	1.65	V	For all S32K3xx variants except S32K388 and S32K389	—
V15_extended	High-current logic supply input voltage, extended range [1][3][4][5]	1.425	3.3 or 5.0	5.5	V	For S32K322, S32K341, S32K342, S32K314, S32K324, S32K344	—
VREFH	ADC high reference voltage [1][6]	2.97	3.3 or 5.0	5.5	V	—	—
VREFL	ADC low reference voltage [1]	-0.1	0	0.1	V	—	—
VSS_DCDC	Power ground for the SMPS gate driver [1]	-0.1	0	0.1	V	—	—
V25	Flash memory and clock supply (2.5 V), internally regulated [1]	—	2.5	—	V	—	—
V11	High-current core logic supply input [1]	—	1.14	—	V	For S32K388 and S32K389	—
V11	Core logic supply (1.1 V), internally regulated [1]	—	1.14	—	V	For all S32K3xx variants except S32K388 and S32K389	—

Table continues on the next page...

Table 3. Operating Conditions...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VGPIO	Input voltage range at any I/O or analog pin [1][7]	-0.3	—	VDD_HV_A/B + 0.3	V	—	—
VODPU	Open-drain pull-up voltage [1][8]	—	—	VDD_HV_A/B	V	—	—
IINJPAD_DC_OP	Continuous DC input current (positive/ negative) that can be injected into an I/O pin [9]	-3	—	3	mA	VDD_HV_A >= 3.6V	—
IINJPAD_DC_OP	Continuous DC input current (positive/ negative) that can be injected into an I/O pin [9]	-2	—	3	mA	VDD_HV_A >= 2.97V	—
IINJSUM_DC_OP	Sum of absolute value of injected currents on all the I/O pins (continuous DC limit) [9][10]	-30	—	30	mA	VDD_HV_A >= 3.6V	—
IINJSUM_DC_OP	Sum of absolute value of injected currents on all the I/O pins (continuous DC limit) [9][10]	-20	—	30	mA	VDD_HV_A >= 2.97V	—
Vramp_slow	Supply ramp rate (slow) [1][11]	0.5	—	—	V/min	—	—
Vramp_fast	Supply ramp rate (fast) [1][11]	—	—	100	V/ms	—	—

[1] All voltages are referred to VSS unless otherwise specified.
[2] Voltage at VDD_DCDC cannot be higher than VDD_HV_A.
[3] Min and Max values are applicable only for non-SMPS mode where V15 is sourced externally.
[4] If total power dissipation and maximum junction temperature allows. Please refer to Thermal operating characteristics table for the maximum junction temperature, and Thermal characteristics table for the thermal characteristics, to determine the maximum power dissipation allowed for a given package.
[5] You must ensure that the junction temperature in the application must not exceed the maximum specified Tj.
[6] VREFH should always be equal to or less than VDD_HV_A +0.1. Any positive differential voltage between VREFH and VDD_HV_A i.e., VDD_HV_A < VREFH <= VDD_HV_A + 0.1V) is for RF-AC only. Appropriate decoupling capacitors should be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC
[7] Keeping the input voltage between this range practically ensures that no (noticeable) current is being injected. When exceeding these limits, the current being injected must be lower than IINJPAD_DC_OP, all the time.
[8] Open-drain outputs must be pulled respectively to their supply rail (VDD_HV_A or VDD_HV_B).
[9] When the input pad voltage levels are close to VDD_HV_A (respectively to VDD_HV_B) or VSS, plus /minus the forward voltage of ESD diodes, practically, no current is being injected. When these limits are exceeded, the maximum input current spec must be honored. Refer to the S32K3 Hardware Design Guidelines AN for more details and recommendations for protecting the devices against injection current.
[10] If a positive injection current is present in one or more I/O pins, and the device is in Low-Speed RUN or STANDBY mode, the VDD_HV_A (or respectively, VDD_HV_B) may lift and cause unexpected behavior. Therefore, it is recommended to add external protection hardware, to safely cover this scenario.
[11] The MCU supply ramp rate parameter must be applicable to the MCU input/external supplies. The ramp rate assumes that the S32K3xx HW design guidelines available on www.nxp.com are followed.

5.3 Thermal operating characteristics

Table 4. Thermal operating characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tamb	Ambient temperature	-40	—	105	°C	V- Grade	—
Tamb	Ambient temperature	-40	—	125	°C	M- Grade	—
TJ	Junction temperature	-40	—	150	°C	—	—

For S32K388 and S32K389, applications running at 125°C Tamb, thermal management schemes at PCB level will have to be deployed to keep TJ below 150°C.

5.4 ESD and Latch-up Protection Characteristics

Table 5. ESD and Latch-up Protection Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vhbm	Electrostatic discharge voltage, human body model (HBM) [1][2][3]	-2000	—	2000	V	—	—
Vcdm	Electrostatic discharge voltage, charged-device model (CDM), all pins except corner [1][2][4]	-500	—	500	V	—	—
Vcdm	Electrostatic discharge voltage, charged-device model (CDM), corner pins [1][2][4]	-750	—	750	V	—	—
Ilat	Latch-up current at ambient temperature of 125°C [5]	-100	—	100	mA	—	—

[1] Device failure is defined as: "If after exposure to ESD pulses, the device does not meet specification requirements."
[2] All ESD testing conforms with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
[3] This parameter is tested in conformity with AEC-Q100-002.
[4] This parameter is tested in conformity with AEC-Q100-011.
[5] This parameter is tested in conformity with AEC-Q100-004.

6 Power management

6.1 Power mode transition operating behaviors

6.1.1 Power mode transition operating behavior

The values in the table below are provided for reference only.

Table 6. Power mode transition operating behavior

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tMODE_ STDBYENTRY	RUN --> STANDBY transition time	—	1035	—	ns	For S32K388 and S32K389	—
tMODE_ STDBYENTRY	RUN --> STANDBY transition time	—	955	—	ns	—	—
tMODE_ STDBYEXIT_FAST	STANDBY --> RUN transition time, FastRecovery, V15External	—	58.5	—	us	For S32K328, S32K338, S32K348, S32K356 and S32K358	—
tMODE_ STDBYEXIT_FAST	STANDBY --> RUN transition time, Fast Recovery exit	—	53	—	us	FIRC ON @48MHz in Standby mode, For all S32K3xx devices except S32K3x8 and S32K389	—
tMODE_ STDBYEXIT	STANDBY --> RUN transition time, normal recovery exit	—	80	—	us	For all S32K3xx devices except S32K3x8 and S32K389	—
tMODE_ STDBYEXIT	STANDBY --> RUN transition time, Normal Recovery, V15 External	—	140	—	us	For S32K328, S32K338, S32K348, S32K356 and S32K358	—
tMODE_ STDBYEXIT	STANDBY --> RUN transition time, V15 SMPS with trickle LDO enabled	—	186	—	us	For S32K388 and S32K389	—
tMODE_ STDBYEXIT	STANDBY --> RUN transition time, with SMPS trickle LDO disabled [1]	—	212	—	us	For S32K388 and S32K389	—
tMODE_ STDBYEXIT	STANDBY --> RUN transition, time Normal Recovery, V15 SMPS	—	154	—	us	For S32K328, S32K338, S32K348, S32K356 and S32K358	—

[1] S32K388 and S32K389 doesn't support the FAST STANDBY EXIT recovery

6.1.2 Boot time, HSE firmware not installed

Table 7. Boot time, HSE firmware not installed

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tBOOT_noHSE	After a POR event, amount of time to	—	2	—	ms	Device running from FIRC (clocking option	—

Table continues on the next page...

Table 7. Boot time, HSE firmware not installed

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	execution of the first instruction of the application core, when HSE firmware is not installed. (HSE FW feature flag is disabled)					D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	

6.1.3 Boot time, HSE firmware installed

The following table provides the boot time of the S32K3 SBAF and Firmware initialization. To obtain the total boot time, the corresponding user code verification time must be added.

Table 8. Boot time, HSE firmware installed

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tBOOT_HSE_ NONSECURE	After a POR event, amount of time to execution of the first instruction of the application core, when HSE firmware is installed. (BOOT SEQ = 0)	—	—	3	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tBOOT_HSE	After a POR event, amount of time to execution of the first instruction of the application core, when HSE firmware is installed.	—	12.36	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tBOOT_HSE	After a POR event, amount of time to execution of the first instruction of the application core, when HSE firmware is installed.	—	9.51	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tBOOT_HSE	After a POR event, amount of time to execution of the first instruction of the application core, when HSE firmware is installed.	—	10.91	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—

6.1.4 HSE firmware memory verification time examples

Table 9. HSE firmware memory verification time examples

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 CMAC cipher.	—	11.3	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tCMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 CMAC cipher.	—	176	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tGMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 GMAC cipher.	—	3.2	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tGMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 GMAC cipher.	—	46.8	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tHMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 HMAC cipher.	—	1.74	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tHMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 HMAC cipher.	—	22.87	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tRSA_64KB	Memory verification of 64 KB of application firmware, using RSA 2048 cipher.	—	31.03	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tRSA_1024KB	Memory verification of 1024 KB of application firmware, using RSA 2048 cipher.	—	52.15	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tECDSA_64KB	Memory verification of 64 KB of application firmware,	—	126.46	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48	—

Table continues on the next page...

Table 9. HSE firmware memory verification time examples...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	using ECDSA 521 bits cipher.					MHz; HSE_CLK = 48 MHz.	
tECDSA_1024KB	Memory verification of 1024 KB of application firmware, using ECDSA 521 bits cipher.	—	147.53	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tSHA2_256_64KB	Memory verification of 64 KB of application firmware, using SHA2 256 bits bits cipher.	—	1.62	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tSHA2_256_ 1024KB	Memory verification of 1024 KB of application firmware, using SHA2 256 bits bits cipher.	—	22.73	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tCMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 CMAC cipher.	—	6.67	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tCMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 CMAC cipher.	—	105.24	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tGMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 GMAC cipher.	—	1.85	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tGMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 GMAC cipher.	—	28.03	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tHMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 HMAC cipher.	—	0.98	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tHMAC_1024KB	Memory verification of 1024 KB of	—	13.68	—	ms	Device running from PLL (clocking option	—

Table continues on the next page...

Table 9. HSE firmware memory verification time examples...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	application firmware, using AES-128 HMAC cipher.					A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	
tRSA_64KB	Memory verification of 64 KB of application firmware, using RSA 2048 cipher.	—	17.39	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tRSA_1024KB	Memory verification of 1024 KB of application firmware, using RSA 2048 cipher.	—	23.32	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tECDSA_64KB	Memory verification of 64 KB of application firmware, using ECDSA 521 bits cipher.	—	72.2	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tECDSA_1024KB	Memory verification of 1024 KB of application firmware, using ECDSA 521 bits cipher.	—	84.91	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tSHA2_256_64KB	Memory verification of 64 KB of application firmware, using SHA2 256 bits bits cipher.	—	0.9	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tSHA2_256_ 1024KB	Memory verification of 1024 KB of application firmware, using SHA2 256 bits bits cipher.	—	13.6	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tCMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 CMAC cipher.	—	4.5	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tCMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 CMAC cipher.	—	69.9	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—

Table continues on the next page...

Table 9. HSE firmware memory verification time examples...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tGMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 GMAC cipher.	—	1.3	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tGMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 GMAC cipher.	—	18.7	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tHMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 HMAC cipher.	—	0.7	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tHMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 HMAC cipher.	—	9.12	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tRSA_64KB	Memory verification of 64 KB of application firmware, using RSA 2048 cipher.	—	15.4	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tRSA_1024KB	Memory verification of 1024 KB of application firmware, using RSA 2048 cipher.	—	23.8	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tECDSA_64KB	Memory verification of 64 KB of application firmware, using ECDSA 521 bits cipher.	—	53.95	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tECDSA_1024KB	Memory verification of 1024 KB of application firmware, using ECDSA 521 bits cipher.	—	62.34	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tSHA2_256_64KB	Memory verification of 64 KB of application firmware,	—	0.64	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120	—

Table continues on the next page...

Table 9. HSE firmware memory verification time examples...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	using SHA2 256 bits bits cipher.					MHz; HSE_CLK = 120 MHz.	
tSHA2_256_1024KB	Memory verification of 1024 KB of application firmware, using SHA2 256 bits bits cipher.	—	9.07	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—

6.2 Supply Monitoring

Certain monitors are present on certain devices. See Power Management chapter in reference manual.

Table 10. Supply Monitoring

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
LVD_V15	Low Voltage Detect (LVD) on V15, deassert threshold (in FPM)	1.34	1.38	1.42	V	—	—
HVD_V15	High Voltage Detect (HVD) on V15, assert threshold (in FPM) [1]	—	2.5	—	V	—	—
LVR_VDD_HV_A	LVR on VDD_HV_A, assert threshold (in FPM)	2.77	2.85	2.93	V	—	—
LVR_VDD_HV_A	LVR on VDD_HV_A, assert threshold (in RPM)	2.77	2.85	2.93	V	—	—
—	VDD_HV_A LVR monitor hysteresis	—	18.75	—	mV	—	—
HVD_VDD_HV_A	HVD on VDD_HV_A, assert threshold (in FPM)	5.787	5.887	5.987	V	—	—
—	VDD_HV_A HVD monitor hysteresis	—	37.5	—	mV	—	—
LVR_VDD_HV_B	LVR on VDD_HV_B, assert threshold (in FPM)	2.77	2.85	2.93	V	—	—
LVR_VDD_HV_B	LVR on VDD_HV_B, assert threshold (in RPM)	2.77	2.85	2.93	V	—	—

Table continues on the next page...

Table 10. Supply Monitoring...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	VDD_HV_B LVR monitor hysteresis	—	18.75	—	mV	—	—
HVD_VDD_HV_B	HVD on VDD_HV_B, assert threshold (in FPM)	5.787	5.887	5.987	V	—	—
—	VDD_HV_B HVD monitor hysteresis	—	37.5	—	mV	—	—
LVD_VDD_HV_A	Low Voltage Detect (LVD5A) on VDD_HV_A, assert threshold (in FPM)	4.33	4.41	4.49	V	—	—
—	VDD_HV_A LVD monitor hysteresis	—	37.5	—	mV	—	—
VPOR_VDD_HV_A	Power-On-Reset (VPOR) on VDD_HV_A, deassert threshold	0.9	1.5	2.2	V	—	—
VREF12	Bandgap reference, trimmed [2]	1.18	1.2	1.22	V	—	—

[1] The HVD_V15 monitor is provided to indicate if the V15 rail is far above the standard V15 operating range , to ensure failures in the V15 regulator are detected

[2] Does not take into consideration the accuracy associated with the ADC or other application-specific factors such as variations in power supply, reference voltage instability, and external sources of noise. See section ADC electrical specification and applicable application note(s) and assess sources of variation in the application when determining limits

6.3 Recommended Decoupling Capacitors

Table 11. Recommended Decoupling Capacitors

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CDEC	Decoupling capacitor (one per supply pin) [1][2][3]	—	100 or 220	—	nF	—	—
CBULK	Input supply bulk capacitor [1][4][5][6]	—	4.7 or 10	—	µF	—	—
COUT_V15_NPN	V15 (1.5V Regulator) output capacitor [1][7]	—	2.2	—	µF	—	—
COUT_V11	V11 (1.1V Regulator) output capacitor (all chips, except	—	2.2	—	µF	—	—

Table continues on the next page...

Table 11. Recommended Decoupling Capacitors*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	S32K312, S32K311, S32K310, S32K388 and S32K389) [1]						
COUT_V11	V11 (1.1V Regulator) output capacitor (S32K312, S32K311 & S32K310) [1]	—	1	—	µF	—	—
COUT_V11	V11 (1.1V Regulator) output capacitor (S32K388 and S32K389) [1]	—	22	—	uF	—	—
COUT_V25	V25 (2.5V Regulator) output capacitor [1][2]	140	220	—	nF	—	—

[1] All capacitors must be low ESR ceramic capacitors (for example, X7R). The minimum recommendation is after considering component aging and tolerance.
[2] These capacitors must be placed as close as possible to the corresponding supply and ground pins. For BGA packages, the capacitors must be placed on the other side of the PCB to minimize the trace lengths.
[3] Optionally, 1 nF capacitors can be added in parallel to the decoupling capacitors.
[4] It is also possible to use higher capacitance values (for example, 10 µF) in place of the 4.7 µF capacitor.
[5] For devices where the VDD_HV_B domain is present, if the VDD_HV_B supply is different supply from VDD_HV_A, a dedicated bulk capacitor is needed.
[6] These capacitors must be placed close to the source.
[7] For devices where V15 is present, the V15 regulator output capacitor and the filter capacitors are required when using an NPN bipolar ballast transistor for the regulation stage. When V15 is supplied from an external regulator, these capacitance recommendations can be followed in addition to the capacitance requirements of the external voltage regulator.

6.3.1 Recommended Decoupling Capacitor diagrams

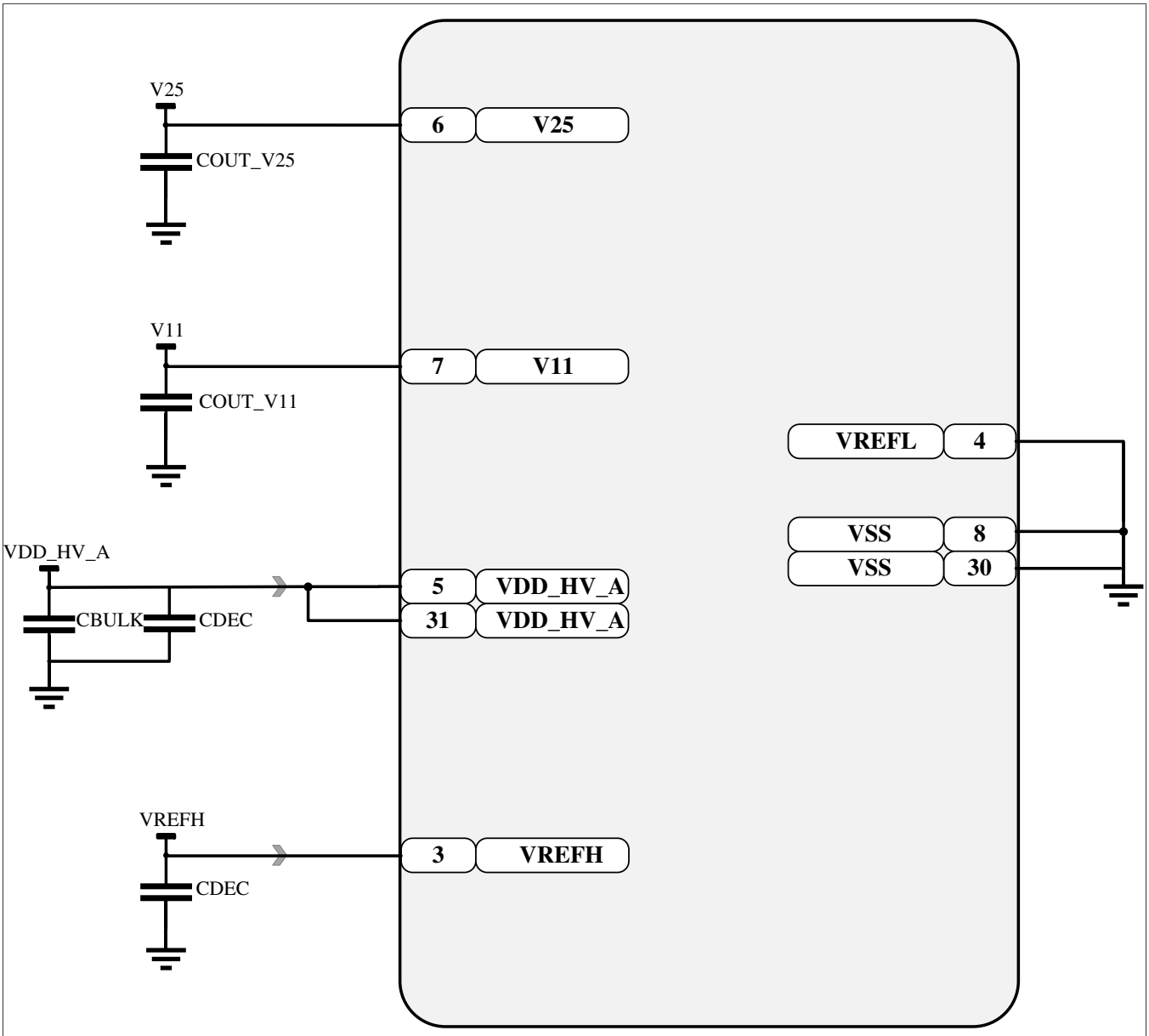


Figure 18. 48-pin LQFP decoupling capacitor pinout diagram (S32K311, S32K310)

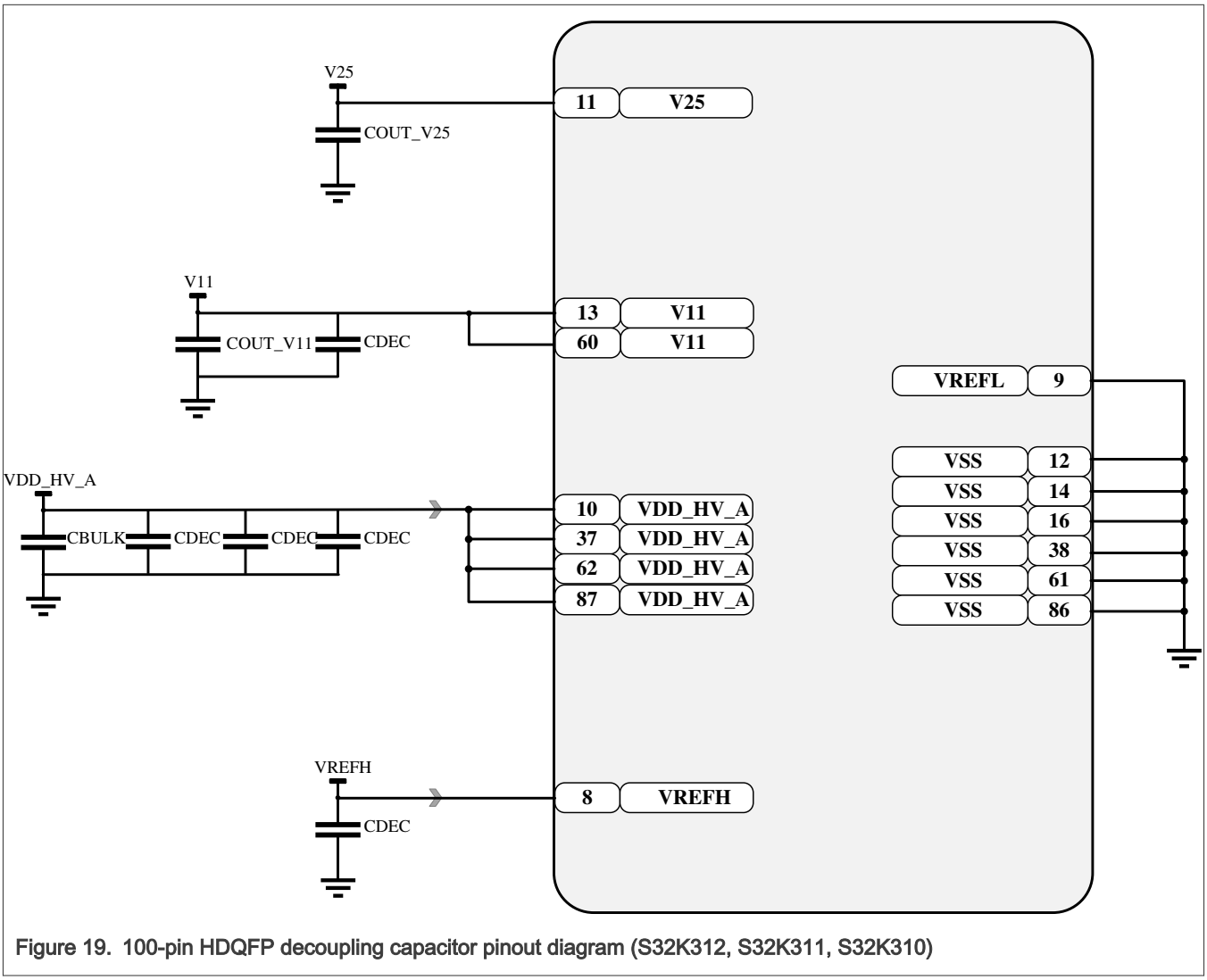


Figure 19. 100-pin HDQFP decoupling capacitor pinout diagram (S32K312, S32K311, S32K310)

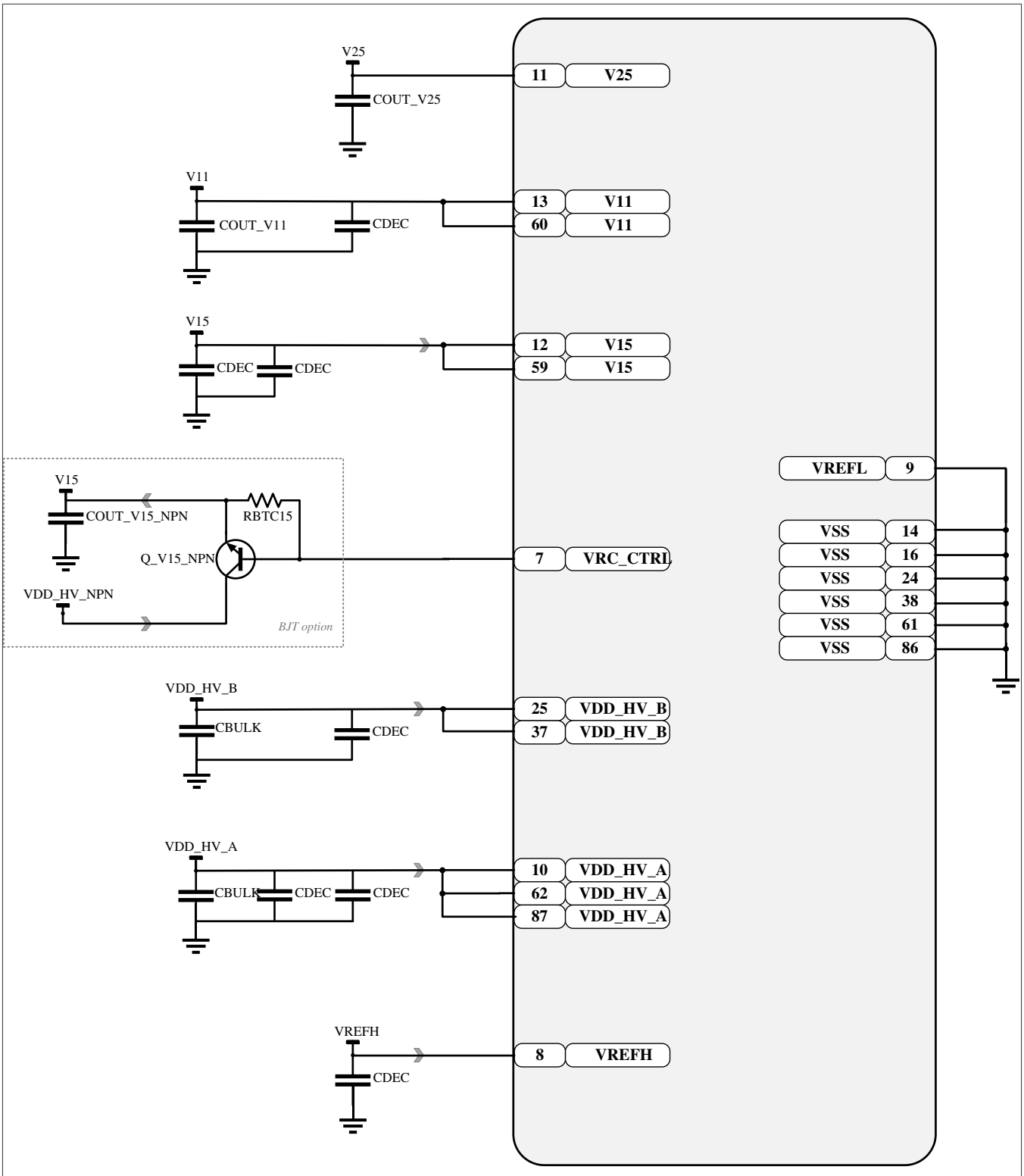


Figure 20. 100-pin HDQFP decoupling capacitor pinout diagram (S32K342, S32K341, S32K322)

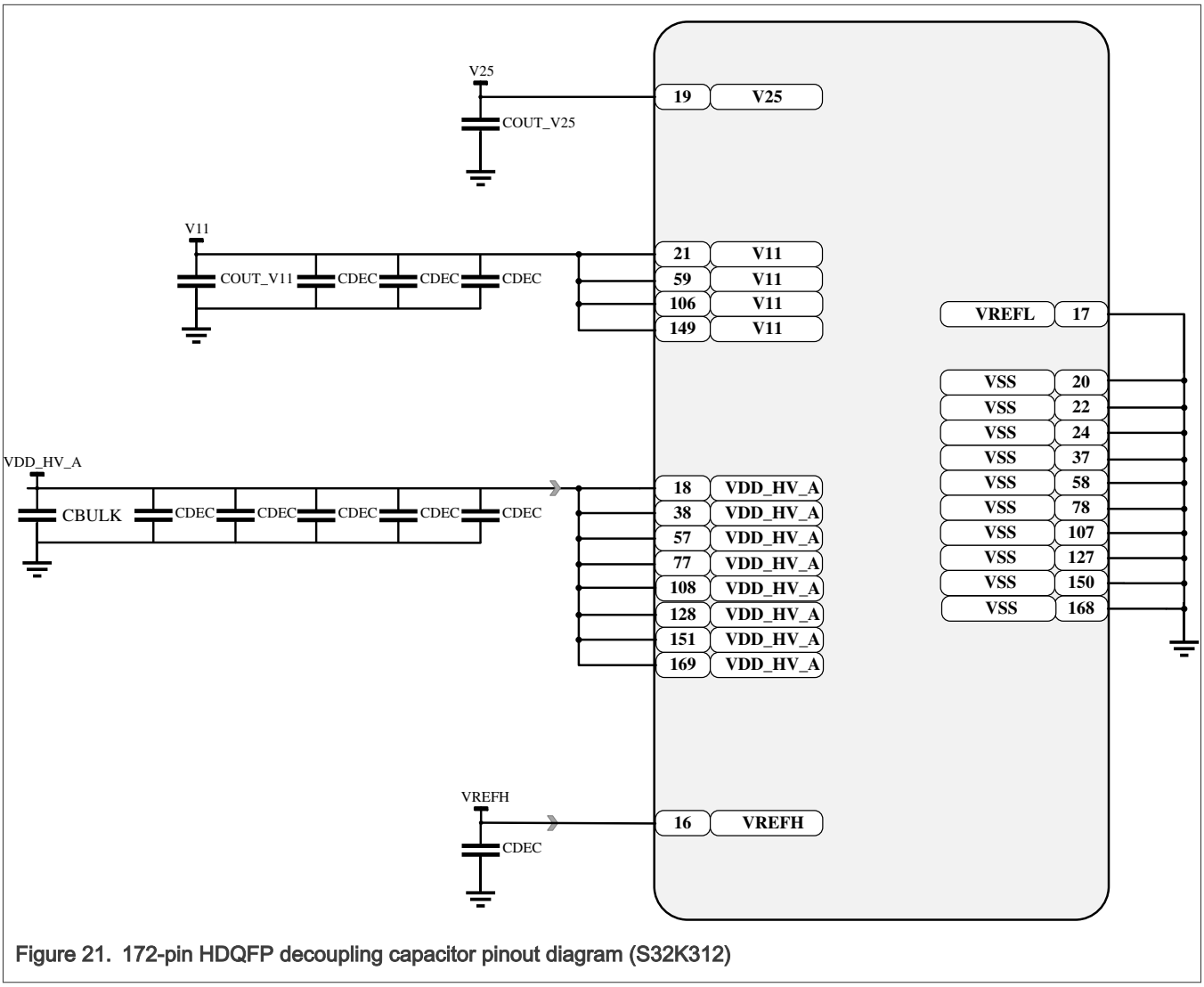


Figure 21. 172-pin HDQFP decoupling capacitor pinout diagram (S32K312)

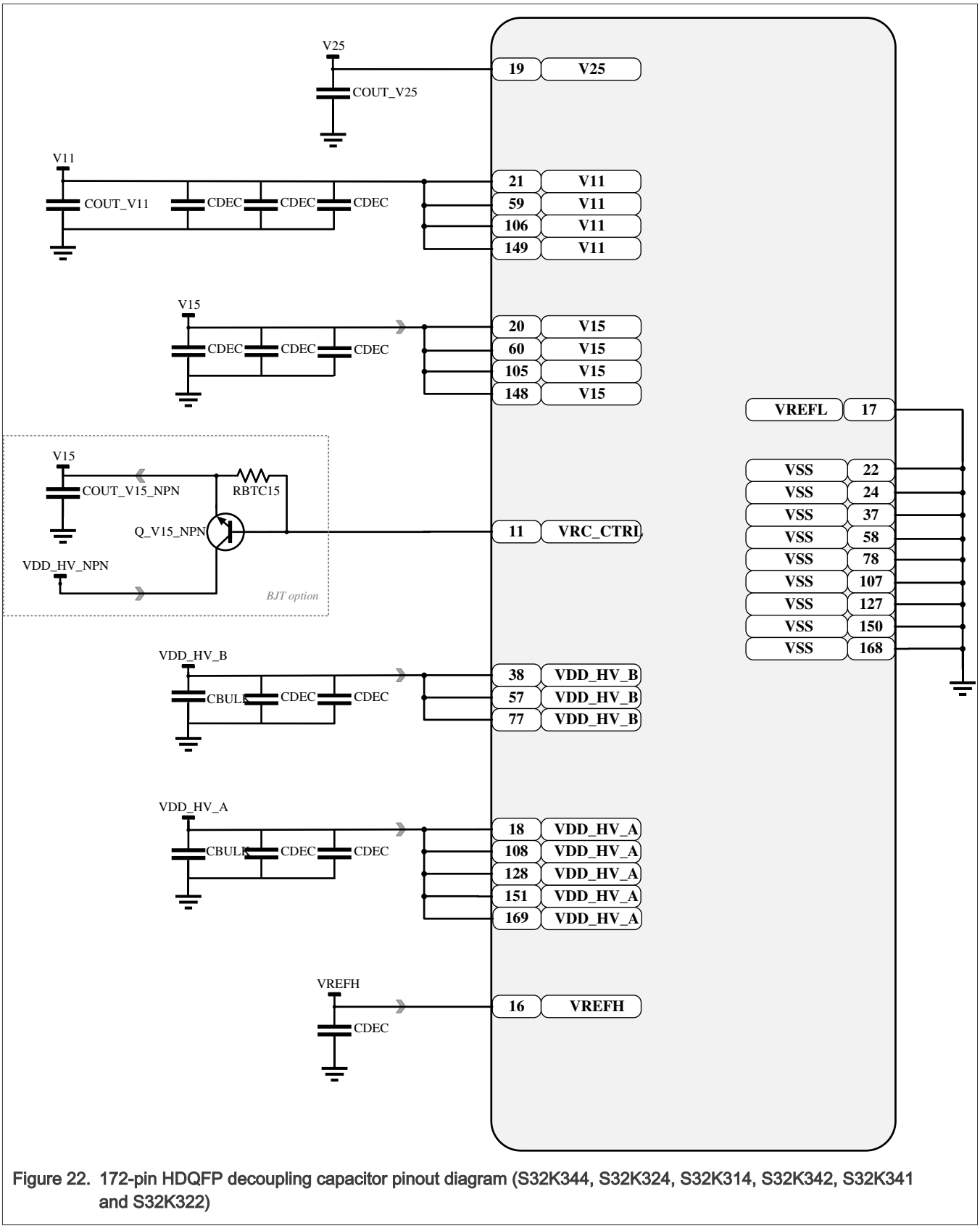


Figure 22. 172-pin HDQFP decoupling capacitor pinout diagram (S32K344, S32K324, S32K314, S32K342, S32K341 and S32K322)

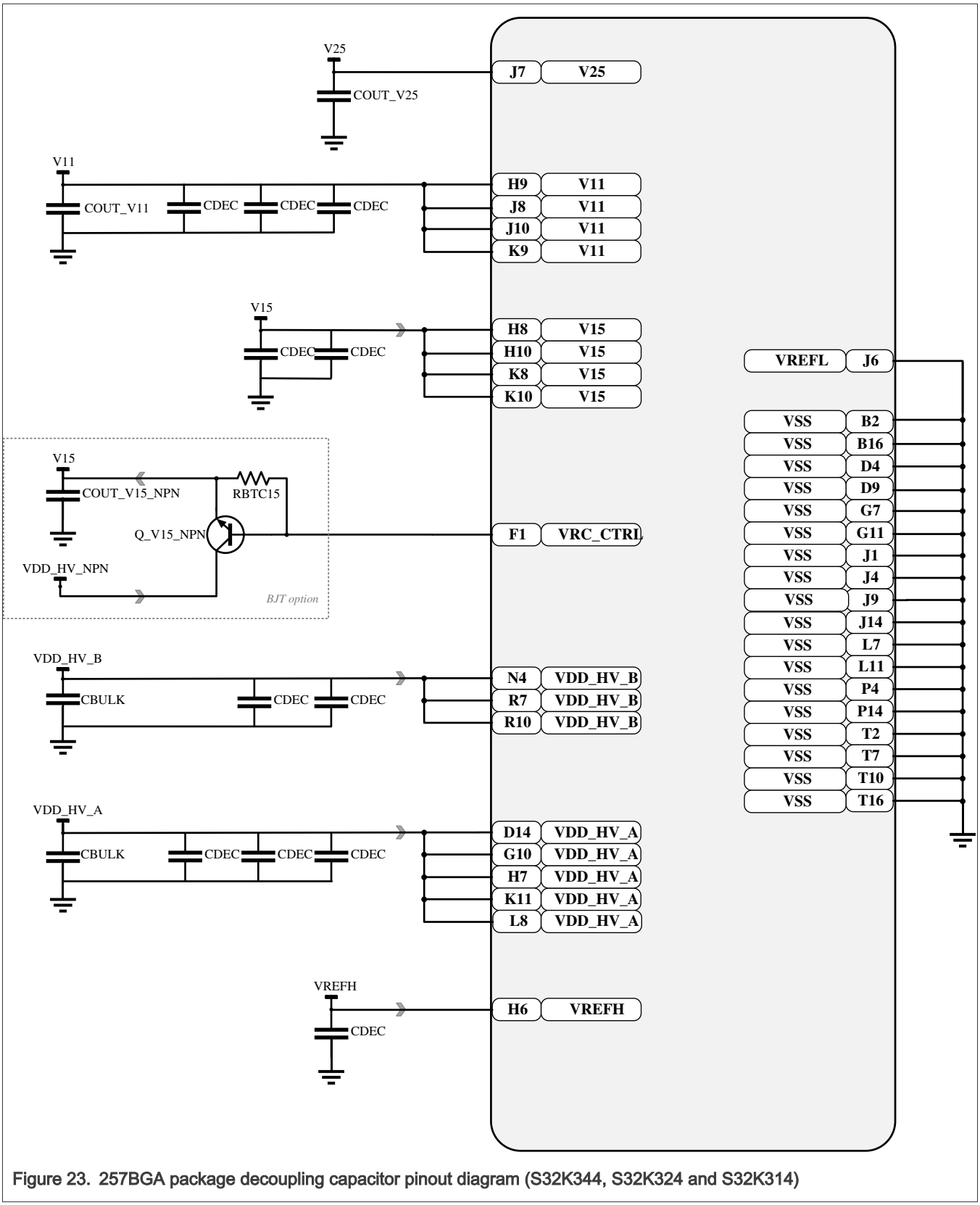


Figure 23. 257BGA package decoupling capacitor pinout diagram (S32K344, S32K324 and S32K314)

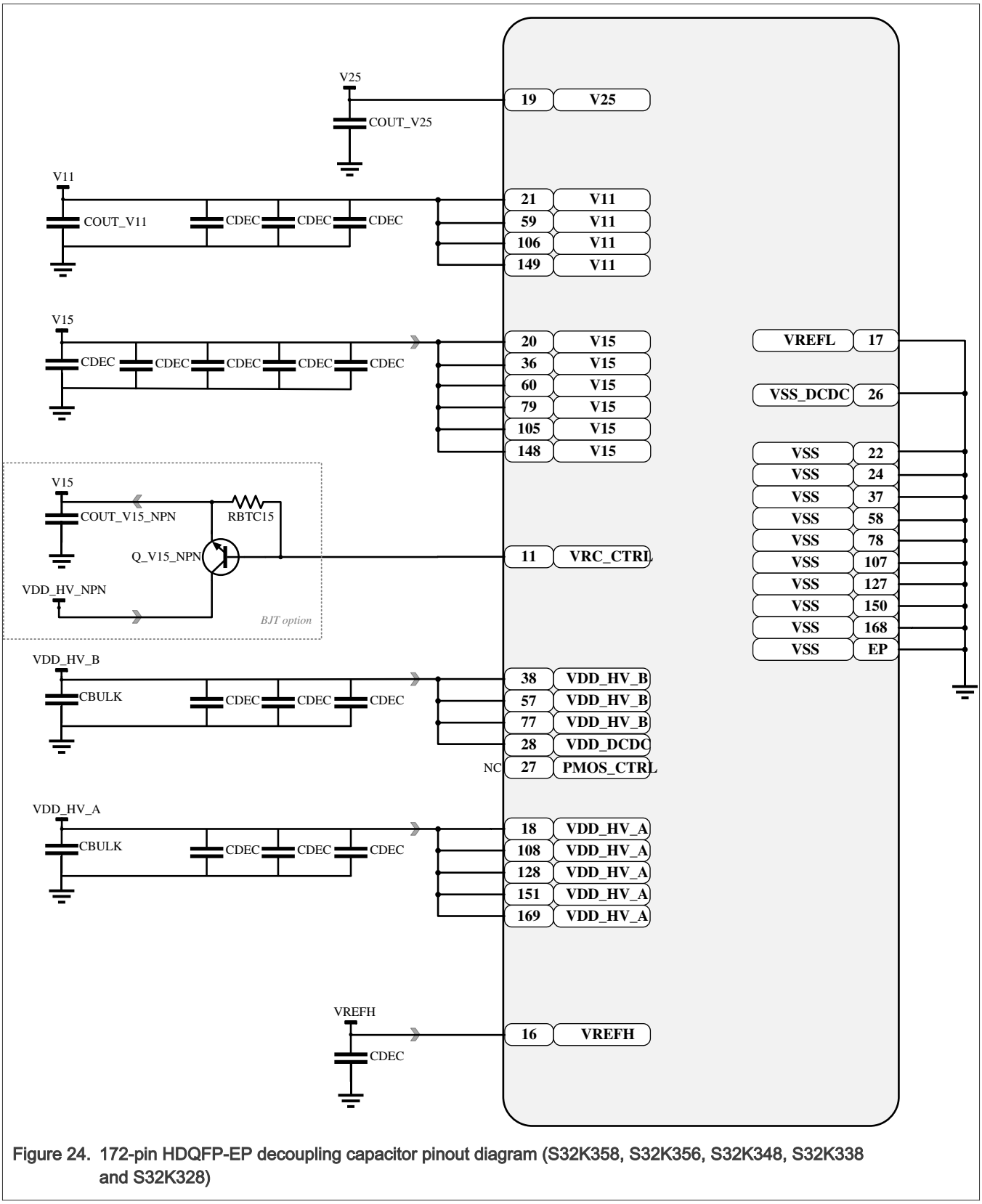


Figure 24. 172-pin HDQFP-EP decoupling capacitor pinout diagram (S32K358, S32K356, S32K348, S32K338 and S32K328)

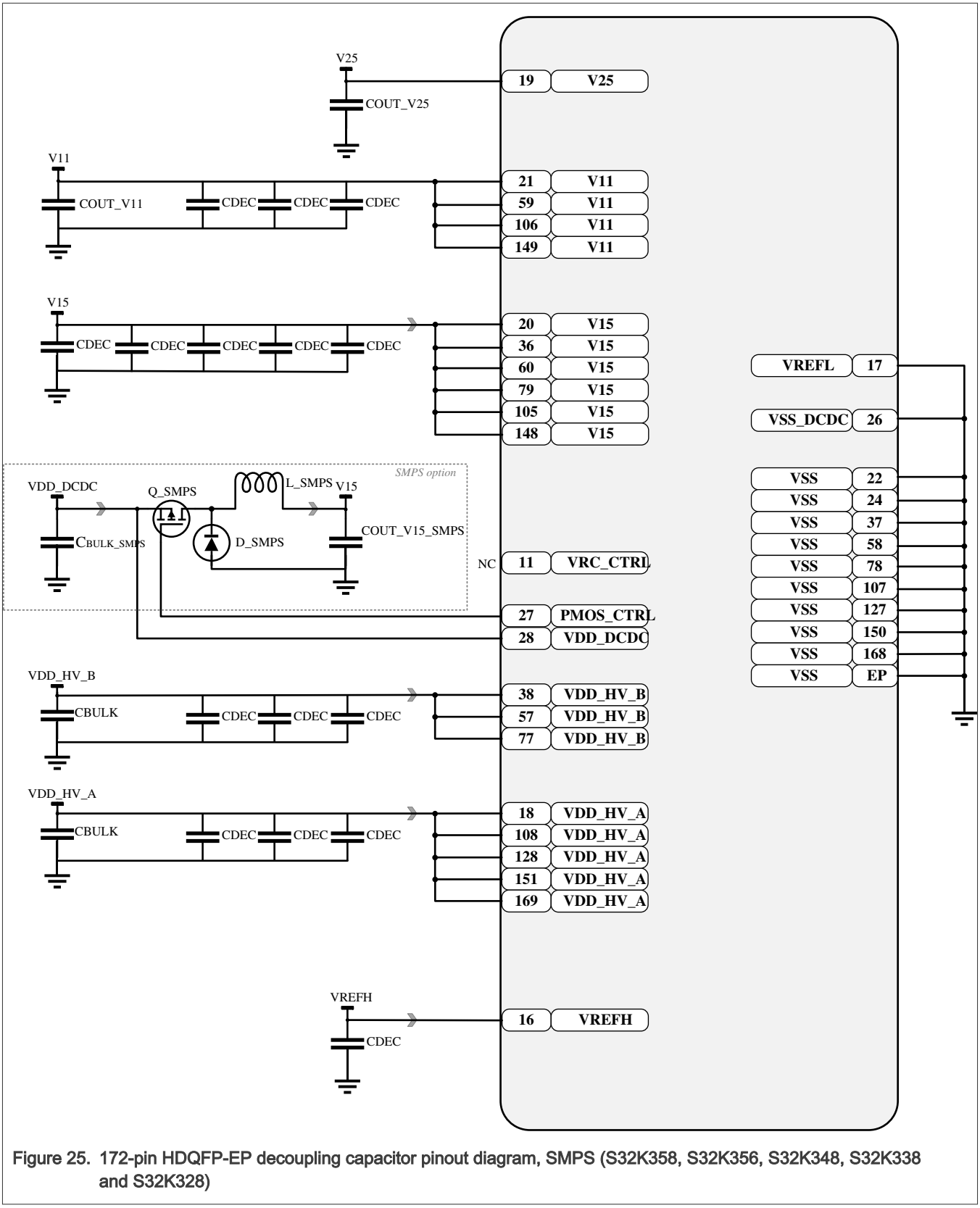


Figure 25. 172-pin HDQFP-EP decoupling capacitor pinout diagram, SMPS (S32K358, S32K356, S32K348, S32K338 and S32K328)

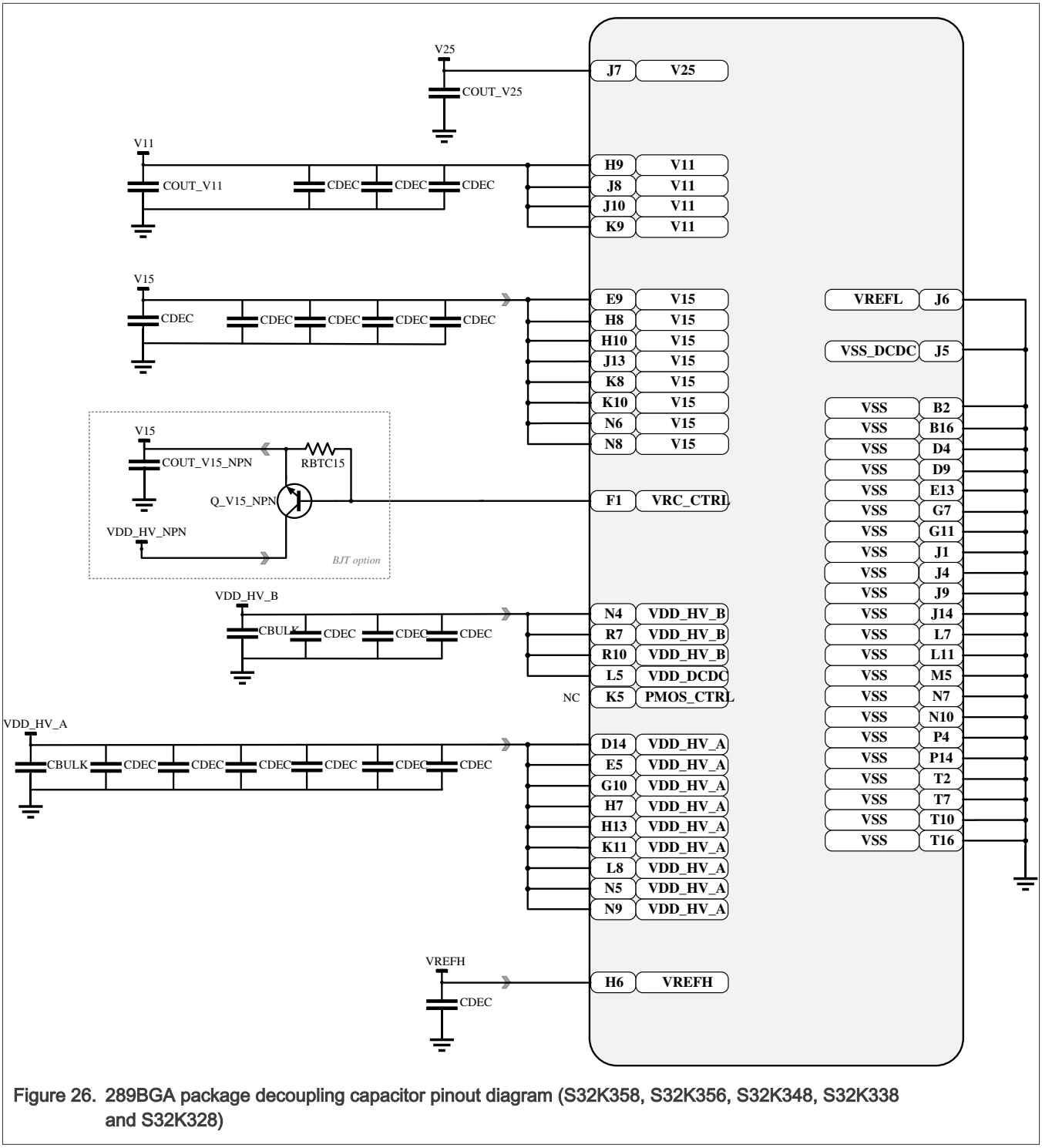


Figure 26. 289BGA package decoupling capacitor pinout diagram (S32K358, S32K356, S32K348, S32K338 and S32K328)

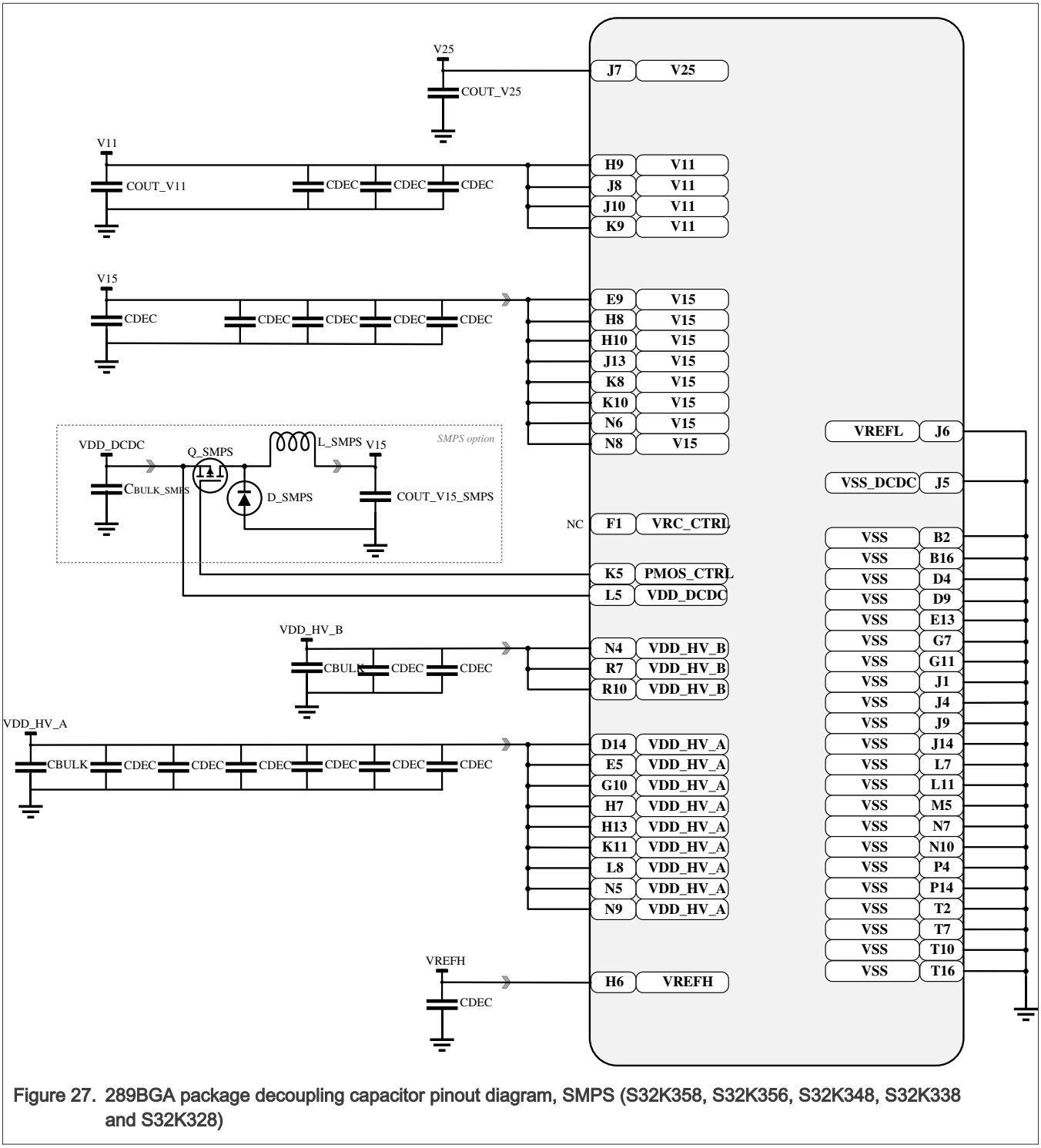


Figure 27. 289BGA package decoupling capacitor pinout diagram, SMPS (S32K358, S32K356, S32K348, S32K338 and S32K328)

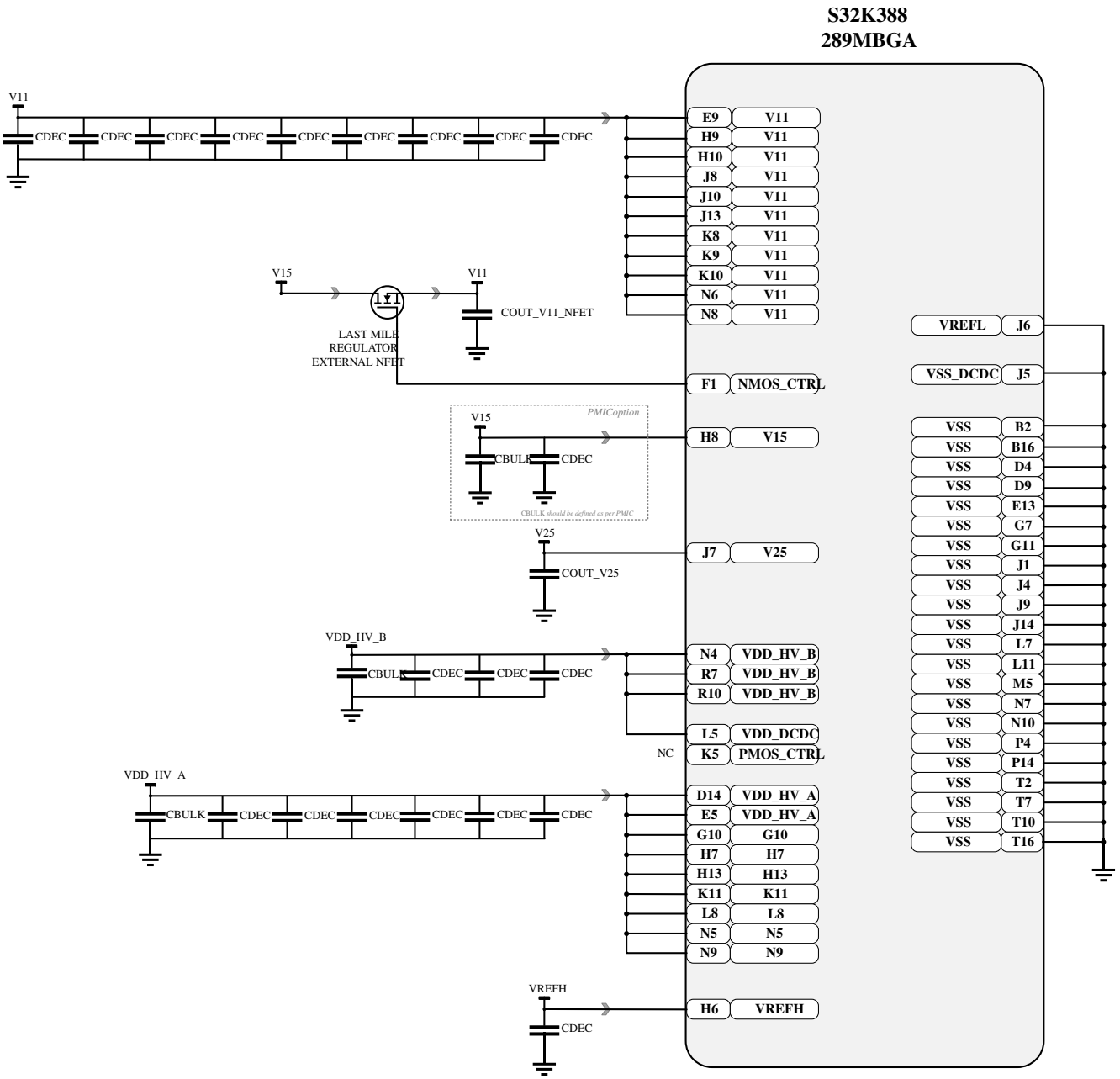


Figure 28. 289BGA package decoupling capacitor pinout diagram, (S32K388)

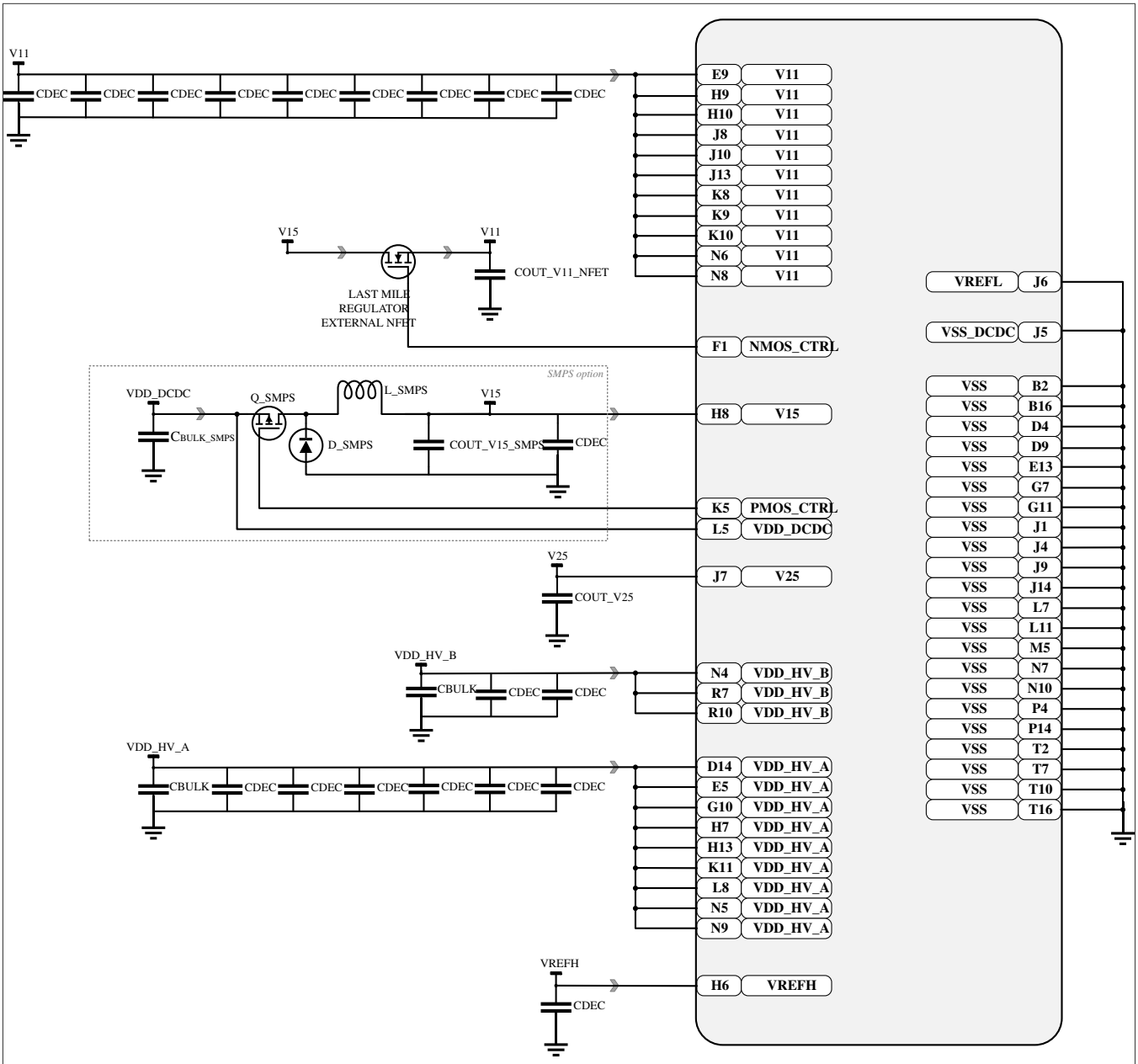


Figure 29. 289BGA package decoupling capacitor pinout diagram, SMPS (S32K388)

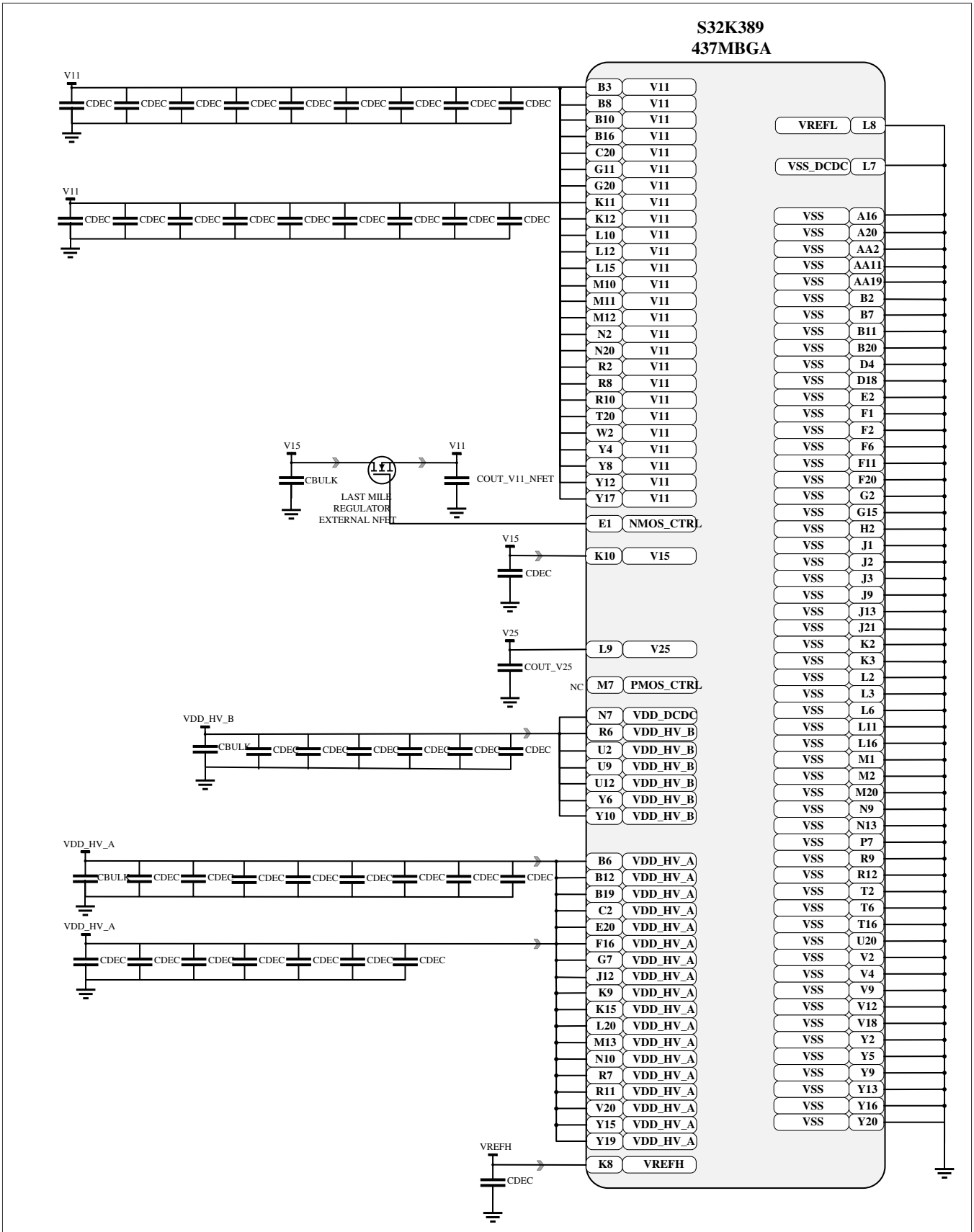


Figure 30. 437BGA package decoupling capacitor pinout diagram(S32K389)

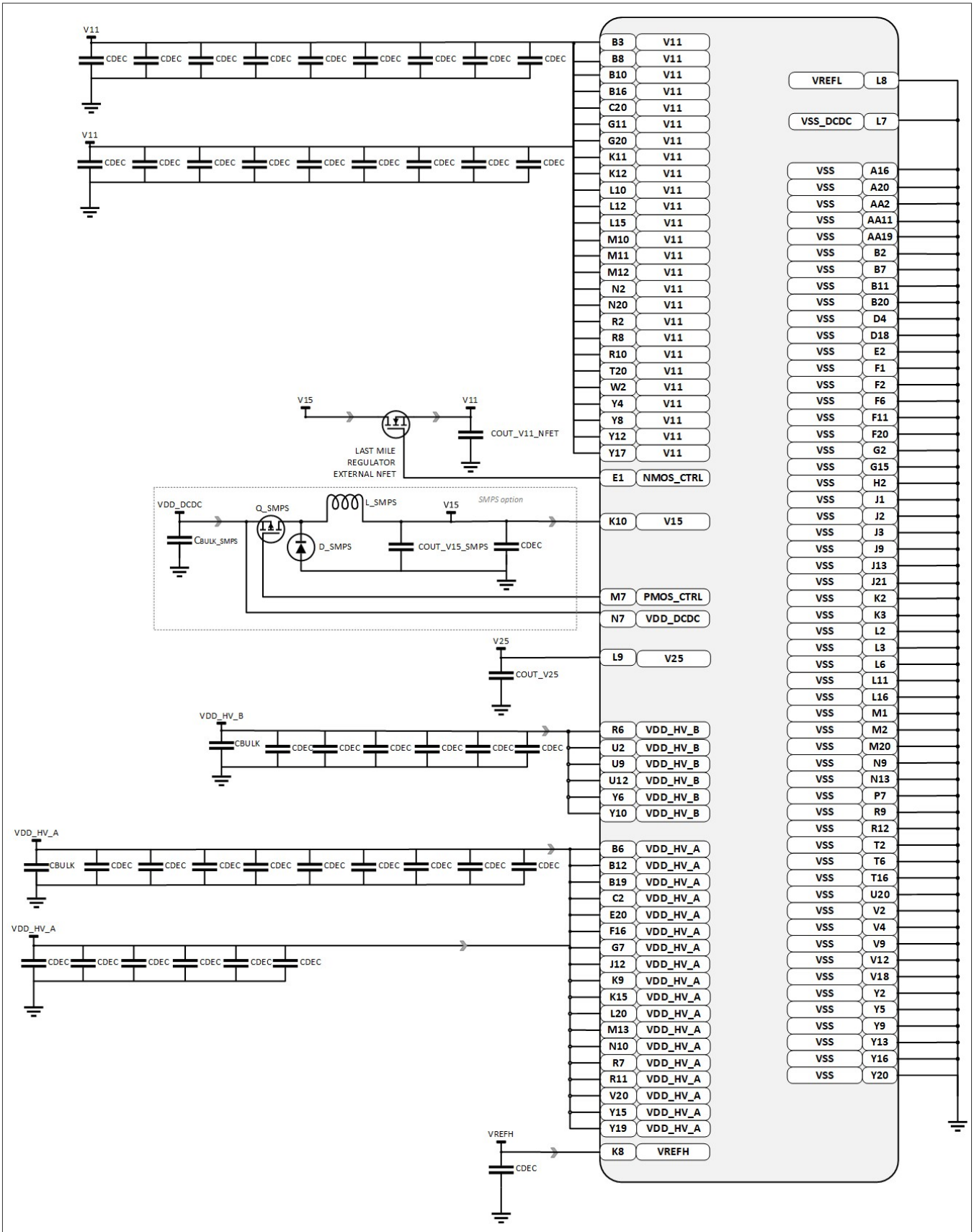


Figure 31. 437BGA package decoupling capacitor pinout diagram, SMPS(S32K389)

6.4 V15 regulator (SMPS option) electrical specifications

Some devices (S32K358, S32K356, S32K348, S32K338, S32K328, S32K388 and S32K389) support a SMPS, DC-DC buck converter stage, with a dedicated pin to control an external Power P-channel MOSFET. In addition to the PMOS, an external inductor and a Schottky diode are required. See related figures in section "Recommended decoupling capacitors".

The chip hardware design guidelines document lists the recommended part numbers for PMOS, Schottky diode and inductor.

Table 12. V15 regulator (SMPS option) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
V15	V15 output	—	1.5	—	V	—	—
L_SMPS	External coil inductance	—	4.7	—	uH	—	—
COUT_V15_SMPS	External bypass capacitor	—	20-22	—	uF	—	—
D_SMPS	External Schottky diode average forward current	—	2	—	A	—	—
VR	Schottky diode reverse voltage	5.0	—	—	V	—	—
IF	Schottky diode forward current	1.0	—	—	A	—	—
—	External P-channel MOSFET total gate charge	—	—	10	nC	VDD_DCDC = 5V	—
—	External P-channel MOSFET threshold voltage	—	—	2	V	—	—
CBULK_SMPS	Input supply bulk capacitor for internal SMPS [1]	—	22	—	µF	—	—

[1] Highly Recommended when internal SMPS is used to generate V15 and VDD_DCDC is supplied with isolated source from VDD_HV_A or VDD_HV_B

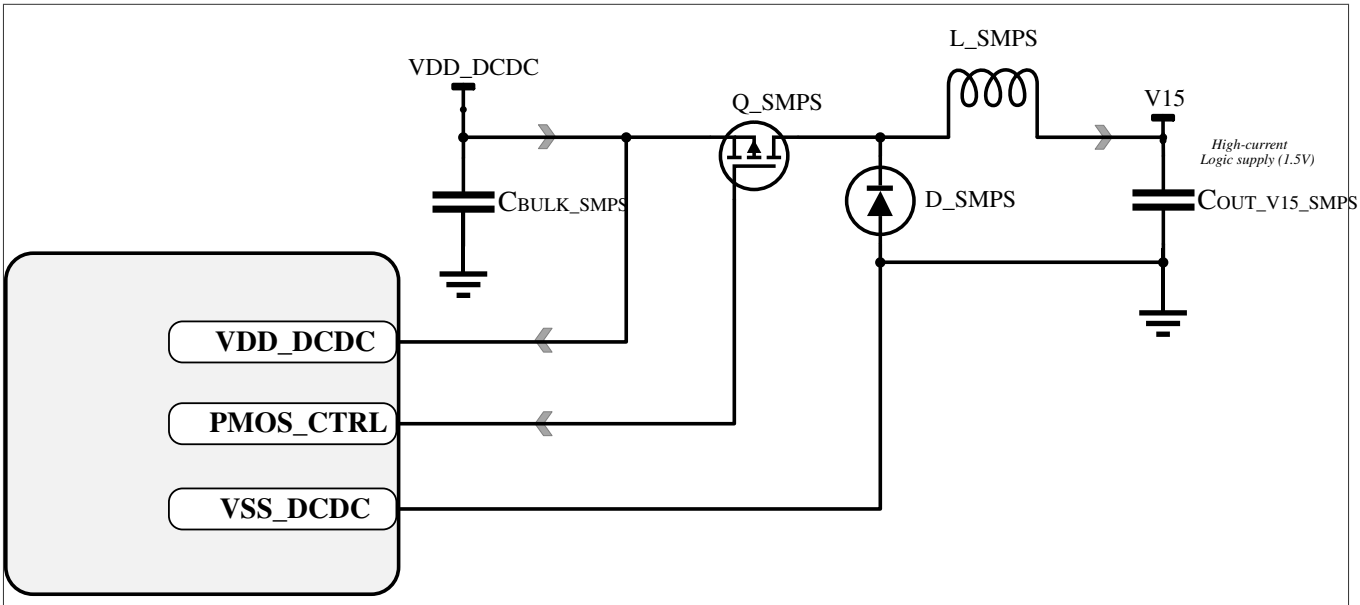


Figure 32. SMPS circuit

6.5 V15 regulator (BJT option, NPN ballast transistor control) electrical specifications

Some devices (S32K358, S32K356, S32K348, S32K338, S32K328, S32K344, S32K324, S32K314, S32K342, S32K322, S32K341) support a linear regulator stage, with a dedicated pin to control an external NPN bipolar transistor. The chip hardware design guidelines document lists the recommended part numbers for the external devices.

The chip hardware design guidelines document lists the recommended part number for NMOS. The S32K388 supports a linear regulator stage for the V11 supply, with a dedicated pin to control an external NMOS transistor.

Table 13. V15 regulator (BJT option, NPN ballast transistor control) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
V15	V15 output	—	1.51	—	V	—	—
IBCTL	IBCTL (V15 reg) source	10	—	—	mA	—	—
IBCTL	IBCTL (V15 reg) sink	—	—	-50	uA	—	—
tsettle_lm	Required setting time from V11 in FPM to load change	10	—	—	us	—	—
VDD_HV_NPN	Input voltage supply for NPN external ballast transistor	2.5	3.3 or 5	—	V	—	—

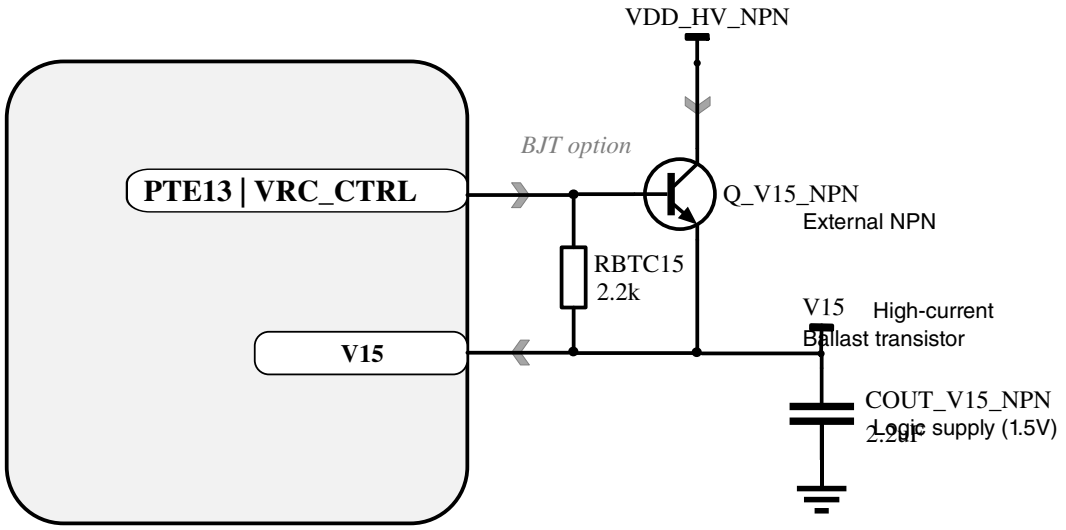


Figure 33. Ballast circuit

6.6 V11 regulator (NMOS ballast transistor control) electrical specifications

The chip hardware design guidelines document lists the recommended part number for NMOS. The S32K388 and S32K389 supports a linear regulator stage for the V11 supply, with a dedicated pin to control an external NMOS transistor.

Table 14. V11 regulator (NMOS ballast transistor control) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
V15	V15 input	—	1.5	—	V	—	—
V11	V11 output	—	1.14	—	V	—	—
VTH_NMOS	Vth of external NMOS	—	—	1.5	V	For 3.3 V supply	—
VTH_NMOS	Vth of external NMOS	—	—	2	V	For 5.0 V supply	—
IDS_NMOS	IDS of external NMOS	3	—	—	A	—	—
tsettle_lm	Required setting time from V11 in FPM to load change	10	—	—	us	—	—
CNMOS	NMOS gate stability capacitor	—	1	—	nF	—	—
ILKG_NMOS	Allowable drain to source leakage thru the external NMOS transistor	—	—	2	mA	—	—

6.7 Supply currents

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, VDD_HV_B = 5V (if the VDD_HV_B domain present in the

device), temperature = 25 °C, and typical silicon process unless otherwise stated. In STANDBY configuration, no current flows through the V15 supply.

Table 15. STANDBY mode supply currents

Chip	Ambient Temperature (°C)	STANDBY [1]			
		VDD_HV_A [2]			VDD_HV_B [2]
		All clocks & peripherals OFF (µA)	SIRC ON (µA)	FIRC ON (24 MHz) (mA)	All Config. (µA)
S32K389	25, typ [3]	101.6	102.1	2.242	4.2
	25, max [4]	320.7	325.0	2.690	5.8
	85, typ [3]	573.2	573.7	2.593	8.2
	85, max [4]	1681.6	1719.1	3.556	18.0
	105, typ [3]	1012.6	1018.3	2.947	14.3
	105, max [4]	2949.8	2991.5	4.703	38.4
	125, typ [4]	1692.8	1702.3	3.617	30.7
	125, max [3]	5140.6	5147.3	7.005	85.4
S32K388	25, typ [3]	74.0	74.0	2.236	3.5
	25, max [4]	233.2	236.4	2.658	5.6
	85, typ [3]	390.3	390.9	2.557	7.5
	85, max [4]	1165.2	1206.3	3.327	17.6
	105, typ [3]	747.5	747.9	2.915	14.3
	105, max [4]	2277.7	2352.5	4.319	38.4
	125, typ [3]	1389.9	1390.1	3.558	30.7
	125, max [4]	4192.3	4243.1	6.044	85.4
S32K358, S32K356, S32K348, S32K338, S32K328	25, typ [3]	64.9	67.1	1.5137	1.9
	25, max [4]	194.0	204.9	2.0132	3.9
	85, typ [3]	326.5	326.4	1.7222	6.1
	85, max [4]	1586.3	1621.4	3.2009	17.9

Table continues on the next page...

Table 15. STANDBY mode supply currents...*continued*

	105, typ [3]	617.8	621.6	2.0290	12.3
	105, max [4]	2977.6	2997.1	4.4926	33.8
	125, typ [3]	1179.5	1180.2	2.5613	32.0
	125, max [4]	4997.2	5067.0	6.4388	77.8
S32K344, S32K324, S32K314	25, typ [3]	50	52	0.91	1.8
	25, max [4]	153	153	1.09	3.8
	85, typ [3]	315	316	1.18	6.1
	85, max[4]	900	910	1.78	15.4
	105, typ [3]	498	530	1.40	8.5
	105, max [4]	1672	1682	2.55	26.2
	125, typ [3]	932	998	1.88	18.5
	125, max [4]	2638	2650	3.5	47.3
S32K342, S32K322, S32K341	25, typ [3]	46.5	49	0.900	1.8
	25, max [4]	88	94	1.090	3.5
	85, typ [3]	220.5	239.4	1.1619	5.4
	85, max [4]	627.0	642.9	1.587	13.9
	105, typ [3]	428.3	456.5	1.3638	7.3
	105, max [4]	1272.6	1301.6	2.2098	22.5
	125, typ [3]	715.2	745	1.6279	16.7
	125, max [4]	2113.4	2160.6	3.0016	41.6
S32K312	25, typ [3]	40	41	0.887	NA
	25, max [4]	79	80	1.031	
	85, typ [3]	178	178	1.027	
	85, max [4]	496	497	1.422	
	105, typ [3]	350	346	1.197	
	105, max [4]	994	997	1.924	

Table continues on the next page...

Table 15. STANDBY mode supply currents*...continued*

	125, typ [3]	620	611	1.457	
	125, max [4]	1788	1792	2.761	
S32K311, S32K310	25, typ [3]	38.9	39.8	1.365	NA
	25, max [4]	77.2	79.8	1.823	
	85, typ [3]	144.3	144.9	1.480	
	85, max [4]	491.5	494.8	2.263	
	105, typ [3]	263.8	264.2	1.559	
	105, max [4]	937.4	947.1	2.597	
	125, typ [3]	508.5	510	1.811	
	125, max [4]	1740.1	1760.3	3.488	

[1] See the configurations in Table 22.
[2] IO load current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
[3] "typ" is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, for the typical silicon process..
[4] "max" is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, for the fast silicon process.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, VDD_HV_B = 5V (if the VDD_HV_B domain present in the device), temperature = 25 °C, and typical silicon process unless otherwise stated.

Table 16. Low speed RUN mode supply currents

Chip	Ambient Temperature (°C)	Low Speed RUN Mode (mA) [1]												
		BOOT Mode [2] [Clock Option C] FIRC @ 24 MHz [Last Mile Disabled]		BOOT Mode [2] [Clock Option C] FIRC @ 24 MHz [Last Mile Enabled]		Low Speed RUN [2] [Clock Option E] FIRC @3 MHz [Last Mile Disabled]		Low Speed RUN [2] [Clock Option E] FIRC @3 MHz [Last Mile Enabled]		Low Speed RUN [2] [Clock Option D] FIRC @48 MHz [Last Mile Disabled]		Low Speed RUN [2] [Clock Option D] FIRC @48 MHz [Last Mile Enabled]		All Config[2].
		VDD_HV_A [3], [4]	V15 [5]/ V11 [6]	VDD_HV_A [3], [4]	V15 [5]/ V11[6]	VDD_HV_A [3], [4]	V15 [5]/ V11[6]	VDD_HV_A [3], [4]	V15 [5]/ V11[6]	VDD_HV_A [3], [4]	V15 [5]/ V11[6]	VDD_HV_A [3], [4]	V15 [5]/ V11[6]	VDD_HV_B [3]

Table continues on the next page...

Table 16. Low speed RUN mode supply currents...*continued*

S32K389	25, typ [7]	NA	3.1	53.0	NA	3.1	27.1	NA	3.1	84.4	2.4
	25, max [8]		3.9	128.8		3.5	102.3		3.9	162.9	3.0
	85, typ [7]		3.3	144.5		3.2	118.4		3.3	176.0	2.4
	105, typ [7]		4.1	346.4		4.0	321.4		4.2	373.9	3.0
	105, max [8]		3.4	218.1		3.3	194.0		3.4	249.3	2.4
	125, typ [7]		4.3	570.1		4.3	542.4		4.4	597.6	3.0
	125, max [8], [9]		3.6	354.9		3.5	338.9		3.6	386.0	2.4
	85, max [8]		5.6	945.8		5.5	917.2		5.7	966.1	3.0
S32K388	25, typ [7]	NA	2.7	43.0	NA	2.7	18.9	NA	2.7	70.4	2.4
	25, max [8]		3.8	153.6		3.1	129.2		3.9	180.7	2.8
	85, typ [7]		2.7	108.2		2.7	84.0		2.7	136.2	2.4
	85, max [8]		4.0	289.7		3.9	266.8		4.1	317.7	2.8
	105, typ [7]		2.8	216.8		2.8	192.7		2.9	243.7	2.4
	105, max [8]		4.2	534.9		4.2	516.1		4.3	558.8	2.8
	125, typ [7]		3.0	343.8		3.0	320.5		3.1	371.1	2.4
	125, max [8], [9]		5.5	936.1		5.3	915.7		5.6	960.0	2.8
S32K358, S32K356, S32K348, S32K338, S32K328	25, typ [7]	NA	3.1	34.1	NA	3.0	8.5	NA	3.2	63.3	1.6
	25, max [8]		3.6	52.7		3.5	26.4		3.7	83.0	2.4
	85, typ [7]		3.1	60.6		3.1	34.9		3.2	90.2	1.6
	85, max [8]		3.7	182.9		3.7	155.5		3.8	212.3	2.4
	105, typ [7]		3.2	88.4		3.2	62.4		3.3	117.8	1.6
	105, max [8]		3.9	297.2		3.9	273.9		4.0	323.4	2.4
	125, typ [7]		3.5	136.6		3.4	110.5		3.5	166.3	1.6

Table continues on the next page...

Table 16. Low speed RUN mode supply currents...*continued*

	125, max [8], [9]			4.5	494.9			4.4	468.6			4.7	521.0	2.4
S32K344, S32K324, S32K314	25, typ [7]	20.5	-	2.8	17.9	6.4	-	2.8	4.5	37.2	-	2.9	34	0.6
	25, max[8]	29.4	-	3.3	27.2	14.8	-	3.3	12.6	46.8	-	3.4	46.6	0.8
	85, typ [7]	34.2	-	2.9	31.2	19.7	-	2.9	17.5	50.4	-	2.9	47.3	0.6
	85, max [8]	71.6	-	3.5	68.7	56.2	-	3.4	54	89.1	-	3.5	86.2	0.8
	105, typ [7]	46.1	-	2.9	43.1	31.7	-	2.9	29.3	62.2	-	2.9	59.2	0.6
	105, max [8]	114	-	3.7	111	99.1	-	3.6	96.1	131	-	3.9	128	0.8
	125, typ [7]	69.9	-	3.0	66.8	55.8	-	3.0	53.1	86	-	3.1	83	0.6
	125, max [8], [9]	161	-	4.2	159	148	-	4.1	145	178	-	4.3	176	0.8
S32K342, S32K322, S32K341	25, typ [7]	19.6	-	2.8	17.6	6.0	-	2.8	4.0	36.2	-	2.9	33	0.5
	25, max [8]	25	-	3.3	24.9	8.8	-	3.3	8.2	41.4	-	3.4	40.8	0.8
	85, typ [7]	28.8	-	2.9	26.8	15.2	-	2.9	13.4	45.7	-	2.9	42.4	0.5
	85, max [8]	41.8	-	3.5	39.6	27.7	-	3.4	25.9	58.7	-	3.5	55.3	0.8
	105, typ [7]	38.6	-	2.9	36.9	25	-	2.9	23.3	55.6	-	2.9	52.4	0.5
	105, max [8]	63.1	-	3.7	61.5	49	-	3.7	46.5	80.1	-	3.9	77.2	0.8
	125, typ [7]	50.7	-	2.9	49.6	37.2	-	2.9	35.5	67.9	-	3.0	64.7	0.5
	125, max [8], [9]	88.2	-	4.1	88.5	75.3	-	4.0	73.3	105.2	-	4.2	103.1	0.8
S32K312	25, typ [7]	15	NA	NA		5	NA	NA		26	NA	NA		NA
	25, max [8]	20				10				32				
	85, typ [7]	20				10				31				
	85, max [8]	35.2				24.6				46.4				
	105, typ [7]	26.1				16.2				37				
	105, max [8]	52.9				42.6				64.2				

Table continues on the next page...

Table 16. Low speed RUN mode supply currents...*continued*

	125, typ [7]	35.3			25.3			46.4			
	125, max [8], [9], [10]	79.8			66.9			90.1			
S32K311, S32K310	25, typ [7]	12.9	NA	NA	4.4	NA	NA	22.4	NA	NA	NA
	25, max [8]	14.9			6.0			24.8			
	85, typ [7]	16.0			7.5			25.6			
	85, max [8]	31.0			22.2			41.1			
	105, typ [7]	19.1			10.5			28.7			
	105, max [8]	45.8			36.8			55.6			
	125, typ [7]	25.2			16.5			34.7			
	125, max [8], [9], [10]	73.2			64.3			82.4			

[1] Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
[2] See the example configurations in Table 22
[3] IO load current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
[4] RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
[5] RUN IDD @ V15 includes Flash memory read current from the V11 voltage rail
[6] For S32K38x, the current from a V15 supply will flow through the external NMOS for the V11 regulation stage, and into the V11 pins of the device.
[7] "typ" is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
[8] "max" is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15 = 1.65V, for the fast silicon process.
[9] For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.
[10] If the total power dissipation would cause the junction temperature to be exceeded when VDD_HV_A is at 5V, then VDD_HV_A should be limited to operate at 3.3V.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, VDD_HV_B = 5V (if the VDD_HV_B domain present in the device), temperature = 25 °C and typical silicon process unless otherwise stated.

Table 17. RUN mode supply currents (peripherals disabled) for S32K389, S32K3x8, S32K34x, S32K32x and S32K314

Chip	Ambient Temperature (°C)	RUN Mode (mA) [1]

Table continues on the next page...

Table 17. RUN mode supply currents (peripherals disabled) for S32K389, S32K3x8, S32K34x, S32K32x and S32K314*...continued*

		Min. Config. [2] [Clock Option F] Single Core @80 MHz	Min. Config. [2] [Clock Option B] Single Core @120 MHz	Min. Config. [2] [Clock Option A] Single Core @160 MHz	Min. Config. [2] [Clock Option F] Dual Core @80 MHz	Min. Config. [2] [Clock Option B] Dual Core @120 MHz	Min. Config. [2] [Clock Option A] Dual Core @160 MHz	Min. Config. [2] [Clock Option A+] Triple Core @240 MHz	Min. Config. [2] [Clock Option A++] 1xLS + 3xCores @320 MHz	All. Config. [2]	All. Config. [2]
		V15 [3]/ V11 [4]	V15 [3]/ V11 [4]	V15 [3]/ V11 [4]	V15 [3]/ V11 [4]	V15 [3]/ V11 [4]	V15 [3]/ V11 [4]	V15 [3]/ V11 [4]	V15 [3]/ V11 [4]	VDD_HV_B [5]	VDD_HV_A [5], [6]
S32K389	25, typ [7][10]	NA		213.6	NA		258.1	363.5	461.5	2.4	4.4
	25, max [8][11]			293.1			328.5	471.6	571.3	2.8	5.0
	85, typ [10]			302.8			347.7	454.3	551.7	2.4	4.5
	85, max [11]			515.8			557.1	677.4	760.9	2.8	5.3
	105, typ [10]			373.6			418.7	525.7	623.0	2.4	4.6
	105, max [11]			717.4			768.9	875.6	978.4	2.8	5.5
	125, typ [10]			475.9			521.5	629.4	726.4	2.4	4.8
	125, max[11], [9][12]			1065.2			1092.0	1185.3	1274.3	2.8	6.3
S32K388	25, typ [10]	NA		196.2	NA		231.4	339.4	440.3	2.4	3.6
	25, max [11]			291.4			318.4	456.6	565.3	2.8	4.3
	85, typ [10]			277.1			312.6	420.9	520.5	2.4	3.7
	85, max [11]			500.8			533.3	634.3	745.9	2.8	4.6
	105, typ [10]			351.8			387.2	495.3	593.8	2.4	3.8
	105, max [11]			703.3			737.6	837.6	951.5	2.8	5.1
	125, typ [10]			468.7			503.5	610.4	707.9	2.4	4.0

Table continues on the next page...

Table 17. RUN mode supply currents (peripherals disabled) for S32K389, S32K3x8, S32K34x, S32K32x and S32K314*...continued*

	125, max[11], [12]			993.5			1040.0	1147.0	1254.1	2.8	5.7
S32K358, S32K356, S32K348, S32K338, S32K328	25, typ[10]	100.6	118.9	144.8	103.3	124.1	166.6	NA	NA	1.8	4.8
	25, max[11]	119.8	138.9	165.6	122.8	144.4	186.3			3.0	5.4
	85, typ [10]	126.9	145.3	171.6	129.8	150.9	193.8			1.8	6.1
	85, max [11]	248.1	267.7	294.4	250.8	274.3	317.6			3.0	6.7
	105, typ [10]	153.4	172.0	198.4	156.6	178.0	221.2			1.8	6.1
	105, max [11]	349.5	371.6	398.2	358.3	381.4	423.7			3.0	6.9
	125, typ [10]	199.3	218.2	245.0	203.3	225.0	268.3			1.8	6.4
	125, max[11], [12]	529.7	551.2	580.9	538.0	563.3	603.0			3.0	7.4
S32K344, S32K324, S32K314	25, typ [10]	51.3	54.8	69.6	62.7	75.1	97.5	NA	NA	0.6	3.1
	25, max [11]	60.2	64.5	80.4	73.3	86.8	110			0.8	3.6
	85, typ [10]	64.5	68.1	83.1	76.2	89	111			0.6	3.2
	85, max [11]	104	108	124	117	131	155			0.8	3.9
	105, typ [10]	75.4	79	93.9	87.3	100	122.6			0.6	3.2
	105, max [11]	145	149	166	159	173	197			0.8	4.0
	125, typ [10]	97.4	101.2	116.4	110	122.9	145.7			0.6	3.3
	125, max [11], [12]	191	196	212	206	220	245			0.8	4.3
S32K342, S32K322, S32K341	25, typ [10]	49.5	52.2	66.3	58.9	72.7	93.7			0.5	3.0
	25, max [11]	58.5	62.4	75.9	68.1	82.9	104.6	NA	NA	0.8	3.6
	85, typ [10]	58.6	63.6	75.7	67.9	82.3	106.1			0.5	3.0
	85, max [11]	89.6	102.3	110.8	105.4	124.1	155			0.8	3.8
	105, typ [10]	68.3	76	85.6	80	92.3	119.3			0.5	3.1
	105, max [11]	124	143.4	157.5	150.5	164.5	191.6			0.8	4.0
	125, typ [10]	79.8	85.1	97.1	89.1	103.8	140.1			0.5	3.2

Table continues on the next page...

Table 17. RUN mode supply currents (peripherals disabled) for S32K389, S32K3x8, S32K34x, S32K32x and S32K314*...continued*

	125, max [11], [12]	146.7	164.7	178	171.3	188.7	235.6			0.8	4.2

[1] Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
[2] See the configurations in Table 23.
[3] RUN IDD @ V15 includes Flash memory read current from the V11 voltage rail.
[4] For S32K38x, the current from a V15 supply will flow through the external NMOS for the V11 regulation stage, and into the V11 pins of the device.
[5] IO load current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
[6] RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
[7] “typ” is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
[8] "max" is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15= 1.65V, for the fast silicon process.
[9] For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.
[10] “typ” is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
[11] "max" is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15= 1.65V, for the fast silicon process.
[12] For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, VDD_HV_B = 5V (if the VDD_HV_B domain present in the device), temperature = 25 °C and typical silicon process unless otherwise stated.

Table 18. RUN mode supply currents (peripherals disabled) for S32K312, S32K311 and S32K310

Chip	Ambient Temperature (°C)	RUN Mode (mA) [1]			
		Min. Config. [2] Single Core @80 MHz [Clock Option F]		Min. Config. [2] Single Core @120 MHz [Clock Option B]	
		VDD_HV_A [3], [4]	V15 [5]/ V11	VDD_HV_A [3], [4]	V15 [5]/ V11
S32K312	25, typ [6]	37	NA	37	NA
	25, max [7]	44		47	
	85, typ [6]	42		43	
	85, max [7]	58.5		59.7	
	105, typ [6]	48.1		48.7	
	105, max [7]	76.4		77.8	
	125, typ [6]	56.5		57	

Table continues on the next page...

Table 18. RUN mode supply currents (peripherals disabled) for S32K312, S32K311 and S32K310*...continued*

	125, max [7], [8], [9]	98.7		99.9	
S32K311 , S32K310	25, typ [6]	34.9	NA	36.5	NA
	25, max [7]	39.1		41.1	
	85, typ [6]	38.1		39.8	
	85, max [7]	54.2		55.9	
	105, typ [6]	41.5		43.2	
	105, max [7]	69.1		71.1	
	125, typ [6]	47.7		49.4	
	125, max [7], [8], [9]	97		99.1	

[1] Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
[2] See the configurations in Table 23.
[3] IO load current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
[4] RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
[5] RUN IDD @ V15 includes Flash memory read current from the V11 voltage rail.
[6] "typ" is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
[7] "max" is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15 = 1.65V, for the fast silicon process.
[8] For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.
[9] If the total power dissipation would cause the junction temperature to be exceeded when VDD_HV_A is at 5V, then VDD_HV_A should be limited to operate at 3.3V.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, VDD_HV_B = 5V (if the VDD_HV_B domain present in the device), temperature = 25 °C and typical silicon process unless otherwise stated.

Table 19. Example RUN mode configuration supply currents for S32K3x8, S32K34x, S32K32x and S32K314

Chip	Ambient Temperature (°C)	RUN Mode (mA) [1]									
		Config. 1 [2] Dual Core @160 MHz	Config. 2 [2] Single Core @160 MHz	Config. 3 [2] Dual Core @120 MHz	Config. 4 [2] Single Core @120 MHz	Config. 5 [2] Single Core @80 MHz	Config. 6-1 [2] Dual Core @240 MHz	Config. 6-2 [2] Triple Core @240 MHz	Config. 7 [2]1xLS + 3x Core (with AES and ENET2 enabled)@320 MHz	All Config. [2]	All Config. [2]

Table continues on the next page...

Table 19. Example RUN mode configuration supply currents for S32K3x8, S32K34x, S32K32x and S32K314...*continued*

		V15 [3]/V11[4]	V15 [3]/ V11[4]	V15 [3]/ V11[4]	V15 [3]/ V11[4]	V15 [3]/ V11[4]	V15 [3]/ V11[4]	V15 [3]/ V11[4]	V15 [3]/ V11[4]	VDD_HV_B [5]	VDD_HV_A [5], [6]
S32K388	25, typ [7]	255.4	241.3	NA			310.8	393.1	620.1	3.0	3.8
	25, max [8]	382.6	378.0				424.4	525.5	774.2	3.3	4.5
	85, typ [7]	324.3	309.5				392.6	474.5	701.5	3.0	3.8
	85, max [8]	499.7	501.2				610.4	712.3	952.4	3.3	4.7
	105, typ [7]	426.8	425.1				466.9	548.5	774.5	3.0	3.9
	105, max [8]	731.2	738.1				823.2	918.7	1160.6	3.3	5.2
	125, typ [7]	554.5	538.7				582.4	663.4	887.5	3.0	4.1
	125, max [8], [9]	1128.4	1121.0				1169.6	1227.0	1467.4	3.3	5.9
S32K358, S32K356, S32K348, S32K338, S32K328	25, typ [7]	207.6	168.6	177.5	146.8	114.9	313	380.2	NA	2.1	5.3
	25, max [8]	229.4	188.3	197.4	167.9	135.3	340	395.9		3.2	6.0
	85, typ [7]	235.5	195.9	205.1	174.0	141.6	333.4	413.6		2.1	6.3
	85, max [8]	363.7	322.1	331.3	299.2	263.2	418.5	552.8		3.2	7.1
	105, typ [7]	263.5	223.5	233.0	201.5	168.9	360.4	446.1		2.1	6.4
	105, max [8]	472.4	429.8	438.8	407.1	369.8	516.5	682.8		3.2	7.1
	125, typ [7]	311.9	271.3	281.0	249.0	216.2	413.8	501.0		2.1	6.7
	125, max [8], [9]	661.0	618.2	624.6	588.8	554.2	707	844.0		3.2	7.9
S32K344, S32K324, S32K314	25, typ [7]	119	102	106	80	68	NA	NA	NA	0.6	3.1
	25, max [8]	133	115	119	92	79				0.8	3.6
	85, typ [7]	134	116	120	94	81.8				0.6	3.2
	85, max [8]	180	160	165	137	123				0.8	3.9
	105, typ [7]	145	128	132	105	93				0.6	3.2
	105, max [8]	222	203	208	179	165				0.8	4.0

Table continues on the next page...

Table 19. Example RUN mode configuration supply currents for S32K3x8, S32K34x, S32K32x and S32K314...*continued*

	125, typ [7]	169	151	155	128	116				0.6	3.3
	125, max [8], [9]	271	250	256	226	213				0.8	4.5
S32K342, S32K322, S32K341	25, typ [7]	115.3	93.2	96.1	79.6	64.1	NA	NA	NA	0.5	3.0
	25, max [8]	128.9	109.3	109.8	90.9	74.5				0.8	3.6
	85, typ [7]	125.0	102.7	105.8	89.2	73.6				0.5	3.0
	85, max [8]	178.8	126.5	132.0	105.0	92.5				0.8	3.6
	105, typ [7]	135.2	111.9	115.5	98.6	83.4				0.5	3.1
	105, max [8]	219.6	184.6	188.5	168.5	152.5				0.8	3.8
	125, typ [7]	145.8	123.8	127.3	110.2	94.7				0.5	3.1
	125, max [8], [9]	258.1	235.2	243.9	206.9	183.7				0.8	4.3

[1] Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
[2] See the configurations in Table 23.
[3] RUN IDD @ V15 includes Flash memory read current from the V11 voltage rail.
[4] For S32K388, the current from a V15 supply will flow through the external NMOS for the V11 regulation stage, and into the V11 pins of the device.
[5] IO current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
[6] RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
[7] "typ" is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
[8] "max" is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15 = 1.65V, for the fast silicon process.
[9] For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.

Table 20. Example RUN mode configuration supply currents for S32K312, S32K311, S32K311

Chip	Ambient Temperature (°C)	RUN Mode (mA) [1]			
		Config. 4 [2] Single Core @120 MHz		Config. 5 [2] Single Core @80 MHz	
		VDD_HV_A [3], [4]	V15 [5]/V11	VDD_HV_A [3], [4]	V15 [5]/ V11
S32K312	25, typ [6]	54	NA	44	NA
	25, max [7]	62		54	
	85, typ [6]	60		49	

Table continues on the next page...

Table 20. Example RUN mode configuration supply currents for S32K312, S32K311, S32K311 *...continued*

	85, max [7]	76.4		66.3	
	105, typ [6]	65.8		55	
	105, max [7]	94.4		84.4	
	125, typ [6]	78.6		64.7	
	125, max [7], [8], [9]	120.7		110.5	
S32K311, S32K310	25, typ [6]	53.4	NA	43	NA
	25, max [7]	57.7		51.2	
	85, typ [6]	56.8		50.8	
	85, max [7]	73.2		66	
	105, typ [6]	60.1		54	
	105, max [7]	88.5		81.9	
	125, typ [6]	66.3		60.2	
	125, max [7], [8],[9]	115.3		109.3	

[1] Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
[2] See the configurations in Table 23.
[3] IO current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
[4] RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
[5] RUN IDD @ V15 includes Flash memory read current from the V11 voltage rail.
[6] “typ” is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process
[7] "max” is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15 = 1.65V, for the fast silicon proce
[8] For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.
[9] If the total power dissipation would cause the junction temperature to be exceeded when VDD_HV_A is at 5V, then VDD_HV_A should be limited to operate at 3.3V.

Table 21. Example RUN mode configuration supply currents for S32K389

Chip	Ambient Temperature (°C)	RUN Mode (mA) [1]							
		Config. 8 [2]1xLS + 3x cores @320 MHz	Config. 9 [2]1xLS + 3x cores @320 MHz	Config. 10 [2]1xLS + 3x cores @240 MHz	Config. 11 [2]1xLS core @240 MHz	Config. 12 [2]1xLS + 1x core @240 MHz	Config. 13 [2]1xLS core @240 MHz	All config	All config
		V15 /V115	V15/V11 [3]	V15/V11 [3]	V15/V11 [3]	V15 /V11[3]	V15 /V11[3]	VDD_HV_B [4], [5]	VDD_HV_A [4]
S32K389	25, typ [6]	641.6	589.2	464.7	311.1	405.9	305.1	1.8	4.5
	25, max [7]	776.1	600.3	514.2	351.0	453.8	350.0	2.7	5.1
	85, typ[6]	741.2	643.3	556.1	402.1	497.0	396.0	1.8	4.6

Table continues on the next page...

Table 21. Example RUN mode configuration supply currents for S32K389...*continued*

	85, max[6]	997.7	860.6	778.9	619.6	717.8	613.9	2.7	5.1
	105, typ [6]	819.9	714.8	628.3	474.7	569.4	468.6	1.8	4.7
	105, max [7]	1192.0	1049.1	972.7	814.8	908.6	808.0	2.7	5.4
	125, typ [6]	931.6	818.5	733.3	579.9	674.3	573.9	1.8	4.9
	125, max [7], [8]	1617.7	1434.3	1348.5	1195.7	1281.6	1184.4	2.7	6.3

[1] Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
[2] See the configurations in Table 23.
[3] RUN IDD @ V15 includes Flash memory read current from the V11 voltage rail.
[4] IO current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
[5] RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
[6] For S32K389, the current from a V15 supply will flow through the external NMOS for the V11 regulation stage, and into the V11 pins of the device.
[7] "typ" is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
[8] "max" is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15 = 1.65V, for the fast silicon process.

6.8 Operating mode

Table 22. STANDBY and low speed RUN configuration options

MODULE	STANDBY All OFF	STANDBY SIRC ON	STANDBY FIRC ON	BOOT Mode (OptionC[1], FIRC @24 MHz)	Low Speed RUN (OptionE [1], FIRC @ 3MHz)	FIRC Mode (OptionD [1], FIRC @48 MHz)
Core M7_0/1	OFF	OFF	OFF	24 MHz	3 MHz	48 MHz
HSE_B	OFF	OFF	OFF	24 MHz	3 MHz	48 MHz
FIRC	OFF	OFF	24 MHz	24 MHz	3 MHz	48 MHz
FXOSC	OFF	OFF	OFF	OFF	OFF	OFF
SIRC	OFF	ON	OFF	ON	ON	ON
PLL	OFF	OFF	OFF	OFF	OFF	OFF
Flash	OFF	OFF	OFF	ON	ON	ON
eDMA	OFF	OFF	OFF	ON	ON	ON
FlexCAN	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
LPUART	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
LPSPI	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
LPI2C	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF

Table continues on the next page...

Table 22. STANDBY and low speed RUN configuration options...*continued*

EMAC/GMAC	OFF	OFF	OFF	OFF	OFF	OFF
eMIOS	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
SAR_ADC	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
LPCMP	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF

[1] See clocking use case examples in the Clocking chapter of the S32K3xx Reference Manual.

Table 23. RUN mode configuration options

MODULE	Min. Config. (OptionF[1]), PLL@ 80 MHz	Min. Config. (OptionB[1]), PLL@ 120 MHz	Min. Config. (OptionA[1]), PLL@ 160 MHz	Min. Config. (OptionA+[1]), PLL@ 240 MHz	Min. Config. (OptionA++[1]), PLL@ 320 MHz	Config. 1 Dual Core @160 MHz	Config. 2 Single Core @160 MHz	Config. 3 Dual Core @120 MHz	Config. 4 Single Core @120 MHz	Config. 5 Single Core @80MHz	Config. 6-1 Dual Core @240 MHz	Config. 6-2 Triple Core @240 MHz	Config. 7 1xLS + 3x cores @320 MHz
Core M7_0	80 MHz	120 MHz	160 MHz	240 MHz	320 MHz	160 MHz	160 MHz	120 MHz	120 MHz	80 MHz	240 MHz	240 MHz	320 MHz
Core M7_1	80 MHz	120 MHz	160 MHz	240 MHz	320 MHz	160 MHz	-	120 MHz	-	-	240 MHz	240 MHz	320 MHz
Core M7_2	-	-	-	240 MHz	320 MHz	-	-	-	-	-	-	240 MHz	320 MHz
Core M7_3	-	-	-	-	320 MHz	-	-	-	-	-	-	-	320 MHz
HSE_B[2]	80 MHz	120 MHz	80 MHz	120 MHz	160 MHz	80 MHz	80 MHz	120 MHz	120 MHz	80 MHz	120 MHz	120 MHz	160 MHz
FIRC	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
FXOSC	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
SIRC	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
PLL	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
Flash	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
eDMA	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
FlexCAN[3]	All OFF	All OFF	All OFF	All OFF	All OFF	6x	2x	4x	6x	1x	8x	8x	8x

Table continues on the next page...

Table 23. RUN mode configuration options...*continued*

MODULE	Min. Config. (OptionF[1]), PLL@ 80 MHz	Min. Config. (OptionB[1]), PLL@ 120 MHz	Min. Config. (OptionA[1]), PLL@ 160 MHz	Min. Config. (OptionA+[1]), PLL@ 240 MHz	Min. Config. (OptionA++[1]), PLL@ 320 MHz	Config. 1 Dual Core @160 MHz	Config. 2 Single Core @160 MHz	Config. 3 Dual Core @120 MHz	Config. 4 Single Core @120 MHz	Config. 5 Single Core @80MHz	Config. 6-1 Dual Core @240 MHz	Config. 6-2 Triple Core @240 MHz	Config. 7 1xLS + 3x cores @320 MHz
LPUART[4]	All OFF	All OFF	All OFF	All OFF	All OFF	16x	4x	10x	8x	7x	16x	16x	16x
LPSPI[5]	All OFF	All OFF	All OFF	All OFF	All OFF	6x	4x	4x	4x	3x	5x	5x	5x
LPI2C[6]	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF	2x	2x	2x	All OFF	1x	1x	1x
EMAC/GMAC[7]	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	ON
SAI	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
QSPI	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
eMIOS[8]	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF	3x	3x	2x	2x	2x	2x	2x
SAR_ADC[9]	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF	3x	3x	2x	2x	3x	3x	3x
LPCMP[10]	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF	2x	3x	All OFF	All OFF	OFF	OFF	OFF

[1] See clocking use case examples in the Clocking chapter of the S32K3xx Reference Manual.
[2] HSE_B: After start-up, the HSE core is in WFI.
[3]
- FlexCAN0: Transmitting an 8-byte CAN-FD data frame at 5 Mbps, every 10 ms.
- FlexCAN1: Transmitting a 64-byte CAN-FD data frame at 2 Mbps, every 20 ms.
- FlexCAN2-5: Transmitting an 8-byte CAN data frame at 500 Kbps, every 20 ms.

[4] LPUART0-15: Transmitting at 19200 bps, every 100ms.
[5]
- LPSPI0: Transmitting 32 bits at 20 Mbps (GPIO Fast pads), every 5 ms.
- LPSPI1-5: Transmitting 32 bits at 1 Mbps, every 5 ms.

[6] LPI2C0-1: Transmitting 3 bytes at 400 Kbps, every 100ms.
[7] EMAC/GMAC: ON for MII interface.
[8]
- eMIOS0: 6 channels in PWM mode @ 20 KHz.
- eMIOS1-2: 8 channels in PWM mode @ 400 Hz.

[9]
- SAR_ADC0: 16 channels at 400 Hz rate, BCTU triggered.
- SAR_ADC1-2: 4 channels at 20 KHz rate, BCTU triggered.

[10] LPCMP0: 8 channels enabled; LPCMP1-2: 4 channels enabled.

Table 24. RUN mode configuration options for S32K389

MODULE	Min. Config.[1] 1xLS +3x Cores @320 MHz [Clock Option A++]	Config. 8[1] 1xLS + 3x cores @320 MHz	Config. 9[1] 1xLS + 3x cores @320 MHz	Config. 10[1] 1xLS + 3x cores @240 MHz	Config. 11[1] 1xLS core @240 MHz	Config. 12[1] 1xLS + 1x core @240 MHz	Config. 13[1] 1xLS core @240 MHz
Core M7_0	ON	ON	ON	ON	OFF	ON	OFF
Core M7_1	ON	ON	ON	ON	OFF	OFF	OFF
Core M7_2	ON	ON	ON	ON	ON	ON	ON
Core M7_3	ON	ON	ON	ON	OFF	OFF	OFF
CM7_CORE_CLK [MHz]	320 MHz	320 MHz	320 MHz	240 MHz	240 MHz	240 MHz	240 MHz
HSE_B [MHz][1]	160 MHz	160 MHz	160 MHz	120 MHz	120 MHz	120 MHz	120 MHz
AES Accel [MHz]	160 MHz	160 MHz	160 MHz	120 MHz	120 MHz	120 MHz	OFF
FIRC	ON	ON	ON	ON	ON	ON	ON
FXOSC	ON	ON	ON	ON	ON	ON	ON
SIRC	ON	ON	ON	ON	ON	ON	ON
PLL	ON	ON	ON	ON	ON	ON	ON
Flash	ON	ON	ON	ON	ON	ON	ON
Memories[2]	OFF	ON	ON	ON	ON	ON	ON
eDMA	ON	ON	ON	ON	ON	ON	ON
FlexCAN [3]	All OFF	12x	4x	4x	2x	2x	2x
LPUART [4]	All OFF	All OFF	16x	16x	8x	8x	8x
LPSPI[5]	All OFF	6x	6x	6x	4x	4x	4x

Table continues on the next page...

Table 24. RUN mode configuration options for S32K389...*continued*

MODULE	Min. Config.[1] 1xLS +3x Cores @320 MHz [Clock Option A++]	Config. 8[1] 1xLS + 3x cores @320 MHz	Config. 9[1] 1xLS + 3x cores @320 MHz	Config. 10[1] 1xLS + 3x cores @240 MHz	Config. 11[1] 1xLS core @240 MHz	Config. 12[1] 1xLS + 1x core @240 MHz	Config. 13[1] 1xLS core @240 MHz
LPI2C[6]	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
EMAC/ GMAC[7]	OFF	2x	1x	1x	1x	1x	1x
SAI	OFF	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
QSPI	OFF	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
eMIOS[8]	All OFF	All OFF	3x	3x	2x	2x	2x
SAR_ADC[9]	All OFF	1x	3x	3x	2x	2x	2x
LPCMP[10]	All OFF	1x	1x	1x	1x	1x	1x

[1] HSE_B: After start-up, the HSE core is in WFI.
[2] Core memories enabled in core CM7_n: D-Cache, I-Cache, D-TCM, I-TCM.
[3]
- FlexCAN0: Transmitting an 8-byte CAN-FD data frame at 5 Mbps, every 10 ms.
- FlexCAN1: Transmitting a 64-byte CAN-FD data frame at 2 Mbps, every 20 ms.
- FlexCAN2-11: Transmitting an 8-byte CAN data frame at 500 Kbps, every 20 ms.

[4] LPUART0-15: Transmitting at 19200 bps, every 100ms.
[5]
- LPSPI0: Transmitting 32 bits at 20 Mbps (GPIO Fast pads), every 5 ms.
- LPSPI1-5: Transmitting 32 bits at 1 Mbps, every 5 ms.

[6] LPI2C0-1: Transmitting 3 bytes at 400 Kbps, every 100ms.
[7] EMAC/GMAC: ON for MII interface.
[8]
- eMIOS0: 6 channels in PWM mode @ 20 KHz.
- eMIOS1-2: 8 channels in PWM mode @ 400 Hz.

[9]
- SAR_ADC0: 16 channels at 400 Hz rate, BCTU triggered.
- SAR_ADC1-2: 4 channels at 20 KHz rate, BCTU triggered.

[10] LPCMP0: 8 channels enabled; LPCMP1-2: 4 channels enabled.

6.9 Cyclic wake-up current

The cyclic wake-up current is the calculated average current consumption during the periodic switching between RUN mode and STANDBY mode. This average current can be calculated with the following formula:

ICYCL = RUN Current According to Ratio + STANDBY Current According to Ratio

Where the Current According to Ratio value is calculated as follows:

Current According to Ratio = Supply Current × Ratio of Duration

As an example, the following data was obtained with an application that periodically (every 40ms) alternates between RUN mode, for approximately 200µs to scan several GPIO inputs (51 GPIOS), and spends the rest of the time in STANDBY mode.

Table 25. Cyclic wake-up current example

Chip	Device Operating Mode	Supply Current[1] [µA]	Duration [2] [ms]	Ratio of Duration [3]	Current According to Ratio [4] [µA]	ICYCL - Average current [5] [µA]
S32K314	RUN	20000	0.2	0.005	100	159.7
	STANDBY	60	39.8	0.995	59.7	

[1] The supply current is obtained through the measurements of the current during the corresponding operating mode.
[2] The duration is defined by the application (how much time will the device spend in the according operating mode).
[3] The ratio of duration is obtained by dividing the duration of the corresponding operating mode by the total duration of the application.
[4] The current according to ratio is obtained by multiplying the supply current and the ratio of duration related to the proper operating mode.
[5] The average current is calculated by the addition of each device operating mode's current according to ratio.

6.10 NXP recomended PMIC

NXP recomended PMIC for the mentioned devices are as follows. Contact NXP sales representative for more information.

Table 26. NXP Recomemded PMIC

MCU	PMIC
S32K312, S32K311, S32K310	FS23, FS26
S32K344, S32K324, S32K314, S32K341, S32K342, S32K322, S32K328, S32K338, S32K348, S32K356, S32K358	FS26
S32K388	FS26
S32K389	FS26, FS27

7 I/O parameters

7.1 GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)

The leakage current on the GPIO pins is specified as a function of the pad type (Standard, Standard Plus, Medium, Fast, or GPI) and the number of Analog functions (CMP and ADC channels) multiplexed per pin.

For S32K388, see the ILKG column in the Pinout section of the IOMUX file attached to the Reference Manual.

For other devices, the "Analog Function Count" is defined from the number of CMP and ADC channels multiplexed to a given pin. This information can be obtained from the "Direct Signals" column in the IOMUX files attached to the Reference Manual. The "Analog Function Count" is shown in the Condition column of the following table.

Table 27. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high level DC voltage threshold	0.70 x VDD_HV_A/B	—	VDD_HV_A/B + 0.3	V	VDD_HV_A/B = 3.3V	—
VIL	Input low level DC voltage threshold	VSS - 0.3	—	0.30 x VDD_HV_A/B	V	VDD_HV_A/B = 3.3V	—

Table continues on the next page...

Table 27. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
WFRST	RESET Input Filtered pulse width [1]	—	—	33	ns	—	—
WNFRST	RESET Input not filtered pulse width [2]	100	—	—	ns	—	—
ILKG_33_S0	3.3V input leakage current for Standard GPIO [3]	-133	—	300	nA	Pins with Analog Function Count = 0	—
ILKG_33_S1	3.3V input leakage current for Standard GPIO [3]	-545	—	445	nA	Pins with Analog Function Count = 1	—
ILKG_33_S2	3.3V input leakage current for Standard GPIO [3]	-749	—	517	nA	Pins with Analog Function Count = 2, plus PTA12, PTD1	—
ILKG_33_S3	3.3V input leakage current for Standard GPIO [3]	-1288	—	679	nA	Pins with Analog Function Count = 3, plus PTD0	—
ILKG_33_S_PTE13	3.3V input leakage current for Standard GPIO [3]	-1935	—	483	nA	PMC VRC_CTRL pin	—
ILKG_33_SP0	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-370	—	575	nA	Pins with Analog Function Count = 0	—
ILKG_33_SP1	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-660	—	659	nA	Pins with Analog Function Count = 1	—
ILKG_33_SP2	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-1094	—	794	nA	Pins with Analog Function Count = 2	—
ILKG_33_M0	3.3V GPIO input leakage current for Medium GPIO [3]	-792	—	750	nA	Pins with Analog Function Count = 0	—
ILKG_33_M1	3.3V GPIO input leakage current for Medium GPIO [3]	-989	—	824	nA	Pins with Analog Function Count = 1, plus PTC16, PTD5	—
ILKG_33_M2	3.3V GPIO input leakage current for Medium GPIO [3]	-1233	—	1248	nA	Pins PTD6 and PTE8	—

Table continues on the next page...

Table 27. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ILKG_33_F0	3.3V GPIO input leakage current for Fast GPIO [3]	-1139	—	1178	nA	Pins with Analog Function Count = 0	—
ILKG_33_F1	3.3V GPIO input leakage current for Fast GPIO [3]	-1464	—	1239	nA	Pins with Analog Function Count = 1	—
ILKG_33_I	3.3V input leakage current for GPI [3]	-120	—	120	nA	—	—
VHYS_33	Input hysteresis voltage [4]	0.06 x VDD_HV_A/B	—	—	mV	Always Enabled, Applies to S32K34x, S32K3x8, S32K32x, S32K314 and S32K389 devices.	—
VHYS_33	Input hysteresis voltage	0.06 x VDD_HV_A/B	—	—	mV	Always Enabled, Applies to S32K311, S32K312, and S32K310 devices.	—
CIN	GPIO Input capacitance	2	4	6	pF	add 2pF for package/ parasitic	—
IPU_33	3.3V GPIO pull up/ down resistance	20	—	60	kΩ	pull up @ 0.3 x VDD_HV_A/B, pull down @ 0.7 x VDD_HV_A/B	—
IOH_33_S	3.3V output high current for Standard GPIO [5][6]	1.0	—	—	mA	VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_SP	3.3V output high current for Standard Plus GPIO and RESET IO [5][6]	1.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_M	3.3V output high current for Medium GPIO [5][6]	3	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_F	3.3V output high current for Fast GPIO [5][6]	4.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_SP	3.3V output high current for Standard Plus GPIO and RESET IO [5][6]	3	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_M	3.3V output high current for Medium GPIO [5][6]	6	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—

Table continues on the next page...

Table 27. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOH_33_F	3.3V output high current for Fast GPIO [5][6]	9	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOL_33_S	3.3V output low current for Standard GPIO [5][6]	1.0	—	—	mA	VOL <= 0.7V	—
IOL_33_SP	3.3V output low current for Standard Plus GPIO and RESET IO [5][6]	1.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_M	3.3V output low current for Medium GPIO [5][6]	3.0	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_F	3.3V output low current for Fast GPIO [5][6]	4.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_SP	3.3V output low current for Standard Plus GPIO and RESET IO [5][6]	3	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_33_M	3.3V output low current for Medium GPIO [5][6]	6	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_33_F	3.3V output low current for Fast GPIO [5][6]	9	—	—	mA	DSE =1, VOL <= 0.7V	—
FMAX_33_S	3.3V maximum frequency for Standard GPIO [5][7]	—	—	10	MHz	2.9V - 3.6V CL(max) = 25pF	—
FMAX_33_SP	3.3V maximum frequency for Standard Plus GPIO [5][7]	—	—	25	MHz	2.9V - 3.6V CL (max) = 25pF	—
FMAX_33_M	3.3V maximum frequency for Medium GPIO [5][7]	—	—	50	MHz	2.9V - 3.6V CL (max) = 25pF	—
FMAX_33_F	3.3V maximum frequency for Fast GPIO [5][7]	—	—	120	MHz	2.9V - 3.6V CL(max) = 25pF, for all S32K3xx except S32K3x8 and S32K389 devices	—

Table continues on the next page...

Table 27. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FMAX_33_F	3.3V maximum frequency for Fast GPIO [5][7]	—	—	125	MHz	2.9V - 3.6V, CL (max) = 25pF, for S32K3x8 and S32K389 devices	—
IOHT	Output high current total for all ports [8]	—	—	100	mA	—	—

[1] Maximum length of RESET pulse will be filtered by an internal filter on this pin.
[2] Minimum length of RESET pulse, guaranteed not to be filtered by the internal filter.
[3] A positive value is leakage flowing into pin with pin at VDD_HV_A/B (the GPIO supply level); a negative value is leakage flowing out the pin with the pin at ground.
[4] Hysteresis spec does not apply to fast pad
[5] GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
[6] I/O output current specifications are valid for the given reference load figure, and the constraints given in the Operating Conditions of this document.
[7] I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load is assumed in addition to a 5 inch microstrip trace on standard FR4 with approximately 3.3pF/inch. For signals with frequency greater than 63MHz, a maximum 2 inch PCB trace is assumed. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected output resistance (ROUT_*) of the I/O pad.
[8] To determine total switching current on any I/O supply, current values per output pin should not be incrementally summed. I/O interfaces on the device are asynchronous to each other, so not all switching occurs at the same instant. Actual use case must be considered.

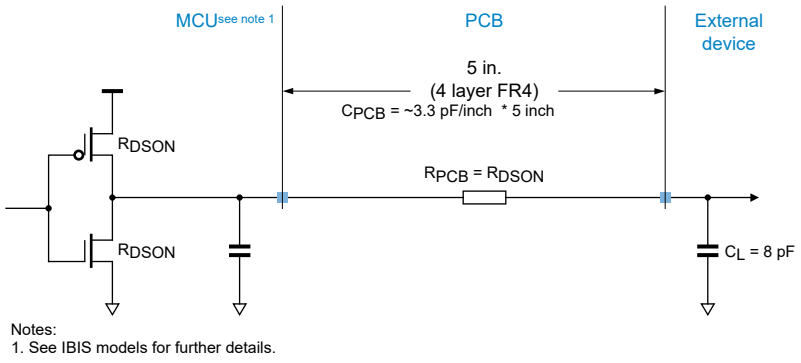


Figure 34. Reference Load Diagram

7.2 GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)

The leakage current on the GPIO pins is specified as a function of the pad type (Standard, Standard Plus, Medium, Fast, or GPI) and the number of Analog functions (CMP and ADC channels) multiplexed per pin.

For S32K388, see the ILKG column in the Pinout section of the IOMUX file attached to the Reference Manual.

For other devices, the "Analog Function Count" is defined from the number of CMP and ADC channels multiplexed to a given pin. This information can be obtained from the "Direct Signals" column in the IOMUX files attached to the Reference Manual. The "Analog Function Count" is shown in the Condition column of the following table.

Table 28. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high level DC voltage threshold	0.65 x VDD_HV_A/B	—	VDD_HV_A/B + 0.3	V	VDD_HV_A/B = 5.0V	—

Table continues on the next page...

Table 28. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIL	Input low level DC voltage threshold	VSS - 0.3	—	0.35 x VDD_HV_A/B	V	VDD_HV_A/B = 5.0V	—
WFRST	RESET Input filtered pulse width [1]	—	—	33	ns	—	—
WNFRST	RESET Input not filtered pulse width [2]	100	—	—	ns	—	—
ILKG_50_S0	5.0V input leakage current for Standard GPIO [3]	-193	—	389	nA	Pins with Analog Function Count = 0	—
ILKG_50_S1	5.0V input leakage current for Standard GPIO [3]	-691	—	580	nA	Pins with Analog Function Count = 1	—
ILKG_50_S2	5.0V input leakage current for Standard GPIO [3]	-947	—	673	nA	Pins with Analog Function Count = 2, plus PTA12, PTD1	—
ILKG_50_S3	5.0V input leakage current for Standard GPIO [3]	-1614	—	879	nA	Pins with Analog Function Count = 3, plus PTD0	—
ILKG_50_S_PTE13	5.0V input leakage current for Standard GPIO [3]	-2335	—	619	nA	PMC VRC_CTRL pin	—
ILKG_50_SP0	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-553	—	736	nA	Pins with Analog Function Count = 0	—
ILKG_50_SP1	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-855	—	846	nA	Pins with Analog Function Count = 1	—
ILKG_50_SP2	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-1389	—	1017	nA	Pins with Analog Function Count = 2	—
ILKG_50_M0	5.0V input leakage current for Medium GPIO [3]	-1036	—	951	nA	Pins with Analog Function Count = 0	—
ILKG_50_M1	5.0V input leakage current for Medium GPIO [3]	-1284	—	1057	nA	Pins with Analog Function Count = 1, plus PTC16, PTD5	—

Table continues on the next page...

Table 28. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ILKG_50_M2	5.0V input leakage current for Medium GPIO [3]	-1518	—	1298	nA	Pins PTD6 and PTE8	—
ILKG_50_F0	5.0V input leakage current for Fast GPIO [3]	-1675	—	1497	nA	Pins with Analog Function Count = 0	—
ILKG_50_F1	5.0V input leakage current for Fast GPIO [3]	-1805	—	1573	nA	Pins with Analog Function Count = 1	—
ILKG_50_I	5.0V input leakage current for GPI [3]	-150	—	150	nA	—	—
VHYS_50	input hysteresis voltage [4]	0.06 x VDD_HV_A/B	—	—	mV	Always enabled, Applies to S32K34x, S32K3x8, S32K32x, S32K314 and S32K389	—
VHYS_50	input hysteresis voltage	0.06 x VDD_HV_A/B	—	—	mV	Always enabled, Applies to S32K311, S32K312 and S32K310 devices.	—
CIN	GPIO Input capacitance	2	4	6	pF	add 2pF for package/ parasitic	—
IPU_50	5.0V GPIO pull up/ down resistance	20	—	55	kΩ	pull up @ 0.3 * VDD_HV_*, pull down @ 0.7 * VDD_HV_*	—
IOH_50_S	5.0V output high current Standard GPIO [5][6]	1.6	—	—	mA	VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_SP	5.0V output high current Standard Plus GPIO and RESET IO [5][6]	2.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_M	5.0V output high current for Medium GPIO [5][6]	4.0	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_F	5.0V output high current for Fast GPIO [5][6]	6.0	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_SP	5.0V output high current for Standard Plus GPIO and RESET IO [5][6]	5.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—

Table continues on the next page...

Table 28. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOH_50_M	5.0V output high current for Medium GPIO [5][6]	8.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_F	5.0V GPIO output high current for Fast GPIO [5][6]	12.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOL_50_S	5.0V output low current for Standard GPIO [5][6]	1.6	—	—	mA	VOL <= 0.7V	—
IOL_50_SP	5.0V output low current for Standard Plus GPIO and RESET IO [5][6]	2.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_50_M	5.0V output low current for Medium GPIO [5][6]	4.0	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_50_F	5.0V output low current for Fast GPIO [5][6]	6.0	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_50_SP	5.0V output low current for Standard Plus GPIO and RESET IO [5][6]	5.0	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_50_M	5.0V output low current for medium GPIO [5][6]	8.0	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_50_F	5.0V output low current for Fast GPIO [5][6]	12.0	—	—	mA	DSE =1, VOL <= 0.7V	—
FMAX_50_S	5.0V maximum frequency for Standard GPIO [5][7]	—	—	10	MHz	3.6V - 5.5V CL (max) = 25pF	—
FMAX_50_SP	5.0V maximum frequency for Standard Plus GPIO [5][7]	—	—	25	MHz	3.6V - 5.5V CL (max) = 25pF	—
FMAX_50_M	5.0V maximum frequency for Medium GPIO [5][7]	—	—	25	MHz	3.6V - 5.5V CL (max) = 25pF	—
FMAX_50_F	5.0V maximum frequency for Fast GPIO [5][7]	—	—	25	MHz	3.6V - 5.5V CL (max) = 25pF	—

Table continues on the next page...

Table 28. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOHT	Output high current total for all ports [8]	—	—	100	mA	—	—

[1] Maximum length of RESET pulse will be filtered by an internal filter on this pin.
[2] Minimum length of RESET pulse, guaranteed not to be filtered by the internal filter.
[3] A positive value is leakage flowing into pin with pin at VDD_HV_A/B (the GPIO supply level); a negative value is leakage flowing out the pin with the pin at ground.
[4] Hysteresis spec does not apply to fast pad
[5] GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
[6] I/O output current specifications are valid for the given reference load figure, and the constraints given in the Operating Conditions of this document.
[7] I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load is assumed in addition to a 5 inch microstrip trace on standard FR4 with approximately 3.3pF/inch.. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected output resistance (ROUT_*) of the I/O pad.
[8] To determine total switching current on any I/O supply, current values per output pin should not be incrementally summed. I/O interfaces on the device are asynchronous to each other, so not all switching occurs at the same instant. Actual use case must be considered.

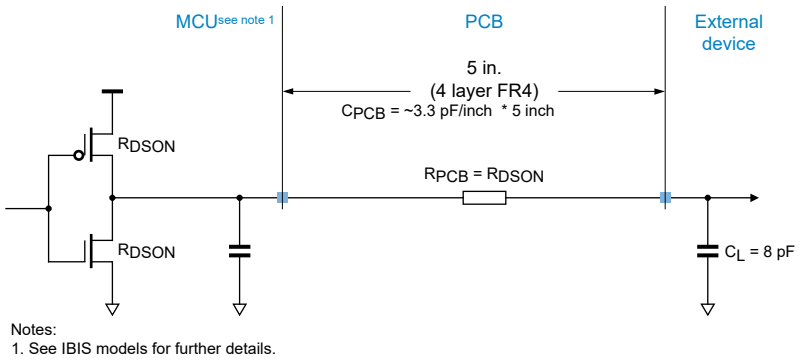


Figure 35. Reference Load Diagram

7.3 5.0V (4.5V - 5.5V) GPIO Output AC Specification

Table 29. 5.0V (4.5V - 5.5V) GPIO Output AC Specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_50_S	5.0V Standard GPIO rise/fall time [1][2][3]	5	—	21	ns	CL (max) = 25pF	—
TR_TF_50_S	5.0V Standard GPIO rise/fall time [1][2][3][4]	8.5	—	31	ns	CL (max) = 50pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time [1][2][3]	3	—	13.2	ns	DSE=0 CL (max) = 25pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time [1][2][3]	1	—	7.1	ns	DSE=1 CL (max) = 25pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time [1][2][3][4]	6.4	—	18.8	ns	DSE=0 CL (max) = 50pF	—

Table continues on the next page...

Table 29. 5.0V (4.5V - 5.5V) GPIO Output AC Specification...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time [1][2][3][4]	3.4	—	11	ns	DSE=1 CL (max) =50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1][2][3]	1.8	—	8.2	ns	DSE=0, SRE=0 CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1][2][3]	2.5	—	9.8	ns	DSE=0, SRE=1 CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1][2][3]	0.7	—	4.5	ns	DSE=1, SRE=0 CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1][2][3]	1.8	—	7.2	ns	DSE=1, SRE=1 CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1][2][3][4]	3.95	—	13.2	ns	DSE=0, SRE=0 CL (max) = 50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1][2][3][4]	4.3	—	13.8	ns	DSE=0, SRE=1 CL (max) = 50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1][2][3][4]	1.6	—	7.1	ns	DSE=1, SRE=0 CL (max) = 50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1][2][3][4]	2.7	—	9.6	ns	DSE=1, SRE=1 CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1][2][3]	0.4	—	3.15	ns	DSE=0, SRE=0 CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1][2][3]	1.5	—	6.7	ns	DSE=0, SRE=1 CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1][2][3]	0.3	—	2.02	ns	DSE=1, SRE=0 CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1][2][3]	0.9	—	4.85	ns	DSE=1, SRE=1 CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1][2][3][4]	1.0	—	5.8	ns	DSE=0, SRE=0 CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1][2][3][4]	1.9	—	8.5	ns	DSE=0, SRE=1 CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1][2][3][4]	0.9	—	3.0	ns	DSE=1, SRE=0 CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1][2][3][4]	1.3	—	6.1	ns	DSE=1, SRE=1 CL (max) = 50pF	—

[1] GPIO rise/fall time specifications are derived from simulation model for the defined operating points (between 20% and 80% of VDD_HV_A/B level). Actual application rise/fall time should be extracted from IBIS model simulations with the microcontroller models and application PCB.

[2] GPIO output transistion time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.

[3] I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load (typical) is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 3.3pF/inch. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected output resistance (ROUT_*) of the I/O pad.

[4] Output timing valid for maximum external load C L = 50pF (includes PCB trace, package trace, and external device input load).

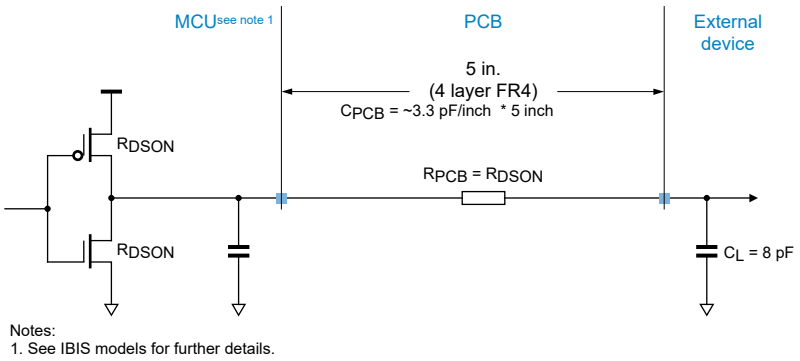


Figure 36. Reference Load Diagram

7.4 3.3V (2.97V - 3.63V) GPIO Output AC Specification

Table 30. 3.3V (2.97V - 3.63V) GPIO Output AC Specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_33_S	3.3V Standard GPIO rise/fall time [1][2][3]	5	—	28	ns	CL (max) = 25pF	—
TR_TF_33_S	3.3V Standard GPIO rise/fall time [1][2][3]	9.5	—	43	ns	CL (max) = 50pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time [1][2][3]	4	—	17.5	ns	DSE=0 CL (max) = 25pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time [1][2][3]	1.9	—	10	ns	DSE=1 CL (max) = 25pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time [1][2][3][4]	7.5	—	27	ns	DSE=0 CL (max) = 50pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time [1][2][3][4]	3.5	—	15	ns	DSE=1 CL (max) = 50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1][2][3]	2.2	—	12.3	ns	DSE=0, SRE=0 CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1][2][3]	3.0	—	14	ns	DSE=0, SRE=1 CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1][2][3]	0.8	—	6.6	ns	DSE=1, SRE=0 CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1][2][3]	2.4	—	10.5	ns	DSE=1, SRE=1 CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1][2][3][4]	4.5	—	17.3	ns	DSE=0, SRE=0 CL (max) = 50pF	—

Table continues on the next page...

Table 30. 3.3V (2.97V - 3.63V) GPIO Output AC Specification...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1][2][3][4]	5	—	19.8	ns	DSE=0, SRE=1 CL (max) = 50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1][2][3][4]	2.2	—	10	ns	DSE=1, SRE=0 CL (max) = 50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1][2][3][4]	3.6	—	13.9	ns	DSE=1, SRE=1 CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1][2][3]	0.5	—	4.9	ns	DSE=0, SRE=0 CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1][2][3]	2.1	—	10	ns	DSE=0, SRE=1 CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1][2][3]	0.4	—	2.2	ns	DSE=1, SRE=0 CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1][2][3]	1.2	—	7.1	ns	DSE=1, SRE=1 CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1][2][3][4]	1.1	—	8	ns	DSE=0, SRE=0 CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1][2][3][4]	2.6	—	12.1	ns	DSE=0, SRE=1 CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1][2][3][4]	0.8	—	4.2	ns	DSE=1, SRE=0 CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1][2][3][4]	1.5	—	8.6	ns	DSE=1, SRE=1 CL (max) = 50pF	—

[1] GPIO rise/fall time specifications are derived from simulation model for the defined operating points (between 20% and 80% of VDD_HV_A/B level). Actual application rise/fall time should be extracted from IBIS model simulations with the microcontroller models and application PCB.

[2] GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.

[3] I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load (typical) is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 3.3pF/inch. For signals with frequency greater than 63MHz, a maximum 2 inch PCB trace is assumed. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected output resistance (ROUT_*) of the I/O pad.

[4] Output timing valid for maximum external load C L = 50pF (includes PCB trace, package trace, and external device input load).

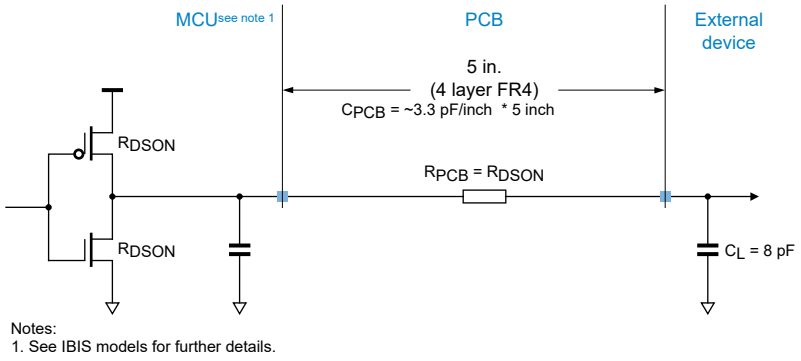


Figure 37. Reference Load Diagram

8 Glitch Filter

The glitch filter parameters in the following table apply to the filters of WKPU pins and TRGMUX inputs 60-63.

Table 31. Glitch Filter

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TFILT	Glitch filter max filtered pulse width [1][2][3]	—	—	20	ns	—	—
TUNFILT	Glitch filter min unfiltered pulse width [1][3][4]	400	—	—	ns	—	—

[1] An input signal pulse is defined by the duration between the input signal's crossing of a Vil/Vih threshold voltage level, and the next crossing of the opposite level.
[2] Pulses shorter than defined by the maximum value are guaranteed to be filtered (not passed).
[3] Pulses in between the max filtered and min unfiltered may or may not be passed through.
[4] Pulses larger than defined by the minimum value are guaranteed to not be filtered (passed).

9 Flash memory specification

9.1 Flash memory program and erase specifications

Table 32. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3],[4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 100,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	102	122	129	111	150		µs
t_{ppgm}	Page (256 bits) program time	142	171	180	157	200		µs
t_{qppgm}	Quad-page (1024 bits) program time	314	377	396	341	450		µs
t_{8kpgm}	8 KB Sector program time	20	24	26	22	30		ms
t_{8kers}	8 KB Sector erase time	4.8	8.5	10.6	6.5	30		ms
$t_{256kbers}$	256KB Block erase time	22.8	27.4	28.8	24.4	40	—	ms
$t_{512kbers}$	512KB Block erase time	25.4	30.5	32.1	27.9	45	—	ms
t_{1mbers}	1MB Block erase time	30.6	36.8	38.7	33.6	50	—	ms
t_{2mbers}	2MB Block erase time	41.1	49.3	51.8	45.2	60	—	ms

[1] Program times are actual hardware programming times and do not include software overhead. Sector program times assume quad-page programming.
[2] Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
[3] Conditions: ≤ 25 cycles, nominal voltage.
[4] Plant Programing times provide guidance for timeout limits used in the factory.
[5] Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
[6] Conditions: -40°C ≤T_J ≤150°C, full spec voltage.

9.2 Flash memory Array Integrity and Margin Read specifications

Table 33. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1] [2]	Units[3]
$t_{ai256kseq}$	Array Integrity time and Margin Read time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai512kseq}$	Array Integrity time and Margin Read time for sequential sequence on 512KB block.	—	—	16384 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai1mseq}$	Array Integrity time and Margin Read time for sequential sequence on 1MB block.	—	—	32768 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai2mseq}$	Array Integrity time and Margin Read time for sequential sequence on 2MB block.	—	—	65536 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai256kprop}$	Array Integrity time for proprietary sequence on 256KB block.	—	—	106496 x Tperiod x Nread	—
$t_{ai512kprop}$	Array Integrity time for proprietary sequence on 512KB block.	—	—	229376 x Tperiod x Nread	—
$t_{ai1mprop}$	Array Integrity time for proprietary sequence on 1MB block.	—	—	491520 x Tperiod x Nread	—
$t_{ai2mprop}$	Array Integrity time for proprietary sequence on 2MB block.	—	—	1048576 x Tperiod x Nread	—

[1] Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including single read, dual read, quad read contribution. Thus for a read setup that requires 6 clocks to read Nread would equal 6.
[2] Array Integrity times are actual hardware execution times and do not include software overhead or system code execution overhead.
[3] The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

9.3 Flash memory module life specifications

Table 34. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 256 KB and 512 KB blocks using Sector Erase.	—	100,000	—	P/E cycles
	Number of program/erase cycles per block for 1 MB and 2 MB blocks using Sector Erase.	—	1,000	—	P/E cycles
	Number of program/erase cycles per block using Block Erase[1]	—	25	—	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	20	—	Years
		Blocks with 100,000 P/E cycles.	10	—	Years

[1] Program and erase supported for factory conditions. Nominal supply values and operation at 25°C.

9.3.1 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure.

The spec window represents qualified limits.

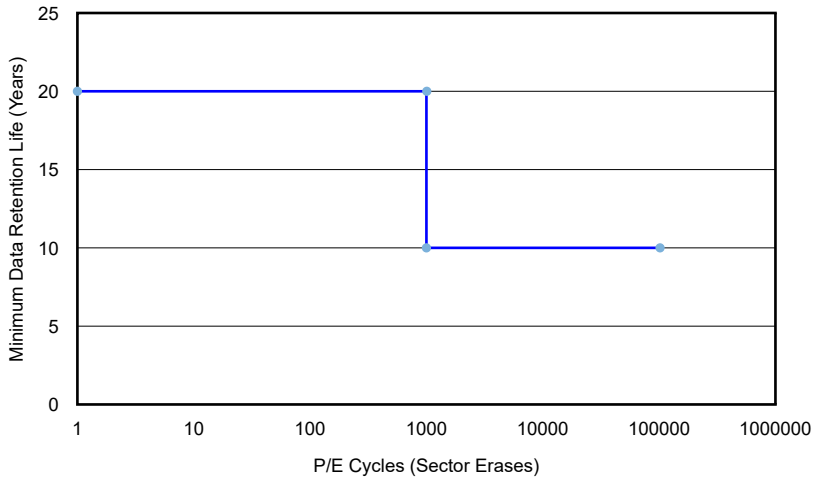


Figure 38. Data retention vs program/erase cycles

9.4 Flash memory AC timing specifications

Table 35. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR[EHV] bit initiating a program/erase until the MCR[DONE] bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR[EHV] bit aborting a program/erase until the MCR[DONE] bit is set to a 1.	5 plus four system clock periods	—	22 plus four system clock periods[1]	µs
t_{drcv}	Time to recover once exiting low power mode.	14 plus seven system clock periods[2]	17.5 plus seven system clock periods	21 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0[AIE] initiating a Margin Read or Array Integrity until the UT0[AID] bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing UT0[AISUS] or clearing UT0[NAIBP]	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0[AIE] initiating an Array Integrity abort until the UT0[AID] bit is set. This time also applies to the UT0[AISUS] to UT0[AID] setting in the event of a Array Integrity suspend request.	—	—	50 system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0[AIE] initiating a Margin Read abort until the UT0[AID] bit is set. This time also applies to the UT0[AISUS] to UT0[AID] setting in the event of a Margin Read suspend request.	—	—	26 plus fifteen system clock periods	µs

[1] For Block Erase, Tdones times may be 3x max spec.
[2] In extreme cases (1 block configurations) Tdrcv min may be faster (12uS plus seven system clocks)

9.5 Flash memory read timing parameters

Table 36. Flash Read Wait State Settings (S32K344, S32K324, S32K314, S32K342, S32K322, S32K341, S32K312, S32K311, S2K310 and S32K389(PFC1))

Flash Frequency (CORE_CLK)	RWSC setting
250 KHz < Freq ≤ 66 MHz	1
66 MHz < Freq ≤ 100 MHz	2
100 MHz < Freq ≤ 133 MHz	3
133 MHz < Freq ≤ 167 MHz	4
167 MHz < Freq ≤ 200 MHz	5

Table continues on the next page...

Table 36. Flash Read Wait State Settings (S32K344, S32K324, S32K314, S32K342, S32K322, S32K341, S32K312, S32K311, S2K310 and S32K389(PFC1))*...continued*

Flash Frequency (CORE_CLK)	RWSC setting
200 MHz < Freq ≤ 233 MHz	6
233 MHz < Freq ≤ 250 MHz	7

Table 37. Flash Read Wait State Settings (S32K358, S32K356, S32K348, S32K338, S32K328, S32K388 and S32K389(PFC0))

Flash Frequency (CORE_CLK)	RWSC setting
250 KHz < Freq ≤ 60 MHz	1
60 MHz < Freq ≤ 90 MHz	2
90 MHz < Freq ≤ 120 MHz	3
120 MHz < Freq ≤ 150 MHz	4
150 MHz < Freq ≤ 180 MHz	5
180 MHz < Freq ≤ 210 MHz	6
210 MHz < Freq ≤ 240 MHz	7
240 MHz < Freq ≤ 250 MHz	8

10 Analog modules

10.1 SAR_ADC

All below specs are applicable only when one ADC instance is in operation and averaging is used or multiple ADC instances are operational at the same time but sampling different channels. Best performance can be achieved if only one ADC is operational at a time sampling one channel

Table 38. SAR_ADC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_A	ADC Supply Voltage [1]	2.97	—	5.5	V	—	—
DVREFL	VSS / VREFL Voltage Difference [2]	-100	—	100	mV	—	—
VAD_INPUT	ADC Input Voltage [3]	VREFL	—	VREFH	V	—	—
fAD_CK	ADC Clock Frequency (S32K344, S32K324, S32K314,	10	—	80	MHz	—	—

Table continues on the next page...

Table 38. SAR_ADC...*continued*

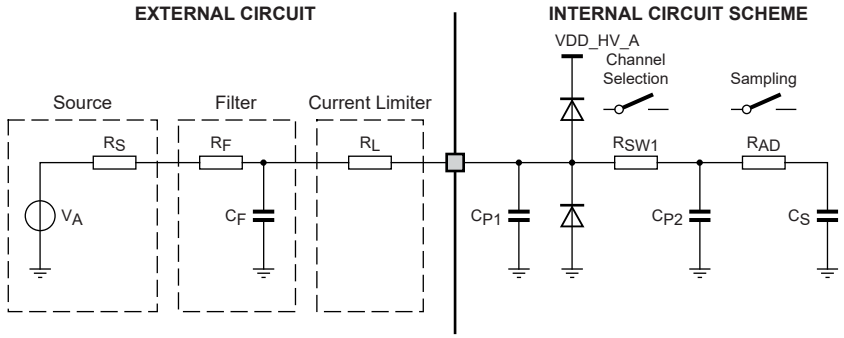
Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	S32K342, S32K341, S32K322)						
fAD_CK	ADC Clock Frequency (S32K312, S32K311, S32K310, S32K358, S32K356, S32K348, S32K338, S32K328, S32K388, S32K389)	10	—	120	MHz	—	—
tSAMPLE	ADC Input Sampling Time	275	—	—	ns	—	—
tCONV	ADC Total Conversion Time	1	—	—	us	12-bit result	—
tCONV	ADC Total Conversion Time	0.9	—	—	us	10-bit result	—
CAD_INPUT	ADC Input Capacitance	—	—	13.8	pF	ADC component plus pad capacitance (~2pF)	—
RAD_INPUT	ADC Input Resistance	—	—	4.6	KΩ	ADC + mux+SOC routing	—
RS	Source Impedance, precision channels	—	20	—	Ω	—	—
RS	Source Impedance, standard channels	—	20	—	Ω	—	—
TUE	ADC Total Unadjusted Error [4] [5]	—	+/-4	+/-6	LSB	without adjacent pin current injection	—
TUE	ADC Total Unadjusted Error [4]	—	+/-4	+/-8	LSB	with up to +/-3mA of current injection on adjacent pins	—
IAD_REF	Current Consumption on ADC Reference pin, VREFH.	—	—	200	uA	Per ADC for dedicated or shared reference pins	—
IDDA	Current Consumption on ADC Supply, VDD_HV_A	—	2.1	—	mA	Current consumption per ADC module, ADC enabled and converting	—
CS	Sampling Capacitance	6.4 (gain=0) 9.72	7.36 (gain=0) 11.12	8.32 (gain=0) 12.52	pF	all channels	—

Table continues on the next page...

Table 38. SAR_ADC...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
		pF(gain=max)	pF(gain=max)	(gain=max)			
RAD	Sampling Switch Impedance	80	170	520	Ohm	all channels	—
CP1	Pin capacitance	1.42	—	5.30	pF	all channels	—
CP1	Pin capacitance	1.42	—	4.38	pF	Precision channels	—
CP1	Pin capacitance	1.61	—	5.30	pF	Standard channels	—
CP2	Analog Bus Capacitance	0.32	—	4.18	pF	all channels	—
CP2	Analog Bus Capacitance	0.32	—	1.42	pF	Precision channels	—
CP2	Analog Bus Capacitance	0.497	—	4.18	pF	Standard channels	—
RSW1	Channel selection Switch impedance	65.9	—	1410	Ohm	all channels	—
RSW1	Channel selection Switch impedance	65.9	—	712	Ohm	Precision channels	—
RSW1	Channel selection Switch impedance	65.9	—	1410	Ohm	Standard channels	—

[1] Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR_ADC.
[2] VSS and VREFL should be shorted on PCB. 100mV difference between VSS and VREFL is for transient only (not for DC).
[3] This is ADC Input range for ADC accuracy guaranteed in this input range only. For SoC Pin capability, see Operation Condition Section.
[4] TUE spec for precision and standard channels is based on 12-bit level resolution.
[5] Spec valid if potential difference between VDD_HV_A and VREFH should follow VDD_HV_A +0.1V >=VREFH >= VDD_HV_A -1.5V



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW1} Channel Selection Switch Impedance
R_{AD} Sampling Switch Impedance
C_P Pin Capacitance (two contributions: C_{P1}, C_{P2})
C_S Sampling Capacitance

Figure 39. SAR_ADC Input Circuit

10.2 Supply Diagnosis

The table below gives the specification for the on die supply diagnosis.

Table 39. Supply Diagnosis

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
AN_ACC	Offset to internally monitored supply at ADC input [1][2][3]	-5	0	5	%	—	—
AN_T_on	Switching time from closed (OFF) to conducting (ON) [3]	—	2.5	12	ns	—	—
AN_TADCSA	Required ADC sampling time [1]	1.2	—	—	µs	—	—

[1] Required ADC sampling time specified by parameter AN_TADCSA needs to be used at the ADC conversion to guarantee the specified accuracy. A smaller sampling time leads to a less accurate result.
[2] If V15 > VDD_HV_A +100mV then the V15 measurement via anamux may be imprecise.
[3] These specs will have degraded performance when used in extended supply voltage operation range, i.e. normal supply voltage range specification is exceeded.

10.3 Low Power Comparator (LPCMP)

Table 40. Low Power Comparator (LPCMP)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
idda(IDHSS)	vdda Supply Current, High Speed Mode [1][2]	—	240	—	uA	—	—
idda(IDLSS)	vdda Supply Current, Low Speed Mode [1][2]	—	17	—	uA	—	—
idda(IDHSS)	vdda Supply Current, high speed mode, DAC only [1]	—	10	—	uA	—	—
idda_lkg	vdda Supply Current, module disabled [1]	—	2	—	nA	vdda=5.5V, T=25C	—
TDHSB	Propagation Delay, High Speed Mode [3]	—	—	200	ns	—	—
TDLSB	Propagation Delay, Low Speed mode [3]	—	—	2	us	—	—
TDHSS	Propagation Delay, High Speed Mode [4]	—	—	400	ns	—	—
TDLSS	Propagation Delay, Low Speed mode [4]	—	—	5	us	—	—

Table continues on the next page...

Table 40. Low Power Comparator (LPCMP)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TIDHS	Initialization Delay, High Speed Mode [5]	—	—	3	us	—	—
TIDLS	Initialization Delay, Low Speed mode [5]	—	—	30	us	—	—
VAIO	Analog Input Offset Voltage, High Speed Mode	-25	+/-1	25	mV	—	—
VAIO	Analog Input Offset Voltage, Low Speed mode	-40	+ /- 5	40	mV	—	—
VAHYST0	Analog Comparator Hysteresis, High Speed Mode	—	0	—	mV	HYSTCTR[1:0]= 2'b00	—
VAHYST1	Analog Comparator Hysteresis, High Speed Mode	—	14	41	mV	HYSTCTR[1:0]= 2'b01	—
VAHYST2	Analog Comparator Hysteresis, High Speed Mode	—	27	76	mV	HYSTCTR[1:0]= 2'b10	—
VAHYST3	Analog Comparator Hysteresis, High Speed Mode	—	40	111	mV	HYSTCTR[1:0]= 2'b11	—
VAHYST0	Analog Comparator Hysteresis, Low Speed mode	—	0	—	mV	HYSTCTR[1:0]= 2'b00	—
VAHYST1	Analog Comparator Hysteresis, Low Speed mode	—	8	60	mV	HYSTCTR[1:0]= 2'b01	—
VAHYST2	Analog Comparator Hysteresis, Low Speed mode	—	15	113	mV	HYSTCTR[1:0]= 2'b10	—
VAHYST3	Analog Comparator Hysteresis, Low Speed mode	—	23	165	mV	HYSTCTR[1:0]= 2'b11	—
INL	DAC integral linearity [1][6][7]	-1	—	1	LSB	vrefh_cmp = vdda, vrefl_cmp = vss	—
INL	DAC integral linearity [1][6][7]	-1.5	—	1.5	LSB	vrefh_cmp < vdda	—
DNL	DAC differential linearity [1][7]	-1	—	1	LSB	vrefh_cmp = vdda, vrefl_cmp = vss	—

Table continues on the next page...

Table 40. Low Power Comparator (LPCMP)...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
DNL	DAC differential linearity [1][7]	-1.5	—	1.5	LSB	vrefh_cmp < vdda	—
tDDAC	DAC Initialization time	—	—	30	us	—	—
VAIN	Analog input voltage	0	—	VDDA	V	—	—

[1] vdda is comparator HV supply and internally shorted to VDD_HV_A pin. vss is comparator ground
[2] Difference at input > 200mV
[3] Applied +/- (100 mV + VAHYST0/1/2/3 + max. of VAIO) around switch point
[4] Applied +/- (30 mV + VAHYST0/1/2/3 + max. of VAIO) around switch point
[5] Applied ± (100 mV + VAHYST0/1/2/3).
[6] Calculation method used: Linear Regression Least Square Method
[7] 1 LSB = (vrefh_cmp - vrefl_cmp) /256. vrefh_cmp and vrefl_cmp are comparator reference high and low

For Comparator IN signals adjacent to VDD_HV_A/VDD_HV_B/VSS or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired Comparator performance. Additionally an external capacitor to ground (1nF) should be used to filter noise on input signal. Also source drive should not be weak (Signal with <50K pull up/down is recommended).

For devices where the VDD_HV_B domain is present, LPCMP0 channels must only be selected/enabled when VDD_HV_A >= VDD_HV_B. These channels must be disabled when VDD_HV_A goes below VDD_HV_B. See GPIO test conditions before applying LPCMP channel input reference.

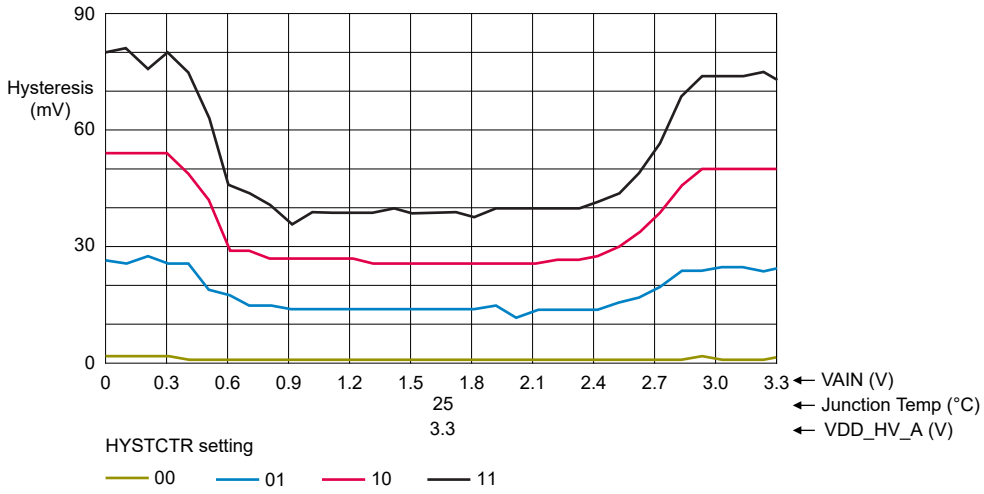


Figure 40. Typical Hysteresis vs VAIN (VDD_HV_A = 3.3 V, High Speed Mode)

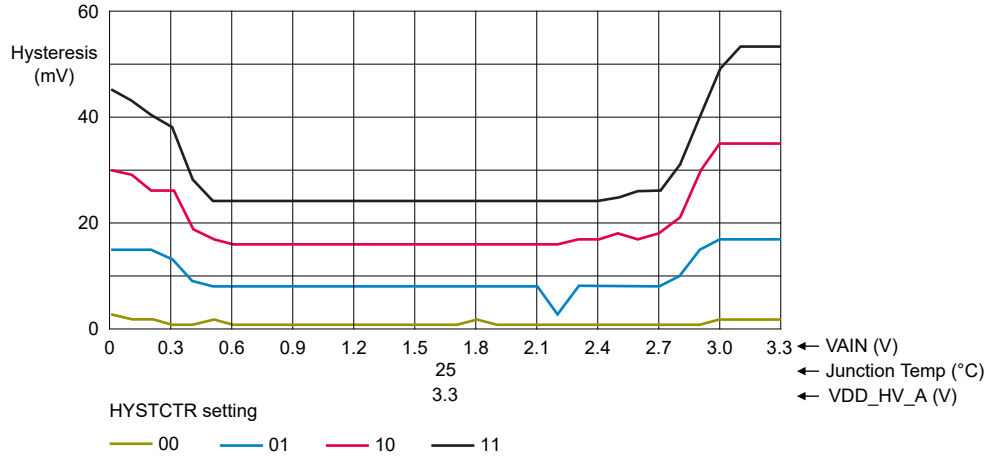


Figure 41. Typical Hysteresis vs VAIN (VDD_HV_A = 3.3 V, Low Speed Mode)

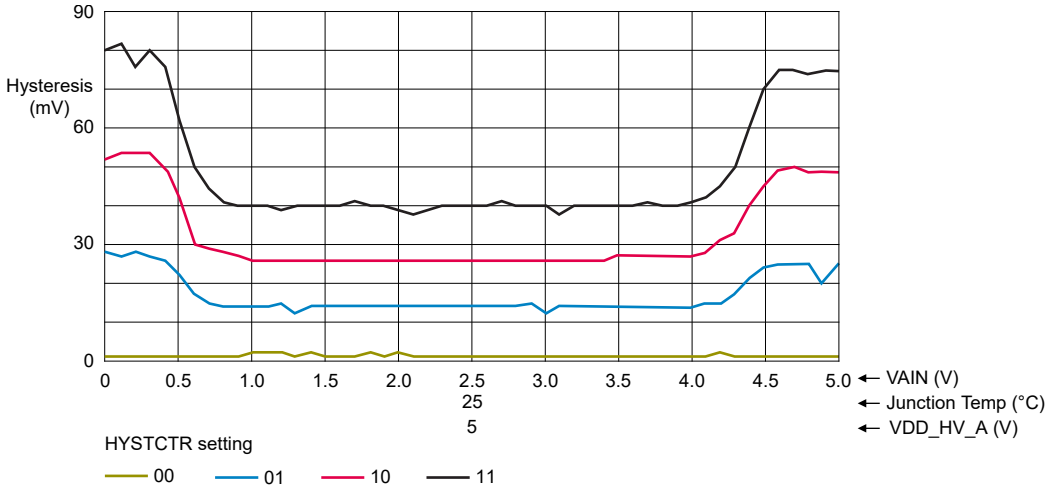


Figure 42. Typical Hysteresis vs VAIN (VDD_HV_A = 5 V, High Speed Mode).png

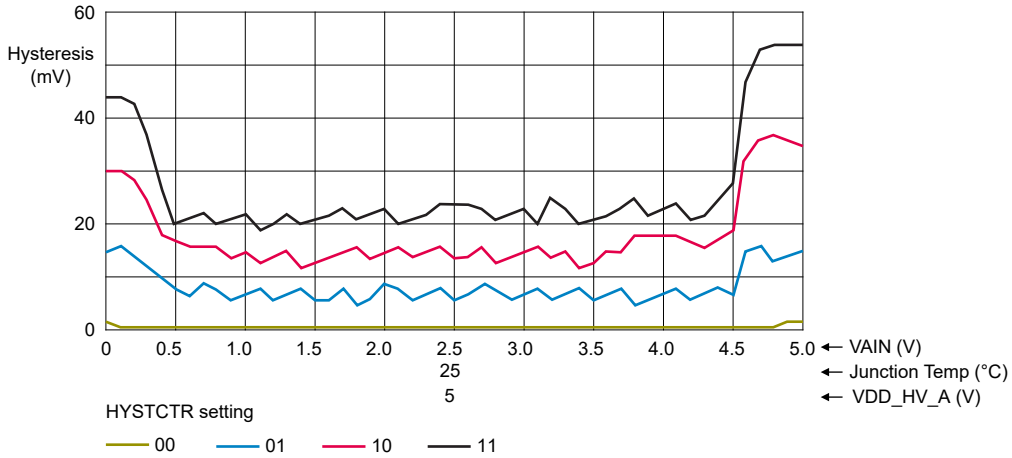


Figure 43. Typical Hysteresis vs VAIN (VDD_HV_A = 5 V, Low Speed Mode).png

10.4 Temperature Sensor

The temperature sensor measures the junction temperature Tj at the location where it is placed on die. The local Tj is modulated by current and previous active state of the circuit elements on die.

The table below gives the specification for the MCU on-die temperature sensor.

Table 41. Temperature Sensor

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TS_TJ	Junction temperature monitoring range	-40	—	150	°C	—	—
TS_IV25	ON state current consumption on V25	—	400	—	µA	ETS_EN=1	—
TS_ACC1	Temperature output error at circuit output (Voltage) [1][2]	-5	0	+5	°C	100 °C < Tj <= 150 °C	—
TS_ACC2	Temperature output error at circuit output (Voltage) [1][2]	-10	0	+10	°C	-40 °C <= Tj <=100 °C	—
TS_TSTART	Circuit start up time	—	4	30	µs	—	—
TS_TADCSA	Required ADC sampling time [2]	1.2	—	—	µs	—	—

[1] The error caused by ADC conversion and provided temperature calculation formula is not included.
[2] Required ADC sampling time specified by parameter TS_TADCSA needs to be used at the ADC conversion to guarantee the specified accuracy. A smaller sampling time leads to a less accurate result.

11 Clocking modules

11.1 FIRC

Table 42. FIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fFIRC	FIRC nominal Frequency	—	48	—	MHz	—	—
FACC	FIRC Frequency deviation across process, voltage, and temperature after trimming	-5	—	5	%	—	—
TSTART	Startup Time [1]	—	10	25	us	—	—

[1] Startup time is for reference only.

11.2 SIRC

Table 43. SIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSIRC	SIRC nominal Frequency	—	32	—	KHz	—	—
fSIRC_ACC	SIRC Frequency deviation across process, voltage, and temperature after trimming	-10	—	10	%	—	—
TSIRC_start	SIRC Startup Time [1]	—	—	3	ms	—	—
TSIRC_DC	SIRC duty cycle	30	—	70	%	—	—

[1] Startup time is for information only.

11.3 PLL

FPLL_DS, FPLL_FM and all fractional mode jitter specifications are not applicable to Auxiliary PLL on S32K328, S32K338, S32K348, S32K356, S32K358, S32K388 and S32K389 devices.

Jitter values specified in this table are applicable for FXOSC reference clock input only.

Table 44. PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FPLL_in	PLL input frequency	8	—	40	MHz	This is the frequency after the Reference Divider within the PLL	—
FPLL_out	PLL output frequency (PLL_PHIn_CLK) [1]	25	—	500	MHz	—	—
FPLL_vcoRange	VCO Frequency range	640	—	1280	MHz	—	—
FPLL_DS	Modulation Depth (down spread)	-0.5	—	-3	%	—	—
FPLL_FM	Modulation frequency	—	—	32	KHz	—	—
TPLL_start	PLL lock time	—	—	1	ms	—	—
JPLL_cyc	PLL period jitter (pk-pk) [2][3][4]	—	—	237	ps	FPLL_out = 240MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [2][3][4]	—	—	487	ps	FPLL_out = 240MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [2][3][4]	—	—	840	ps	FPLL_out = 240MHz, Integer Mode	—

Table continues on the next page...

Table 44. PLL...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
JPLL_acc	PLL accumulated jitter (pk-pk) [2][3][4]	—	—	1680	ps	FPLL_out = 240MHz, Fractional Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [2][3][4]	—	—	295	ps	FPLL_out = 160MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [2][3][4]	—	—	670	ps	FPLL_out = 160MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [2][3][4]	—	—	840	ps	FPLL_out = 160MHz, Integer Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [2][3][4]	—	—	1680	ps	FPLL_out = 160MHz, Fractional Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [2][3][4]	—	—	353	ps	FPLL_out = 120MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [2][3][4]	—	—	853	ps	FPLL_out = 120MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [2][3][4]	—	—	840	ps	FPLL_out = 120MHz, Integer Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [2][3][4]	—	—	1680	ps	FPLL_out = 120MHz, Fractional Mode	—

[1] The PLL output frequency must be configured such that the clock driven by this PLL output does not exceeded the maximum allowed for each device (see the Clocking chapter of the Reference Manual).
[2] Jitter numbers are valid only at IP boundary and does not include any degradation due to IO pad for clock measurement.
[3] Jitter numbers calculated by extrapolating RMS jitter numbers to +/- 7 sigma .
[4] For SSCG, jitter due to systematic modulation needs to be added as per applied modulation. Accumulated jitter specification is not valid with SSCG

11.4 FXOSC

Table 45. FXOSC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FREQ_BYPASS	Input clock frequency in bypass mode [1]	—	—	50	MHz	—	—
TRF_BYPASS	Input clock rise/fall time in bypass mode [1]	—	—	5	ns	—	—
CLKIN_DUTY_BYPASS	Input clock duty cycle in bypass mode [1]	47.5	—	52.5	%	—	—
FXOSC_CLK	output clock frequency in crystal mode	8	—	40	MHz	—	—

Table continues on the next page...

Table 45. FXOSC...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TFXOSC	Fxosc start up time (ALC enabled) [2]	—	—	2	ms	—	—
IFXOSC	Oscillator Analog circuit supply current, V25 supply (ALC enable)	—	—	1	mA	using 8, 16 or 40 MHz crystal	—
IFXOSC	Oscillator Analog circuit supply current, V25 supply (ALC disabled)	—	—	2.7	mA	using 8, 16 or 40 MHz crystal	—
EXTAL_SWING_PP	Peak-to-peak voltage swing on EXTAL pin in crystal oscillator mode (ALC enabled)	0.3	—	1.4	V	—	—
EXTAL_SWING_PP	Peak-to-peak voltage swing on EXTAL pin in crystal oscillator mode (ALC disabled) [3]	1.2	—	2.75	V	—	—
CLKIN_VIL_EXTAL_BYPASS	Input clock low level in bypass mode [4]	0	—	vref-1	V	vref=0.5*VDD_HV_A	—
CLKIN_VIH_EXTAL_BYPASS	Input clock high level in bypass mode [4]	vref+1	—	VDD_HV_A	V	vref=0.5*VDD_HV_A	—
VSB	Self Bias Voltage	350	—	850	mV	—	—
GM	Amplifier Transconductance	9.7	14.04	18.5	mA/V	GM_SEL[3:0] = 4`b1111	—

[1] For bypass mode applications, the EXTAL pin should be driven low when FXOSC is in off/disabled state.
[2] The startup time specification is valid only when the recommended crystal and load capacitors are used. For higher load capacitances, the actual startup time might be higher.
[3] The recommended gm setting to ensure extal swing < 2.75V at 8MHz in ALC-disabled mode is gm=4'b0010. Recommended gm settings in ALC-disabled mode for all other supported frequencies and crystals remain the same.
[4] For bypass mode applications, the EXTAL pin should be driven symmetrical around Vref =0.5* VDD_HV_A

To ensure stable oscillations, FXOSC incorporates the feedback resistance internally.

In single ended bypass mode, the XTAL pin can be left unconnected.

Drive level is a crystal specification and if crystal load capacitance is increased beyond the recommended value, it may violate the crystal drive level rating. In such cases, contact NXP sales representative for selecting the correct crystal.

Crystal oscillator circuit provides stable oscillations when gmXOSC > 5 * gm_crit. The gm_crit is defined as:

$gm\_crit = 4 * (ESR + RS) * (2\pi F)^2 * (C0 + CL)^2$

where:

- gmXOSC is the transconductance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- RS is the series resistance connected between XTAL pin and external crystal for current limitation
- F is the external crystal oscillation frequency
- C0 is the shunt capacitance of the external crystal
- CL is the external crystal total load capacitance. CL = Cs+ [C1*C2/(C1+C2)]
- Cs is stray or parasitic capacitance on the pin due to any PCB traces
- C1, C2 external load capacitances on EXTAL and XTAL pins

See manufacture datasheet for external crystal component values

Figure 44. Oscillation build-up equation

Note: *To improve the FXOSC & PLL jitter performance in S32K328, S32K338, S32K348, S32K356, S32K358 the functionality of the pins (namely - PTG0,PTG3,PTF11,PTF19,PTF30, PMOS_CTRL in BGA289 package) cannot be toggling edge aligned.*

Note: *To improve the FXOSC jitter & duty cycle performance in S32K310, S32K311, S32K312, S32K322, S32K341 S32K342, S32K314,S32K324 and S32K344, the functionality of the pin next to the Oscillator (namely, PTE14 in HDQFP172 and PTE3 in HDQFP100 package) must be limited to static GPIO operation.*

Note: *To improve the FXOSC & PLL jitter performance in S32K388, the functionality of the pins (namely - PTG0, PTG2, PTG3, PTF30, PTE12, PTA29, PMOS_CTRL in BGA289 package) cannot be toggling edge-aligned.*

Note: *To improve the FXOSC & PLL jitter performance in S32K389, the functionality of the pins (namely - PTE3, PTD15, PTE8, PTE4, PTG6, PTG0 and PMOS_CTRL in BGA437 package) cannot be toggling edge-aligned.*

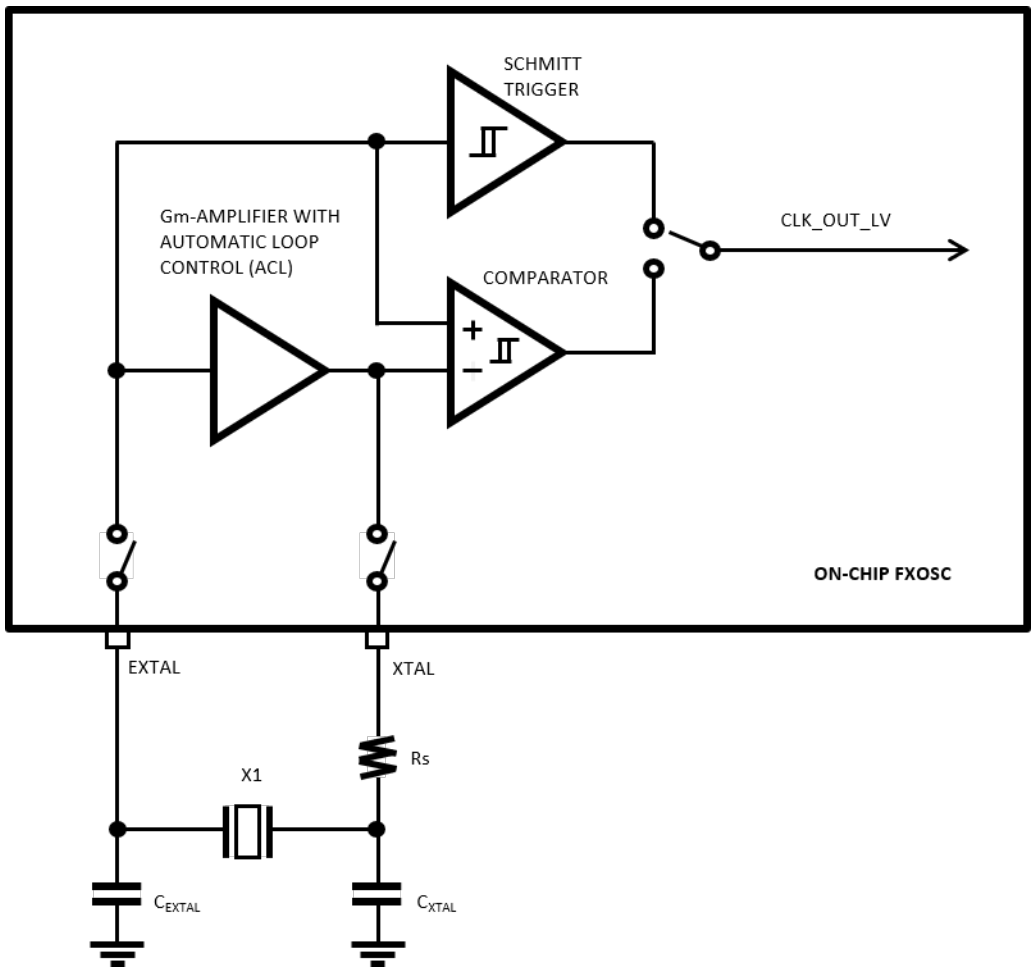


Figure 45. Block diagram

11.5 SXOSC

Table 46. SXOSC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsxosc	Oscillator Crystal Frequency [1]	—	32.768	—	KHz	IP in crystal mode	—
Tstart	SXOSC startup time	—	—	2	s	start up time is dependent upon board and crystal model.	—
ISXOSC	Oscillator Analog circuit supply current	—	2.1	10	uA	—	—
gm_sxocs	NMOS Amplifier Transconductance	3	—	40	u A/V	—	—

[1] Supports single frequency

12 Communication interfaces

12.1 LPSPI

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with controller and peripheral operations. Many of the transfer attributes are programmable. The following table provides timing characteristics for classic LPSPI timing modes.

1. All timing is shown with respect to 50% VDD_HV_A/B thresholds.

2. All measurements are with maximum output load of 30pF (except 50pF support on K3x8 and S32K389 with Fast/Medium/Standard-Plus IOs), input transition of 1 ns and pad configured DSE = 1, SRC = 0.

Table 47. LPSPI

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fperiph	Peripheral Frequency [1][2][3]	—	—	40	MHz	Controller, Applies to all S32K3xx except S32K389	—
fperiph	Peripheral Frequency [1][2][3]	—	—	80	MHz	Controller, Applies to S32K389	—
fperiph	Peripheral Frequency [1][2][3]	—	—	40	MHz	Peripheral, Applies to all S32K3xx except S32K389	—
fperiph	Peripheral Frequency [1][2][3]	—	—	80	MHz	Peripheral, Applies to S32K389	—
fperiph	Peripheral Frequency [1][2][4]	—	—	80	MHz	Controller Loopback	—
fop	Operating frequency	—	—	15	MHz	Peripheral	1
fop	Operating frequency	—	—	15	MHz	Controller	1
fop	Operating frequency [5]	—	—	10	MHz	Peripheral_10Mbps	1
fop	Operating frequency [5]	—	—	10	MHz	Controller_10Mbps	1
fop	Operating frequency [4][6]	—	—	20	MHz	Controller Loopback	1
tSPSCK	SPSCK period	66	—	—	ns	Peripheral	2
tSPSCK	SPSCK period	66	—	—	ns	Controller	2
tSPSCK	SPSCK period [4]	50	—	—	ns	Controller Loopback	2
tSPSCK	SPSCK period	100	—	—	ns	Controller_10Mbps	2
tSPSCK	SPSCK period	100	—	—	ns	Peripheral_10Mbps	2
tLEAD	Enable lead time (PCS to SPSCK delay) [7]	tSPCK/2	—	—	ns	Peripheral	3

Table continues on the next page...

Table 47. LPSPI*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tLEAD	Enable lead time (PCS to SPSCK delay) [7]	30	—	—	ns	Controller	3
tLEAD	Enable lead time (PCS to SPSCK delay) [4][7]	30	—	—	ns	Controller Loopback	3
tLAG	Enable lag time (After SPSCK delay) [8]	tSPCK/2	—	—	ns	Peripheral	4
tLAG	Enable lag time (After SPSCK delay) [8]	30	—	—	ns	Controller	4
tLAG	Enable lag time (After SPSCK delay) [4][8]	30	—	—	ns	Controller Loopback	4
tWSPCK	Clock (SPSCK) time (SPSCK duty cycle) [9]	tSPSCK/2 - 3	—	tSPSCK/2 + 3	ns	Peripheral	5
tWSPCK	Clock (SPSCK) time (SPSCK duty cycle) [9]	tSPSCK/2 - 3	—	tSPSCK/2 + 3	ns	Controller	5
tWSPCK	Clock (SPSCK) time (SPSCK duty cycle) [4][9]	tSPSCK/2 - 3	—	tSPSCK/2 + 3	ns	Controller Loopback	5
tSU	Data setup time(inputs)	6	—	—	ns	Peripheral	6
tSU	Data setup time(inputs)	25	—	—	ns	Controller	6
tSU	Data setup time(inputs)	5	—	—	ns	Peripheral_10Mbps	6
tSU	Data setup time(inputs)	36	—	—	ns	Controller_10Mbps	6
tSU	Data setup time(inputs) [4]	6	—	—	ns	Controller_Loopback	6
tHI	Data hold time(inputs)	3	—	—	ns	Peripheral	7
tHI	Data hold time(inputs)	0	—	—	ns	Controller	7
tHI	Data hold time(inputs)	4	—	—	ns	Peripheral_10Mbps	7

Table continues on the next page...

Table 47. LPSPI*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tHI	Data hold time(inputs)	0	—	—	ns	Controller_10Mbps	7
tHI	Data hold time(inputs) [4]	3	—	—	ns	Controller Loopback	7
tA	MISO valid time after SS assertion	—	—	50	ns	Peripheral	8
tDIS	Peripheral MISO (SOUT) disable time	—	—	50	ns	Peripheral	9
tV	Data valid (after SPSCK edge) [10]	—	—	26	ns	Peripheral	10
tV	Data valid (after SPSCK edge) [10]	—	—	14	ns	Controller	10
tV	Data valid (after SPSCK edge) [10]	—	—	36	ns	Peripheral_10Mbps	10
tV	Data valid (after SPSCK edge) [10]	—	—	21	ns	Controller_10Mbps, for all S32K3xx variants except S32K3x8	10
tV	Data valid (after SPSCK edge) [10]	—	—	24	ns	Controller_10Mbps, for S32K3x8	10
tV	Data valid (after SPSCK edge) [4][10]	—	—	8	ns	Controller Loopback, applies to S32K388 LPSPI2 and LPSPI5 @20MHz	10
tV	Data valid (after SPSCK edge) [4][10]	—	—	8	ns	Controller Loopback, applies to S32K389 LPSPI1, LPSPI2, LPSPI3, LPSPI4 and LPSPI5 @20MHz	10
tV	Data valid (after SPSCK edge) [4][10]	—	—	17.5	ns	Controller Loopback, applies to all devices LPSPI0 @20 MHz	10
tHO	Data hold time (outputs) [10]	3	—	—	ns	Peripheral	11
tHO	Data hold time (outputs) [10]	-8	—	—	ns	Controller	11
tHO	Data hold time (outputs) [10]	3	—	—	ns	Peripheral_10Mbps	11
tHO	Data hold time (outputs) [10]	-15	—	—	ns	Controller_10Mbps, for all S32K3xx variants except S32K3x8	11

Table continues on the next page...

Table 47. LPSPI...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tHO	Data hold time (outputs) [10]	-18	—	—	ns	Controller_10Mbps, for S32K3x8	11
tHO	Data hold time (outputs) [4][10]	-4.5	—	—	ns	Controller Looopback, applies to S32K389 LPSPI1, LPSPI2, LPSPI3, LPSPI4 and LPSPI5 @20MHz	11
tHO	Data hold time (outputs) [4][10]	-4.5	—	—	ns	Controller Looopback, applies to S32K388 LPSPI2 and LPSPI5 @20MHz	11
tHO	Data hold time (outputs) [4][10]	-2	—	—	ns	Controller Loopback, applies to all devices LPSPI0 @20 MHz	11
tRI/FI	Rise/Fall time input [11]	—	—	1	ns	Peripheral	—
tRI/FI	Rise/Fall time input [11]	—	—	1	ns	Controller	—
tRI/FI	Rise/Fall time input [4][11]	—	—	1	ns	Controller Loopback	—

[1] fperiph = LPSPI peripheral clock
[2] tperiph = 1/fperiph
[3] For LPSPI0 instance, max. peripheral frequency is equal to AIPS_PLAT_CLK.
[4] Controller Loopback mode: In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1.
[5] These specifications apply to the SPI operation, as Controller or Peripheral, at up to 10 Mbps for the combinations not indicated in the table below. Unless otherwise noted, all other ‘Controller’ and ‘Peripheral’ specifications are also applicable in the 10Mbps configurations. See table "LPSPI 20 MHz and 15 MHz Combinations.
[6] LPSPI0 support up to 20MHz on fast pin.
[7] Minimum configuration value for CCR[PCSSCK] field is 3(0x00000011).
[8] Minimum configuration value for CCR[SCKPCS] field is 3(0x00000011).
[9] While selecting odd dividers, ensure Duty Cycle is meeting this parameter.
[10] Output rise/fall time is determined by the output load and GPIO pad drive strength setting. See the GPIO specifications for detail.
[11] The input rise/fall time specification applies to both clock and data, and is required to guarantee related timing parameters.

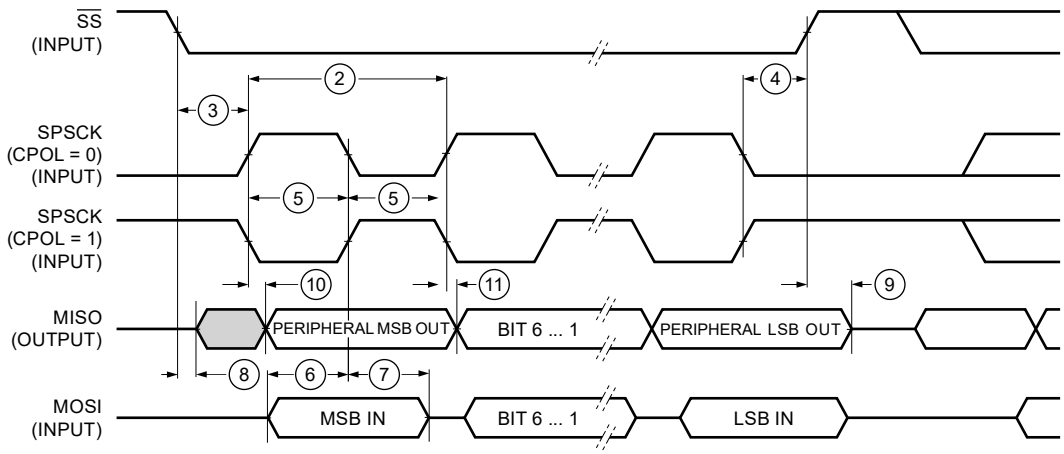


Figure 46. LPSPI Peripheral Mode Timing (CPHA=1)

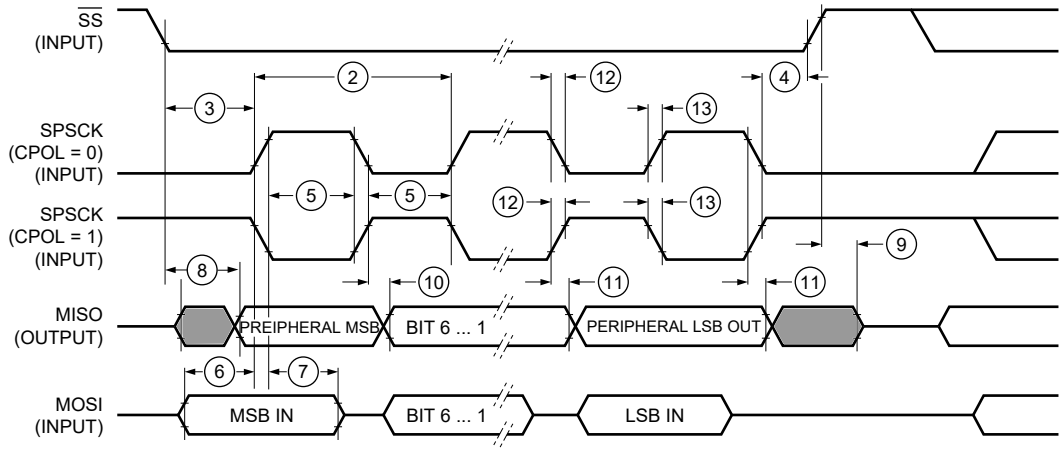


Figure 47. LPSPI Peripheral Mode Timing (CPHA=0)

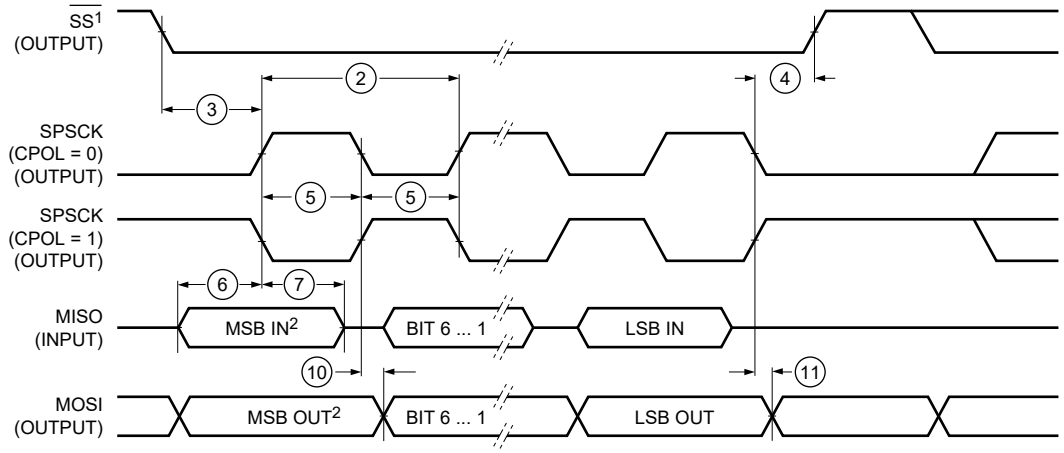


Figure 48. LPSPI Controller Mode Timing (CPHA=0)

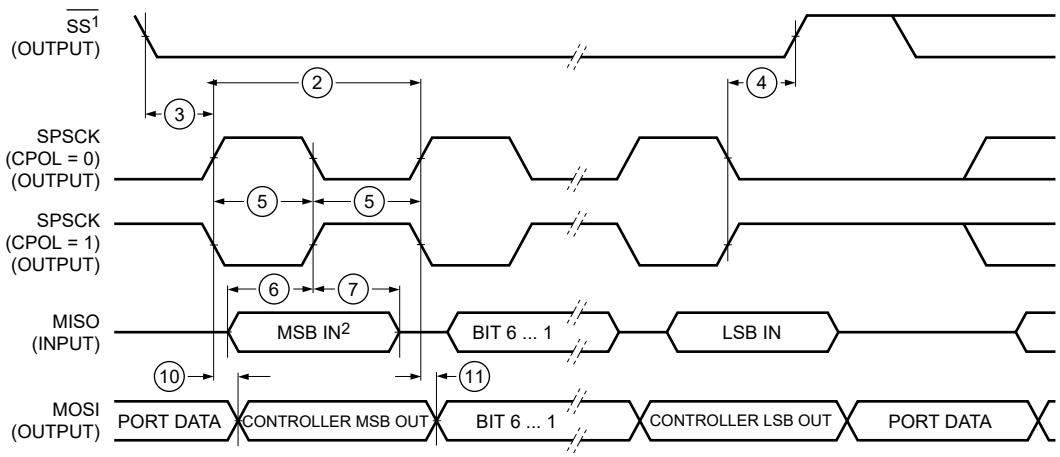


Figure 49. LPSPI Controller Mode Timing (CPHA=1)

12.2 LPSPI0 20 MHz and 15 MHz Combinations

Note: *15 and 20 Mbps is supported on LPSPI0 only.*

All measurements are with maximum output load of 25pF (except 30pF support on S32K356 and S32K358 with Standard-Plus IOs, and 50pF support on S32K388 and S32K389 with Standard-Plus IOs). S32K31x devices support only 15 MHz modes and all other devices support both 15 and 20 MHz combinations.

Table 48. LPSPI0 20 MHz and 15 MHz Combinations

PORT	SPI Signal	20Mbps (In loopback mode only)	15 Mbps
PTB1	LPSPI0_SOUT		LPSPI0_SOUT
PTB0	LPSPI0_PCS0		LPSPI0_PCS0
PTC9	LPSPI0_SIN		LPSPI0_SIN
PTC8	LPSPI0_SCK		LPSPI0_SCK
PTD6	LPSPI0_PCS0	LPSPI0_PCS0	
PTD5	LPSPI0_PCS1	LPSPI0_PCS1	
PTD12	LPSPI0_SOUT	LPSPI0_SOUT	
PTD11	LPSPI0_SCK	LPSPI0_SCK	
PTD10	LPSPI0_SIN	LPSPI0_SIN	

Note: *Trace length should not exceed 11 inches for SCK pad when used in Controller loopback mode.*

12.3 LPSPI* 20MHz combination for S32K388 and S32K389

Note: *LPSPI running at 20MHz speed is possible only on specific pads as per table below.*

All measurements are with maximum output load of 25pF.

Table 49. LPSPI2 and LPSPI5 20MHz combination for S32K388 and S32K389

LPSPI Instance	Signal Type	PIN	LPSPI Signal
LPSPI2 Controller Loopback	PCS	PTF7	LPSPI2_PCS0
	SCK	PTA11	LPSPI2_SCK
	SOUT	PTF4	LPSPI2_SOUT
	SIN	PTE24	LPSPI2_SIN
LPSPI5 Controller Loopback	PCS	PTG23	LPSPI5_PCS0
	SCK	PTD31	LPSPI5_SCK
	SOUT	PTG25	LPSPI5_SOUT
	SIN	PTD28	LPSPI5_SIN

Table 50. LPSPI5 and LPSPI0 20MHz combination for S32K388 and S32K389

LPSPI Instance	Signal Type	PIN	LPSPI Signal
LPSPI5 Controller Loopback	PCS	PTD17	LPSPI5_PCS0
	SCK	PTD14	LPSPI5_SCK
	SOUT(MOSI)	PTE9	LPSPI5_SOUT
	SIN(MISO)	PTD13	LPSPI5_SIN
LPSPI0 Controller Loopback	PCS	PTD6	LPSPI0_PCS0
	SCK	PTD11	LPSPI0_SCK
	SOUT(MOSI)	PTD12	LPSPI0_SOUT
	SIN(MISO)	PTD10	LPSPI0_SIN

Table 51. LPSPI1, LPSPI3 and LPSPI4 20 MHz combination for S32K389

LPSPI Instance	Signal Type	PIN	LPSPI Signal	I/O Power Domain
LPSPI1 Controller Loopback	PCS	PTI16	LPSPI1_PCS0	VDD_HV_A
	SCK	PTI23	LPSPI1_SCK	VDD_HV_A
	SOUT	PTI18	LPSPI1_SOUT	VDD_HV_A
	SIN	PTI20	LPSPI1_SIN	VDD_HV_A
LPSPI3 Controller Loopback	PCS	PTJ16	LPSPI3_PCS0	VDD_HV_A
	SCK	PTJ10	LPSPI3_SCK	VDD_HV_A
	SOUT	PTJ14	LPSPI3_SOUT	VDD_HV_A
	SIN	PTJ12	LPSPI3_SIN	VDD_HV_A
LPSPI4 Controller Loopback	PCS	PTK0	LPSPI4_PCS0	VDD_HV_B
	SCK	PTJ29	LPSPI4_SCK	VDD_HV_B
	SOUT	PTJ26	LPSPI4_SOUT	VDD_HV_B
	SIN	PTJ23	LPSPI4_SIN	VDD_HV_B

12.4 Communication between two S32K38x devices

S32K38x devices supports fast data sending between two of them. Interface uses is four data lines at frequency of 6.6MHz in one direction and four data lines at frequency of 6.6MHz in opposite direction. Configuration of LPSPI interface is 4x data lines half duplex mode. For purpose of this communication LPSPI2, LPSPI5 and set of PINs was designed. Below figure shows diagram of connection between two S32K38x devices. Left device will use LPSPI2 in Conroller 4x data line half duplex mode to send data to LPSPI2 in Peripheral 4x dataline half duplex mode on second device. Similarly LPSPI5, but for in opposite direction than LPSPI2 do.

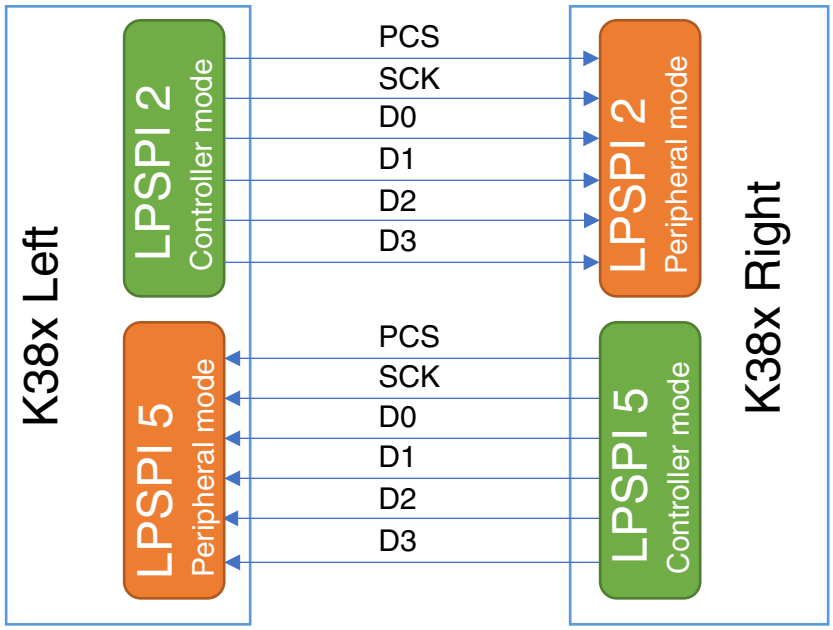


Figure 50. Connection between two S32K38x devices

Table 52. Pins and signals assignment for this communication.

K38x Left				K38x Right			
LPSPI instance	Signal type	PIN	LPSPI signal	LPSPI instance	Signal type	PIN	LPSPI signal
LPSPI2 Controller mode	PCS	PTF7	LPSPI2_PCS0	LPSPI2 Peripheral mode	PCS	PTF7	LPSPI2_PCS0
	SCK	PTA11	LPSPI2_SCK		SCK	PTA11	LPSPI2_SCK
	D0	PTF4	LPSPI2_SOUT		D0	PTF4	LPSPI2_SOUT
	D1	PTE24	LPSPI2_SIN		D1	PTE24	LPSPI2_SIN
	D2	PTH0	LPSPI2_PCS2		D2	PTH0	LPSPI2_PCS2
	D3	PTH1	LPSPI2_PCS3		D3	PTH1	LPSPI2_PCS3

Table continues on the next page...

Table 52. Pins and signals assignment for this communication....*continued*

LPSPI5 Peripheral mode	PCS	PTG23	LPSPI5_PCS0	LPSPI5 Controller mode	PCS	PTG28	LPSPI5_PCS0
	SCK	PTD31	LPSPI5_SCK		SCK	PTG31	LPSPI5_SCK
	D0	PTG25	LPSPI5_SOUT		D0	PTG30	LPSPI5_SOUT
	D1	PTD28	LPSPI5_SIN		D1	PTG29	LPSPI5_SIN
	D2	PTG24	LPSPI5_PCS2		D2	PTG13	LPSPI5_PCS2
	D3	PTD30	LPSPI5_PCS3		D3	PTG8	LPSPI5_PCS3

12.4.1 Timing specification for S32K38x to S32K38x communication

Below table lists the timing parameters for this communication. This parameters is valid only on set of pins preselected for this device to device communication. All timing is shown with respect to 50% VDD_HV_A/B thresholds. All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1'b1).

Table 53. Timing specification for S32K38x to S32K38x communication

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fcom	Communication frequency	—	—	6.6	MHz	—	—
tWSPCK	Clock (SPSCK) high or low time (SPSCK duty cycle)	69	—	79	ns	—	—
tSU	Data setup time	34	—	—	ns	Controller mode	6
tSU	Data setup time	5	—	—	ns	Peripheral mode	6
tV	Data valid (after SPSCK edge)	—	—	21	ns	Controller mode	10
tV	Data valid (after SPSCK edge)	—	—	34	ns	Peripheral mode	10
tHO	Input hold time	0	—	—	ns	Controller mode input	7
tHO	Input hold time	4	—	—	ns	Peripheral mode input	7
tHO	Output hold time	3	—	—	ns	Peripheral mode output	11
tHO	Output hold time	-15	—	—	ns	Controller mode output	11
tLEAD	Enable lead time (PCS to SPSCK delay)	30	—	—	ns	Controller mode	3
tA	Peripheral access time	—	—	50	ns	—	—
tDIS	Peripheral MISO (SOUT) disable time	—	—	50	ns	—	—
tLAG	Enable lag time (After SPSCK delay)	30	—	—	ns	—	—

12.5 I²C

See I/O parameters for I²C specification.

"For supported baud rate see section 'Chip-specific LPI2C information' of the Reference Manual."

12.6 FlexCAN characteristics

See I/O parameters for FlexCAN specification.

"For supported baud rate, see section 'Protocol timing' of the Reference Manual."

12.7 SAI electrical specifications

12.7.1 SAI Electrical Characteristics, Target Mode

The following table describes the SAI electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Table 54. SAI Electrical Characteristics, Target Mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S13	SAI_BCLK cycle time (input)	80	—	—	ns	—	—
S14	SAI_BCLK pulse width high/low (input) [1]	45	—	55	%	—	—
S15	SAI_RXD input setup before SAI_BCLK	8	—	—	ns	Applies to all S32K3xx except S32K389	—
S15	SAI_RXD input setup before SAI_BCLK	8.5	—	—	ns	Applies to S32K389	—
S16	SAI_RXD input hold after SAI_BCLK	2	—	—	ns	—	—
S17	SAI_BCLK to SAI_TXD output valid	—	—	28	ns	—	—
S18	SAI_BCLK to SAI_TXD output invalid	0	—	—	ns	—	—
S19	SAI_FS input setup before SAI_BCLK	8	—	—	ns	Applies to all S32K3xx except S32K389	—
S19	SAI_FS input setup before SAI_BCLK	8.5	—	—	ns	Applies to S32K389	—
S20	SAI_FS input hold after SAI_BCLK	2	—	—	ns	—	—

Table continues on the next page...

Table 54. SAI Electrical Characteristics, Target Mode...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S21	SAI_BCLK to SAI_FS output valid	—	—	28	ns	—	—
S22	SAI_BCLK to SAI_FS output invalid	0	—	—	ns	—	—

[1] The target mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the controller timing.

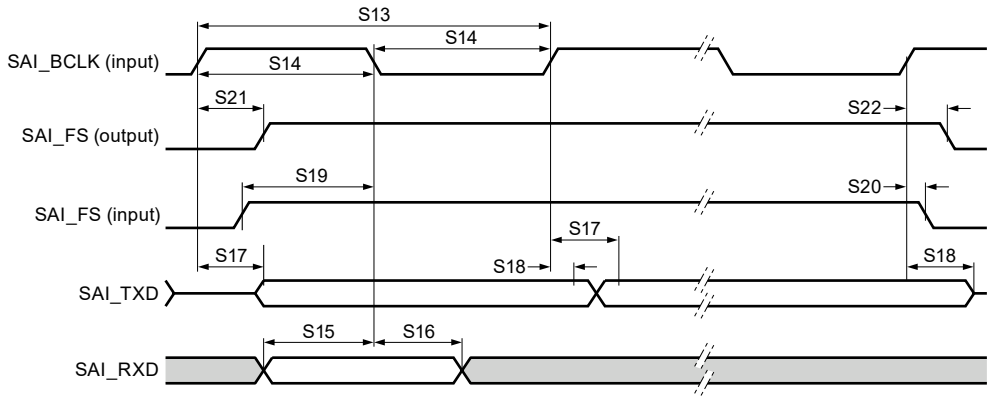


Figure 51. SAI slave mode

12.7.2 SAI Electrical Characteristics, Controller Mode

The following table describes the SAI electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b 0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Table 55. SAI Electrical Characteristics, Controller Mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SAI_MCLK cycle time	40	—	—	ns	—	—
S2	SAI_MCLK pulse width high/low	45	—	55	%	—	—
S3	SAI_BCLK cycle time	80	—	—	ns	—	—
S4	SAI_BCLK pulse width high/low	45	—	55	%	—	—
S5	SAI_RXD input setup before SAI_BCLK	28	—	—	ns	Applies to all S32K3xx except S32K389	—

Table continues on the next page...

Table 55. SAI Electrical Characteristics, Controller Mode...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S5	SAI_RXD input setup before SAI_BCLK	10	—	—	ns	Applies to S32K389	—
S6	SAI_RXD input hold after SAI_BCLK	0	—	—	ns	—	—
S7	SAI_BCLK to SAI_TXD output valid	—	—	8	ns	Applies to all S32K3xx except S32K389	—
S7	SAI_BCLK to SAI_TXD output valid	—	—	10	ns	Applies to S32K389	—
S8	SAI_BCLK to SAI_TXD output invalid	-2	—	—	ns	—	—
S9	SAI_FS input setup before SAI_BCLK	28	—	—	ns	Applies to all S32K3xx except S32K389	—
S9	SAI_FS input setup before SAI_BCLK	10	—	—	ns	Applies to S32K389	—
S10	SAI_FS input hold after SAI_BCLK	0	—	—	ns	—	—
S11	SAI_BCLK to SAI_FS output valid	—	—	8	ns	Applies to all S32K3xx except S32K389	—
S11	SAI_BCLK to SAI_FS output valid	—	—	10	ns	Applies to S32K389	—
S12	SAI_BCLK to SAI_FS output invalid	-2	—	—	ns	—	—

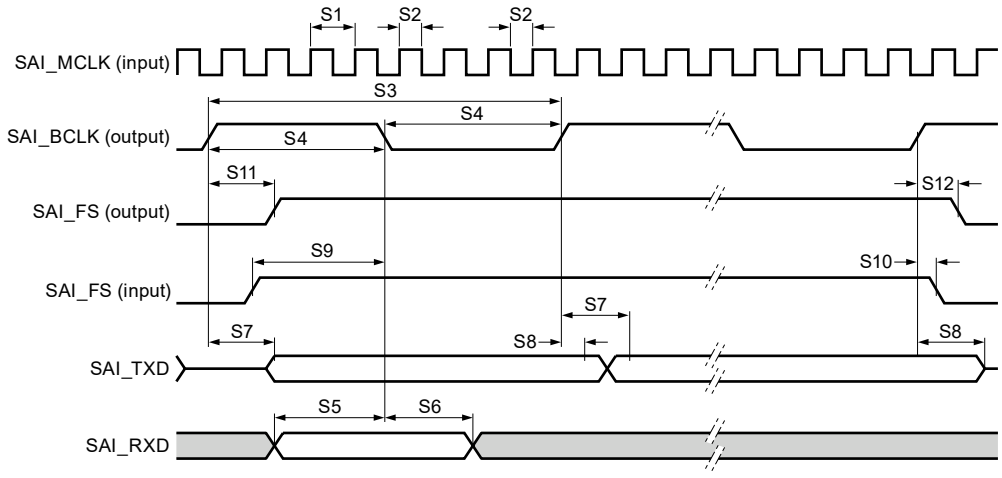


Figure 52. SAI controller mode

12.8 Ethernet characteristics

12.8.1 Ethernet MII (10/100 Mbps)

The following timing specs are defined at the device I/O pin and must be translated appropriately to arrive at timing specs/ constraints for the physical interface. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Table 56. Ethernet MII (10/100 Mbps)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	RXCLK frequency	—	2.5/25	—	MHz	10/100 Mbps	—
MII1	RXCLK pulse width high	35	—	65	%RXCLK period	—	—
MII2	RXCLK pulse width low	35	—	65	%RXCLK period	—	—
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	—	ns	10/100 Mbps	—
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	—	ns	10/100 Mbps	—
tCYC_TX	TXCLK frequency	—	2.5 / 25	—	MHz	10/100 Mbps	—
MII5	TXCLK pulse width high	35	—	65	%TXCLK period	—	—
MII6	TXCLK pulse width low	35	—	65	%TXCLK period	—	—

Table continues on the next page...

Table 56. Ethernet MII (10/100 Mbps)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	—	ns	—	—
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	—	25	ns	—	—

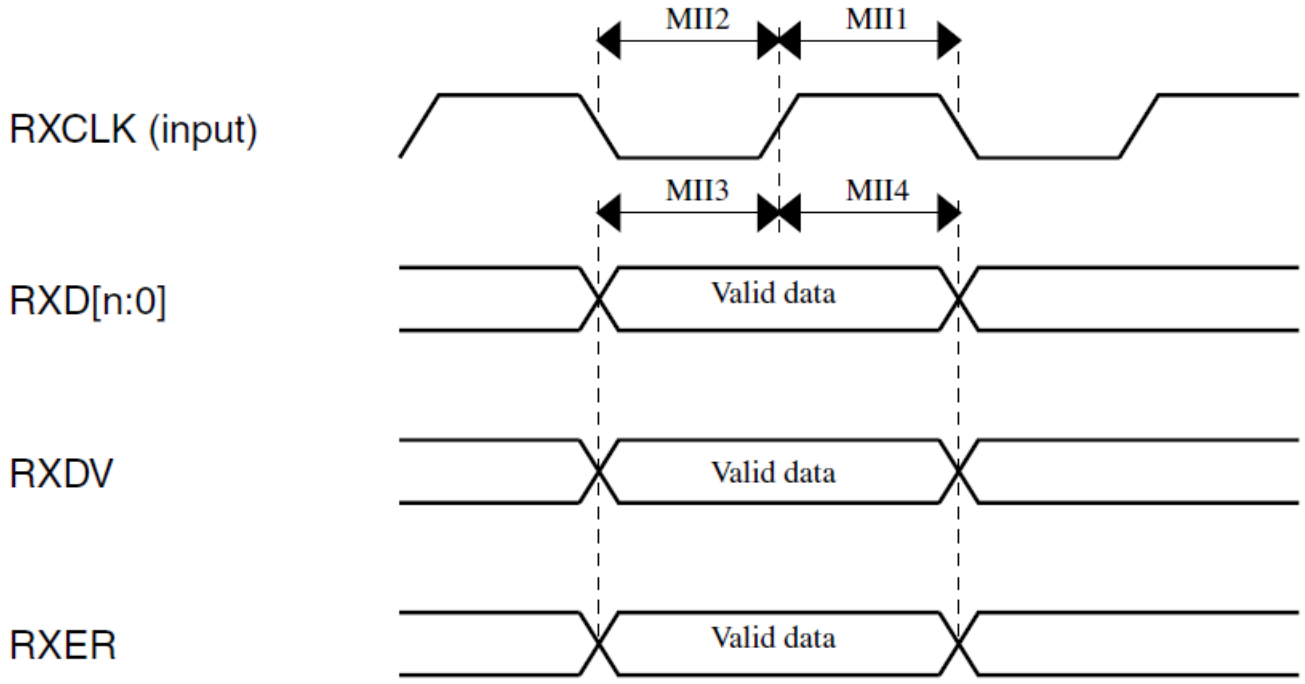


Figure 53. MII receive diagram

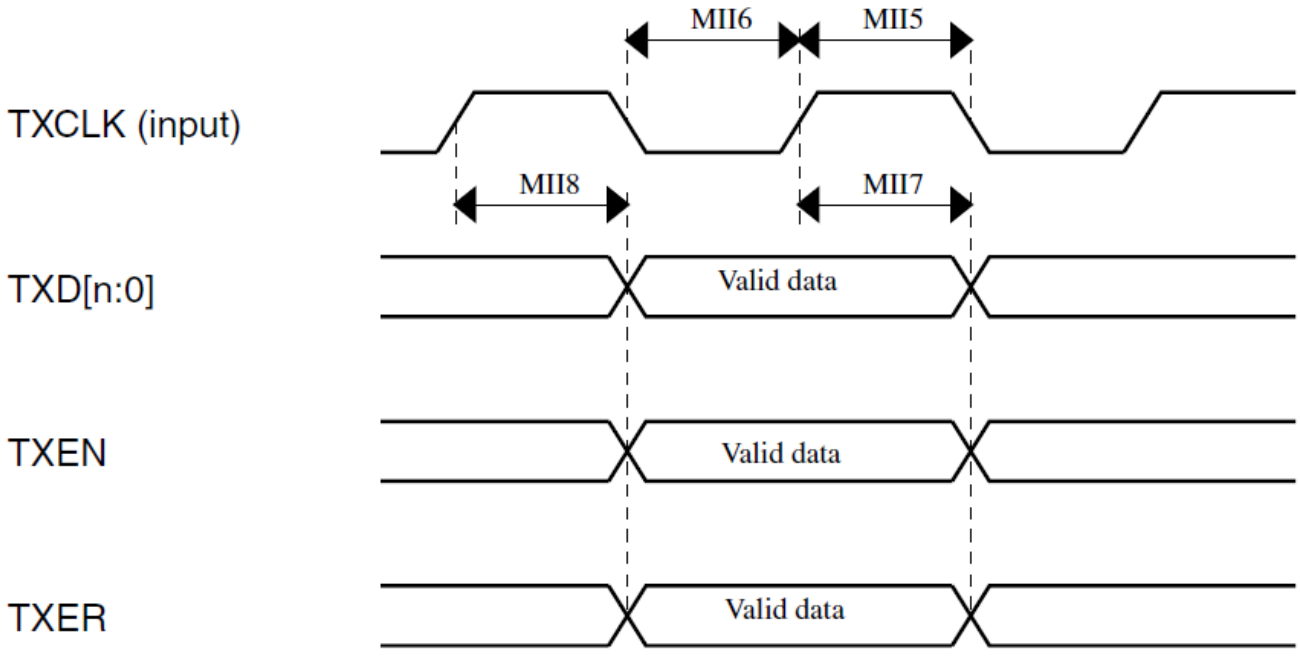


Figure 54. MII transmit diagram

12.8.2 Ethernet MII (200 Mbps)

The following timing specs are defined at the device I/O pin and must be translated appropriately to arrive at timing specs/ constraints for the physical interface. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Table 57. Ethernet MII (200 Mbps)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	RXCLK frequency	—	—	50	MHz	—	—
MII1	RXCLK pulse width high	35	—	65	% RXCLK period	—	—
MII2	RXCLK pulse width low	35	—	65	% RXCLK period	—	—
MII3	RXD[3:0], RXDV, RXER to RXCLK setup time	4	—	—	ns	—	—
MII4	RXCLK to RXD[3:0], RXDV, RXER hold time	2	—	—	ns	—	—
—	TXCLK frequency	—	—	50	MHz	—	—

Table continues on the next page...

Table 57. Ethernet MII (200 Mbps)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
MII5	TXCLK pulse width high	35	—	65	% TXCLK period	—	—
MII6	TXCLK pulse width low	35	—	65	% TXCLK period	—	—
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	—	ns	—	—
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	—	15	ns	Applies to all S32K3xx except S32K389	—
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	—	16	ns	Applies to S32K389	—

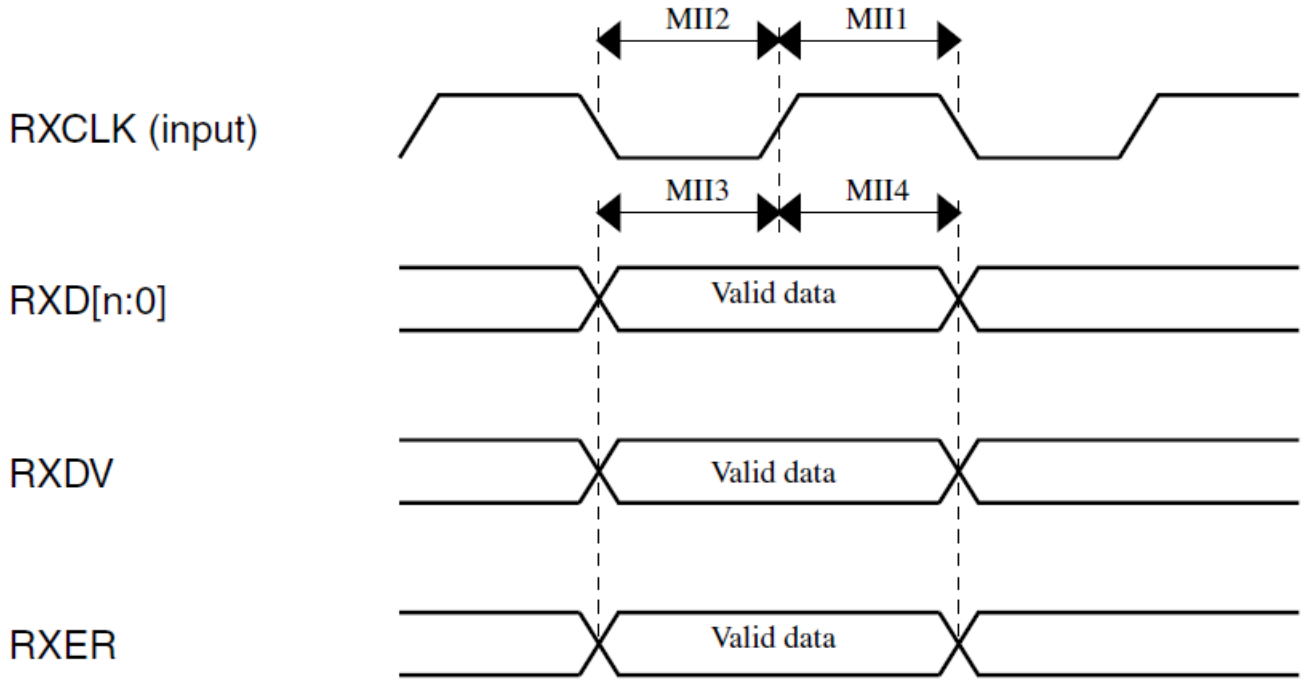


Figure 55. MII receive diagram

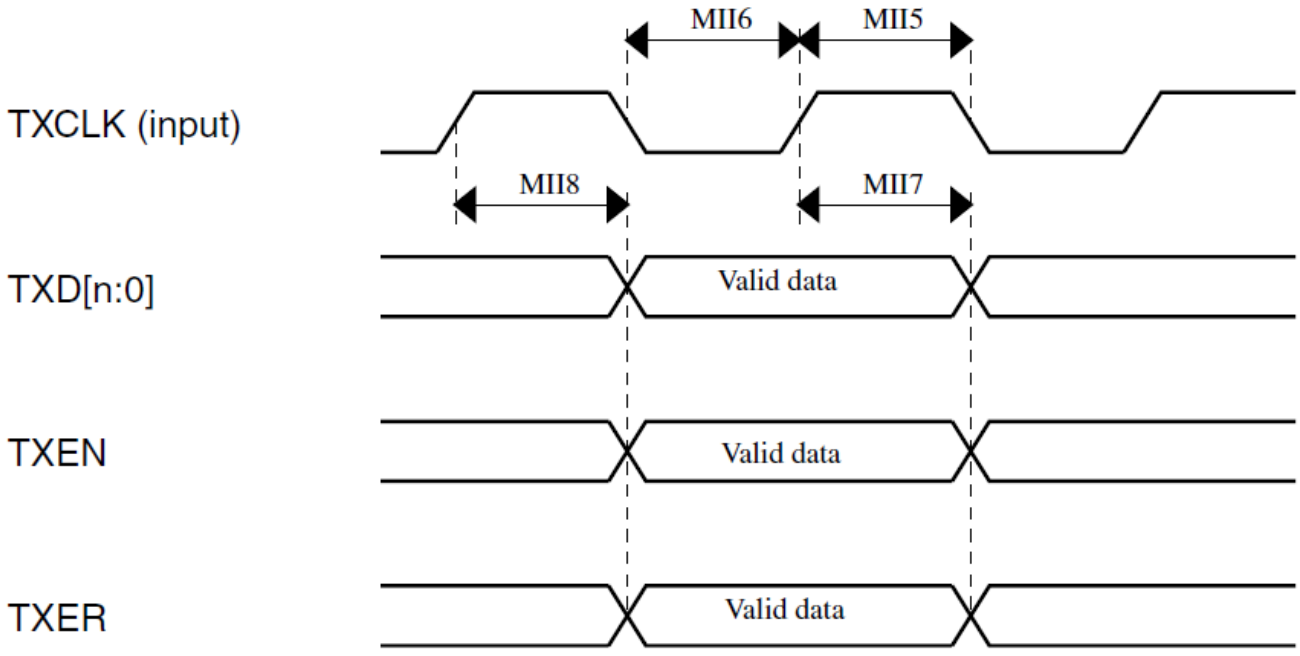


Figure 56. MII transmit diagram

12.8.3 Ethernet RMII (10/100 Mbps)

The following timing specs are defined at the device I/O pin and must be translated appropriately to arrive at timing specs/ constraints for the physical interface. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Table 58. Ethernet RMII (10/100 Mbps)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	RMII input clock frequency (RMII_CLK)	—	—	50	MHz	10/100 Mbps	—
RMII1,RMII5	RMII_CLK pulse width high	35	—	65	%RMII_CLK period	—	—
RMII2,RMII6	RMII_CLK pulse width low	35	—	65	%RMII_CLK period	—	—
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	—	ns	—	—
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	—	ns	—	—

Table continues on the next page...

Table 58. Ethernet RMII (10/100 Mbps)*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
RMII8	RMII_CLK to TXD[1:0], TXEN data valid	—	—	15	ns	—	—
RMII7	RMII_CLK to TXD[1:0], TXEN data invalid	2	—	—	ns	—	—

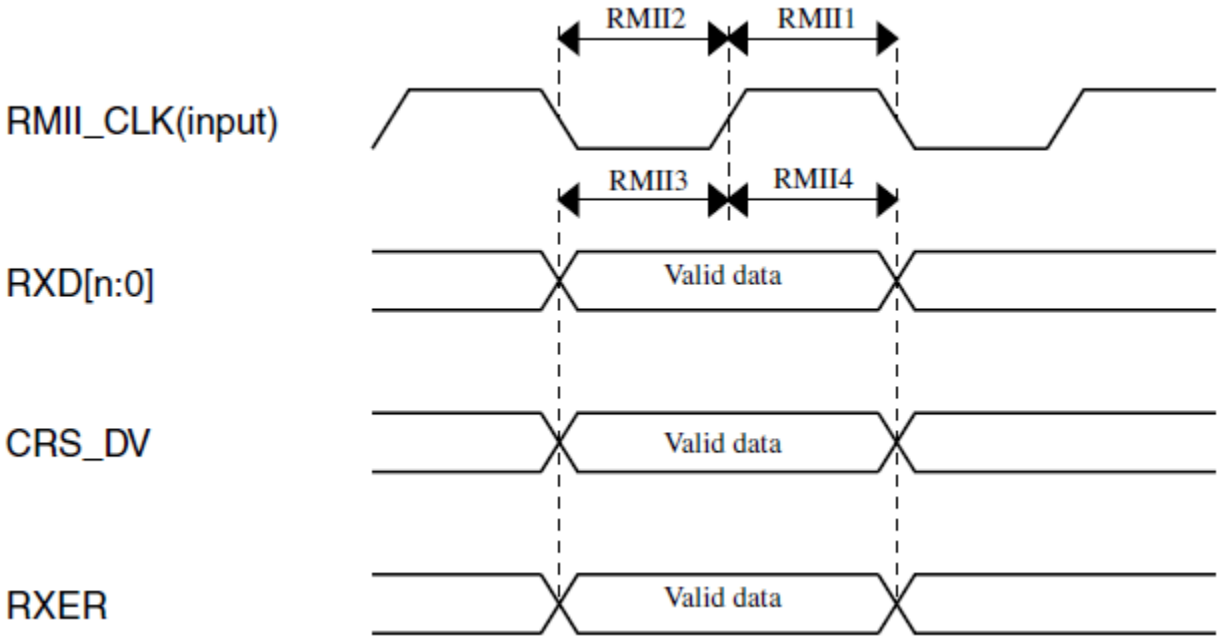


Figure 57. RMII receive diagram

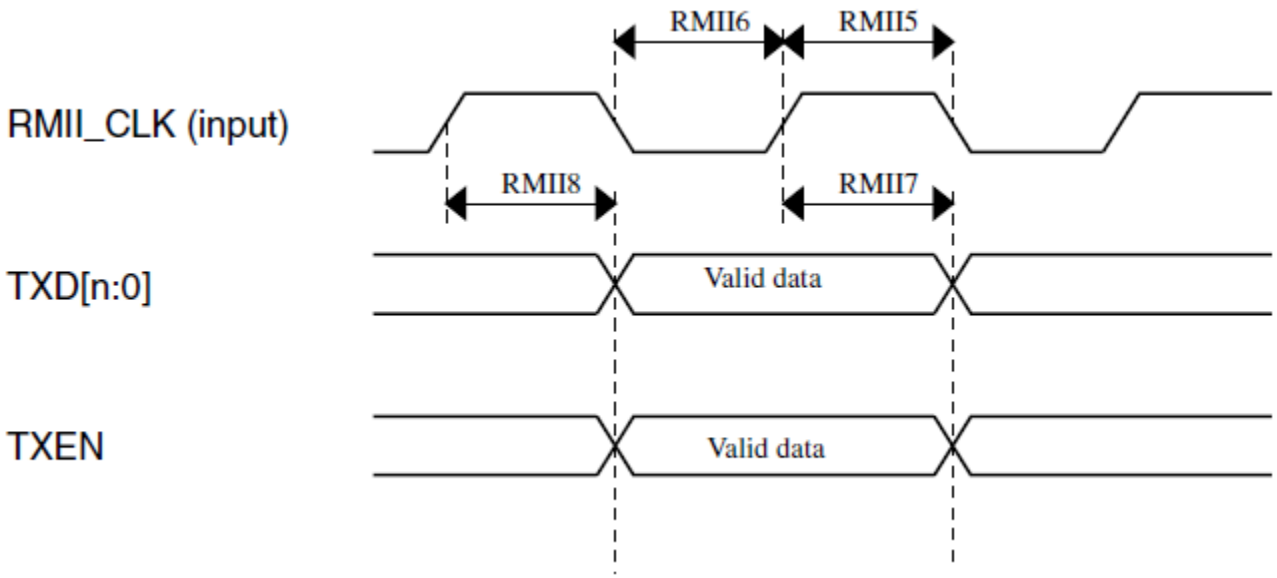


Figure 58. RMII transmit diagram

12.8.4 Ethernet RGMII

The following timing specs are defined at the device I/O pin and must be translated appropriately to arrive at timing specs/ constraints for the physical interface. Measurements are with maximum output load of 13.5pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Table 59. Ethernet RGMII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tcyc	Clock cycle duration [1][2]	7.2	—	8.8	ns	SRC = 0	—
TskewT	Data to clock output skew (at transmitter) [2]	-500	—	500	ps	SRC=0	—
TskewRi	Data to clock input skew (at receiver) [2]	1	—	2.6	ns	SRC=0	—
TskewRo	Data to clock output skew (at receiver) [2]	-650	—	650	ps	SRC=0	—
Duty_G	Clock duty cycle for Gigabit [2]	45	—	55	%	SRC=0	—
Duty_T	Clock duty cycle for 10/100T [2]	40	—	60	%	SRC=0	—
Tr	Output rise time [3]	—	—	1	ns	SRC=0	—
Tf	Output fall time [3]	—	—	1	ns	SRC=0	—

[1] For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

[2] RGMII timing specifications is valid for 3.3V nominal I/O pad supply voltage.
[3] Output timing valid for maximum external load CL = 13.5 pF (includes PCB trace, package trace (around 2pF) and flash input load).

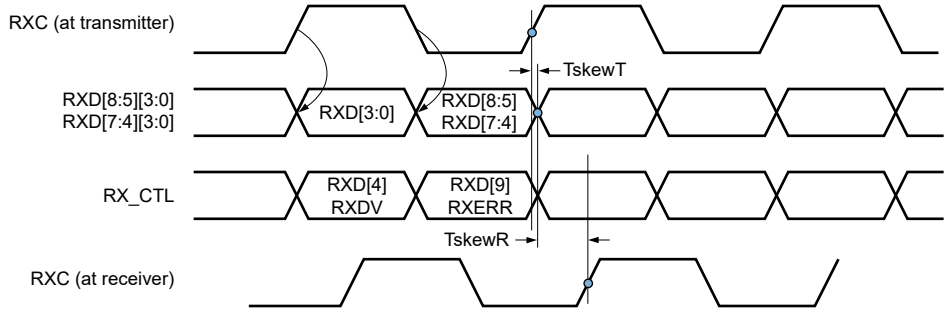


Figure 59. RGMII Receive Timing

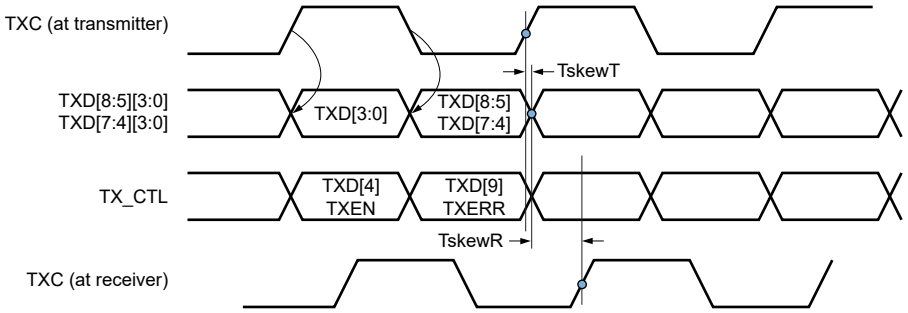


Figure 60. RGMII Transmit Timing

12.8.5 MDIO timing specifications

The following table describes the MDIO electrical characteristics. Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1 and SRE = 1’b0). I/O operating voltage ranges from 2.97 V to 3.63 V. MDIO pin must have external Pull-up.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Table 60. MDIO timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	MDC clock frequency	—	—	2.5	MHz	—	—
MDC1	MDC pulse width high	40	—	60	%MDC period	—	MDC1
MDC2	MDC pulse width low	40	—	60	%MDC period	—	MDC2
MDC5	MDC falling edge to MDIO output valid(maximum propagation delay)	—	—	25	ns	—	MDC5
MDC6	MDC falling edge to MDIO output	-10	—	—	ns	—	MDC6

Table continues on the next page...

Table 60. MDIO timing specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	invalid(minimum propagation delay)						
MDC3	MDIO (input) to MDC rising edge setup time	25	—	—	ns	Applies to S32K3x4, S32K342, S32K341, S32K322, S32K328, S32K338, S32K348, S32K356, S32K358 and all GPIO pads of S32K388 except GPIO[113]	MDC3
MDC3	MDIO (input) to MDC rising edge setup time	29.5	—	—	ns	Applies to GPIO[113] pad of S32K388	MDC3
MDC4	MDIO (input) to MDC rising edge hold time	0	—	—	ns	—	MDC4

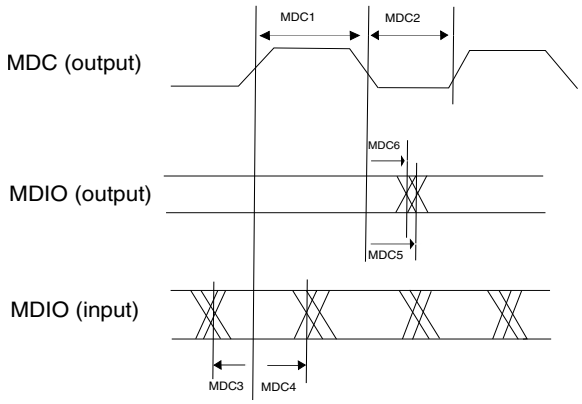


Figure 61. MII/RMII serial management channel timing

12.9 QuadSPI

12.9.1 QuadSPI Quad 3.3V SDR 120MHz

The following table applies to S32K344, S32K324, S32K314, S32K342, S32K341, S32K322, S32K328, S32K338, S32K348, and S32K358.

The following table describes the QuadSPI electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pads configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97V to 3.63V. QuadSPI trace length should be less than or equal to 2 inches. For Single and Dual IO modes of operation if external device doesn't have pull-up feature, then external pull-up must be added at board level for unused device pins. With external pull-up, performance of the interface may degrade in Quad IO mode based on load associated with external pull-up. QuadSPI support delay chain upto length 16, wherein delay length of low-frequency segment is 16 and length of high-frequency segment is 0. See the device Reference Manual for register and bit descriptions.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux

Program register value QuadSPI_FLSHCR[TCSS] = 4`h3.

Program register value QuadSPI_FLSHCR[TCSH] = 4`h3.

Program register value QuadSPI_DLLCRA[SLV_FINE_OFFSET] to 4'b0001.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 61. QuadSPI Quad 3.3V SDR 120MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1]	—	—	120	MHz	Pad Loopback	—
fSCK	SCK clock frequency [1]	—	—	60	MHz	Internal Loopback	—
tSCK	SCK clock period	1/fSCK	—	—	ns	Pad Loopback	—
tSCK	SCK clock period	1/fSCK	—	—	ns	Internal Loopback	—
tSDC	SCK duty cycle [2]	45	—	55	%	Internal Loopback	—
tSDC	SCK duty cycle [2]	45	—	55	%	Pad Loopback	—
tIS	Data input setup time	1.75	—	—	ns	Pad Loopback	—
tIS	Data input setup time	9	—	—	ns	Internal Loopback	—
tIH	Data input hold time	1	—	—	ns	Pad Loopback	—
tIH	Data input hold time	1	—	—	ns	Internal Loopback	—
tOV	Data output valid time	—	—	1.75	ns	Pad Loopback	—
tOV	Data output valid time	—	—	1.75	ns	Internal Loopback	—
tIV	Data output invalid time	-1.5	—	—	ns	Pad Loopback	—
tIV	Data output invalid time	-1.5	—	—	ns	Internal Loopback	—
tCSSCK	CS to SCK time	5	—	—	ns	Pad Loopback	—
tCSSCK	CS to SCK time	5	—	—	ns	Internal Loopback	—
tSCKCS	SCK to CS time	3	—	—	ns	Pad Loopback	—
tSCKCS	SCK to CS time	3	—	—	ns	Internal Loopback	—

[1] This frequency specification is valid only if output valid time of external flash is ≤ 5.5ns, and if output valid time of external flash is more than 5.5ns but ≤ 6.5ns, then maximum fSCK is 104MHz.

[2] For S32K342 100HDQFP, tSDC spec would be 44%-56% when ENET and SAI active along with QuadSPI at 120MHZ

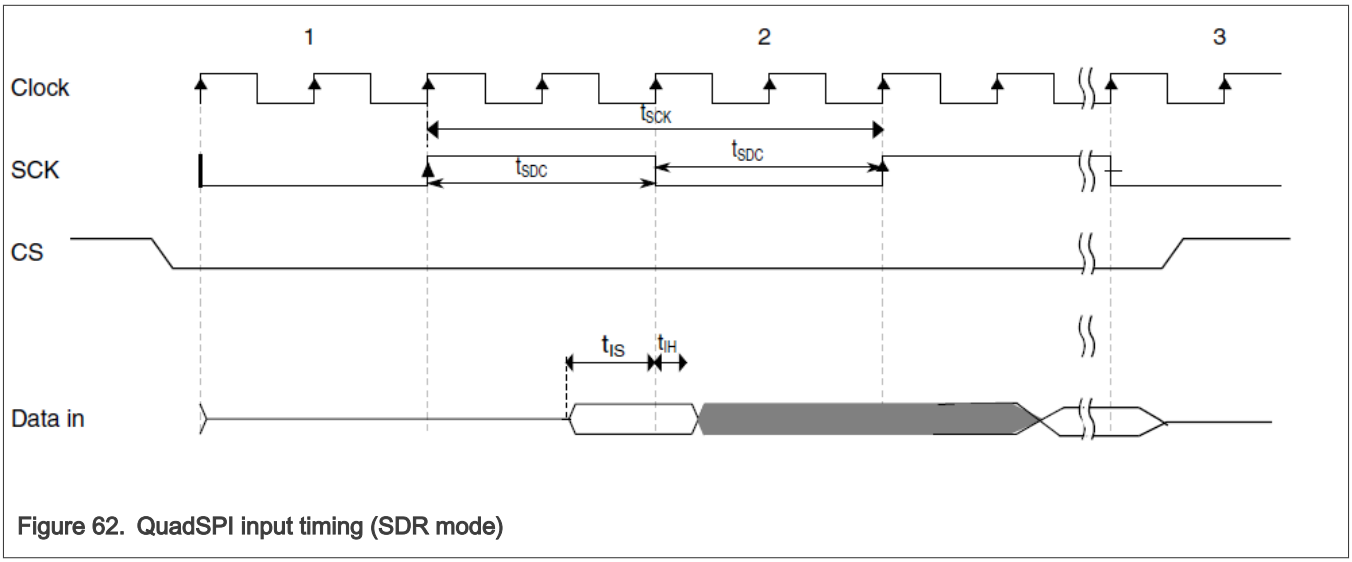


Figure 62. QuadSPI input timing (SDR mode)

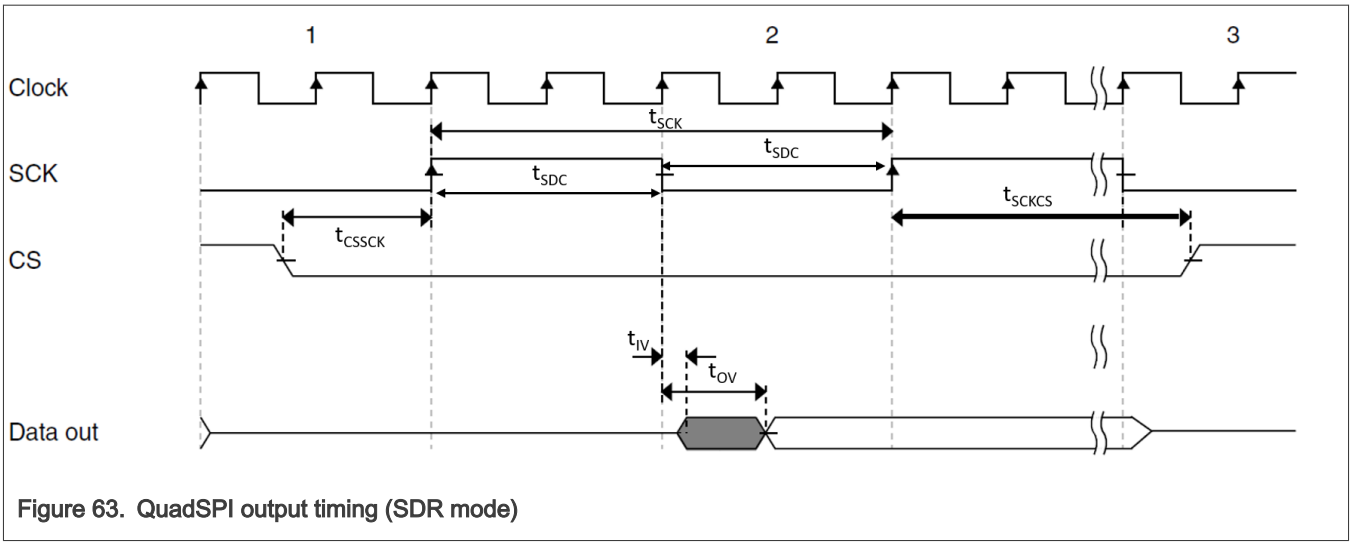


Figure 63. QuadSPI output timing (SDR mode)

12.9.2 QuadSPI Octal 3.3V DDR 100MHz

The following table applies to S32K328, S32K338, S32K348, S32K356, S32K358.

The following table describes the QuadSPI electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pads configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97V to 3.63V. QuadSPI trace length should be less than or equal to 2 inches. For Single and Dual IO modes of operation if external device doesn't have pull-up feature, then external pull-up must be added at board level for unused device pins. With external pull-up, performance of the interface may degrade in Quad IO mode based on load associated with external pull-up. QuadSPI support delay chain upto length 16, wherein delay length of low-frequency segment is 16 and length of high-frequency segment is 0. See the device Reference Manual for register and bit descriptions.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Set FLSHCR[TCSS]=2 and FLSHCR[TCSH]=5.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 62. QuadSPI Octal 3.3V DDR 100MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK_DQS	SCK / DQS frequency [1]	—	—	100	MHz	—	—
tSDC	SCK duty cycle	45	—	55	%	—	—
tCL_SCK_DQS	SCK / DQS low time [1]	4.500	—	—	ns	—	—
tCH_SCK_DQS	SCK / DQS high time [1]	4.500	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK)	1.016	—	3.484	ns	—	—
tOD_CSL	CS low to clock high	8.516	—	—	ns	—	—
tOD_CSH	Clock low to CS high	8.516	—	—	ns	—	—
tDVW	Input data valid window [1]	3.284	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.816	—	—	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	3.684	—	—	ns	—	—

[1] Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.

12.9.3 QuadSPI Quad 3.3V SDR 103.33MHz

The following table applies only to S32K388 and S32K389.

The following table describes the QuadSPI electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pads configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97V to 3.63V. QuadSPI trace length should be less than or equal to 2 inches. For Single and Dual IO modes of operation if external device doesn't have pull-up feature, then external pull-up must be added at board level for unused device pins. With external pull-up, performance of the interface may degrade in Quad IO mode based on load associated with external pull-up. QuadSPI support delay chain upto length 16, wherein delay length of low-frequency segment is 16 and length of high-frequency segment is 0. See the device Reference Manual for register and bit descriptions.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 63. QuadSPI Quad 3.3V SDR 103.33MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency	—	—	103.33	MHz	—	—
tCL_SCK	SCK clock low time [1]	4.327	—	—	ns	—	—

Table continues on the next page...

Table 63. QuadSPI Quad 3.3V SDR 103.33MHz*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCH_SCK	SCK clock high time [1]	4.327	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK)	-2.330	—	2.880	ns	—	—
tOD_CSL	CS low to clock high	8.516	—	—	ns	—	—
tOD_CSH	Clock low to CS high	8.516	—	—	ns	—	—
tDVW	Input data valid window [1]	5.5	—	—	ns	—	—
tISU_SCK	Input setup time (w.r.t. SCK) [1]	2.152	—	—	ns	—	—
tIH_SCK	Input hold time (w.r.t. SCK) [1]	2.0	—	—	ns	—	—

[1] Input timing assumes maximum input signal transition of 1ns (20%/80%).

12.9.4 QuadSPI Octal 3.3V DDR 120MHz

The following table applies to S32K328, S32K338, S32K348, S32K356, S32K358.

The following table describes the QuadSPI electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pads configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97V to 3.63V. QuadSPI trace length should be less than or equal to 2 inches. For Single and Dual IO modes of operation if external device doesn't have pull-up feature, then external pull-up must be added at board level for unused device pins. With external pull-up, performance of the interface may degrade in Quad IO mode based on load associated with external pull-up. QuadSPI support delay chain upto length 16, wherein delay length of low-frequency segment is 16 and length of high-frequency segment is 0. See the device Reference Manual for register and bit descriptions.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Set FLSHCR[TCSS]=2 and FLSHCR[TCSH]=5.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply

Table 64. QuadSPI Octal 3.3V DDR 120MHz

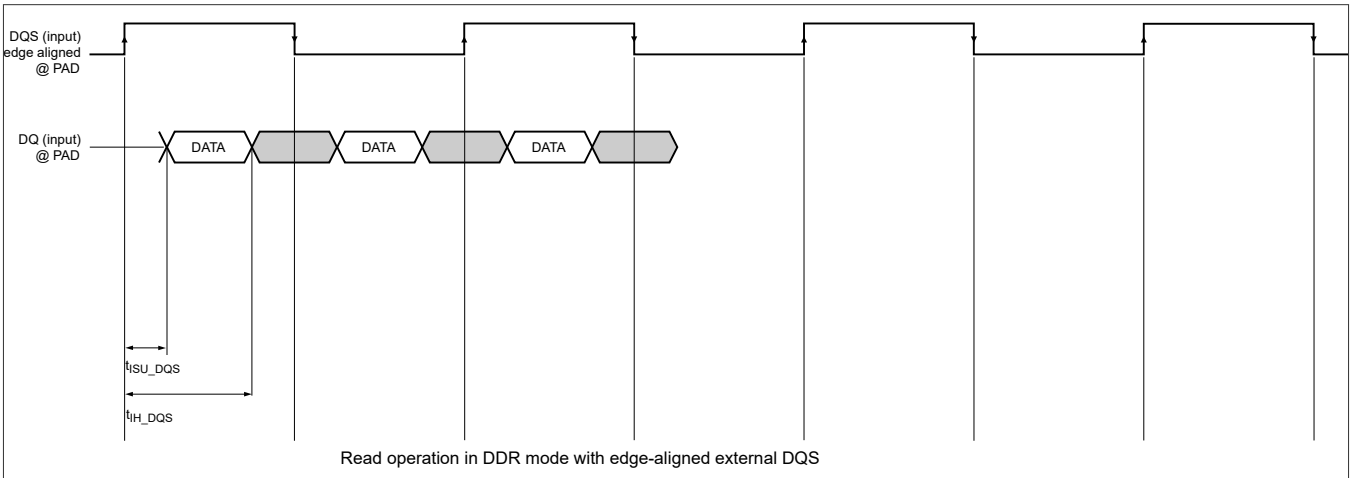
Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK_DQS	SCK / DQS frequency [1]	—	—	120	MHz	DLL enabled	—
fSCK_DQS	SCK / DQS frequency [1]	—	—	120	MHz	DLL mode enabled	—
tSCK	SCK clock period	1/ fSCK_DQS	—	—	ns	External DQS	—
tSDC	SCK / DQS duty cycle	45	—	55	%	External DQS	—

Table continues on the next page...

Table 64. QuadSPI Octal 3.3V DDR 120MHz...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCL_SCK_DQS	SCK / DQS low time [1]	3.75	—	—	ns	—	—
tCH_SCK_DQS	SCK / DQS high time [1]	3.75	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK)	0.816	—	2.934	ns	—	—
tOD_CSL	CS low to clock high	8.516	—	—	ns	—	—
tOD_CSH	Clock low to CS high	8.516	—	—	ns	—	—
tDVW	Input data valid window [1]	2.518	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.616	—	—	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	3.134	—	—	ns	—	—

[1] Input timing assumes an input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.



Read operation in DDR mode with edge-aligned external DQS

Figure 64. QuadSPI input timing (DDR mode)

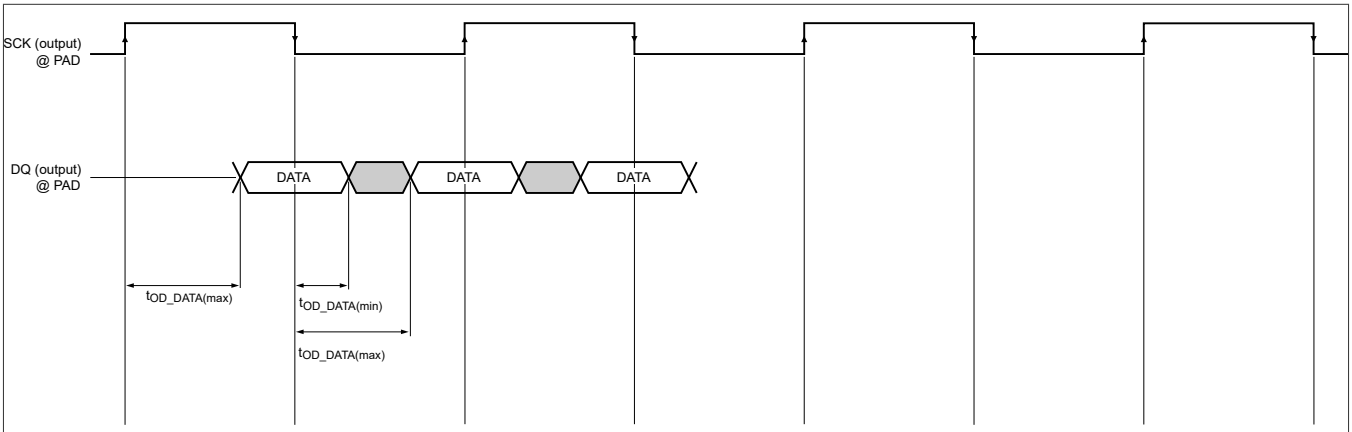


Figure 65. QuadSPI output timing (DDR mode)

12.9.5 QuadSPI Quad 3.3V SDR 125MHz

The following table applies only to S32K388 and S32K389.

The following table describes the QuadSPI electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pads configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97V to 3.63V. QuadSPI trace length should be less than or equal to 2 inches. For Single and Dual IO modes of operation if external device doesn't have pull-up feature, then external pull-up must be added at board level for unused device pins. With external pull-up, performance of the interface may degrade in Quad IO mode based on load associated with external pull-up. QuadSPI support delay chain upto length 16, wherein delay length of low-frequency segment is 16 and length of high-frequency segment is 0. See the device Reference Manual for register and bit descriptions.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 65. QuadSPI Quad 3.3V SDR 125MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1]	—	—	125	MHz	—	—
tCL_SCK	SCK clock low time [1]	3.6	—	—	ns	—	—
tCH_SCK	SCK clock high time [1]	3.6	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK)	-1.294	—	1.844	ns	—	—
tOD_CSL	CS low to clock high	8.516	—	—	ns	—	—
tOD_CSH	Clock low to CS high	8.516	—	—	ns	—	—
tDVW	Input data valid window [1]	4.724	—	—	ns	—	—

Table continues on the next page...

Table 65. QuadSPI Quad 3.3V SDR 125MHz...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tISU_SCK	Input setup time (w.r.t. SCK) [1]	1.580	—	—	ns	—	—
tIH_SCK	Input hold time (w.r.t. SCK) [1]	1.5	—	—	ns	—	—

[1] Input timing assumes maximum input signal transition of 1ns (20%/80%).

12.9.6 QuadSPI configurations

Device	S32358, S32K356, S32K348, S32K338, and S32K328		S32K342, S32K341, S32K322	S32K344, S32K324, S32K314
Frequency (MHz)	120	120	120	120
DDR/SDR	SDR	DDR	SDR	SDR
DQS alignment	Internal DQS Dummy pad loopback	External DQS, Edge Aligned	Internal DQS Dummy pad loopback	Internal DQS Dummy pad loopback
FLSHCR[TDH]	0	1	0	0
FLSHCR[TCHS]	3	3	2	2
FLSHCR[TCSS]	3	3	2	2
DLPEN[MCR]	0	0	0	0
DLLCR[DLLEN]	0	1	0	0
DLLCR[FREQEN]	0	0	0	0
DLLCR[DLL_REFCNTR]	NA	2	NA	NA
DLLCR[DLLRES]	NA	8	NA	NA
DLLCR[SLV_FINE_OFFSET]	0	0	0	0
DLLCR[SLV_DLY_OFFSET]	0	0	0	0
DLLCR[SLV_DLY_COARSE]	0	0	0	0
DLLCR[SLV_DLY_FINE]	0	1	0	0
DLLCR[SLAVE_AUTO_UPDT]	0	1	0	0
DLLCR[SLV_EN]	1	1	1	1
DLLCR[SLV_DLL_BYPASS]	1	0	1	1
DLLCR[SLV_UPD]	1[1]	1[1]	1 [1]	1[1]
SMPR[DLLFSMPF*]	0	4	5	5
SMPR[FSDLY]	0	0	0	0
SMPR[FSPHS]	1	NA	1	1

[1] Refer programming sequence in Reference Manual.

12.10 uSDHC

12.10.1 uSDHC SDR electrical specifications

The following table describes the uSDHC electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns(20%/80%) and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Data transitions measured at 25%/62.5% at 3.3V for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 66. uSDHC SDR electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fpp	Clock frequency (low speed) [1]	—	—	400	kHz	—	SD1
fpp	Clock frequency (eMMC4.4/4.41 SDR, SD3.0 SDR) [1] [2]	—	—	50	MHz	Medium/Fast Pad	SD1
fpp	Clock frequency (eMMC4.4/4.41 SDR, SD3.0 SDR) [1] [3]	—	—	25	MHz	Standard plus/Medium pad	SD1
fOD	Clock frequency (identification mode) [1]	100	—	400	kHz	—	SD1
tWL	Clock low time	6	—	—	ns	Medium/Fast pad	SD2
tWL	Clock low time	12	—	—	ns	Standard plus/Medium pad	SD2
tWH	Clock high time	6	—	—	ns	Medium/Fast pad	SD3
tWH	Clock high time	12	—	—	ns	Standard plus/Medium pad	SD3
tTLH	Clock rise time [1][4]	—	—	4	ns	Medium/Fast pad	SD4
tTLH	Clock rise time [1][4]	—	—	8	ns	Standard plus/Medium pad	SD4
tTHL	Clock fall time [1][4]	—	—	4	ns	Medium/Fast pad	SD5
tTHL	Clock fall time [1][4]	—	—	8	ns	Standard plus/Medium pad	SD5
tOD	SDHC output delay (output valid) [1]	-5.6	—	2.6	ns	fpp= 50 MHz, SDHC_CLK to SDHC_DAT	SD6

Table continues on the next page...

Table 66. uSDHC SDR electrical specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tOD	SDHC output delay (output valid) [1]	-5.6	—	10.64	ns	fpp= 25 MHz, 400 KHz, SDHC_CLK to SDHC_CMD / SDHC_DAT	SD6
tOD	SDHC output delay (output valid) [1]	-5.6	—	3.1	ns	fpp= 50 MHz, SDHC_CLK to SDHC_CMD	SD6
tISU	SDHC Input setup time	6.3	—	—	ns	fpp= 25 MHz, 400 KHz, SDHC_CMD / SDHC_DAT to SDHC_CLK	—
tISU	SDHC Input setup time	4.8	—	—	ns	fpp= 50 MHz, SDHC_CMD / SDHC_DAT to SDHC_CLK	SD7
tIH	SDHC Input hold time	2	—	—	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT	SD8

[1] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[2] In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
[3] In normal (full) speed mode for MMC card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
[4] The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.

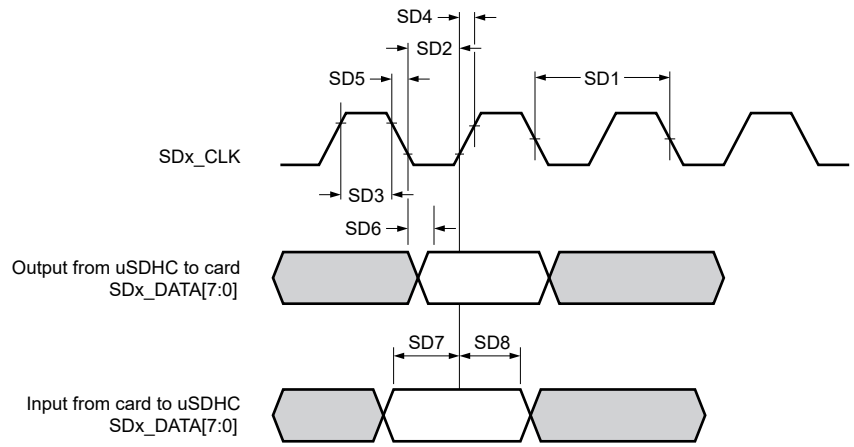


Figure 66. SD/eMMC4.3 High Speed Mode Interface Timing

12.10.2 uSDHC DDR electrical specifications

The following table describes the uSDHC electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns(20%/80%) and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Valid pin combinations to be referred from K3xx*_Use sheet in IOmux.

Data transitions measured at 25%/62.5% at 3.3V for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 67. uSDHC DDR electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fpp	Clock frequency (eMMC4.4/4.41 DDR) [1]	—	—	50	MHz	Medium/Fast pad	SD1
tWL	Clock low time	6	—	—	ns	Medium/Fast pad	—
tWH	Clock high time	6	—	—	ns	Medium/Fast pad	—
tTLH	Clock rise time [1][2]	—	—	4	ns	Medium/Fast pad	SD9
tTHL	Clock fall time [1][2]	—	—	4	ns	Medium/Fast pad	SD10
tOD	SDHC output delay (output valid) [1]	2.7	—	6.53	ns	SDHC_CLK to SDHC_DAT	SD2
tOD	SDHC output delay (output valid) [1]	-5.6	—	2.6	ns	SDHC_CLK to SDHC_CMD	SD6 (See SDR figure)
tISU	SDHC Input setup time	1.6	—	—	ns	SDHC_DAT to SDHC_CLK	SD3
tISU	SDHC Input setup time	4.8	—	—	ns	SDHC_CMD to SDHC_CLK	SD7 (See SDR figure)
tIH	SDHC Input hold time	1.5	—	—	ns	SDHC_CLK to SDHC_DAT	SD4
tIH	SDHC Input hold time	1.5	—	—	ns	SDHC_CLK to SDHC_CMD	SD8 (See SDR figure)

[1] Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
[2] The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.

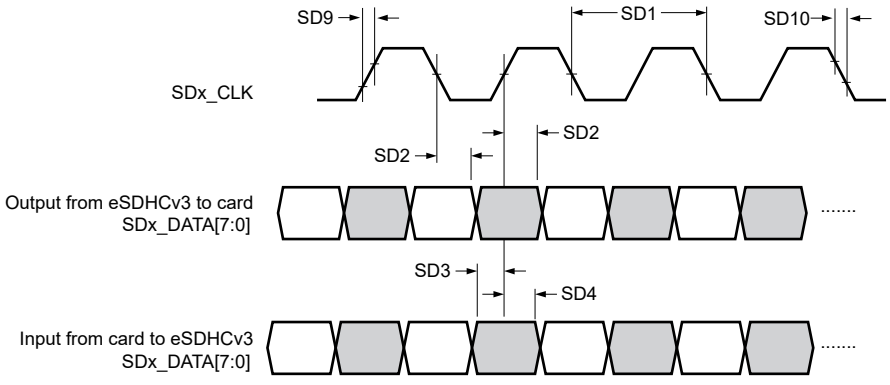


Figure 67. SD/eMMC4.4/4.41 DDR50 Mode Interface Timing

12.11 LPUART specifications

See I/O parameters for LPUART specifications.

13 Debug modules

13.1 Debug trace timing specifications

The following table describes the Debug trace electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 68. Debug trace timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fTRACE	Trace clock frequency (trace on Fast pads)	—	—	120	MHz	Applies to all K3xx variants except S32K388 and S32K389	—
fTRACE	Trace clock frequency (trace on Fast pads)	—	—	125	MHz	Applies to S32K388 and S32K389	—
fTRACE	Trace clock frequency (trace on StandardPlus pads)	—	—	25	MHz	—	—
tDVW	Data output valid window	1.2	—	—	ns	—	—
tDIV	Data output invalid	0.3	—	—	ns	—	—

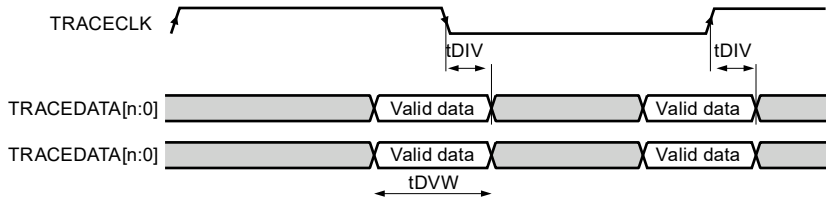


Figure 68. Trace CLKOUT specifications

13.2 SWD electrical specifications

The following table describes the SWD electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 69. SWD electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SWD_CLK frequency	—	—	33	MHz	—	S1

Table continues on the next page...

Table 69. SWD electrical specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S2	SWD_CLK cycle period	1 / S1	—	—	ns	—	S2
S3	SWD_CLK pulse width	40	—	60	%	—	S3
S4	SWD_CLK rise and fall times	—	—	1	ns	—	S4
S9	SWD_DIO input data setup time to SWD_CLK rise	5	—	—	ns	—	S9
S10	SWD_DIO input data hold time after SWD_CLK rising edge	5	—	—	ns	—	S10
S11	SWD_CLK high to SWD_DIO output data valid	—	—	22	ns	—	S11
S12	SWD_CLK high to SWD_DIO output data hi-Z	—	—	22	ns	—	S12
S13	SWD_CLK high to SWD_DIO output data invalid	0	—	—	ns	—	S13

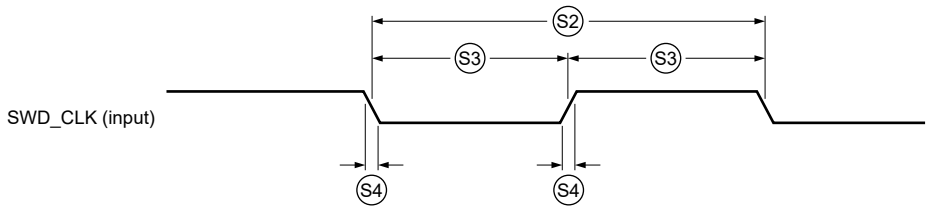


Figure 69. SWD Input Clock Timing

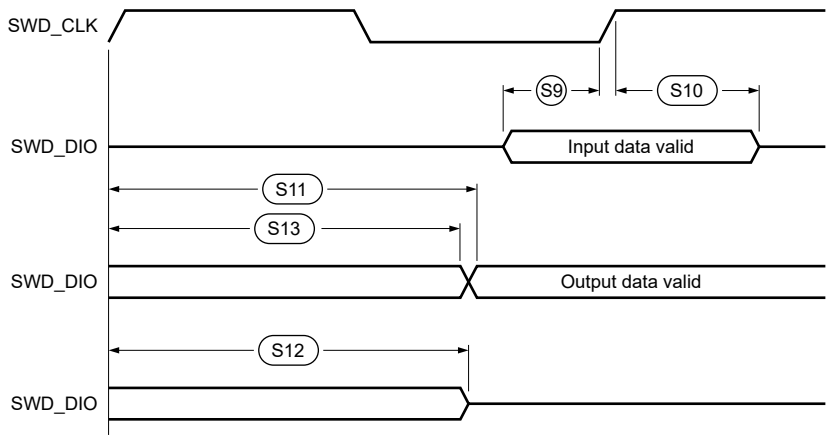


Figure 70. SWD Output Data Timing

13.3 JTAG electrical specifications

The following table describes the JTAG electrical characteristics. These specifications apply to JTAG and boundary scan. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 70. JTAG electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tJCYC	TCK cycle time [1][2]	30	—	—	ns	—	1
tJDC	TCK clock pulse width	40	—	60	%	—	2
tTCKRISE	TCK rise/fall times (40%-70%)	—	—	1	ns	—	3
tTMSS, tTDIS	TMS, TDI data setup time	5	—	—	ns	—	4
tTMSH, tTDIH	TMS, TDI data hold time	5	—	—	ns	—	5
tTDOV	TCK low to TDO data valid [3]	—	—	22	ns	—	6
tTDOI	TCK low to TDO data invalid	0	—	—	ns	—	7
tTDOHZ	TCK low to TDO high impedance	—	—	22	ns	—	8
tBSDV	TCK falling edge to output valid [4]	—	—	600	ns	—	11
tBSDVZ	TCK falling edge to output valid out of high impedance	—	—	600	ns	—	12

Table continues on the next page...

Table 70. JTAG electrical specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tBSDHZ	TCK falling edge to output high impedance	—	—	600	ns	—	13
tBSDST	Boundary scan input valid to TCK rising edge	15	—	—	ns	—	14
tBSDHT	TCK rising edge to boundary scan input invalid	15	—	—	ns	—	15

[1] This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
[2] Cycle time is 30ns assuming full cycle timing. Cycle time is 60ns assuming half cycle timing.
[3] Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
[4] Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

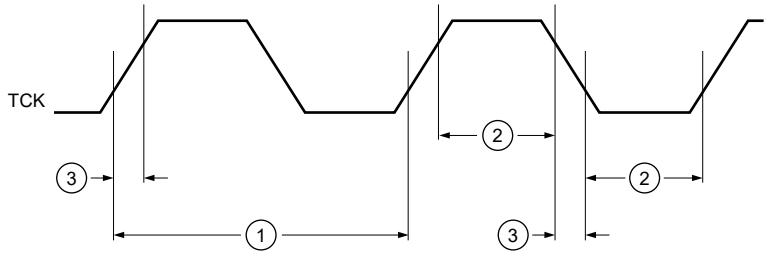


Figure 71. JTAG TCK Input Timing

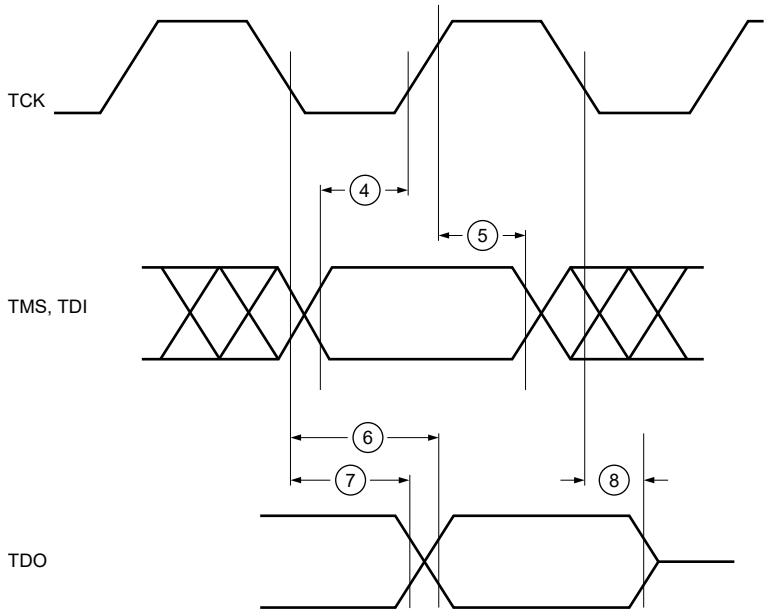


Figure 72. JTAG Test Access Port Timing

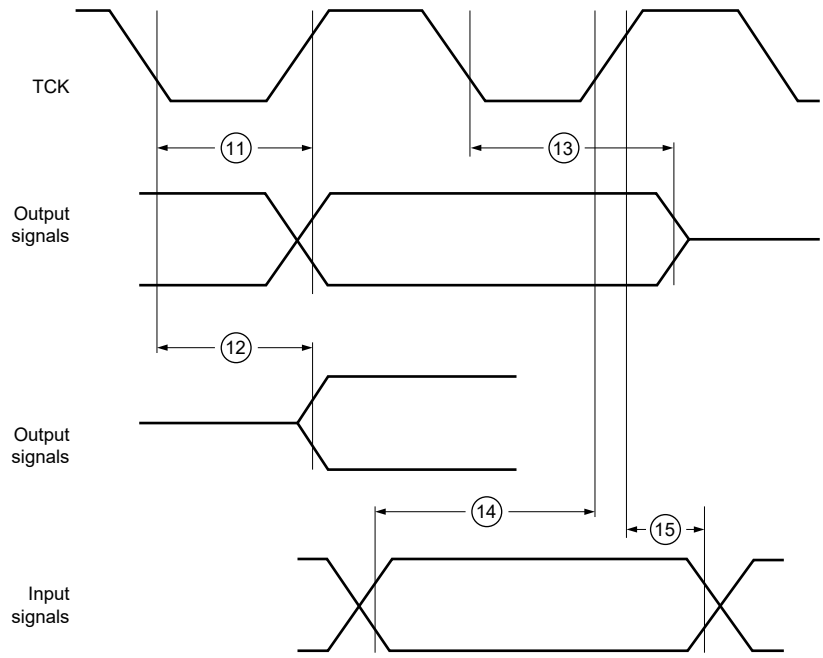


Figure 73. Boundary Scan Timing

14 Thermal Attributes

14.1 Description

The tables in the following sections describe the thermal characteristics of the device.

Note: *Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.*

14.2 Thermal characteristics

Thermal Design and Characteristics

- Junction temperature of the device does not solely depend on package thermal resistance but is also a function of chip power dissipation, PCB attributes, environmental conditions (ambient temperature & air flow) and cumulative effects of other heat generating ICs on the PCB.
- The appropriate thermal design must be carried out on package so that it can safely dissipate the necessary amount of power needed for it to function properly without exceeding the maximum junction temperature. This may involve adding a cooling solution on the package, creating thermal enhancements on the PCB and improving environmental conditions.
- The customer is encouraged to use the package model to perform design and risk assessment through simulations. Package models in FloTHERM or Icepak formats can be obtained under NDA from the sales team.

Thermal Ratings

- The table below is the package thermal ratings for LQFP, HDQFP & MAPBGA package variants. These numbers are derived through simulations based on standardized tests as described in the footnotes.
- Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment :

Thermal TIM considerations

For high-end applications using S32K38x, a robust thermal design is required for the increased system power dissipation, especially when operating in a high ambient temperature environment. Passive thermal management techniques by enhancing conduction and natural convection provide a cost effective solution.

Including a Thermal Interface material (TIIM) between the MCU and the enclosure is recommended to improve the heat transfer efficiency between the MCU and the enclosure, to help ensure the operating temperature of the device is within specifications.

Ensure that the efficiency of the TIM element will be limited by the heat spreading capability of the system enclosure. Additionally, these same TIM recommendations apply for the Last Mile Regulator (LMR) (MOSFET).

The recommended dimension for the TIM should be the same as the selected MOSFET and the thickness of 1.5 mm (whose thermal conductivity is in range to internal thermal simulations 2.4 – 6.5 W/m-k).

Table 71. Thermal values at enclosure and 105C at ambient temperature

Parameter	Value	Unit	Condition
Increase temperature of the MCU in the enclosure[1][2][3]	35	C	TIM 2.4 W/m-k
	33		TIM 6.5 W/m-k
Expected temperature in the enclosure[2][3]	<125	C	

[1] The simulation is based on a worst case scenario where the MCU is consuming 2.34W.
[2] The results could vary according with the design and thermal considerations added to the layout, for the simulation a HIGH-END board of 10 layer board and dimensions of 95 x 165 x 1.6 mm^3 were taken as a reference based on several customer use cases.
[3] A plastic enclosure with aluminum baseplate was used for simulation, the case dimension was 100 x 175 x 30 mm^3 with a thickness of 1.2mm

Table 72. Thermal characteristics

Rating	Conditions	Symbol	Package	Device							Unit
				S32K311 S32K310	S32K312	S32K342 S32K341 S32K322	S32K344 S32K314 S32K324	S32K358 S32K356 S32K348 S32K328 S32K338	S32K388	S32K389	
Thermal resistance, Junction to Ambient (Natural Convection)[1]	Four-layer board (2s2p)[2]	$R_{\Theta JA}$	48-LQFP	45	NA	NA	NA	NA	NA	NA	°C/W
			100-LQFP	NA	TBD	NA	TBD	NA	NA	NA	°C/W
			100-HDQFP	35.3	38	33.8	NA	NA	NA	NA	°C/W
			172-HDQFP	NA	30.5	29.6	28.9	NA	NA	NA	°C/W
			257-MAPBGA	NA	NA	NA	26.8	NA	NA	NA	°C/W
			172 HDQFP_EP	NA	NA	NA	NA	15.6	NA	NA	°C/W
			289-MAPBGA	NA	NA	NA	NA	20.9	20.4	NA	°C/W
			437-BGA	NA	NA	NA	NA	NA	NA	20.5	°C/W
Thermal characterization parameter, Junction-to-Top of package[1]	Natural Convection	Ψ_{JT}	48-LQFP	2	NA	NA	NA	NA	NA	NA	°C/W
			100-LQFP	NA	TBD	NA	TBD	NA	NA	NA	°C/W
			100-HDQFP	0.66	0.8	0.5	NA	NA	NA	NA	°C/W
			172-HDQFP	NA	0.5	0.5	0.4	NA	NA	NA	°C/W
			257-MAPBGA	NA	NA	NA	0.3	NA	NA	NA	°C/W
			172 HDQFP_EP	NA	NA	NA	NA	0.3	NA	NA	°C/W
			289-MAPBGA	NA	NA	NA	NA	0.4	0.4	NA	°C/W
			437-BGA	NA	NA	NA	NA	NA	NA	0.7	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment

[2] Thermal test board meets JEDEC specification for this package (JESD51-9).

15 Dimensions

15.1 Obtaining package dimensions

Package dimensions are provided in the package drawings. To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

Package option	Document Number
48-pin LQFP	98ASH00962A
100-pin LQFP	98ASS23308W
257-ball MAPBGA	98ASA01483D
172-pin HDQFP	98ASA01107D
100-pin HDQFP	98ASA01570D
172-pin HDQFP_EP	98ASA01667D
289-ball MAPBGA	98ASA01216D
437-BGA	98ASA01918D

16 Revision history

The following table lists the changes in this document.

Document ID	Release date	Description
S32K3XX v.13	12 November 2025	• In Features updated "120-bit Unique Identification (ID) number" to "64-bit Unique Identification (ID) number". • In "Feature comparision", added support for 100-LQFP for S32K312 and S32K344. • In "Ordering information": — Updated MaxQFP and MaxQFP-EL to HDQFP and HDQFP-EP — Added package suffix letter 100-LQFP as LL. — Added "N" character in Product status for ordering and marking • In section "Recommended Decoupling Capacitors", "COUT_V11" is added for S32K389 as 22uF. • In PMIC, added pointer to NXP. • In section "Low Power Comparator (LPCMP)", footnote updated "For devices where the VDD_HV_B domain is present, …..". • In section "PLL":

Table continues on the next page...

Document ID	Release date	Description
		— updated leading sentence to correct the mantioned parts, ""FPLL_DS, FPLL_FM and all fractional mode jitter specifications are not applicable to..." — for Symbol "FPLL_out" Max changed from "320" to "500" and added a footnote as "The PLL output frequency must be configu...". • Added 100-LQFP row in thermal characteristics and added package drawing number in "Obtaining package dimentions". • Removed the footnote "6.0 V maximum for 10 hours over lifetime; 7.0 V maximum for 60 seconds over lifetime." from first two V15 symbols in Absolute Maximum ratings • Added footnote to Bandgap reference voltage spec in Supply monitoring table • Updated 289BGA package decoupling capacitor pinout diagram for S32K388 and added 437BGA package decoupling capacitor pinout diagram for S32K389. • Added Supply current values for S32K389 • Added Note "To improve the FXOSC & PLL jitter performance in S32K389, the functionality of the pins (namely - PTE3, PTD15, PTE8, PTE4, PTG6, PTG0 and PMOS_CTRL in BGA437 package) cannot be toggling edge-aligned" after FXOSC section • Added Solder temperature specifications and associated footnote in Absolute Maximum Ratings • Split tOD_CS into tOD_CSH and tOD_CSL in following table — QuadSPI Octal 3.3V DDR 100MHz — QuadSPI Quad 3.3V SDR 103.33MHz — QuadSPI Octal 3.3V DDR 120MHz — QuadSPI Quad 3.3V SDR 125MHz • Added QSPI input timing diagram and QSPI output timing diagram in DDR mode • Added QuadSPI configurations section

Document ID	Release date	Description
S32K3XX v.12.0	10 July 2025	• Added S32K356 variant througout the document wherever applicable. • In front page, updated sentence "M7 supports up to 320 MHz...". • Moved V15 input from "V15 regulator (BJT option, NPN ballast transistor control) electrical specifications" to "V11 regulator (NMOS ballast transistor control) electrical specifications" • Added "Recomended PMIC" section. • In "LPSPI", used inclusive terms "Controller and Peripheral" in place of "Master and Slave" at remaining places.

Document ID	Release date	Description
S32K3XX v.11	16 April 2024	• In first page added information "This document includes key information in the file attached to it. See the attachment icon in the PDF window to see the list of attachments.". • Spreadsheet attached to the pdf containing part numbers is updated. • In section features merged DMIPS for S32K388 and S32K389 and updated S32K389 frequency to 320 MHz. • Ordering information figure updated. • In section "Absolute maximum ratings", footnotes updated: — When the input pad voltage levels are close to VDD_HV_A... — If a positive injection current is present in one or more I/O pins when... • Updated section title name from "Voltage and current operating requirements" to "Operating Conditions" and added V15 current consumption for S32K388/89. • In section "Power mode transition operating behavior", Symbol "tMODE_ STDBYEXIT_FAST" • In section "Recommended Decoupling Capacitors", for Symbol "CDEC" Min "70" deleted and Typ changed from "100" to "100 or 220". • In section "Recommended Decoupling Capacitors", updated diagrams for 437MAPBGA. — Updated the quantity of caps of VDD_HV_A, VDD_HV_B and V11 in SMPS mode. — Added VDD_DCDC connected to VDD_HV_B in non-SMPS mode. • In section "Recommended Decoupling Capacitors", for Symbol "CBULK" Typ changed from "4.7" to "4.7 or 10". • In section "Recommended Decoupling Capacitors", updated diagrams for 437MAPBGA. — Updated the quantity of caps of VDD_HV_A, VDD_HV_B and V11 in SMPS mode. — Added VDD_DCDC connected to VDD_HV_B in non-SMPS mode. • Updated "supply currents" and "operating mode" section to include changes for S32K389 at 320 MHz. • In section "V11 regulator (NMOS ballast transistor control) electrical specifications" added ILKG_NMOS. • In section "Flash memory read timing parameters", updated "Flash Frequency" to "Flash Frequency (CORE_CLK)" • In section "Temperature Sensor", this footnote is moved to top of table as generic sentence "The temperature sensor measures the junction temperature Tj ... • In section "PLL", for Symbol "FPLL_out" Max changed from "480" to "320". • In "LPSPI", used inclusive terms "Controller and Peripheral" in place of "Master and Slave".

Table continues on the next page...

Document ID	Release date	Description
		• In "SAI", used inclusive terms "Controller and Target" in place of "Master and Slave". • In section "Ethernet MII (200 Mbps)", for Symbol ""MII7" and "MII8" changed TXDV to TXEN. • In section "Ethernet MII (200 Mbps)", for Symbol "MII8" added new value for S32K389. • In section "Thermal characteristics" added TIM information and added S32K389 thermal data. • Removed "See I/O parameters for GPIO electrical specifications" in LPSPI, SWD, JTAG and Debug Trace timing Specifications. • Updated LPSPI to add updated frequency for S32K389.

Document ID	Release date	Description
S32K3XX v.11A.0	October 2024	• In "Feature Comparison" updated values for "ASIL-B DMIPS, ASIL-D DMIPS, ASIL-B CoreMark and ASIL-D CoreMark" • Updated the example in figure. "Ordering Information" • Updated chapter "Supply current" and also added table "Example RUN mode configuration supply currents for S32K389" • In section "Operating Mode", added table "RUN mode configuration options for S32K389" • In GPIO, added spec "VHYS_50" and "VHYS_33" for S32K389 device. • In section "FXOSC", update the typ. value of spec GM to 14.04. • Updated table "LPSPI1, LPSPI3 and LPSPI4 for S32K389" • Updated section name to "Communication between two S32K38x devices" and "Timing specification for S32K38x to S32K38x communication" • Added document number for 437-BGA in section "Obtaining package dimensions" • In table. "usdhc DDR electrical specifications", added spec number for clock rise time and fall time. Also mentioend in figure. • Added S32K39 part numbers in the attached "Part number List"

Document ID	Release date	Description
S32K3XX v.10.0	July 2024	• Updated front matter, from "Upto 128K of flexible program" to "Upto 256KB of flexible program" • In "Absolute Max Ratings" updated footnote from "…. the voltage in the respective I/O power domain (VDD_HV_A or VDD_HV_B) would increase …." to "…voltage in the respective I/O power domain (VDD_HV_A or VDD_HV_B) would increase and may cause damage to the MCU. It is recommended to.."

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Document ID	Release date	Description
		• In "S32K328" and "S32K348" block diagrams, updated the instances of FlexCAN to 8. • Updated Part number nomenclature diagram. • In "Power mode transition operating behavious", removed Fast Recovery from description of "tMODE_STDBYEXIT" for S32K388 and S32K389. • Updated table. "HSE Firmware memory verification time examples". • In "289BGA package decoupling cap pinout digram(S32K388)", added CBULK capacitor, to H8. • In section "V15 regulator(SMPS option)", updated the footnote from "Only needed..." to "Highly Recommended..." • Added C_{BULK_SMPS} in fig "SMPS circuit" • In "V11 regulator (NMOS ballast transistor control) electrical specifications", updated the Typ value of V11 to 1.14V. • In Supply current added values for S32K388. • In table. Run mode configuration options, updated footnote from EMAC to EMAC/GMAC • In GPIO DC electrical specifications, updated spec "VHSYS_33" and added footnote " Hysteresis spec does not apply to fast pad" • In PLL, for spec "FPLL_out" updated the Max value to 480 MHz. • In section "FXOSC": — Updated the Max value of CLKIN_VIL_EXTAL_BYPASS and Min value of CLKIN_VIH_EXTAL_BYPASS and added new footnote "For bypass mode application, the EXTAL..." — Added new note "To improve the FXOSC & PLL jitter performance in S32K388, the functionality of the pins (namely -PTG0, PTG2, PTG3, PTF30, PTE12, PTA2..." specifically for S32K388. • In LPSPI : — Added new spec "tV" and "tHO" specifically for S32K389 — Updated the desciption of tA to "MISO valid time after SS assertion" and its reference in figure. • Added new table ""LPSPI1, LPSPI3 and LPSPI4 for S32K389. • In uSDHC SDR and DDR electrical specifications sections, updated the footnote "Öutput timing valid for maximum external load CL= 25pF(includes PCB trace.…)" • In section "V15 regulator (SMPS option) electrical specifications", added devices S32K388 and S32K389. • In "FXOSC", added information "In single ended bypass mode, the XTAL pin can be left unconnected". • Added CBULK capacitors for SMPS figures in Decoupling capacitor figures.

Table continues on the next page...

Document ID	Release date	Description
		• In Table. "Thermal characteristics", added values for S32K388. • Updated the attached Part Number sheet. • Added information "See I/O parameters for GPIO electrical specifications" in LPSPI, SWD, JTAG and Debug Trace timing Specifications.

Document ID	Release date	Description
S32K3XX v.10A.0	March 2024	• Updated front matter as below : — Added package : 437BGA — Program flash memory to 12MB — SRAM with ECC to 2304 KB — HMI upto 320 GPIO Pins — FlexCAN modules to 12 • Added block diagram for S32K389 • Added information for S32K389 device throught the data sheet.

Document ID	Release date	Description
S32K3XX v.9.1	March 2024	• In table "LPSPI5 and LPSPI0 20MHz combination for S32K388", updated the instances of LPSPI2 to LPSPI5. • In "GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)", updated conditions for "FMAX_33_F" mentioning it for specific devices.

Document ID	Release date	Description
S32K3XX v.9.0	January 2024	• In "features", updated "Up to 512 KB SRAM with ECC, includes 192 KB" to "Up to 1152 KB SRAM with ECC, includes 384 KB". • Updated "feature comparison". • Updated the DMIPS values in the Table of Features to align with the footnotes. • In Absolute Max Ratings : — Updated footnote "When the input pad voltage levels are close to VDD_HV_A (respectively to VDD_HV_B)..." and referred to S32K3xx hardware design guidelines instead of AN. — Updated footnotes "Absolute max ratings must be..." and "When the input pad voltage levels.." — Added new footnote "If a positive injection current is present..." to spec "I_INJSUM_DC_ABS".

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Document ID	Release date	Description
		— Added "S32K388" in statement "The VDD_DCDC supply voltage is only present in certain devices.." — Updated condition for V15 and V11 spec. • In Voltage and current operating requirements : — Updated footnote "When input pad voltage levels are close to VDD_HV_A..." — Added new footnotes "Keeping the input voltage between" and "If a positive injection current is present..." — Added "S32K388" in statement "The VDD_DCDC supply voltage is only present in certain devices.." — Updated condition for V15 and V11 spec. • In "Power mode transition operating behaviour", added values for S32K3x8 devices. • In "Supply Monitoring", added footnote "The HVD_V15 monitor is provided to indicate if the V15 rail is far above the standard V15 operating range...". • In Recommneded Decoupling capacitors diagrams and SMPS Circuit updated "VDD_HV_SMPS" to "VDD_DCDC". • In Table. "V15 regulator (SMPS option) electrical specifications" added symbol "L_SMPS" for External coil inductance and "D_SMPS" for External Schottky diode average forward current. • Added IBCTL label in "Ballast circuit" figure. • In "V11 regulator (NMOS ballast transistor control) electrical specifications" added new spec "VTH_NMOS" for 5.0 V supply and updated Max value to "1.5" for VTH spec for 3.3 V supply. • In "Supply currents" section , added values for "S32K358, S32K348, S32K338, S32K328". • In RUN mode supply currents (peripherals disabled) for S32K3x8, deleted values from " Min. Config. [Clock Option A+] Triple Core @240 MHz " for S32K358, S32K348, S32K338, S32K328 variants. • In GPIO DC electrical specifications:- — Updated footnote "I/O timing specifications are valid for the un-terminated 50ohm..." and figure related to it with correct load details. — Updated the conditions for FMAX specs. • In "GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)", added spec "FMAX_33_F" with max frequency 125 MHz. • In GPIO Output AC electrical specifications, updated spec values and added new footnotes and figure. • In "GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)" and "GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)", updated the max and min values of ILKG parameters.

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Document ID	Release date	Description
		• Updated table "FIRC" mentioning FACC +/-5% for all K3xx devices. • Updating figure title to "S32K310: ASIL B Single Core 512 KB General Purpose MCU". • In "FXOSC": — Added note "To improve the FXOSC & PLL jitter performance..." — Updated the footnote "To improve the FXOSC jitter & duty cycle performance.." • In "PLL", updated min value for "FPLL_out" from 48 to 25 MHz. • In LPSPI, updated the output loads. • In "LPSPI2 and LPSPI5 20MHz combination for S32K388", added new table "LPSPI2 and LPSPI0 20MHz combination for S32K388". • In "LPSPI" — Updating min values of tLEAD/tLAG to ""tSPCK/2" for LPSPI Slave mode. — For "tWPSCK", removed "high or low" from description. — Updated information "All measurements are with maximum output load of 30pf.." at the top of the table. — Removed Rise/Fall time output specs. — Added footnotes "Output rise/fall time is determined by the output load and GPIO pad drive strength setting..." and "The input rise/fall time specification applies to both clock and data..." — Added "tV" and "tHO" spec with condition "Master Loopback, S32K388 LPSPI2 and LPSPI5 @20MHz" — For "tV" with max value "17.5" ns, updated condition to ""Master Loopback, applies to all devices LPSPI0 @20 MHz" — For "tHO" with min value "-2" ns, updated condition to ""Master Loopback, applies to all devices LPSPI0 @20 MHz" — Updated LPSPI timing diagrams with 50/50 levels. • In "LPSPI" and "Timing specification for S32K388 to S32K388", updated information from "All timing is shown with respect to 20% VDD_HV_A/B and 80% VDD_HV_A/B thresholds" to "All timing is shown with respect to 50% VDD_HV_A/B thresholds." • Added information "Valid pin combinations to be referred from K3xx*_Use sheet in IOmux." in all SAI, uSHDC, QSPI and Ethernet modes. • Added information "Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply." in all QSPI modes. • Changed footer to "Preliminary Information for S32K388" • Updated Preliminary Information for S32K388 throughout the data sheet.

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Document ID	Release date	Description
		• In "HSE Firmware memory verification time examples" table, there are some TBC's. Those will be updated in the next revision as new measurements showed different timings. There is no major performance degradation to be expected. • Added information in section "LPSPI 20 MHz and 15MHz combinations", and removed S32K344 PAD TYPE column from Table. "LPSPI 20 MHz and 15MHz combinations". • Added new section "LPSPI2 and LPSPI5 20MHz combination for S32K388". • In "Timing specification for S32K388 to S32K388", updated maximum output load from 30pF to 50pF. • In "Ethernet RGMII", updated footnote to "Output timing valid for maximum external load CL = 13.5 pF (includes PCB trace, package trace (around 2pF) and flash input load)...." • In "QuadSPI Octal 3.3V DDR 120MHz", for spec "fSCK_DQS", updated condition from "DLL and Auto-Learning mode enabled" to "DLL enabled" • In section "uSDHC SDR electrical specifications": — Updated description for "fpp" spec. — Updated condition for "tOD" with description "SDHC Output delay(Output valid)" — Added 2 rows of spec "tOD" with value "-5.6" and description ""fpp= 25 MHz, 400 KHz,..." and "fpp= 50 MHz, SDHC_ CLK to SDHC_CMD". — Updated min value for spec "tIH" to 2 ns. — Removed footnote " In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7V to 3.6V." • In "'uSDHC" modes : — Added information "Data transitions measured at 25%/62.5% at 3.3V for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply." — Removed footnote "Input timing assumes an input signal slew rate of 3ns (20%/80%)" from "uSDHC SDR electrical specifications" and "uSDHC DDR electrical specifications" table. Added input transition of 1ns (20%/80%) information to top of the table. • In section "uSDHC DDR electrical specifications", removed spec "fpp" with description "Clock frequency (SD3.0 DDR)". • In uSDHC SDR and uSDHC DDR electrical specifications updated footnote to "Output timing valid for maximum external load CL = 25 pF..."

Document ID	Release date	Description
S32K3XX v.8.1	November 2023	• Updated "supply currents" for "S32K344, S32K324, S32K314, S32K342, S32K322, S32K341 and S32K312".

Document ID	Release date	Description
S32K3XX v.8.0	June 2023	• Moved S32K311 and S32K310 to support list from preliminary and added S32K322 to supported list. • Updated frequency to 320 MHz for S32K388 mentioned in features and updated S32K388 block diagram. • In section "Thermal operating characteristics" added ambient temperature seperately for both V- and M-grade parts. • Deleted power management figures. See reference manual for these figures. • Decoupling capacitors are updated with new formats. • In section "V15 regulator (SMPS option) electrical specifications" updated the SMPS circuit figure. • In section "V11 regulator (NMOS ballast transistor control) electrical specifications" updated V11 output from 1.14 to 1.155 V. • In section "Supply currents" added current numbers for S32K311 and S32K310 and added support for 320MHz for S32K388. • In section "Supply currents" merged VDD_HV_A for S32K3x8, S32K34x, S32K32x and S32K314 and mentioned the max current. • Added table title to table in section "Cyclic wake-up current". • In section "Low Power Comparator (LPCMP)", — for symbol tDDAC updated description from "DAC Initialization and switching settling time" to "DAC Initialization time". — updated footnote attached to TDHSS and TDLSS from "Applied +/- (30 mV + 2 x VAHYST0/1/2/3 + max. of VAIO) around switch point" to "Applied +/- (30 mV + VAHYST0/1/2/3 + max. of VAIO) around switch point" • In section "Temperature Sensor" clarified that its an MCU on-die temperature sensor. • In section "FIRC" updated FACC for S32K311 and S32K310 for different temperature ranges. • In section "PLL", added sentence "Jitter values specified in this table are applicable for FXOSC reference clock input only". • In section "Fast External Oscillator (FXOSC)", added IFXOSC for ALC disabled. • In section "Slow Crystal Oscillator (SXOSC)" updated ISXOSC max from 4 to 10 uA. • In section " LPSPI" updated symbols of Data hold time (inputs) to tHI. • Updated heading of Ethernet MII and RMII to mention support of 10 and 100 Mbps. • In "uSDHC SDR electrical specifications" updated conditions for the supported pads. • In "uSDHC DDR electrical specifications" updated conditions for the supported pads and deleted 25 MHz specifications. • Updated $R_{\Theta JA}$ for 172HDQFP_EP to 15.6 °C/W.

Document ID	Release date	Description
S32K3XX v.7.0	April 2023	• Updated caution in overview and updated feature comparison. • In "S32K3xx chip's feature comparison" section clarified via footnote that S32K388 supports QuadSPI SDR modes only. • Updated S32K312 and S32K388 block diagram. • QFP package references updated to HDQFP. • In section "Absolute maximum ratings" added footnote to VDD_DCDC as "Voltage at VDD_DCDC cannot be higher than VDD_HV_A". • In section "Voltage and current operating requirements" added footnote to V15 as "Min and Max values are applicable only for non-SMPS mode where V15 is sourced externally". • Updated descriptions and condition in following sections: — Boot time, HSE firmware not installed — Boot time, HSE firmware installed — HSE firmware memory verification time examples • In section "Recommended Decoupling Capacitors" updated variants for COUT V11. • In section "V15 regulator (SMPS option) electrical specifications" added CBULK_SMPS. • In section "V15 regulator (BJT option, NPN ballast transistor control) electrical specifications" added V15 input. • In section "SAR ADC" updated paragraph "All below specs are applicable...". and added footnote to TUE as "Spec valid if potential difference between VDD_HV_A.." and figure updated to show VDD_HV_A instead of VREFH. • In LPCMP section changed ACMP0 to LPCMP0. • In PLL added paragraph to mention Auxiliary PLL applicability and footnote updated to mention "Accumulated jitter specification is not valid with SSCG". • In PLL added CLKIN_VIL_EXTAL_BYPASS and CLKIN_VIH_EXTAL_BYPASS specifications. • Added section "Communication between two S32K388 devices". • In section "Ethernet MII (100 Mbps)" updated specification for 10 and 100 Mbps. • In section "Ethernet RGMII" added paragraph "The following timing specs are defined at the device". • In section "MDIO timing specifications" updated MDC3 for GPIO[113]pad of S32K388. • Added following QuadSPI modes for S32K388: — QuadSPI Quad 3.3V SDR 103.33MHz — QuadSPI Quad 3.3V SDR 125MHz • In QuadSPI modes, mentioned the applicability to the devices in K3 family.

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Document ID	Release date	Description
		• In "Debug trace timing specifications" section added row for 125 MHz for S32K388. • Updated "Thermal characteristics" to add information on Thermal design and characteristics.

Document ID	Release date	Description
S32K3XX v.6.0	November 2022	• Added S32K388 decoupling capacitor diagrams. • In section "Power mode transition operating behavior" tMODE_STDBYEXIT time is added as 80 us. • In "V15 regulator (SMPS option) electrical specifications" section changed V15 output supply from 1.51V to 1.5V. • In "5.0V (4.5V - 5.5V) GPIO Output AC Specification" — TR_TF_50_F with condition DSE=1, SRE=0, Capacitance=25pF changed from 0.9 to 1.9 ns. — TR_TF_50_F with condition DSE=0, SRE=0, Capacitance=50pF changed from 5.3 to 6.0 ns. — TR_TF_50_F with condition DSE=0, SRE=1, Capacitance=50pF changed from 7.7 to 9.0 ns. — TR_TF_50_F with condition DSE=1, SRE=1, Capacitance=50pF changed from 5.1 to 6.5 ns. • In "3.3V (2.97V - 3.63V) GPIO Output AC Specification" — TR_TF_33_F with condition DSE=0, SRE=0, Capacitance=25pF changed from 4 to 4.5 ns. — TR_TF_33_F with condition DSE=1, SRE=0, Capacitance=25pF changed from 2 to 2.5 ns. — TR_TF_33_F with condition DSE=0, SRE=0, Capacitance=50pF changed from 7 to 8 ns. • In section "Fast External Oscillator (FXOSC)" added EXTAL_SWING_PP and VSB specs and related footnote.

Document ID	Release date	Description
S32K3XX v.5.2	October 2022	• Added S32K310 and S32K388 where applicable. • Updated "overview". • In "features": — Updated M7 support upto 300 MHz. — Updated Ethernet instance from one to two.

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Document ID	Release date	Description
		— Added Support to AES accelerator(for K388 only) — Removed I3C instances. • Added S32K310 and S32K388 block diagram and updated others to remove I3C. • Updated "Feature comparison". • Updated "Ordering information". • In "Absolute maximum ratings": — Added symbol "V15" as "Voltage sensing input" for S32K388 and changed max value to 2.75V for S32K358. — Added symbol "V11" for S32K388. • In "Voltage and current operating requirements": — Added symbol "V15" as "Voltage sensing input" for S32K388 and updated conditions for V15 and V15_extended. Also added a footnote to V15_extended as You must ensure that the junction temperature"...". — Added symbol "V11" for S32K388. — Updated link to download hardware design guidelines document. • In section "Thermal operating characteristics" added sentence as "For S32K388, applications running at 125°C Tamb.....". • Added S32K388 power management diagram and added other variants to diagrams as applicable. • In section "Power mode transition operating behavior, added condition for tMODE_STDBYEXIT_FAST as "FIRC ON @48MHz in Standby mode". • In section "Supply monitoring" added sentence as "Certain monitors are present on certain...". • In section "Recommended Decoupling Capacitors" added COUT_V11 for S32K388 and updated decoupling capacitor diagrams. • Section "SMPS regulator electrical specifications" changed to "V15 regulator (SMPS option) electrical specifications" and following changes done: — Added paragraphs at the begining of table as: ◦ "Some devices (S32K358, S32K348, S32K338, and S32K328)...." ◦ "The table below describes the electrical parameters for the components needed to implement an SMPS...." ◦ Updated existing to include inductor "The chip hardware design guidelines document lists the recommended...". ◦ Added figure, removed redundant sentence "The table below describes the electrical parameters.." and updated part numbers. — Added "External Schottky diode average forward current" as 2A.

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Document ID	Release date	Description
		— Added "External P-channel MOSFET threshold voltage" as 2V. • Section "NPN Ballast Transistor Control Specification" renamed to "V15 regulator (BJT option, NPN ballast transistor control) electrical specifications" and updated the following: — added paragraph "Some devices (S32K358, S32K348, S32K338, S32K328, S32K344, S32K324, S32K314, S32K342, S32K322, S32K341) support ...." — Updated ballast circuit figure. • Added section "V11 regulator (NMOS ballast transistor control) electrical specifications". • In section "Supply currents": — added template for S32K388. — added values for S32K342. — added S32K310 along with S32K311. • GMAC term is added along with EMAC in "Operating mode" section. • Updated GPIO specs to clarify leakage specifications. • In SAR ADC section, removed TBD from RS max specification. • In section "SXOSC", Oscillator Analog circuit supply current max updated to 4 uA. • In section "LPSPI", updated tV and tHO for S32K358 and a note is added as "15 and 20 Mbps is supported on LPSPI0 only.". • In section "uSDHC SDR electrical specifications" relaxed tISU for 25 MHz and 400 KHz from 4.8 to 6.3 ns. • Deleted I3C specifications • Updated "Thermal characteristics" • Added 48-pin LQFP package drawing number in "Obtaining package dimensions" section. • Editorial updates.

Document ID	Release date	Description
S32K3XX v.4.0	April 2022	• Removed S32K312 from preliminary list from the title of the document and "Overview". • In features on first page added MAPBGA289 to the package list and updated GPIO pins upto 235. • Removed "NDA required" term from all block diagrams. • In "Ordering information", added HDQFP-EP package suffix.

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Document ID	Release date	Description
		• In section "Absolute maximum ratings", and "Voltage and current operating requirements", added S32K341 variant to the sentence "The VDD_HV_B and V15 voltage supply domains are only present....". • In section “Voltage and current operation requirement”, the footnote attached to supply ramp rate is updated as “ The MCU Supply ramp applicable to the MCU input/external supplies...". • Updated capacitor symbol to non-polarity in following figures at V25 and V11: — Power management system - S32K344, S32K324, S32K341, S32K314, S32K342, and S32K322. — Power management system - S32K312, S32K311 • In "Power management system - S32K358" figure, updated connections to optional circuit with dashed lines for PGATE_CTRL and VSS_DCDC. • In section “SMPS regulator electrical specifications”, added a sentence “The chip hardware design guidelines documents lists the recommended part numbers of PMOS & Schottky diode." • In table "SMPS regulator electrical specifications" : — The typ. value of "External coil inductance" changed from 5 to 4.7uH. — Added “Schottky diode reverse voltage” with Min value 5.0 V. — Added “Schottky diode forward current” with Min value 1.0 A. • In section "SMPS regulator electrical specifications" changed "COUT_V15" to "COUT_V15_SMPS" to match it with corresponding figure. • In section "Recommended Decoupling Capacitors" changed "COUT_V15" to "COUT_V15_NPN" to match it with corresponding figure. • In section "Recommended Decoupling Capacitors", following footnotes updated: — Footnote attached to CDEC "Optionally, 1 nF capacitors can be added...". — Footnote attached to CBULK "For devices where the VDD_HV_B domain is present, if the VDD_HV_B...". — Added footnote to CBULK "These capacitors must be placed close to the source." • In section "Recommended Decoupling Capacitors", updated and added decoupling capacitors diagrams. • In section "NPN Ballast Transistor Control Specification" added specification for VDD_HV_NPN. • Updated "Ballast circuit" figure under section " NPN Ballast Transistor Control Specification". • Current IDD specs are updated for S32K12 for following : — Table “STANDBY mode supply currents” — Table “Low speed RUN mode supply currents”

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Document ID	Release date	Description
		— Table “RUN mode supply currents (peripherals disabled)” — Table “Example RUN mode configuration supply current” • In section “supply current”, Removed table “Recommended current limits in board design” and related sentence “The power supplies for the voltage ....” • In section “Power management”, added section ”Cyclic wake-up current” and removed table "Low-power, cyclic operation mode" from supply currents. • In section "GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)",with symbol "ILKG_33_S", the condition has been changed from PTC0 to PTD0. • In section "5.0V (4.5V - 5.5V) GPIO Output AC Specification": — for Symbol "TR_TF_50_F" with condition "DSE=0, SRE=1, Capacitance=50pF" Min changed from "2.8" to "1.9". — for Symbol "TR_TF_50_F" with condition "DSE=0, SRE=1, Capacitance=50pF" Max changed from "10.2" to "7.7". — for Symbol "TR_TF_50_F" with condition "DSE=1, SRE=1, Capacitance=50pF" Min changed from "1.9" to "1.3". — for Symbol "TR_TF_50_F" with condition "DSE=1, SRE=1, Capacitance=50pF" Max changed from "6.7" to "5.1". — for Symbol "TR_TF_50_F" with condition "DSE=0, SRE=0, Capacitance=50pF" Min changed from "2.0" to "1.0". — for Symbol "TR_TF_50_F" with condition "DSE=0, SRE=0, Capacitance=50pF" Max changed from "7.4" to "5.3". — for Symbol "TR_TF_50_F" with condition "DSE=1, SRE=0, Capacitance=25pF" Min changed from "0.9" to "0.3". — for Symbol "TR_TF_50_F" with condition "DSE=1, SRE=0, Capacitance=25pF" Max changed from "3.0" to "0.9". — for Symbol "TR_TF_50_F" with condition "DSE=1, SRE=1, Capacitance=25pF" Min changed from "1.3" to "0.9". — for Symbol "TR_TF_50_F" with condition "DSE=1, SRE=1, Capacitance=25pF" Max changed from "5.1" to "4.1". — for Symbol "TR_TF_50_F" with condition "DSE=1, SRE=0, Capacitance=50pF" Min changed from "1.6" to "0.9". — for Symbol "TR_TF_50_F" with condition "DSE=1, SRE=0, Capacitance=50pF" Max changed from "3.6" to "3.0". — for Symbol "TR_TF_50_F" with condition "DSE=0, SRE=0, Capacitance=25pF" Min changed from "1.0" to "0.4". — for Symbol "TR_TF_50_F" with condition "DSE=0, SRE=0, Capacitance=25pF" Max changed from "5.3" to "3.1". — for Symbol "TR_TF_50_F" with condition "DSE=0, SRE=1, Capacitance=25pF" Min changed from "1.9" to "1.5".

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Document ID	Release date	Description
		— for Symbol "TR_TF_50_F" with condition "DSE=0, SRE=1, Capacitance=25pF" Max changed from "7.7" to "6.1". • In section “SAR ADC“, the footnote attached to “ADC Total Unadjusted Error” is updated as “TUE spec for precision and standard channels is based on 12-bit level resolution”. • In section "Supply Diagnosis", for Symbol "AN_ACC" and "AN_T_on" footnote added "These specs will have degraded performan..." • In section "Fast External Oscillator (FXOSC)", for Symbol "TFXOSC" description changed from "Fxosc start up time" to "Fxosc start up time (ALC enabled)". • In section "Fast External Oscillator (FXOSC)", removed the crystal part numbers and related information which includes following sentences, "In crystal mode NX5032GA crystal .....", " In crystal mode NX8045GB crystal …" and updated sentence "To ensure stable oscillations, FXOSC incorporates the feedback resistance internally.". • In section "LPSPI", updated the sentence updated maximum output load of 50pF to 30pF. • In section "LPSPI", footnote attached to "fperiph" is udated to mention clock name instead of frequency. "For LPSPI0 instance, max. peripheral...". • In section "I3C Push-Pull Timing Parameters for SDR Mode", Symbol "tV" and tHI are deleted. • Added section "Ethernet RGMII". • In all QuadSPI modes updated trace length from 3 inches to 2 inches. • Added "QuadSPI Octal 3.3V DDR 100MHz" mode. • Deleted "QuadSPI Quad 3.3V DDR 80MHz" mode. • In section "QuadSPI Octal 3.3V DDR 120MHz" : — For symbol “tOD_DATA”, Max. value changed from “2.567” to “ 2.934”. — For symbol “tOD_CS”, Min value has been changed from “3.015” to “3.016” and Max. value changed from “-1.33” to “-0.766”. — For symbol “tDVW”, Min value has been changed from “2.314” to “2.518”. — For symbol “tIH_DQS”, Min value has been changed from “2.767” to “3.134”. • uSDHC specifications are updated thoroughly. • In "Thermal characteristics": — Updated table header to include all variants. — For S32K312 100-HDQFP updated $R_{\Theta JA}$ from 34.8 to 38 °C/W and $R_{\Theta JT}$ from 0.6 to 0.8 °C/W. — For S32K3x4, 257MAPBGA updated $R_{\Theta JA}$ from 27 to 26.8 °C/W. • Updated Legal information.

Document ID	Release date	Description
S32K3XX v.3.0	October 2022	• Datasheet classification is updated to "Technical data" for S32K344. • In section "Supply currents" added values for 85C (typ and max) and updated 105 (max) and 125 (max) values for S32K344. • In front page features, added HDQFP172 with Exposed pad (EP) option and information on I3C. • In section "Overview", added a note "S32K3x1, S32K3x2 and S32K3x8 specific information ....". • In "Feature comparision" section added footnote to add information about HDQFP172 with Exposed pad (EP) package for S32K3x8 devices. • VDD_HV_SMPS is changed to VDD_DCDC throughout. • In section "Absolute maximum ratings", footnote attached to "I_INJSUM_DC_ABS" is exteded to add information "See application note AN4731 for...". • Figure "Power management system - S32K344, S32K324, S32K341, S32K314, S32K342, and S32K322." is updated to add COUT_V15 capacitor. • Figure "Power management system - S32K358" is updated to add COUT_V15 capacitor and optional circuit explained in the notes. • In section "SMPS regulator electrical specifications", COUT_V15 is added to "External bypass capacitor". • Figure "Package decoupling capacitor pinout diagram" is updated to show HDQFP172-EP package. • Table title "Current limit requirements for board design" is changed to "Recommended current limits in board design" and added a note as "The power supplies for the voltage rails must be...". • In section "GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)": — for ILKG_33_S updated condition to update pins which has Analog Function Count=2/3 — for ILKG_33_M updated condition to update pins which has Analog Function Count=1 — added ILKG_33_M with condition "PTE8 and PTD6" — udpdated ILKG_33, -120 nA (min) and 120 nA (max). — updated condition of IOH_*, IOL_* to add < and > symbols. — added IOHT specification. — Updated sentence "I/O current specifications are...". and removed "RMS current values are given....". • In section "GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)": — for ILKG_50_S updated condition to update pins which has Analog Function Count=2/3

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Document ID	Release date	Description
		— for ILKG_50_M updated condition to update pins which has Analog Function Count=1 — added ILKG_50_M with condition "PTE8 and PTD6" — udpdated ILKG_50, -150 nA (min) and 150 nA (max). — updated condition of IOH_*, IOL_* to add < and > symbols. — added IOHT specification. — Updated sentence "I/O current specifications are...". and removed "RMS current values are given....". • In section "5.0V (4.5V - 5.5V) GPIO Output AC Specification": — for Symbol "TR_TF_50_S" with condition "Capacitance=25pF" Min changed from "TBD" to "5" — for Symbol "TR_TF_50_S" with condition "Capacitance=25pF" Max changed from "TBD" to "21" — for Symbol "TR_TF_50_S" with condition "Capacitance=50pF" Min changed from "TBD" to "10" — for Symbol "TR_TF_50_S" with condition "Capacitance=50pF" Max changed from "TBD" to "31" — for Symbol "TR_TF_50_SP" with condition "DSE=0, Capacitance=25pF" Min changed from "5" to "3.5" — for Symbol "TR_TF_50_SP" with condition "DSE=1, Capacitance=25pF" Min changed from "2.4" to "1.2" — for Symbol "TR_TF_50_SP" with condition "DSE=0, Capacitance=50pF" Min changed from "8.9" to "7.1" — for Symbol "TR_TF_50_SP" with condition "DSE=1, Capacitance=50pF" Min changed from "4.1" to "3.4" — for Symbol "TR_TF_50_M" with condition "DSE=0, SRE=0, Capacitance=25pF" Min changed from "2.5" to "1.8" — for Symbol "TR_TF_50_M" with condition "DSE=0, SRE=1, Capacitance=25pF" Min changed from "3" to "2.5" — for Symbol "TR_TF_50_M" with condition "DSE=1, SRE=0, Capacitance=25pF" Min changed from "1" to "0.8" — for Symbol "TR_TF_50_F" with condition "DSE=0, SRE=0, Capacitance=25pF" Max changed from "4.3" to "5.3" — for Symbol "TR_TF_50_F" with condition "DSE=1, SRE=0, Capacitance=25pF" Max changed from "1.6" to "3.0" • In section "3.3V (2.97V - 3.63V) GPIO Output AC Specification": — for Symbol "TR_TF_33_S" with condition "Capacitance=25pF" Min changed from "TBD" to "6.5"

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Document ID	Release date	Description
		— for Symbol "TR_TF_33_S" with condition "Capacitance=25pF" Max changed from "TBD" to "28" — for Symbol "TR_TF_33_S" with condition "Capacitance=50pF" Min changed from "TBD" to "11" — for Symbol "TR_TF_33_S" with condition "Capacitance=50pF" Max changed from "TBD" to "43" — for Symbol "TR_TF_33_SP" with condition "DSE=0, Capacitance=25pF" Min changed from "5" to "4" — for Symbol "TR_TF_33_SP" with condition "DSE=1, Capacitance=25pF" Min changed from "2.4" to "2.0" — for Symbol "TR_TF_33_M" with condition "DSE=0, SRE=0, Capacitance=25pF" Min changed from "3.2" to "2.2" — for Symbol "TR_TF_33_M" with condition "DSE=0, SRE=1, Capacitance=25pF" Min changed from "3.8" to "3.0" — for Symbol "TR_TF_33_M" with condition "DSE=1, SRE=0, Capacitance=25pF" Min changed from "1" to "0.8" — for Symbol "TR_TF_33_F" with condition "DSE=0, SRE=0, Capacitance=25pF" Min changed from "1.1" to "0.5" — for Symbol "TR_TF_33_F" with condition "DSE=0, SRE=0, Capacitance=25pF" Max changed from "7.0" to "4" — for Symbol "TR_TF_33_F" with condition "DSE=0, SRE=1, Capacitance=25pF" Min changed from "2.6" to "2.1" — for Symbol "TR_TF_33_F" with condition "DSE=0, SRE=1, Capacitance=25pF" Max changed from "11.0" to "9" — for Symbol "TR_TF_33_F" with condition "DSE=1, SRE=0, Capacitance=25pF" Min changed from "0.8" to "0.4" — for Symbol "TR_TF_33_F" with condition "DSE=1, SRE=0, Capacitance=25pF" Max changed from "3.4" to "2" — for Symbol "TR_TF_33_F" with condition "DSE=1, SRE=1, Capacitance=25pF" Min changed from "1.5" to "1.2" — for Symbol "TR_TF_33_F" with condition "DSE=1, SRE=1, Capacitance=25pF" Max changed from "7.8" to "6.4" — for Symbol "TR_TF_33_F" with condition "DSE=0, SRE=0, Capacitance=50pF" Min changed from "2.5" to "1.1" — for Symbol "TR_TF_33_F" with condition "DSE=0, SRE=0, Capacitance=50pF" Max changed from "10.8" to "7" — for Symbol "TR_TF_33_F" with condition "DSE=0, SRE=1, Capacitance=50pF" Min changed from "3.6" to "2.6" — for Symbol "TR_TF_33_F" with condition "DSE=0, SRE=1, Capacitance=50pF" Max changed from "15.0" to "11"

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Document ID	Release date	Description
		— for Symbol "TR_TF_33_F" with condition "DSE=1, SRE=0, Capacitance=50pF" Min changed from "1.5" to "0.8" — for Symbol "TR_TF_33_F" with condition "DSE=1, SRE=0, Capacitance=50pF" Max changed from "5.5" to "4.2" — for Symbol "TR_TF_33_F" with condition "DSE=1, SRE=1, Capacitance=50pF" Min changed from "2.2" to "1.5" — for Symbol "TR_TF_33_F" with condition "DSE=1, SRE=1, Capacitance=50pF" Max changed from "10.0" to "7.8" • In section "SAR ADC", added paragraph "All below specs are applicable when only one ADC instance is in operation ..... to determine the most appropriate settings for AVGS." and removed footnote from RS specification. • In section "SAR ADC", added specifications for CP1, CP2 and RSW1 corresponding to all channels, shared channels and precision channels. Also added the related figure. • In section "PLL", removed some non-applicable footnotes. • In section "LPSPI", added information before the table The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master....". • In section "LPSPI0 20 MHz and 15 MHz Combinations", added note as "Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode." • Added "I3C" specifications. • In section "Ethernet MII (100 Mbps)", for "RXCLK frequency" typ value moved to max. • In section "Ethernet RMII", added paragraph "The following timing specs are defined at the device I/O pin and must be .....I/O operating voltage ranges from 2.97 V to 3.63 V." • In section "QuadSPI Quad 3.3V SDR 120MHz", for Symbol "tSDC" footnote added "For S32K342 100MQFP, tSDC spec would be ..." • In section "QuadSPI Quad 3.3V SDR 120MHz" added sentence "Program register value QuadSPI_DLLCRA[SLV_FINE_OFFSET] to 4'b0001.". • In section "QuadSPI Octal 3.3V DDR 120MHz", Symbol "tSCK" min is calrified, condition updated to External DQS and "tSCK" with condition Internal Loopback is deleted. • In section "QuadSPI Octal 3.3V DDR 120MHz", Symbol "tSDC" condition updated to External DQS and "tSDC" with condition Internal Loopback is deleted.. • In section "QuadSPI Octal 3.3V DDR 120MHz", specifications tISU_PCS, tIH_PCS, tCK2CKmin and tCK2CKmax are deleted.

Document ID	Release date	Description
S32K3XX v.2.0	August 2021	• Added section "Overview". • In block diagrams: — S32K311/S32K312/S32K314 removed "Scalable ARM M7 core in Lock step" and added "Single ARM M7 core". — S32K322/S32K324 removed "Scalable ARM M7 core in Lock step" and added "Two independent ARM M7 cores". • In "Absolute maximum ratings" and "Voltage and current operating requirements": — Some general footnotes are moved to top of table — VDD_HV_SMPS added footnotes • In "Voltage and current operating requirements" for VREFH extended footnote "VREFH should always be equal to...". • Updated title - Power management system - S32K344, S32K324, S32K341, S32K314, S32K342, and S32K322. • In figure "Power management system - S32K358" updated double bond to triple bond. • In section "Recommended Decoupling Capacitors" added COUT_V11 with typ as 1 uF. • Added section "Power mode transition operating behaviors" and its subsections: — Power mode transition operating behaviour — Boot time, HSE firmware not installed — Boot time, HSE firmware installed — HSE firmware memory verification time examples • Moved information from "Supply monitoring" to "Supply diagnosos" and attached it to "AN_ACC". The information is "If V15 > VDD_HV_A +100mV then..." • Updated figure "Package decoupling capacitor pinout diagram" to add 289 MapBGA • In section "Glitch Filter", added sentence ".... WKPU pins and TRGMUX inputs 60-63.". • Section "Flash memory program and erase specifications" updated thoroughly. • In section "Flash memory module life specifications" removed footnotes 1 and 2. • In section "Data retention vs program/erase cycles" added sentence before related to figure "The spec window represents qualified limits.". • In section "Flash memory AC timing specifications": — Updated register naming representation — Added footnote to t_{drcv} min as " In extreme cases (1 block configurations)...".

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Document ID	Release date	Description
		— Max updated to "50 system clock periods" for t_{aistop} • Ins ection "Flash memory read timing parameters" mantioned part numbers for each table as applicable. • >In section "SAR ADC", for Symbol "fAD_CK" added new spec and max updated to 120. • In section "FIRC", Symbol "IFIRC" is deleted. • In section "SIRC", Symbol "Ivdda" with condition "On state" is deleted. • In section "PLL", clarification added in condition column for jitter specifications. • In section "Fast External Oscillator (FXOSC)", for Symbol "FREQ_BYPASS", "TRF_BYPASS" and "CLKIN_DUTY_BYPASS" footnote added "For bypass mode applications, the EXTAL ...". • In section "Fast External Oscillator (FXOSC)", for Symbol "TFXOSC" footnote added "The startup time specification is valid ...". • In section "Fast External Oscillator (FXOSC)", Symbol "IFXOSC" specs are merged into one and description and condition updated. • In section "Fast External Oscillator (FXOSC)", added paragraph "Drive level is a crystal specification and ....". • In section "LPSPI", Symbol "tSPSCK" with condition "Slave_10Mbps" is added. • In section "LPSPI", Symbol "tSPSCK" with condition "Master_10Mbps" is added. • Updated title to mention LPSPI0 of "LPSPI0 20 MHz and 15 MHz Combinations", and updated header "20Mbps" to "20Mbps (In loopback mode only)". • In "I3C" section, added two sentences. • Updated "QuadSPI" sections. • Editorial updates.

Document ID	Release date	Description
S32K3XX v.2.B	March 2021	• Updated "block diagrams" and "Feature comparison" • Updated "Ordering information" to add 289 pagkage and removed one. • In section "Absolute maximum ratings", Symbol "VDD_HV_SMPS" is added. • In section "Absolute maximum ratings", for Symbol "I_INJPAD_DC_ABS" and "I_INJSUM_DC_ABS" footnote updated "When input pad voltage levels are close ...". • In section "Voltage and current operating requirements", Symbol "IINJSUM_DC_OP" and "IINJPAD_DC_OP" condition is updated • In section "Voltage and current operating requirements", Symbol "VDD_HV_SMPS" is added.

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Document ID	Release date	Description
		• In section "Voltage and current operating requirements", for Symbol "I_INJPAD_DC_ABS" and "I_INJSUM_DC_ABS" footnote updated "When input pad voltage levels are close ...". • In section "Power management": — "Power management system - S32K344, S32K324, S32K314" figure updated. — "Power management system - S32K312, S32K311" figure updated. — "Power management system - S32K358" figure added. • In section "Supply Monitoring", Symbol "HVD_V15" is added. • In section "Supply Monitoring", for "LVD_VDD_HV_A", symbol and description updated. • Added section "SMPS regulator electrical specifications" • In section "NPN Ballast Transistor Control Specification", fig with title "Ballast circuit" is changed. • In section "Supply currents" and "operating mode" tables are updated. • In section "GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)", fig with title "Reference Load Diagram" is changed. • In section "GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)", footnote updated "A positive value is leakage flowing into...". • In section "GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)", Symbol "ILKG_50_S_PTE13" with condition "PMC VRC_CTRL pin" is added. • In section "GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)", footnote updated "A positive value is leakage flowing into...". • In section "GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)", fig with title "Reference Load Diagram" is changed. • In section "Flash memory specification", added specs for 512KB and 2MB specifications. • In table "Flash memory AC timing specifications", taistop max updated. • Updated "Flash Read Wait State Settings" • In section "Low Power Comparator (LPCMP)", updated IDLSS typ to 17uA. • In section "Low Power Comparator (LPCMP)", updated INL and DNL. • In section "Low Power Comparator (LPCMP)", updated paragraph "For devices where the VDD_HV_B domain is present..." • In "Low Power Comparator (LPCMP)" added hysterisis plots. • In section "PLL", symbol "FPLL_out" description updated to add (PLL_PHIn_CLK) • In section "PLL", "IPLL_V25" deleted. • In section "PLL", updated jitter specifications.

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Document ID	Release date	Description
		• In section "FXOSC", updated paragraph "To improve the FXOSC jitter and duty cycle performance...". • In section "SXOSC", updated description of "ISXOSC" to Oscillator Analog circuit supply current. • In section "I2C", added paragraph "For supported baud rate ....." • Added section "I3C". • In section "FlexCAN characteristics", added paragraph "For supported baud rate ....." • Added QuadSPI DDR electrical specifications for Octal and Quad. • Added uSDHC specifications. • Updated "Thermal characteristics" and "Obtaining package dimensions"

Document ID	Release date	Description
S32K3XX v.2.A	November 2020	• Updated features to show maximum memory support up to 8 MB. • Added information for S32K341. • Updated "Block diagrams". • Updated "Feature comparision" • Updated "Thermal characterstics" to add data for S32K312 and S32K342. • Added document number for 172-pin HDQFP package in section "Obtaining package dimensions"

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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