



**THE DATASHEET OF  
LPC11E36FBD64/501E**





# LPC11E3x

32-bit ARM Cortex-M0 microcontroller; up to 128 kB flash; up to 12 kB SRAM and 4 kB EEPROM; USART

Rev. 1 — 7 November 2012

Objective data sheet

## 1. General description

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The LPC11E3x are a ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC11E3x operate at CPU frequencies of up to 50 MHz.

The peripheral complement of the LPC11E3x includes up to 128 kB of flash memory, up to 12 kB of SRAM data memory and 4 kB EEPROM, one Fast-mode Plus I<sup>2</sup>C-bus interface, one RS-485/EIA-485 USART with support for synchronous mode and smart card interface, two SSP interfaces, four general purpose counter/timers, a 10-bit ADC, and up to 54 general purpose I/O pins.

## 2. Features and benefits

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- System:
  - ◆ ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
  - ◆ ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - ◆ Non Maskable Interrupt (NMI) input selectable from several input sources.
  - ◆ System tick timer.
- Memory:
  - ◆ Up to 128 kB on-chip flash program memory with sector (4 kB) and page erase (256 byte) access.
  - ◆ 4 kB on-chip EEPROM data memory; byte erasable and byte programmable; on-chip API support.
  - ◆ 12 kB SRAM data memory.
  - ◆ 16 kB boot ROM.
  - ◆ In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
  - ◆ ROM-based 32-bit integer division routines.
- Debug options:
  - ◆ Standard JTAG (Joint Test Action Group) test interface for BSDL (Boundary Scan Description Language).
  - ◆ Serial Wire Debug.
- Digital peripherals:
  - ◆ Up to 54 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.



- ◆ Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
- ◆ Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- ◆ High-current source output driver (20 mA) on one pin.
- ◆ High-current sink driver (20 mA) on true open-drain pins.
- ◆ Four general purpose counter/timers with a total of up to 8 capture inputs and 13 match outputs.
- ◆ Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDO).
- Analog peripherals:
  - ◆ 10-bit ADC with input multiplexing among eight pins.
- Serial interfaces:
  - ◆ USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - ◆ Two SSP controllers with FIFO and multi-protocol capabilities.
  - ◆ I<sup>2</sup>C-bus interface supporting the full I<sup>2</sup>C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - ◆ Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator).
  - ◆ 12 MHz high-frequency Internal RC oscillator (IRC) that can optionally be used as a system clock.
  - ◆ Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - ◆ PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - ◆ Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - ◆ Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
  - ◆ Power profiles residing in boot ROM provide optimized performance and minimized power consumption for any given application through one simple function call.
  - ◆ Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - ◆ Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, or the watchdog interrupt.
  - ◆ Processor wake-up from Deep power-down mode using one special function pin.
  - ◆ Power-On Reset (POR).
  - ◆ Brownout detect with four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Temperature range –40 °C to +85 °C.
- Available as LQFP64, LQFP48, and HVQFN33 packages.

### 3. Applications

- Consumer peripherals
- Medical
- Handheld scanners
- Industrial control

### 4. Ordering information

Table 1. Ordering information

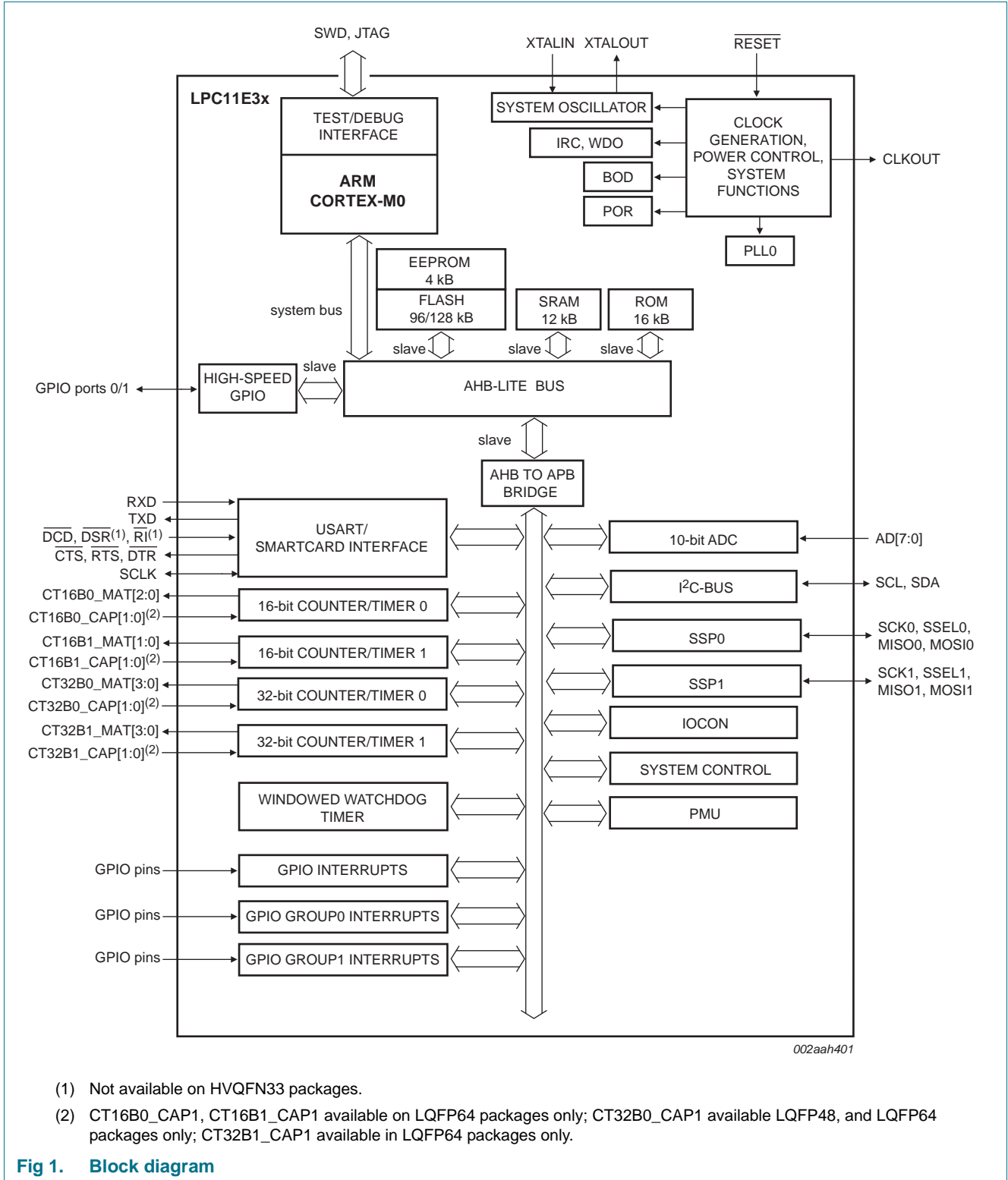
Type number	Package		
	Name	Description	Version
LPC11E36FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11E36FHN33/501	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11E37FBD48/501	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11E37FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

## 4.1 Ordering options

Table 2. Ordering options

Type number	Flash	EEPROM	Total SRAM	USART	I <sup>2</sup> C-bus FM+	SSP	ADC channels	GPIO pins
LPC11E36FBD64/501	96 kB	4 kB	12 kB	1	1	2	8	54
LPC11E36FHN33/501	96 kB	4 kB	12 kB	1	1	2	8	28
LPC11E37FBD48/501	128 kB	4 kB	12 kB	1	1	2	8	40
LPC11E37FBD64/501	128 kB	4 kB	12 kB	1	1	2	8	54

5. Block diagram

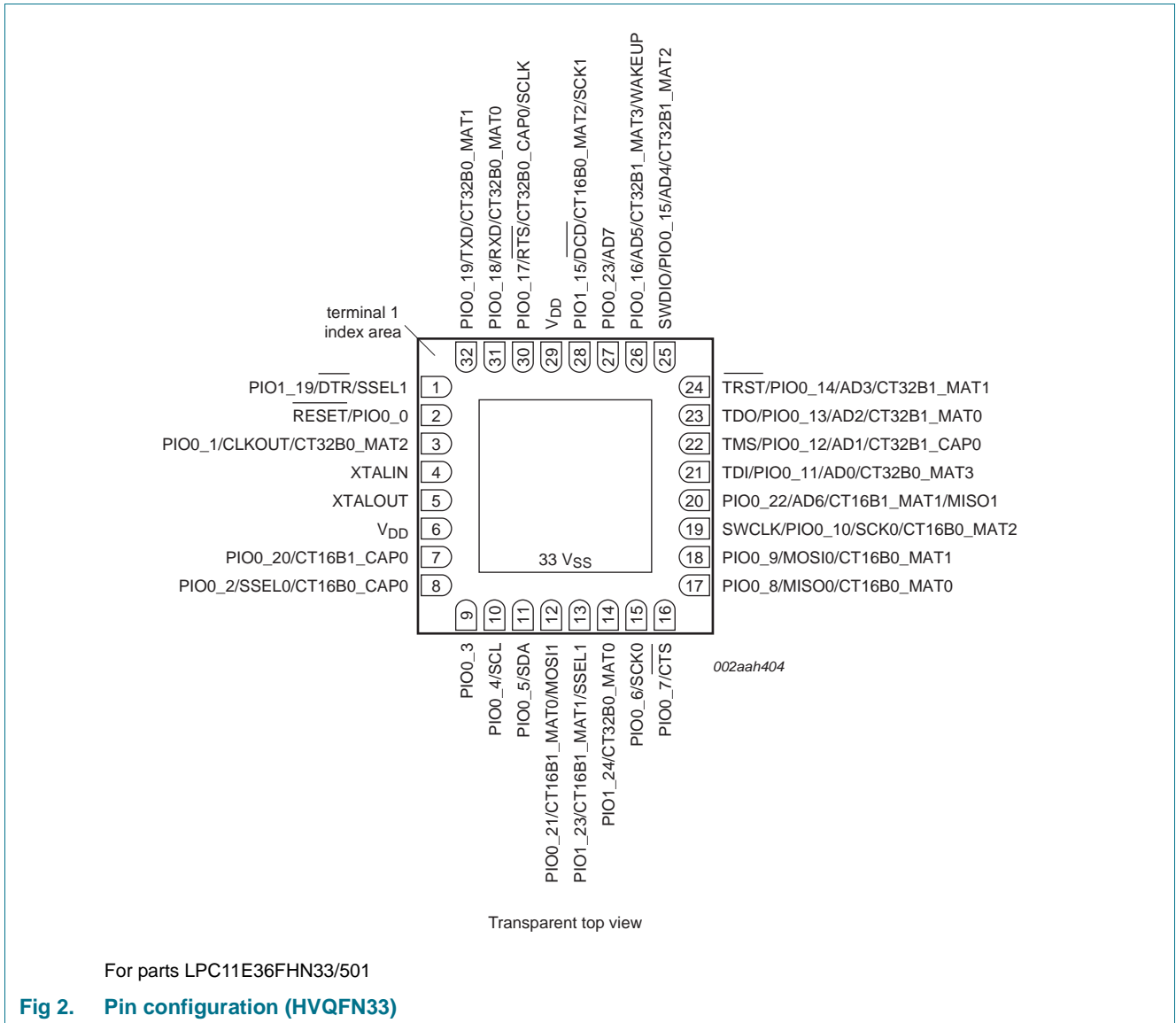


- (1) Not available on HVQFN33 packages.
- (2) CT16B0\_CAP1, CT16B1\_CAP1 available on LQFP64 packages only; CT32B0\_CAP1 available LQFP48, and LQFP64 packages only; CT32B1\_CAP1 available in LQFP64 packages only.

Fig 1. Block diagram

## 6. Pinning information

### 6.1 Pinning



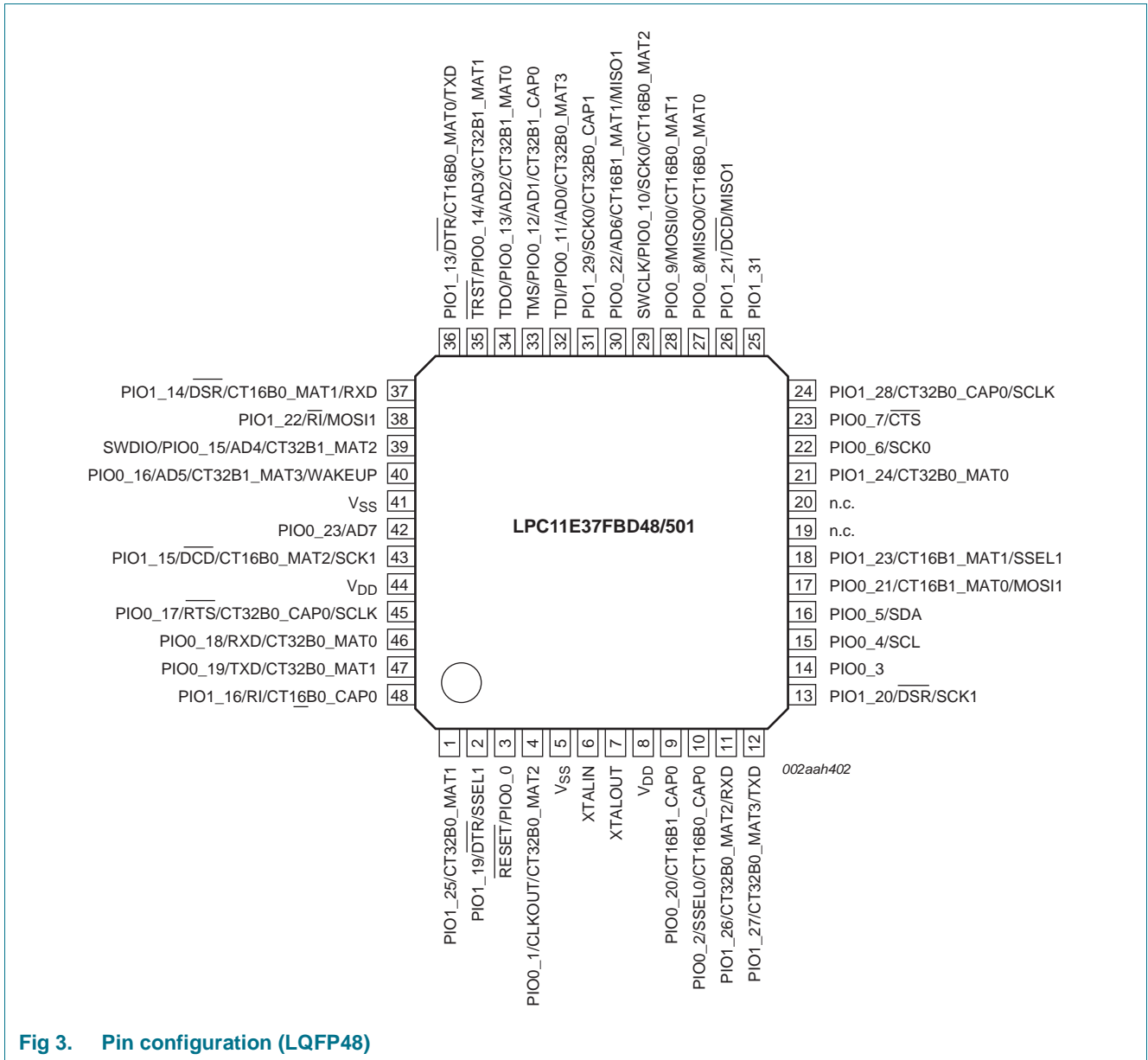
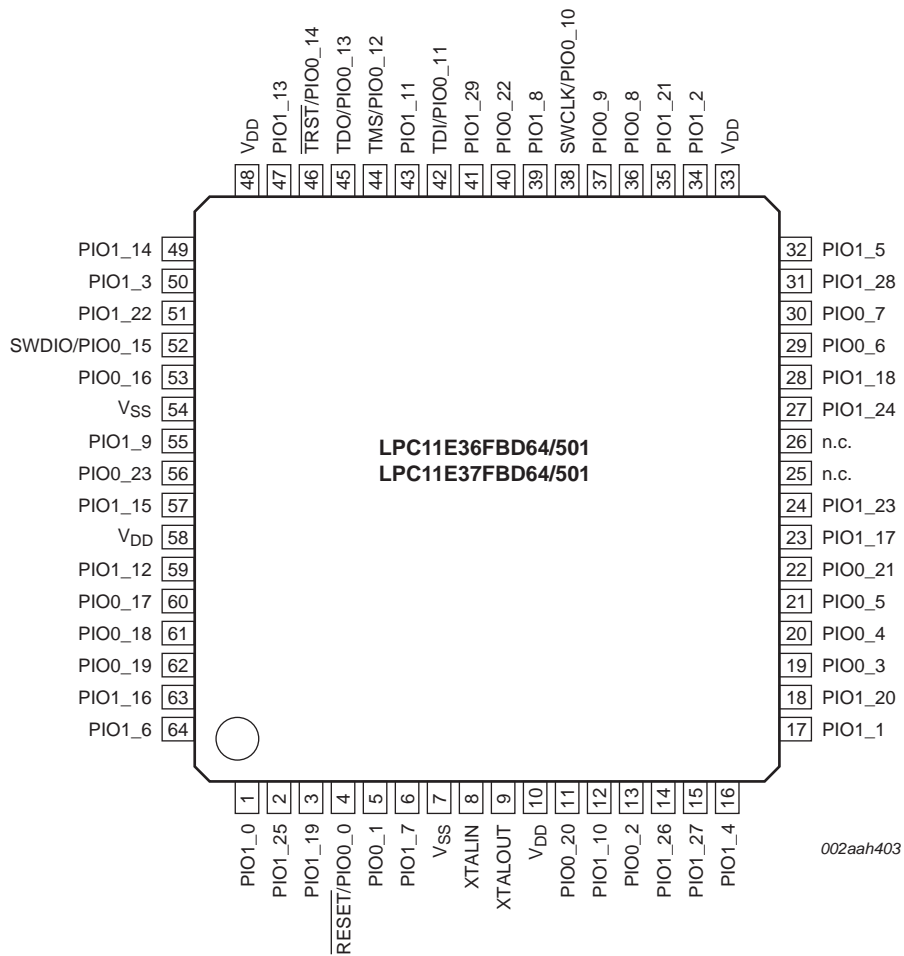


Fig 3. Pin configuration (LQFP48)



See [Table 3](#) for the full pin name.

**Fig 4. Pin configuration (LQFP64)**

## 6.2 Pin description

Table 3 shows all pins and their assigned digital or analog functions in order of the GPIO port number. The default function after reset is listed first. All port pins have internal pull-up resistors enabled after reset except for the true open-drain pins PIO0\_4 and PIO0\_5.

Every port pin has a corresponding IOCON register for programming the digital or analog function, the pull-up/pull-down configuration, the repeater, and the open-drain modes.

The USART, counter/timer, and SSP functions are available on more than one port pin.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
RESET/PIO0_0	2	3	4	[2]	I; PU	I <b>RESET</b> — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
				-	I/O	<b>PIO0_0</b> — General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2	3	4	5	[3]	I; PU	I/O <b>PIO0_1</b> — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
				-	O	<b>CLKOUT</b> — Clockout pin.
				-	O	<b>CT32B0_MAT2</b> — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	8	10	13	[3]	I; PU	I/O <b>PIO0_2</b> — General purpose digital input/output pin.
				-	I/O	<b>SSEL0</b> — Slave select for SSP0.
				-	I	<b>CT16B0_CAP0</b> — Capture input 0 for 16-bit timer 0.
PIO0_3	9	14	19	[3]	I; PU	I/O <b>PIO0_3</b> — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
PIO0_4/SCL	10	15	20	[4]	I; IA	I/O <b>PIO0_4</b> — General purpose digital input/output pin (open-drain).
				-	I/O	<b>SCL</b> — I <sup>2</sup> C-bus clock input/output (open-drain). High-current sink only if I <sup>2</sup> C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11	16	21	[4]	I; IA	I/O <b>PIO0_5</b> — General purpose digital input/output pin (open-drain).
				-	I/O	<b>SDA</b> — I <sup>2</sup> C-bus data input/output (open-drain). High-current sink only if I <sup>2</sup> C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/R/ SCK0	15	22	29	[3]	I; PU	I/O <b>PIO0_6</b> — General purpose digital input/output pin.
				-	-	<b>R</b> — Reserved.
				-	I/O	<b>SCK0</b> — Serial clock for SSP0.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin LQFP64	Reset state <a href="#">[1]</a>	Type	Description
PIO0_7/ $\overline{\text{CTS}}$	16	23	30	<a href="#">[5]</a>	I; PU	I/O <b>PIO0_7</b> — General purpose digital input/output pin (high-current output driver).
					-	I <b>CTS</b> — Clear To Send input for USART.
PIO0_8/MISO0/ CT16B0_MAT0	17	27	36	<a href="#">[3]</a>	I; PU	I/O <b>PIO0_8</b> — General purpose digital input/output pin.
					-	I/O <b>MISO0</b> — Master In Slave Out for SSP0.
					-	O <b>CT16B0_MAT0</b> — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	18	28	37	<a href="#">[3]</a>	I; PU	I/O <b>PIO0_9</b> — General purpose digital input/output pin.
					-	I/O <b>MOSI0</b> — Master Out Slave In for SSP0.
					-	O <b>CT16B0_MAT1</b> — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	19	29	38	<a href="#">[3]</a>	I; PU	I <b>SWCLK</b> — Serial wire clock and test clock TCK for JTAG interface.
					-	I/O <b>PIO0_10</b> — General purpose digital input/output pin.
					-	O <b>SCK0</b> — Serial clock for SSP0.
					-	O <b>CT16B0_MAT2</b> — Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	21	32	42	<a href="#">[6]</a>	I; PU	I <b>TDI</b> — Test Data In for JTAG interface.
					-	I/O <b>PIO0_11</b> — General purpose digital input/output pin.
					-	I <b>AD0</b> — A/D converter, input 0.
					-	O <b>CT32B0_MAT3</b> — Match output 3 for 32-bit timer 0.
TMS/PIO0_12/AD1/ CT32B1_CAP0	22	33	44	<a href="#">[6]</a>	I; PU	I <b>TMS</b> — Test Mode Select for JTAG interface.
					-	I/O <b>PIO0_12</b> — General purpose digital input/output pin.
					-	I <b>AD1</b> — A/D converter, input 1.
					-	I <b>CT32B1_CAP0</b> — Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	23	34	45	<a href="#">[6]</a>	I; PU	O <b>TDO</b> — Test Data Out for JTAG interface.
					-	I/O <b>PIO0_13</b> — General purpose digital input/output pin.
					-	I <b>AD2</b> — A/D converter, input 2.
					-	O <b>CT32B1_MAT0</b> — Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$ /PIO0_14/AD3/ CT32B1_MAT1	24	35	46	<a href="#">[6]</a>	I; PU	I <b>TRST</b> — Test Reset for JTAG interface.
					-	I/O <b>PIO0_14</b> — General purpose digital input/output pin.
					-	I <b>AD3</b> — A/D converter, input 3.
					-	O <b>CT32B1_MAT1</b> — Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	25	39	52	<a href="#">[6]</a>	I; PU	I/O <b>SWDIO</b> — Serial wire debug input/output.
					-	I/O <b>PIO0_15</b> — General purpose digital input/output pin.
					-	I <b>AD4</b> — A/D converter, input 4.
					-	O <b>CT32B1_MAT2</b> — Match output 2 for 32-bit timer 1.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin LQFP64	Reset state	Type	Description
PIO0_16/AD5/ CT32B1_MAT3/WAKEUP	26	40	53	[6]	I; PU	I/O <b>PIO0_16</b> — General purpose digital input/output pin.
				-	I	<b>AD5</b> — A/D converter, input 5.
				-	O	<b>CT32B1_MAT3</b> — Match output 3 for 32-bit timer 1.
				-	I	<b>WAKEUP</b> — Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally to enter Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
PIO0_17/RTS/ CT32B0_CAP0/SCLK	30	45	60	[3]	I; PU	I/O <b>PIO0_17</b> — General purpose digital input/output pin.
				-	O	<b>RTS</b> — Request To Send output for USART.
				-	I	<b>CT32B0_CAP0</b> — Capture input 0 for 32-bit timer 0.
				-	I/O	<b>SCLK</b> — Serial clock input/output for USART in synchronous mode.
PIO0_18/RXD/ CT32B0_MAT0	31	46	61	[3]	I; PU	I/O <b>PIO0_18</b> — General purpose digital input/output pin.
				-	I	<b>RXD</b> — Receiver input for USART. Used in UART ISP mode.
				-	O	<b>CT32B0_MAT0</b> — Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	32	47	62	[3]	I; PU	I/O <b>PIO0_19</b> — General purpose digital input/output pin.
				-	O	<b>TXD</b> — Transmitter output for USART. Used in UART ISP mode.
				-	O	<b>CT32B0_MAT1</b> — Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	7	9	11	[3]	I; PU	I/O <b>PIO0_20</b> — General purpose digital input/output pin.
				-	I	<b>CT16B1_CAP0</b> — Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	12	17	22	[3]	I; PU	I/O <b>PIO0_21</b> — General purpose digital input/output pin.
				-	O	<b>CT16B1_MAT0</b> — Match output 0 for 16-bit timer 1.
				-	I/O	<b>MOSI1</b> — Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	20	30	40	[6]	I; PU	I/O <b>PIO0_22</b> — General purpose digital input/output pin.
				-	I	<b>AD6</b> — A/D converter, input 6.
				-	O	<b>CT16B1_MAT1</b> — Match output 1 for 16-bit timer 1.
				-	I/O	<b>MISO1</b> — Master In Slave Out for SSP1.
PIO0_23/AD7	27	42	56	[6]	I; PU	I/O <b>PIO0_23</b> — General purpose digital input/output pin.
				-	I	<b>AD7</b> — A/D converter, input 7.
PIO1_0/CT32B1_MAT0	-	-	1	[3]	I; PU	I/O <b>PIO1_0</b> — General purpose digital input/output pin.
				-	O	<b>CT32B1_MAT0</b> — Match output 0 for 32-bit timer 1.
PIO1_1/CT32B1_MAT1	-	-	17	[3]	I; PU	I/O <b>PIO1_1</b> — General purpose digital input/output pin.
				-	O	<b>CT32B1_MAT1</b> — Match output 1 for 32-bit timer 1.
PIO1_2/CT32B1_MAT2	-	-	34	[3]	I; PU	I/O <b>PIO1_2</b> — General purpose digital input/output pin.
				-	O	<b>CT32B1_MAT2</b> — Match output 2 for 32-bit timer 1.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin LQFP64	Reset state	Type	Description
PIO1_3/CT32B1_MAT3	-	-	50	[3]	I; PU	I/O <b>PIO1_3</b> — General purpose digital input/output pin.
					-	O <b>CT32B1_MAT3</b> — Match output 3 for 32-bit timer 1.
PIO1_4/CT32B1_CAP0	-	-	16	[3]	I; PU	I/O <b>PIO1_4</b> — General purpose digital input/output pin.
					-	I <b>CT32B1_CAP0</b> — Capture input 0 for 32-bit timer 1.
PIO1_5/CT32B1_CAP1	-	-	32	[3]	I; PU	I/O <b>PIO1_5</b> — General purpose digital input/output pin.
					-	I <b>CT32B1_CAP1</b> — Capture input 1 for 32-bit timer 1.
PIO1_6	-	-	64	[3]	I; PU	I/O <b>PIO1_6</b> — General purpose digital input/output pin.
PIO1_7	-	-	6	[3]	I; PU	I/O <b>PIO1_7</b> — General purpose digital input/output pin.
PIO1_8	-	-	39	[3]	I; PU	I/O <b>PIO1_8</b> — General purpose digital input/output pin.
PIO1_9	-	-	55	[3]	I; PU	I/O <b>PIO1_9</b> — General purpose digital input/output pin.
PIO1_10	-	-	12	[3]	I; PU	I/O <b>PIO1_10</b> — General purpose digital input/output pin.
					-	-
					-	-
					-	-
PIO1_11	-	-	43	[3]	I; PU	I/O <b>PIO1_11</b> — General purpose digital input/output pin.
					-	-
					-	-
					-	-
PIO1_12	-	-	59	[3]	I; PU	I/O <b>PIO1_12</b> — General purpose digital input/output pin.
					-	-
					-	-
					-	-
PIO1_13/DTR/ CT16B0_MAT0/TXD	-	36	47	[3]	I; PU	I/O <b>PIO1_13</b> — General purpose digital input/output pin.
					-	O <b>DTR</b> — Data Terminal Ready output for USART.
					-	O <b>CT16B0_MAT0</b> — Match output 0 for 16-bit timer 0.
					-	O <b>TXD</b> — Transmitter output for USART.
PIO1_14/DSR/ CT16B0_MAT1/RXD	-	37	49	[3]	I; PU	I/O <b>PIO1_14</b> — General purpose digital input/output pin.
					-	I <b>DSR</b> — Data Set Ready input for USART.
					-	O <b>CT16B0_MAT1</b> — Match output 1 for 16-bit timer 0.
					-	I <b>RXD</b> — Receiver input for USART.
PIO1_15/DCD/ CT16B0_MAT2/SCK1	28	43	57	[3]	I; PU	I/O <b>PIO1_15</b> — General purpose digital input/output pin.
					-	I <b>DCD</b> — Data Carrier Detect input for USART.
					-	O <b>CT16B0_MAT2</b> — Match output 2 for 16-bit timer 0.
					-	I/O <b>SCK1</b> — Serial clock for SSP1.
PIO1_16/RI/ CT16B0_CAP0	-	48	63	[3]	I; PU	I/O <b>PIO1_16</b> — General purpose digital input/output pin.
					-	I <b>RI</b> — Ring Indicator input for USART.
					-	I <b>CT16B0_CAP0</b> — Capture input 0 for 16-bit timer 0.
PIO1_17/CT16B0_CAP1/ RXD	-	-	23	[3]	I; PU	I/O <b>PIO1_17</b> — General purpose digital input/output pin.
					-	I <b>CT16B0_CAP1</b> — Capture input 1 for 16-bit timer 0.
					-	I <b>RXD</b> — Receiver input for USART.
PIO1_18/CT16B1_CAP1/ TXD	-	-	28	[3]	I; PU	I/O <b>PIO1_18</b> — General purpose digital input/output pin.
					-	I <b>CT16B1_CAP1</b> — Capture input 1 for 16-bit timer 1.
					-	O <b>TXD</b> — Transmitter output for USART.
PIO1_19/DTR/SSEL1	1	2	3	[3]	I; PU	I/O <b>PIO1_19</b> — General purpose digital input/output pin.
					-	O <b>DTR</b> — Data Terminal Ready output for USART.
					-	I/O <b>SSEL1</b> — Slave select for SSP1.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin LQFP64	Reset state	Type	Description
PIO1_20/ $\overline{\text{DSR}}$ /SCK1	-	13	18	[3]	I; PU	I/O <b>PIO1_20</b> — General purpose digital input/output pin.
					-	I <b>DSR</b> — Data Set Ready input for USART.
					-	I/O <b>SCK1</b> — Serial clock for SSP1.
PIO1_21/ $\overline{\text{DCD}}$ /MISO1	-	26	35	[3]	I; PU	I/O <b>PIO1_21</b> — General purpose digital input/output pin.
					-	I <b>DCD</b> — Data Carrier Detect input for USART.
					-	I/O <b>MISO1</b> — Master In Slave Out for SSP1.
PIO1_22/ $\overline{\text{RI}}$ /MOSI1	-	38	51	[3]	I; PU	I/O <b>PIO1_22</b> — General purpose digital input/output pin.
					-	I <b>RI</b> — Ring Indicator input for USART.
					-	I/O <b>MOSI1</b> — Master Out Slave In for SSP1.
PIO1_23/CT16B1_MAT1/ SSEL1	13	18	24	[3]	I; PU	I/O <b>PIO1_23</b> — General purpose digital input/output pin.
					-	O <b>CT16B1_MAT1</b> — Match output 1 for 16-bit timer 1.
					-	I/O <b>SSEL1</b> — Slave select for SSP1.
PIO1_24/CT32B0_MAT0	14	21	27	[3]	I; PU	I/O <b>PIO1_24</b> — General purpose digital input/output pin.
					-	O <b>CT32B0_MAT0</b> — Match output 0 for 32-bit timer 0.
PIO1_25/CT32B0_MAT1	-	1	2	[3]	I; PU	I/O <b>PIO1_25</b> — General purpose digital input/output pin.
					-	O <b>CT32B0_MAT1</b> — Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD	-	11	14	[3]	I; PU	I/O <b>PIO1_26</b> — General purpose digital input/output pin.
					-	O <b>CT32B0_MAT2</b> — Match output 2 for 32-bit timer 0.
					-	I <b>RXD</b> — Receiver input for USART.
PIO1_27/CT32B0_MAT3/ TXD	-	12	15	[3]	I; PU	I/O <b>PIO1_27</b> — General purpose digital input/output pin.
					-	O <b>CT32B0_MAT3</b> — Match output 3 for 32-bit timer 0.
					-	O <b>TXD</b> — Transmitter output for USART.
PIO1_28/CT32B0_CAP0/ SCLK	-	24	31	[3]	I; PU	I/O <b>PIO1_28</b> — General purpose digital input/output pin.
					-	I <b>CT32B0_CAP0</b> — Capture input 0 for 32-bit timer 0.
					-	I/O <b>SCLK</b> — Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	-	31	41	[3]	I; PU	I/O <b>PIO1_29</b> — General purpose digital input/output pin.
					-	I/O <b>SCK0</b> — Serial clock for SSP0.
					-	I <b>CT32B0_CAP1</b> — Capture input 1 for 32-bit timer 0.
PIO1_31	-	25	-	[3]	I; PU	I/O <b>PIO1_31</b> — General purpose digital input/output pin.
n.c.	-	19	25	-	-	Not connected.
n.c.	-	20	26	-	-	Not connected.
XTALIN	4	6	8	[7]	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Pin LQFP64	Reset state	Type	Description
XTALOUT	5	7	9	<a href="#">U</a>	-	Output from the oscillator amplifier.
V <sub>DD</sub>	6; 29	8; 44	10; 33; 48; 58	-	-	Supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V <sub>SS</sub>	33	5; 41	7; 54	-	-	Ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.
- [2] See [Figure 28](#) for the reset pad configuration.  $\overline{\text{RESET}}$  functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 27](#)).
- [4] I<sup>2</sup>C-bus pins compliant with the I<sup>2</sup>C-bus specification for I<sup>2</sup>C standard mode, I<sup>2</sup>C Fast-mode, and I<sup>2</sup>C Fast-mode Plus.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 27](#)); includes high-current output driver.
- [6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see [Figure 27](#)); includes digital input glitch filter.
- [7] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). Leave XTALOUT floating.

## 7. Functional description

### 7.1 On-chip flash programming memory

The LPC11E3x contain up to 128 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages can be erased using the IAP erase page command.

### 7.2 EEPROM

The LPC11E3x contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

### 7.3 SRAM

The LPC11E3x contain a total of 12 kB on-chip static RAM memory.

## 7.4 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command
- IAP support for EEPROM
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines

## 7.5 Memory map

The LPC11E3x incorporates several distinct memory regions, shown in the following figures. [Figure 5](#) shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

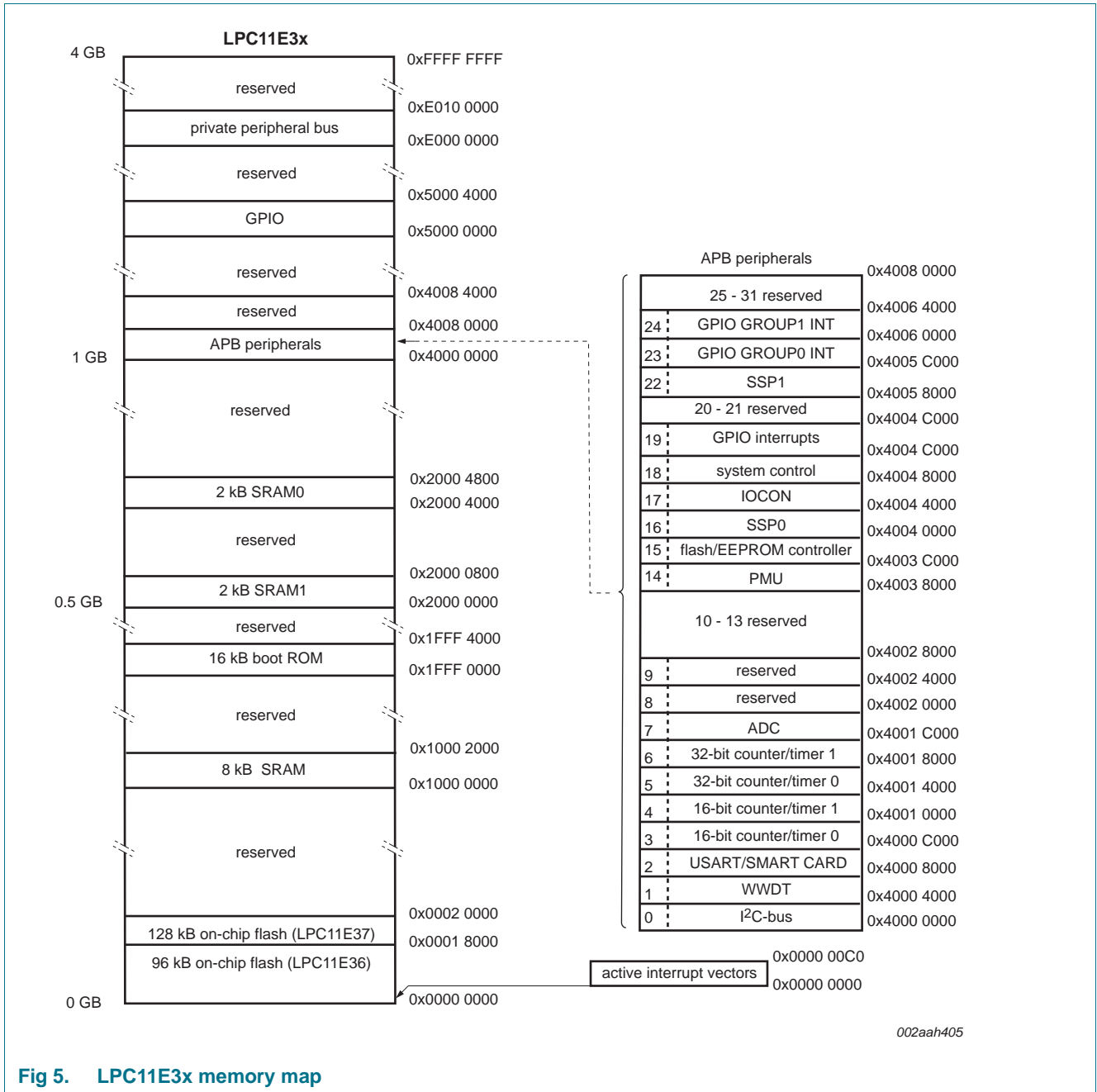


Fig 5. LPC11E3x memory map

## 7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

### 7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11E3x, the NVIC supports 24 vectored interrupts.

- Four programmable interrupt priority levels, with hardware priority level masking.
- Software interrupt generation.

### 7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

## 7.7 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Connect peripherals to the appropriate pins before activating the peripheral and before enabling any related interrupt. Activity of any enabled peripheral function that is not mapped to a related pin is treated as undefined.

### 7.7.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All GPIO pins (except PIO0\_4 and PIO0\_5) are pulled up to 3.3 V ( $V_{DD} = 3.3$  V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable 10 ns glitch filter on pins PIO0\_22, PIO0\_23, and PIO0\_11 to PIO0\_16. The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.

## 7.8 General-Purpose Input/Output GPIO

The GPIO registers control device pin functions that are not connected to a specific peripheral function. Pins can be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11E3x use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Any GPIO pin providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

The GPIO block consists of three parts:

1. The GPIO ports.
2. The GPIO pin interrupt block to control eight GPIO pins selected as pin interrupts.
3. Two GPIO group interrupt blocks to control two combined interrupts from all GPIO pins.

### 7.8.1 Features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Any pin or pins in each port can trigger a port interrupt.

## 7.9 USART

The LPC11E3x contains one USART.

The USART includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

### 7.9.1 Features

- Maximum USART data bit rate of 3.125 Mbit/s.
- 16 byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.

## 7.10 SSP serial I/O controller

The SSP controllers operate on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

### 7.10.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI (Serial Peripheral Interface), 4-wire Texas Instruments SSI (Serial Synchronous Interface), and National Semiconductor Microwire buses

- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

## 7.11 I<sup>2</sup>C-bus serial I/O controller

The LPC11E3x contain one I<sup>2</sup>C-bus controller.

The I<sup>2</sup>C-bus is bidirectional for inter-IC control using only two wires: a Serial CLock line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I<sup>2</sup>C-bus is a multi-master bus, and more than one bus master connected to the interface can be controlled the bus.

### 7.11.1 Features

- The I<sup>2</sup>C-interface is an I<sup>2</sup>C-bus compliant interface with open-drain pins. The I<sup>2</sup>C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I<sup>2</sup>C-bus can be used for test and diagnostic purposes.
- The I<sup>2</sup>C-bus controller supports multiple address recognition and a bus monitor mode.

## 7.12 10-bit ADC

The LPC11E3x contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

### 7.12.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V<sub>DD</sub>.
- 10-bit conversion time  $\geq 2.44 \mu\text{s}$  (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.

- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

### 7.13 General purpose external event counter/timers

The LPC11E3x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

#### 7.13.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to two capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler can be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

### 7.14 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

### 7.15 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

#### 7.15.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

- Optional warning interrupt can be generated at a programmable time before watchdog time-out.
- Software enables the WWDT, but a hardware reset or a watchdog reset/interrupt is required to disable the WWDT.
- Incorrect feed sequence causes reset or interrupt, if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from  $(T_{cy(WDCLK)} \times 256 \times 4)$  to  $(T_{cy(WDCLK)} \times 2^{24} \times 4)$  in multiples of  $T_{cy(WDCLK)} \times 4$ .
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). The clock source selection provides a wide range of potential timing choices of watchdog operation under different power conditions.

## 7.16 Clocking and power control

### 7.16.1 Integrated oscillators

The LPC11E3x include three independent oscillators: the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC11E3x operates from the internal RC oscillator until software switches to a different clock source. The IRC allows the system to operate without any external crystal and the bootloader code to operate at a known frequency.

See [Figure 6](#) for an overview of the LPC11E3x clock generation.

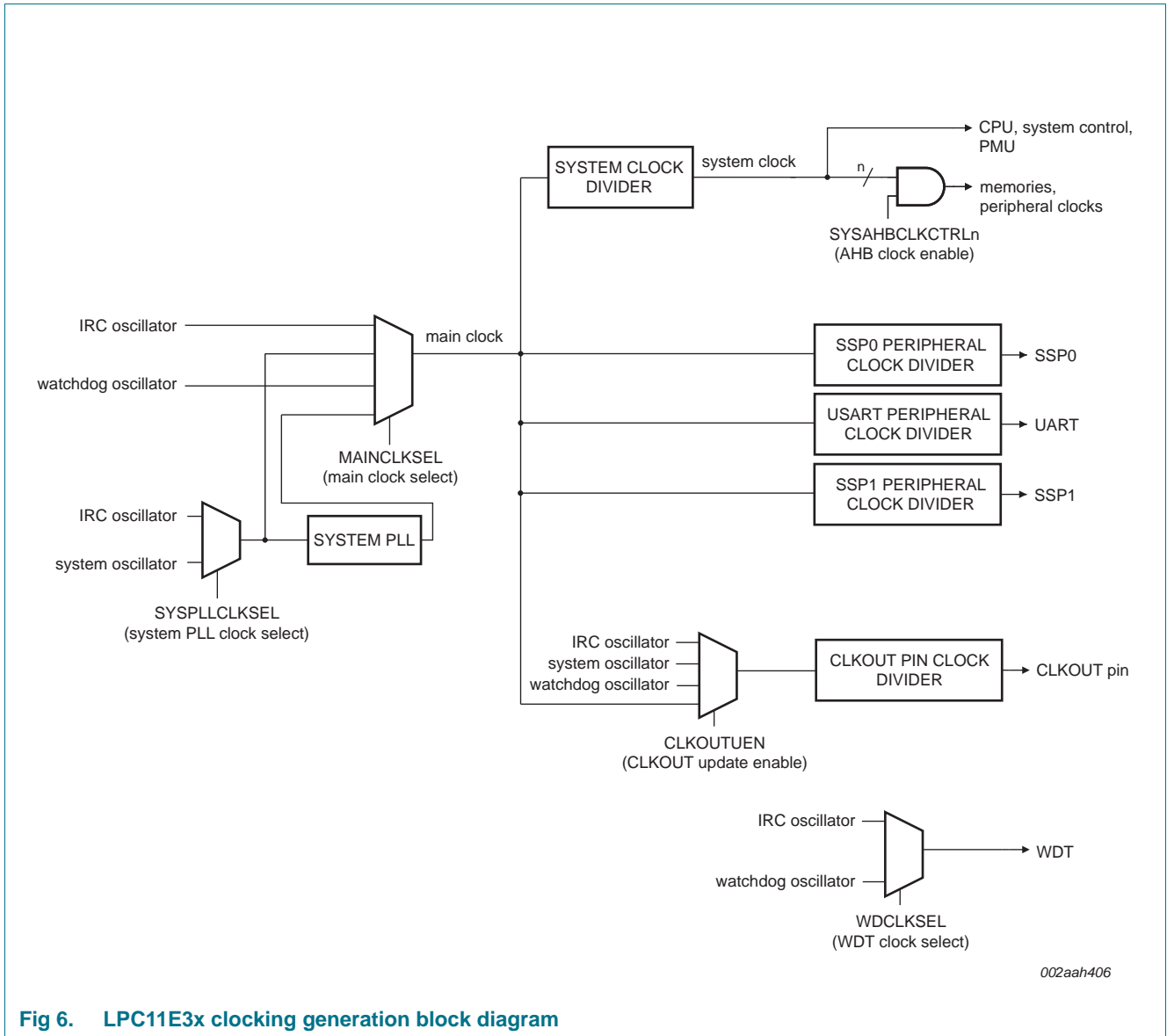


Fig 6. LPC11E3x clocking generation block diagram

**7.16.1.1 Internal RC oscillator**

The IRC can be used as the clock source for the WDT, and/or as the clock that drives the system PLL and then the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC11E3x use the IRC as the clock source. Software can later switch to one of the other available clock sources.

**7.16.1.2 System oscillator**

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

### 7.16.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is  $\pm 40\%$  (see also [Table 13](#)).

### 7.16.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100  $\mu$ s.

### 7.16.3 Clock output

The LPC11E3x feature a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

### 7.16.4 Wake-up process

The LPC11E3x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

### 7.16.5 Power control

The LPC11E3x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

#### 7.16.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11E3x for one of the following power modes:

- Default mode corresponding to power configuration after reset.

- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

#### 7.16.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

#### 7.16.5.3 Deep-sleep mode

In Deep-sleep mode, the LPC11E3x is in Sleep-mode and all peripheral clocks and all clock sources are off except for the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC11E3x can wake up from Deep-sleep mode via reset, selected GPIO pins or a watchdog timer interrupt.

Deep-sleep mode saves power and allows for short wake-up times.

#### 7.16.5.4 Power-down mode

In Power-down mode, the LPC11E3x is in Sleep-mode and all peripheral clocks and all clock sources are off except for watchdog oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

The LPC11E3x can wake up from Power-down mode via reset, selected GPIO pins or a watchdog timer interrupt.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

#### 7.16.5.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin. The LPC11E3x can wake up from Deep power-down mode via the WAKEUP pin.

The LPC11E3x can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. Pull the  $\overline{\text{RESET}}$  pin HIGH to prevent it from floating while in Deep power-down mode.

## 7.16.6 System control

### 7.16.6.1 Reset

Reset has four sources on the LPC11E3x: the  $\overline{\text{RESET}}$  pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The  $\overline{\text{RESET}}$  pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the  $\overline{\text{RESET}}$  pin.

### 7.16.6.2 Brownout detection

The LPC11E3x includes four levels for monitoring the voltage on the  $V_{DD}$  pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four additional threshold levels can be selected to cause a forced reset of the chip.

### 7.16.6.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0\_1 pin can be disabled without enabling CRP. For details, see the *LPC11Exx user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0\_1 pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

**CAUTION**

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0\_1 for valid user code can be disabled. For details, see the *LPC11Exx user manual*.

**7.16.6.4 APB interface**

The APB peripherals are located on one APB bus.

**7.16.6.5 AHBLite**

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the ROM.

**7.16.6.6 External interrupt inputs**

All GPIO pins can be level or edge sensitive interrupt inputs.

## 7.17 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0 is configured to support up to four breakpoints and two watch points.

The  $\overline{\text{RESET}}$  pin selects between the JTAG boundary scan ( $\overline{\text{RESET}} = \text{LOW}$ ) and the ARM SWD debug ( $\overline{\text{RESET}} = \text{HIGH}$ ). The ARM SWD debug port is disabled while the LPC11E3x is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the  $\overline{\text{RESET}}$  pin pulled HIGH externally.
3. Wait for at least 250  $\mu\text{s}$ .
4. Pull the  $\overline{\text{RESET}}$  pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the  $\overline{\text{TRST}}$  pin to enable the SWD debug mode, and release the  $\overline{\text{RESET}}$  pin (pull HIGH).

**Remark:** The JTAG interface cannot be used for debug purposes.

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage (core and external rail)		<sup>[2]</sup> -0.5	+4.6	V
$V_I$	input voltage	5 V tolerant digital I/O pins; $V_{DD} \geq 1.8$ V	<sup>[3]</sup> -0.5	+5.5	V
		$V_{DD} = 0$ V	<sup>[3]</sup> -0.5	+3.6	V
$I_{DD}$	supply current	per supply pin	-	100	mA
$I_{SS}$	ground current	per ground pin	-	100	mA
$I_{latch}$	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$ ; $T_j < 125$ °C	-	100	mA
$T_{stg}$	storage temperature	non-operating	<sup>[4]</sup> -65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W
$V_{ESD}$	electrostatic discharge voltage	human body model; all pins	<sup>[5]</sup> -	+6500	V

[1] The following applies to the limiting values:

- a) This product includes circuitry designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
  - b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{SS}$  unless otherwise noted.
- [2] Maximum/minimum voltage above the maximum operating voltage (see [Table 5](#)) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.
- [3] Including voltage on outputs in 3-state mode.
- [4] The maximum non-operating storage temperature is different than the temperature for required shelf life which can be determined based on required shelf lifetime. Refer to the JEDEC spec (J-STD-033B.1) for further details.
- [5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 k $\Omega$  series resistor.

## 9. Static characteristics

**Table 5. Static characteristics**

$T_{amb} = -40\text{ °C}$  to  $+85\text{ °C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit	
$V_{DD}$	supply voltage (core and external rail)		1.8	3.3	3.6	V	
$I_{DD}$	supply current	Active mode; $V_{DD} = 3.3\text{ V}$ ; $T_{amb} = 25\text{ °C}$ ; code <code>while(1){}</code> executed from flash;					
		system clock = 12 MHz	<a href="#">[2]</a> <a href="#">[3]</a> <a href="#">[4]</a> <a href="#">[5]</a> <a href="#">[6]</a>	2	-	mA	
		system clock = 50 MHz	<a href="#">[3]</a> <a href="#">[4]</a> <a href="#">[5]</a> <a href="#">[6]</a>	7	-	mA	
		Sleep mode; $V_{DD} = 3.3\text{ V}$ ; $T_{amb} = 25\text{ °C}$ ; system clock = 12 MHz	<a href="#">[2]</a> <a href="#">[3]</a> <a href="#">[4]</a> <a href="#">[5]</a> <a href="#">[6]</a>	1	-	mA	
		Deep-sleep mode; $V_{DD} = 3.3\text{ V}$ ; $T_{amb} = 25\text{ °C}$	<a href="#">[3]</a>	300	-	$\mu\text{A}$	
		Power-down mode; $V_{DD} = 3.3\text{ V}$ ; $T_{amb} = 25\text{ °C}$	-	2	-	$\mu\text{A}$	
		Deep power-down mode; $V_{DD} = 3.3\text{ V}$ ; $T_{amb} = 25\text{ °C}$	<a href="#">[8]</a>	220	-	nA	
<b>Standard port pins, RESET</b>							
$I_{IL}$	LOW-level input current	$V_I = 0\text{ V}$ ; on-chip pull-up resistor disabled	-	0.5	10	nA	
$I_{IH}$	HIGH-level input current	$V_I = V_{DD}$ ; on-chip pull-down resistor disabled	-	0.5	10	nA	
$I_{OZ}$	OFF-state output current	$V_O = 0\text{ V}$ ; $V_O = V_{DD}$ ; on-chip pull-up/down resistors disabled	-	0.5	10	nA	
$V_I$	input voltage	pin configured to provide a digital function	<a href="#">[9]</a> <a href="#">[10]</a> <a href="#">[11]</a>	0	-	5.0	V
$V_O$	output voltage	output active	0	-	$V_{DD}$	V	
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD}$	-	-	V	
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DD}$	V	
$V_{hys}$	hysteresis voltage		-	0.4	-	V	
$V_{OH}$	HIGH-level output voltage	$2.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ ; $I_{OH} = -4\text{ mA}$ $1.8\text{ V} \leq V_{DD} < 2.0\text{ V}$ ; $I_{OH} = -3\text{ mA}$	$V_{DD} - 0.4$	-	-	V	
$V_{OL}$	LOW-level output voltage	$2.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ ; $I_{OL} = 4\text{ mA}$ $1.8\text{ V} \leq V_{DD} < 2.0\text{ V}$ ; $I_{OL} = 3\text{ mA}$	-	-	0.4	V	
$I_{OH}$	HIGH-level output current	$V_{OH} = V_{DD} - 0.4\text{ V}$ ; $2.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.8\text{ V} \leq V_{DD} < 2.0\text{ V}$	-4	-	-	mA	
			-3	-	-	mA	

**Table 5. Static characteristics ...continued**  
*T<sub>amb</sub> = -40 °C to +85 °C, unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V 2.0 V ≤ V <sub>DD</sub> ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V <sub>DD</sub> < 2.0 V	3	-	-	mA
I <sub>OHS</sub>	HIGH-level short-circuit output current	V <sub>OH</sub> = 0 V	<sup>[12]</sup> -	-	-45	mA
I <sub>OLS</sub>	LOW-level short-circuit output current	V <sub>OL</sub> = V <sub>DD</sub>	<sup>[12]</sup> -	-	50	mA
I <sub>pd</sub>	pull-down current	V <sub>I</sub> = 5 V	10	50	150	μA
I <sub>pu</sub>	pull-up current	V <sub>I</sub> = 0 V; 2.0 V ≤ V <sub>DD</sub> ≤ 3.6 V	-15	-50	-85	μA
		1.8 V ≤ V <sub>DD</sub> < 2.0 V	-10	-50	-85	μA
		V <sub>DD</sub> < V <sub>I</sub> < 5 V	0	0	0	μA
<b>High-drive output pin (PIO0_7)</b>						
I <sub>IL</sub>	LOW-level input current	V <sub>I</sub> = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I <sub>IH</sub>	HIGH-level input current	V <sub>I</sub> = V <sub>DD</sub> ; on-chip pull-down resistor disabled	-	0.5	10	nA
I <sub>OZ</sub>	OFF-state output current	V <sub>O</sub> = 0 V; V <sub>O</sub> = V <sub>DD</sub> ; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V <sub>I</sub>	input voltage	pin configured to provide a digital function	<sup>[9][10]</sup> 0 <sup>[11]</sup>	-	5.0	V
V <sub>O</sub>	output voltage	output active	0	-	V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.3V <sub>DD</sub>	V
V <sub>hys</sub>	hysteresis voltage		0.4	-	-	V
V <sub>OH</sub>	HIGH-level output voltage	2.5 V ≤ V <sub>DD</sub> ≤ 3.6 V; I <sub>OH</sub> = -20 mA	V <sub>DD</sub> - 0.4	-	-	V
		1.8 V ≤ V <sub>DD</sub> < 2.5 V; I <sub>OH</sub> = -12 mA	V <sub>DD</sub> - 0.4	-	-	V
V <sub>OL</sub>	LOW-level output voltage	2.0 V ≤ V <sub>DD</sub> ≤ 3.6 V; I <sub>OL</sub> = 4 mA	-	-	0.4	V
		1.8 V ≤ V <sub>DD</sub> < 2.0 V; I <sub>OL</sub> = 3 mA	-	-	0.4	V
I <sub>OH</sub>	HIGH-level output current	V <sub>OH</sub> = V <sub>DD</sub> - 0.4 V; 2.5 V ≤ V <sub>DD</sub> ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V <sub>DD</sub> < 2.5 V	12	-	-	mA
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V 2.0 V ≤ V <sub>DD</sub> ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V <sub>DD</sub> < 2.0 V	3	-	-	mA
			<sup>[12]</sup> -	-	50	mA
I <sub>OLS</sub>	LOW-level short-circuit output current	V <sub>OL</sub> = V <sub>DD</sub>	<sup>[12]</sup> -	-	50	mA
I <sub>pd</sub>	pull-down current	V <sub>I</sub> = 5 V	10	50	150	μA
I <sub>pu</sub>	pull-up current	V <sub>I</sub> = 0 V 2.0 V ≤ V <sub>DD</sub> ≤ 3.6 V	-15	-50	-85	μA
		1.8 V ≤ V <sub>DD</sub> < 2.0 V	-10	-50	-85	μA
		V <sub>DD</sub> < V <sub>I</sub> < 5 V	0	0	0	μA

**Table 5. Static characteristics ...continued**  
*T<sub>amb</sub> = -40 °C to +85 °C, unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>I<sup>2</sup>C-bus pins (PIO0_4 and PIO0_5)</b>						
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.3V <sub>DD</sub>	V
V <sub>hys</sub>	hysteresis voltage		-	0.05V <sub>DD</sub>	-	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V; I <sup>2</sup> C-bus pins configured as standard mode pins 2.0 V ≤ V <sub>DD</sub> ≤ 3.6 V	3.5	-	-	mA
		1.8 V ≤ V <sub>DD</sub> < 2.0 V	3	-	-	
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V; I <sup>2</sup> C-bus pins configured as Fast-mode Plus pins 2.0 V ≤ V <sub>DD</sub> ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V <sub>DD</sub> < 2.0 V	16	-	-	
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>DD</sub>	<sup>[13]</sup> -	2	4	μA
		V <sub>I</sub> = 5 V	-	10	22	μA
<b>Oscillator pins</b>						
V <sub>i(xtal)</sub>	crystal input voltage		-0.5	1.8	1.95	V
V <sub>o(xtal)</sub>	crystal output voltage		-0.5	1.8	1.95	V

- [1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
- [2] IRC enabled; system oscillator disabled; system PLL disabled.
- [3] I<sub>DD</sub> measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.
- [4] BOD disabled.
- [5] All peripherals disabled in the AHBCLKCTRL register. Peripheral clocks to USART, SSP0/1 disabled in the SYSCON block.
- [6] Low-current mode PWR\_LOW\_CURRENT selected when running the set\_power routine in the power profiles.
- [7] IRC disabled; system oscillator enabled; system PLL enabled.
- [8] WAKEUP pin pulled HIGH externally. An external pull-up resistor is required on the RESET pin for the Deep power-down mode.
- [9] Including voltage on outputs in 3-state mode.
- [10] V<sub>DD</sub> supply voltage must be present.
- [11] 3-state outputs go into 3-state mode in Deep power-down mode.
- [12] Allowed as long as the current limit does not exceed the maximum current allowed by the device.
- [13] To V<sub>SS</sub>.

**Table 6. ADC static characteristics**

$T_{amb} = -40\text{ °C}$  to  $+85\text{ °C}$  unless otherwise specified; ADC frequency 4.5 MHz,  $V_{DD} = 2.5\text{ V}$  to  $3.6\text{ V}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IA}$	analog input voltage		0	-	$V_{DD}$	V
$C_{ia}$	analog input capacitance		-	-	1	pF
$E_D$	differential linearity error		[1][2]	-	$\pm 1$	LSB
$E_{L(adj)}$	integral non-linearity		[3]	-	$\pm 1.5$	LSB
$E_O$	offset error		[4]	-	$\pm 3.5$	LSB
$E_G$	gain error		[5]	-	0.6	%
$E_T$	absolute error		[6]	-	$\pm 4$	LSB
$R_{vsi}$	voltage source interface resistance		-	-	40	k $\Omega$
$R_i$	input resistance		[7][8]	-	2.5	M $\Omega$

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error ( $E_D$ ) is the difference between the actual step width and the ideal step width. See [Figure 7](#).

[3] The integral non-linearity ( $E_{L(adj)}$ ) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 7](#).

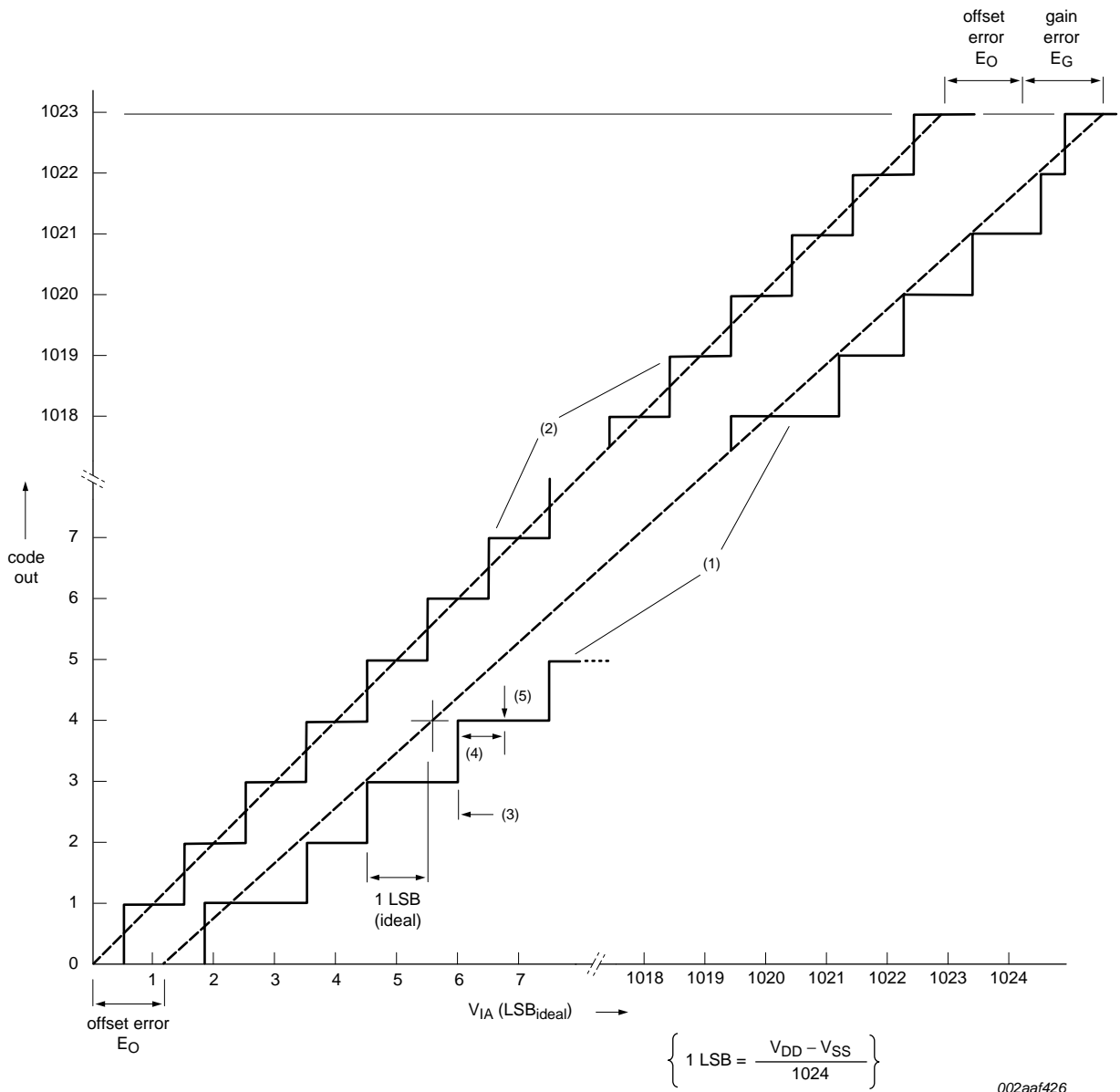
[4] The offset error ( $E_O$ ) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 7](#).

[5] The gain error ( $E_G$ ) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 7](#).

[6] The absolute error ( $E_T$ ) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 7](#).

[7]  $T_{amb} = 25\text{ °C}$ ; maximum sampling frequency  $f_s = 400\text{ kSamples/s}$  and analog input capacitance  $C_{ia} = 1\text{ pF}$ .

[8] Input resistance  $R_i$  depends on the sampling frequency  $f_s$ :  $R_i = 1 / (f_s \times C_{ia})$ .



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- (1) Example of an actual transfer curve.
- (2) The ideal transfer curve.
- (3) Differential linearity error (E<sub>D</sub>).
- (4) Integral non-linearity (E<sub>L(adj)</sub>).
- (5) Center of a step of the actual transfer curve.

**Fig 7. ADC characteristics**

## 9.1 BOD static characteristics

**Table 7. BOD static characteristics**<sup>[1]</sup>

$T_{amb} = 25\text{ °C}$ .

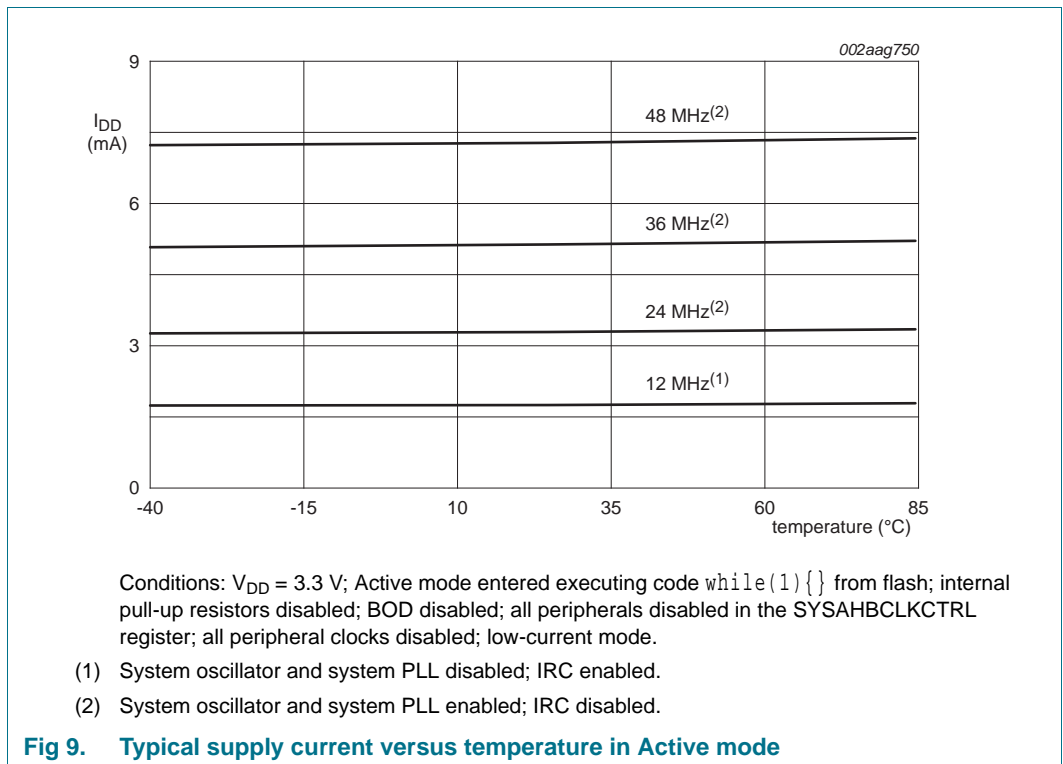
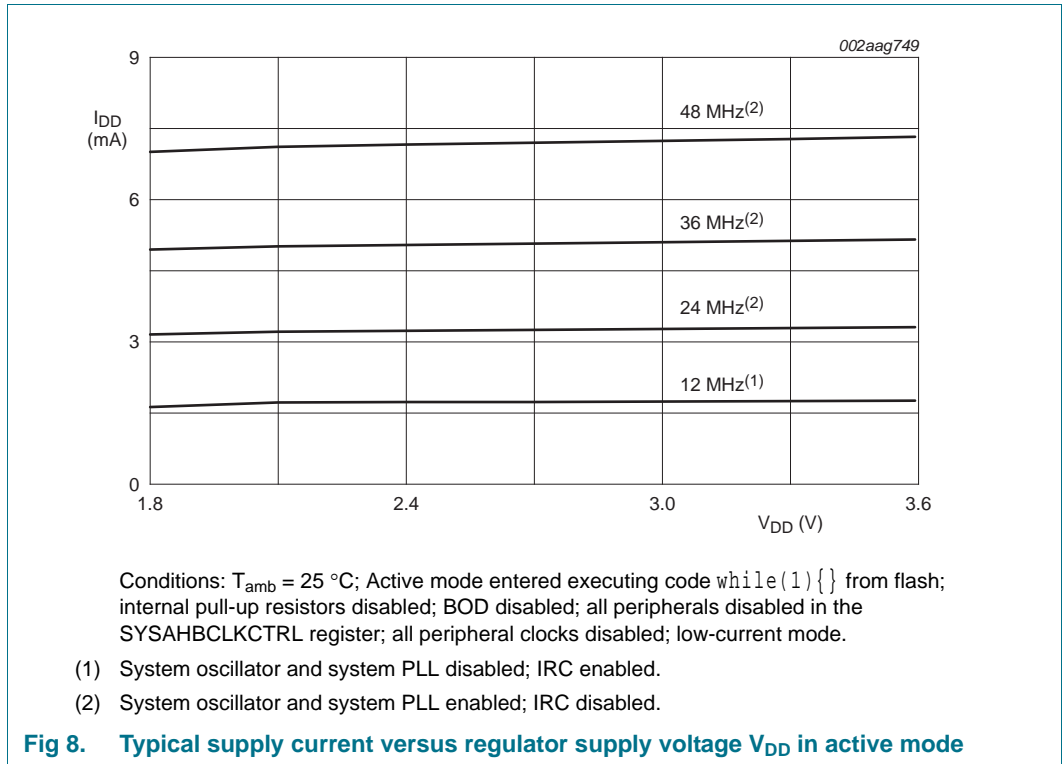
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{th}$	threshold voltage	interrupt level 0					
		assertion	-	1.65	-	V	
		de-assertion	-	1.80	-	V	
		interrupt level 1					
		assertion	-	2.22	-	V	
		de-assertion	-	2.35	-	V	
		interrupt level 2					
		assertion	-	2.52	-	V	
		de-assertion	-	2.66	-	V	
		interrupt level 3					
		assertion	-	2.80	-	V	
		de-assertion	-	2.90	-	V	
		reset level 0					
		assertion	-	1.46	-	V	
		de-assertion	-	1.63	-	V	
		reset level 1					
		assertion	-	2.06	-	V	
		de-assertion	-	2.15	-	V	
		reset level 2					
		assertion	-	2.35	-	V	
		de-assertion	-	2.43	-	V	
		reset level 3					
		assertion	-	2.63	-	V	
		de-assertion	-	2.71	-	V	

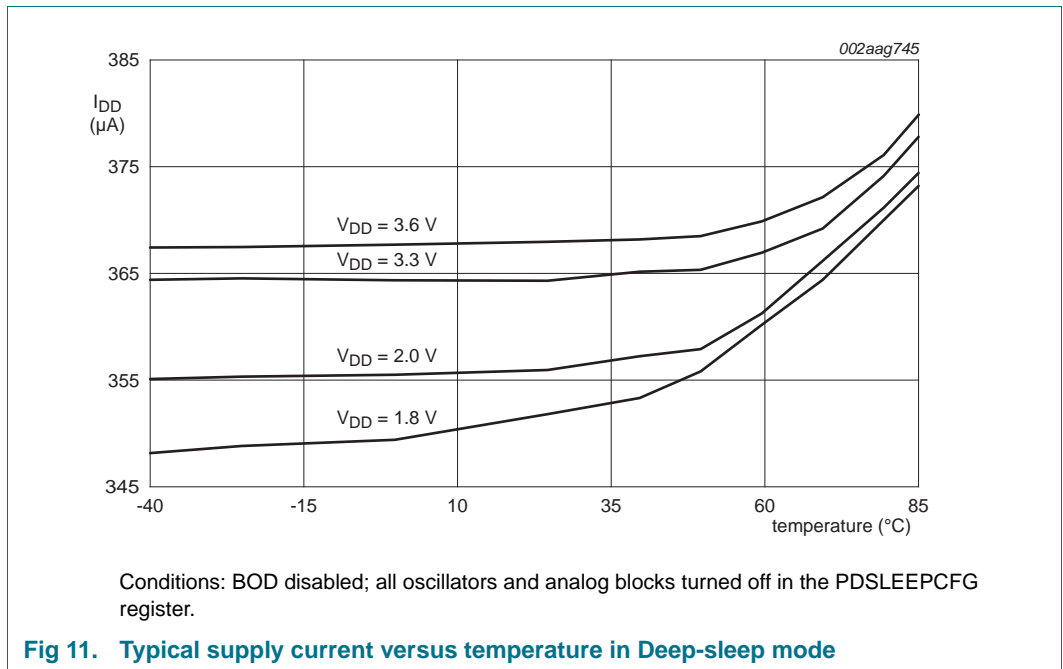
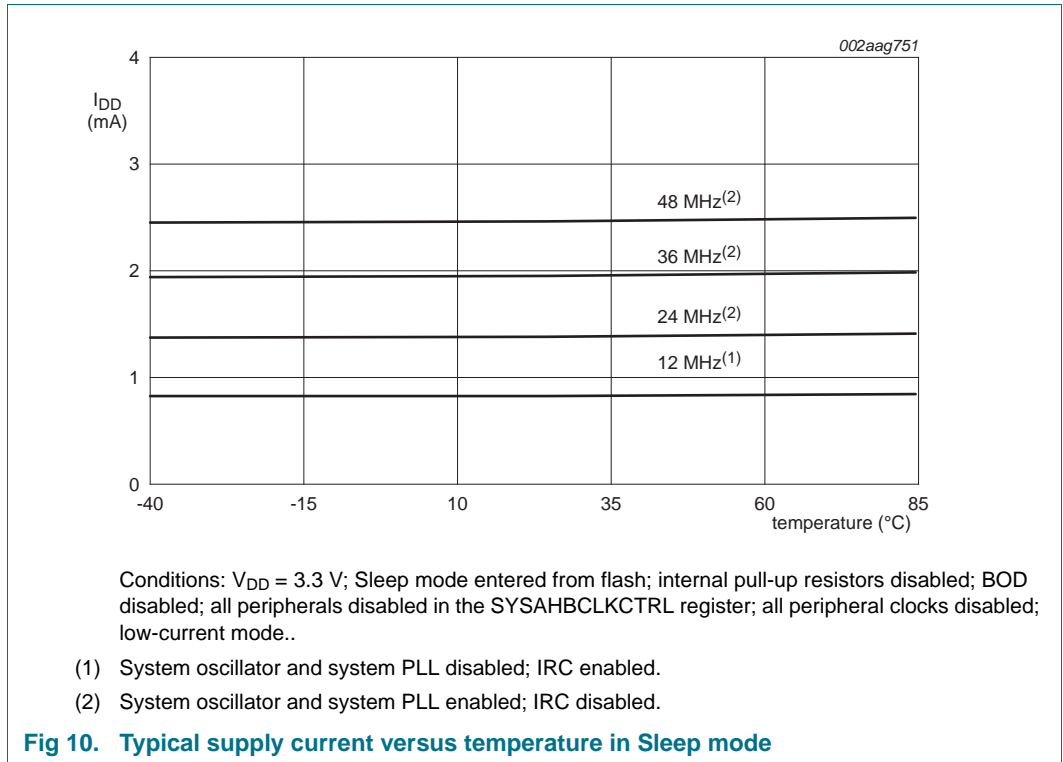
[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the LPC11Exx user manual*.

## 9.2 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see the *LPC11Exx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIODIR registers.
- Write 0 to all GPIODATA registers to drive the outputs LOW.





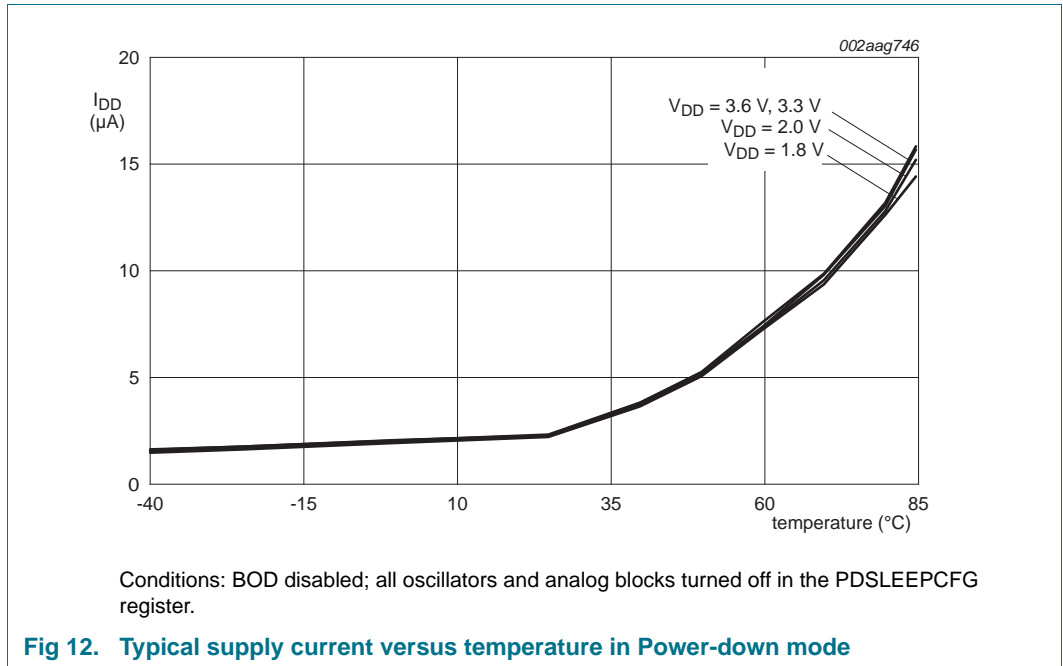


Fig 12. Typical supply current versus temperature in Power-down mode

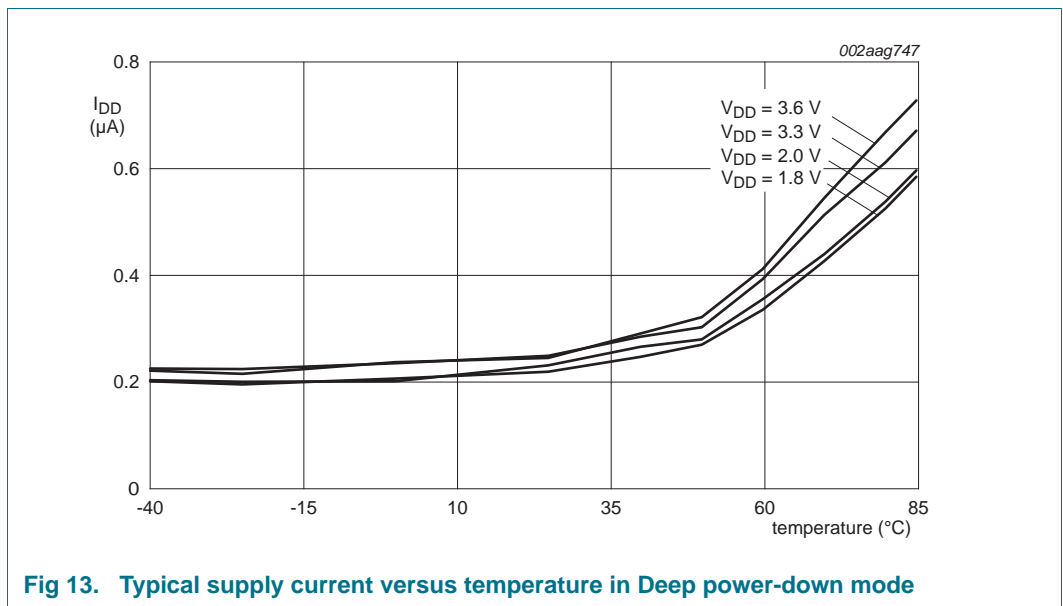


Fig 13. Typical supply current versus temperature in Deep power-down mode

### 9.3 Peripheral power consumption

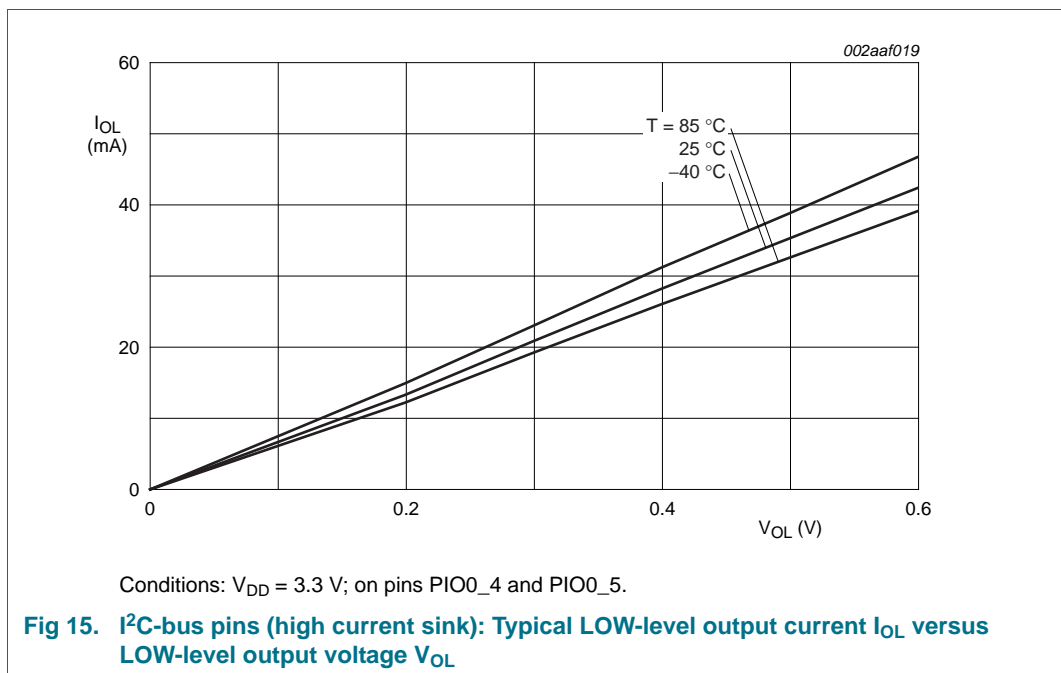
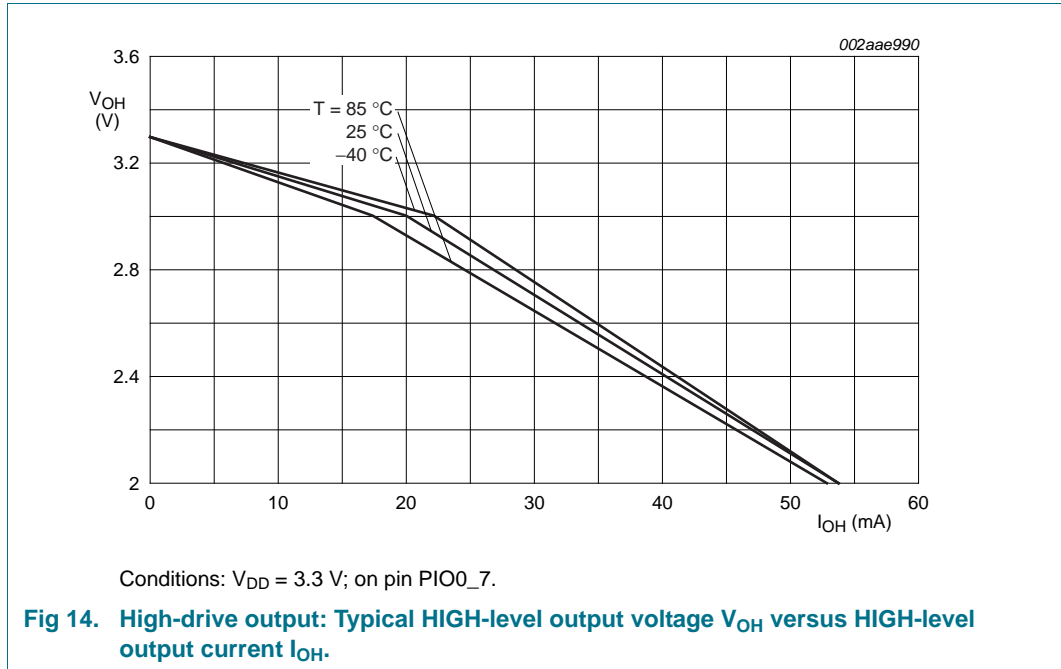
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at  $T_{amb} = 25^{\circ}C$ . Unless noted otherwise, the system oscillator and PLL are running in both measurements.

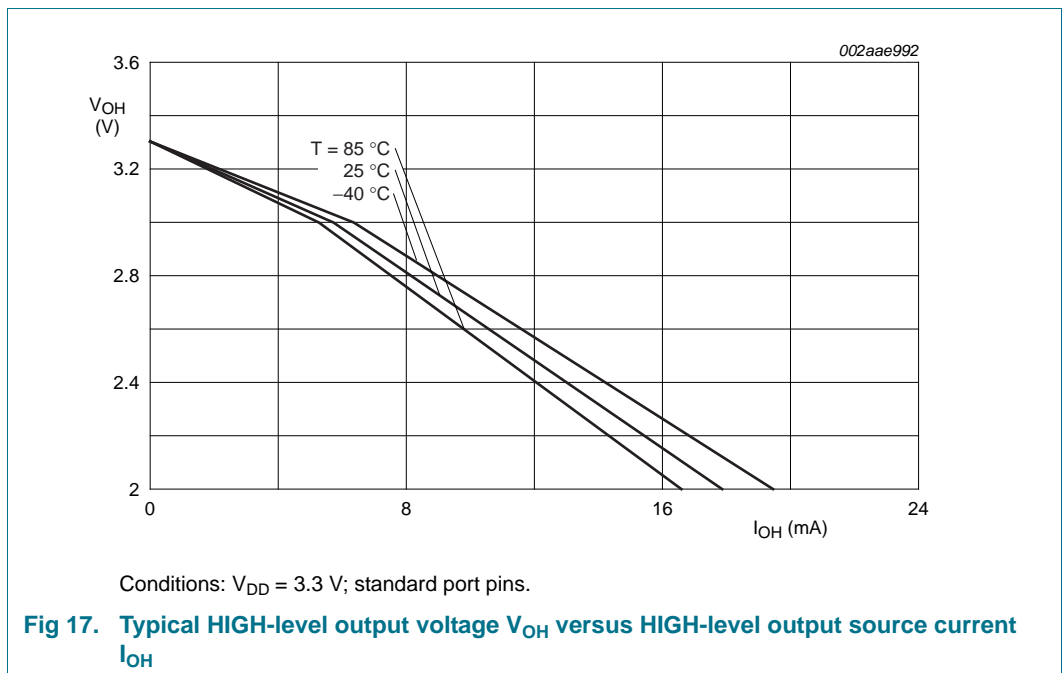
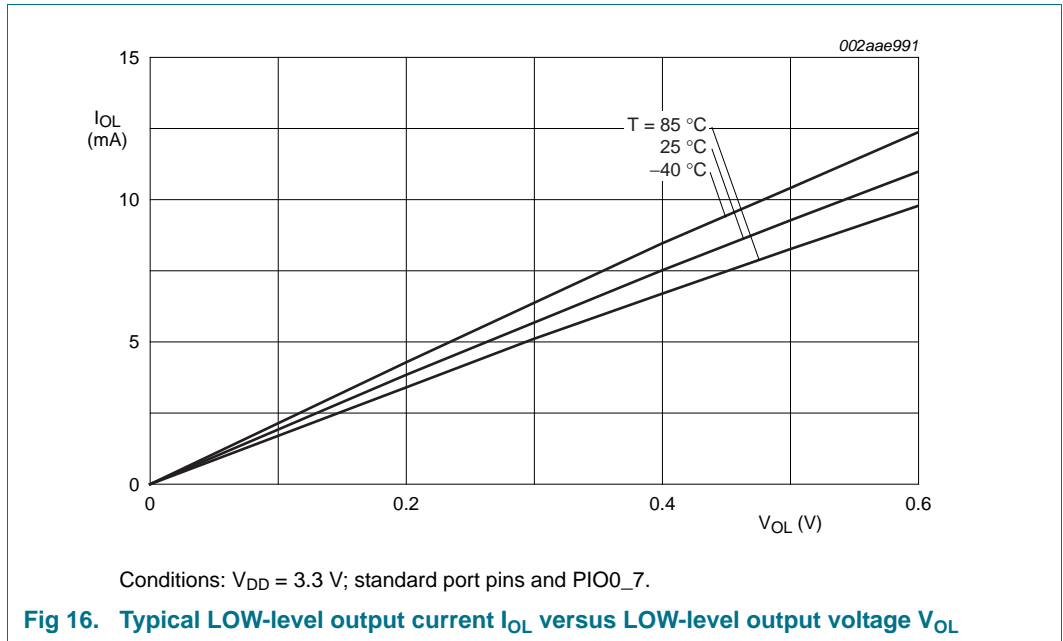
The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

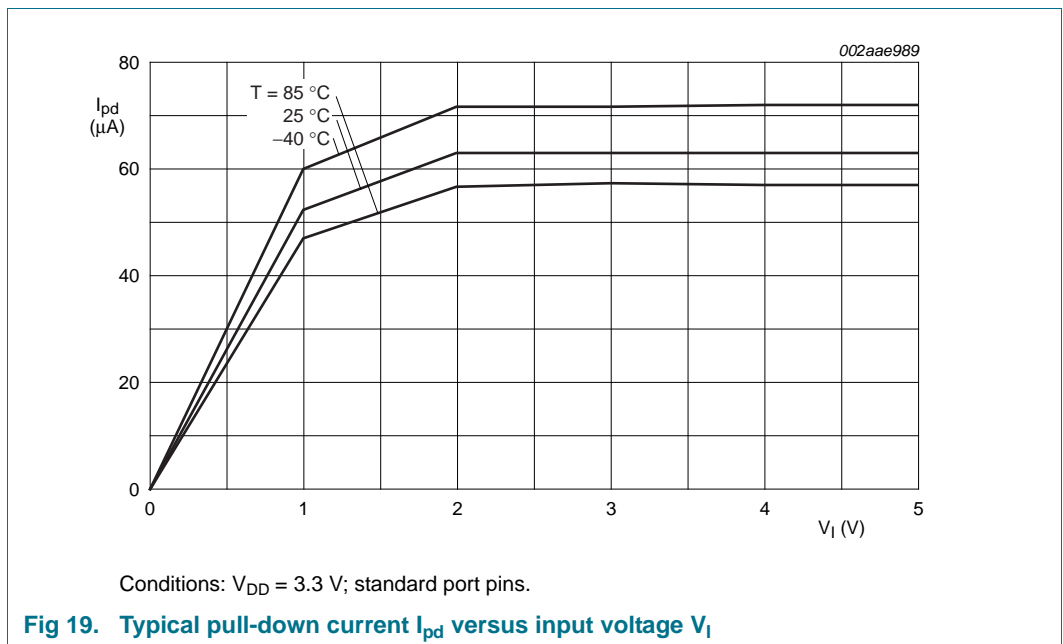
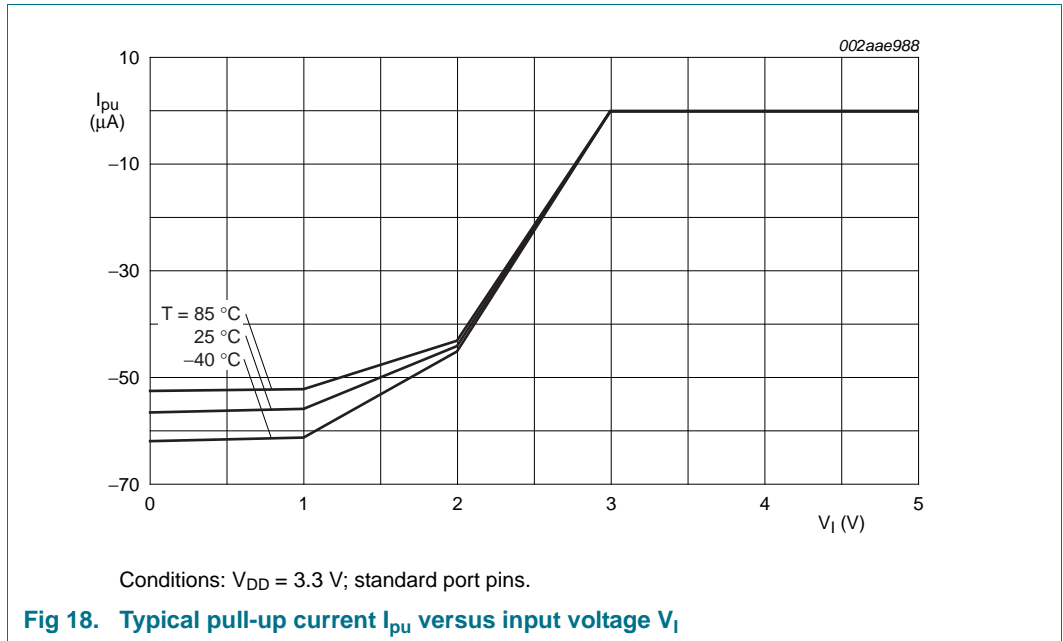
**Table 8. Power consumption for individual analog and digital blocks**

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	-
ADC	-	0.08	0.29	-
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	-
CT16B1	-	0.02	0.06	-
CT32B0	-	0.02	0.07	-
CT32B1	-	0.02	0.06	-
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	-
I2C	-	0.04	0.13	-
ROM	-	0.04	0.15	-
SPI0	-	0.12	0.45	-
SPI1	-	0.12	0.45	-
UART	-	0.22	0.82	-
WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.

9.4 Electrical pin characteristics







## 10. Dynamic characteristics

### 10.1 Flash memory

**Table 9. Flash characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{endu}$	endurance		[1] 10000	100000	-	cycles
$t_{ret}$	retention time	powered	10	-	-	years
		unpowered	20	-	-	years
$t_{er}$	erase time	sector or multiple consecutive sectors	95	100	105	ms
$t_{prog}$	programming time		[2] 0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

**Table 10. EEPROM characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{DD} = 2.7\text{ V}$  to  $3.6\text{ V}$ . Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk}$	clock frequency		200	375	400	kHz
$N_{endu}$	endurance		100000	1000000	-	cycles
$t_{ret}$	retention time	powered	100	200	-	years
		unpowered	150	300	-	years
$t_{er}$	erase time	64 bytes	-	1.8	-	ms
$t_{prog}$	programming time	64 bytes	-	1.1	-	ms

### 10.2 External clock

**Table 11. Dynamic characteristic: external clock**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{DD}$  over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc}$	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
$t_{CHCX}$	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
$t_{CLCX}$	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
$t_{CLCH}$	clock rise time		-	-	5	ns
$t_{CHCL}$	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

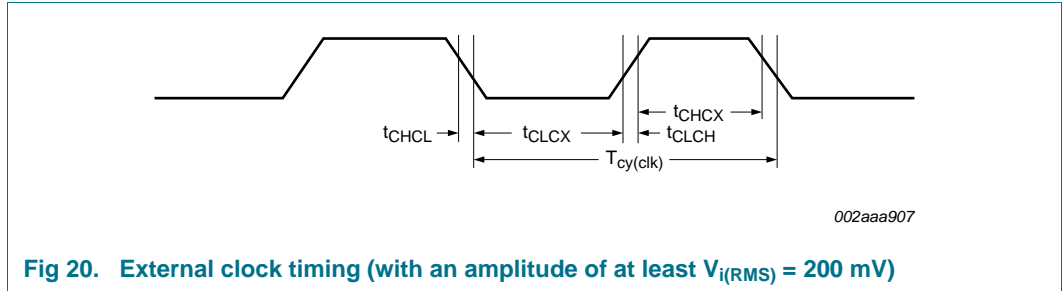


Fig 20. External clock timing (with an amplitude of at least  $V_{i(RMS)} = 200\text{ mV}$ )

### 10.3 Internal oscillators

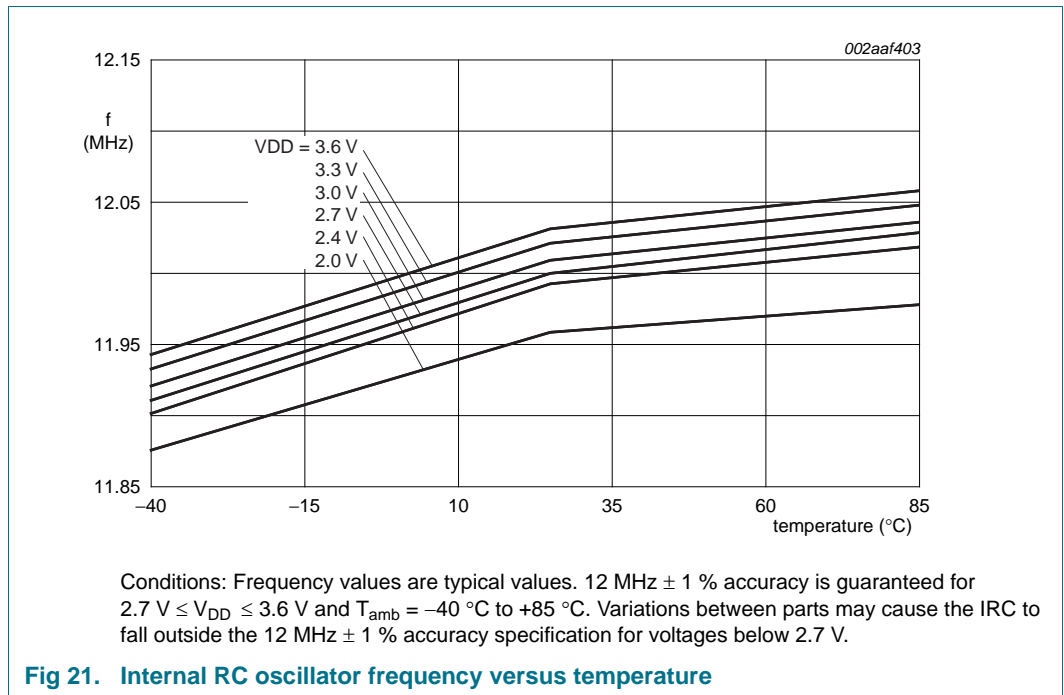
Table 12. Dynamic characteristics: IRC

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  [1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature ( $25\text{ }^{\circ}\text{C}$ ), nominal supply voltages.



Conditions: Frequency values are typical values.  $12\text{ MHz} \pm 1\%$  accuracy is guaranteed for  $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  and  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ . Variations between parts may cause the IRC to fall outside the  $12\text{ MHz} \pm 1\%$  accuracy specification for voltages below 2.7 V.

Fig 21. Internal RC oscillator frequency versus temperature

Table 13. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit	
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

- [2] The typical frequency spread over processing and temperature ( $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ) is  $\pm 40\%$ .
- [3] See the *LPC11Exx user manual*.

## 10.4 I/O pins

**Table 14. Dynamic characteristics: I/O pins<sup>[1]</sup>**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_r$	rise time	pin configured as output	3.0	-	5.0	ns
$t_f$	fall time	pin configured as output	2.5	-	5.0	ns

- [1] Applies to standard port pins and  $\overline{\text{RESET}}$  pin.

## 10.5 I<sup>2</sup>C-bus

**Table 15. Dynamic characteristic: I<sup>2</sup>C-bus pins<sup>[1]</sup>**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .<sup>[2]</sup>

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{SCL}$	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz
$t_f$	fall time	<a href="#">[4][5][6][7]</a> of both SDA and SCL signals	-	300	ns
		Standard-mode			
		Fast-mode	$20 + 0.1 \times C_b$	300	ns
$t_{LOW}$	LOW period of the SCL clock	Standard-mode	4.7	-	$\mu\text{s}$
		Fast-mode	1.3	-	$\mu\text{s}$
		Fast-mode Plus	0.5	-	$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock	Standard-mode	4.0	-	$\mu\text{s}$
		Fast-mode	0.6	-	$\mu\text{s}$
		Fast-mode Plus	0.26	-	$\mu\text{s}$
$t_{HD;DAT}$	data hold time	<a href="#">[3][4][8]</a> Standard-mode	0	-	$\mu\text{s}$
		Fast-mode	0	-	$\mu\text{s}$
		Fast-mode Plus	0	-	$\mu\text{s}$
$t_{SU;DAT}$	data set-up time	<a href="#">[9][10]</a> Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus	50	-	ns

- [1] See the I<sup>2</sup>C-bus specification *UM10204* for details.
- [2] Parameters are valid over operating temperature range unless otherwise specified.
- [3]  $t_{HD;DAT}$  is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.
- [4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the  $V_{IH}(\text{min})$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- [5]  $C_b$  = total capacitance of one bus line in pF.
- [6] The maximum  $t_f$  for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage  $t_f$  is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified  $t_f$ .

- [7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- [8] The maximum  $t_{HD;DAT}$  could be 3.45  $\mu$ s and 0.9  $\mu$ s for Standard-mode and Fast-mode but must be less than the maximum of  $t_{VD;DAT}$  or  $t_{VD;ACK}$  by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
- [9]  $t_{SU;DAT}$  is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.
- [10] A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system but the requirement  $t_{SU;DAT} = 250$  ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$  ns (according to the Standard-mode I<sup>2</sup>C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

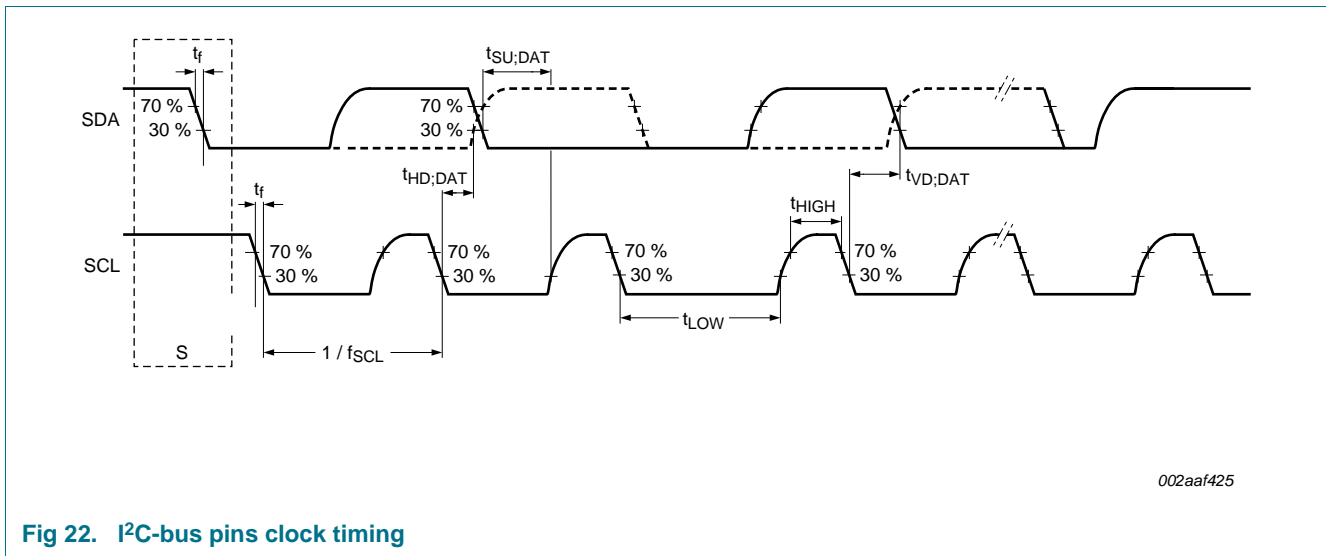


Fig 22. I<sup>2</sup>C-bus pins clock timing

## 10.6 SSP interface

Table 16. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>SPI master (in SPI mode)</b>							
$T_{cy(\text{clk})}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40	-	-	ns
$t_{DS}$	data set-up time	in SPI mode	[2]	15	-	-	ns
		$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$					
		$2.0\text{ V} \leq V_{DD} < 2.4\text{ V}$	[2]	20			ns
		$1.8\text{ V} \leq V_{DD} < 2.0\text{ V}$	[2]	24	-	-	ns
$t_{DH}$	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
<b>SPI slave (in SPI mode)</b>							
$T_{cy(\text{PCLK})}$	PCLK cycle time			20	-	-	ns
$t_{DS}$	data set-up time	in SPI mode	[3][4]	0	-	-	ns
$t_{DH}$	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(\text{PCLK})} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(\text{PCLK})} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(\text{PCLK})} + 5$	ns

[1]  $T_{cy(\text{clk})} = (\text{SSPCLKDIV} \times (1 + \text{SCR}) \times \text{CPSDVSR}) / f_{\text{main}}$ . The clock cycle time derived from the SPI bit rate  $T_{cy(\text{clk})}$  is a function of the main clock frequency  $f_{\text{main}}$ , the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2]  $T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ .

[3]  $T_{cy(\text{clk})} = 12 \times T_{cy(\text{PCLK})}$ .

[4]  $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ ; for normal voltage supply range:  $V_{DD} = 3.3\text{ V}$ .

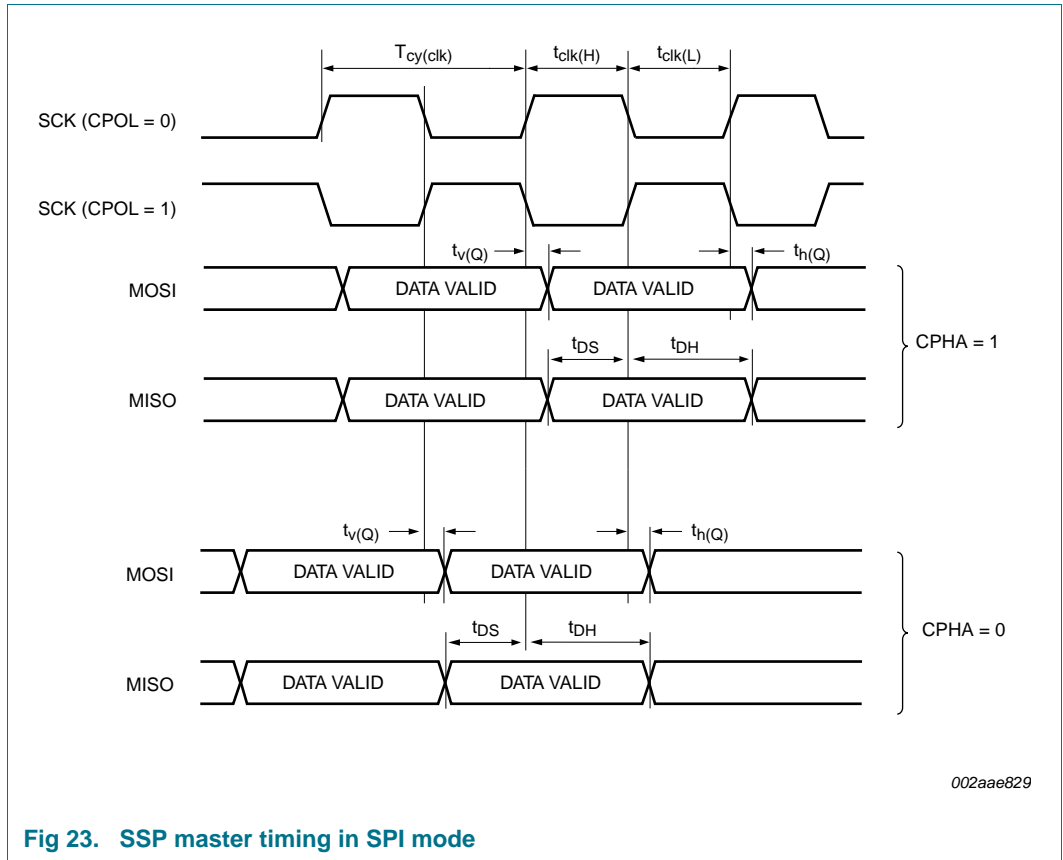


Fig 23. SSP master timing in SPI mode

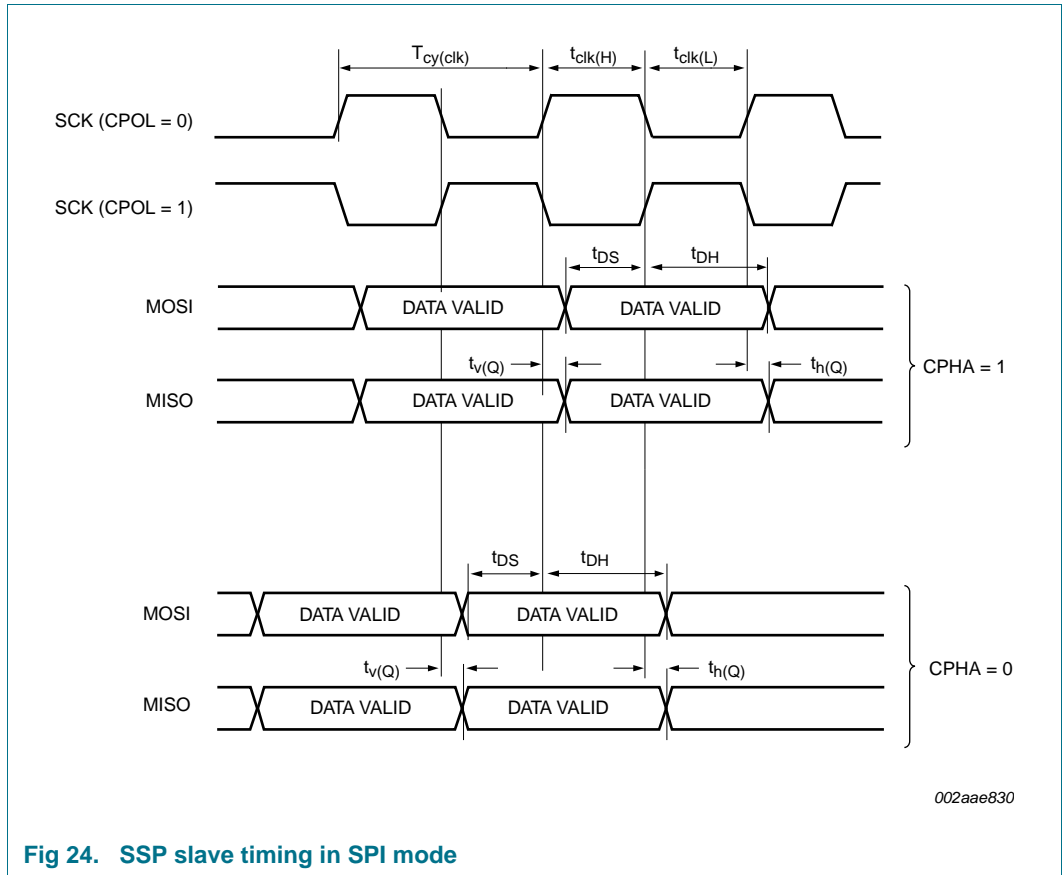


Fig 24. SSP slave timing in SPI mode

## 11. Application information

### 11.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with  $C_i = 100$  pF. To limit the input voltage to the specified range, choose an additional capacitor to ground  $C_g$  which attenuates the input voltage by a factor  $C_i / (C_i + C_g)$ . In slave mode, a minimum of 200 mV (RMS) is needed.

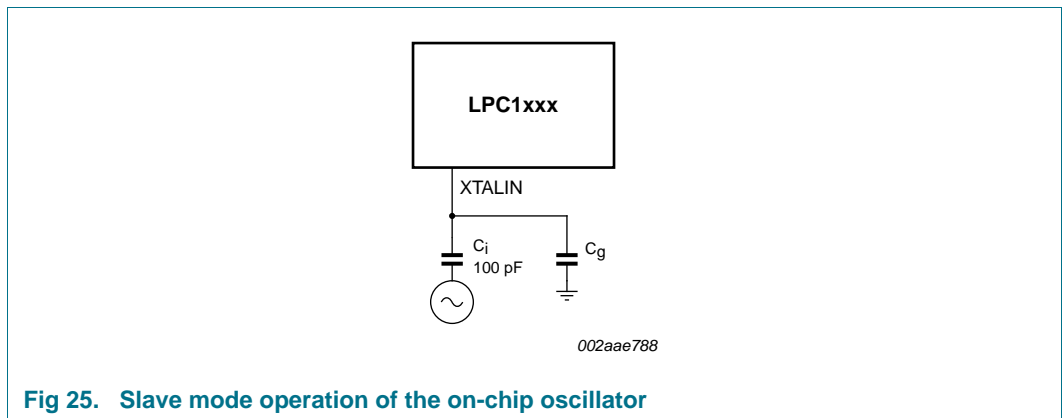
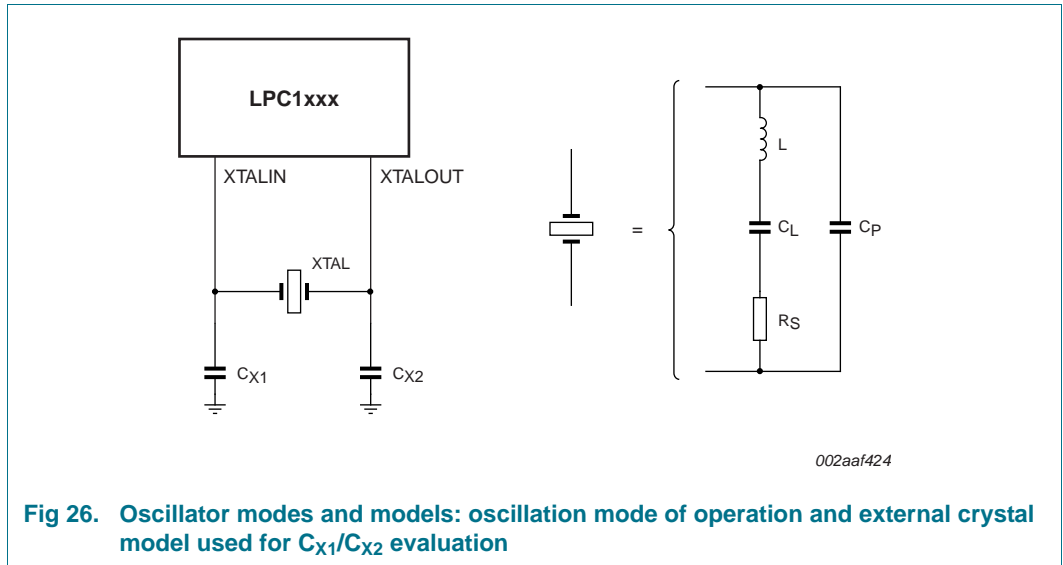


Fig 25. Slave mode operation of the on-chip oscillator

In slave mode, couple the input clock signal with a capacitor of 100 pF (Figure 25), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This signal corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 26 and in Table 17 and Table 18. Since the feedback resistance is integrated on chip, only a crystal and the capacitances  $C_{X1}$  and  $C_{X2}$  need to be connected externally in case of fundamental mode oscillation ( $L$ ,  $C_L$  and  $R_S$  represent the fundamental frequency). Capacitance  $C_P$  in Figure 26 represents the parallel package capacitance and must not be larger than 7 pF. Parameters  $F_{OSC}$ ,  $C_L$ ,  $R_S$  and  $C_P$  are supplied by the crystal manufacturer.



**Table 17. Recommended values for  $C_{X1}/C_{X2}$  in oscillation mode (crystal and external components parameters) low frequency mode**

Fundamental oscillation frequency $F_{osc}$	Crystal load capacitance $C_L$	Maximum crystal series resistance $R_S$	External load capacitors $C_{X1}, C_{X2}$
1 MHz - 5 MHz	10 pF	< 300 $\Omega$	18 pF, 18 pF
	20 pF	< 300 $\Omega$	39 pF, 39 pF
	30 pF	< 300 $\Omega$	57 pF, 57 pF
5 MHz - 10 MHz	10 pF	< 300 $\Omega$	18 pF, 18 pF
	20 pF	< 200 $\Omega$	39 pF, 39 pF
	30 pF	< 100 $\Omega$	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 $\Omega$	18 pF, 18 pF
	20 pF	< 60 $\Omega$	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 $\Omega$	18 pF, 18 pF

**Table 18. Recommended values for  $C_{X1}/C_{X2}$  in oscillation mode (crystal and external components parameters) high frequency mode**

Fundamental oscillation frequency $F_{osc}$	Crystal load capacitance $C_L$	Maximum crystal series resistance $R_S$	External load capacitors $C_{X1}, C_{X2}$
15 MHz - 20 MHz	10 pF	< 180 $\Omega$	18 pF, 18 pF
	20 pF	< 100 $\Omega$	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 $\Omega$	18 pF, 18 pF
	20 pF	< 80 $\Omega$	39 pF, 39 pF

## 11.2 XTAL Printed-Circuit Board (PCB) layout guidelines

Follow these guidelines for PCB layout:

- Connect the crystal on the PCB as close as possible to the oscillator input and output pins of the chip.
- Take care that the load capacitors  $C_{x1}$ ,  $C_{x2}$ , and  $C_{x3}$  in case of third overtone crystal use have a common ground plane.

- Connect the external components to the ground plain.
- To keep parasitics and the noise coupled in via the PCB as small as possible, keep loops as small as possible.
- Choose smaller values of  $C_{x1}$  and  $C_{x2}$  if parasitics of the PCB layout increase.

### 11.3 Standard I/O pad configuration

Figure 27 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

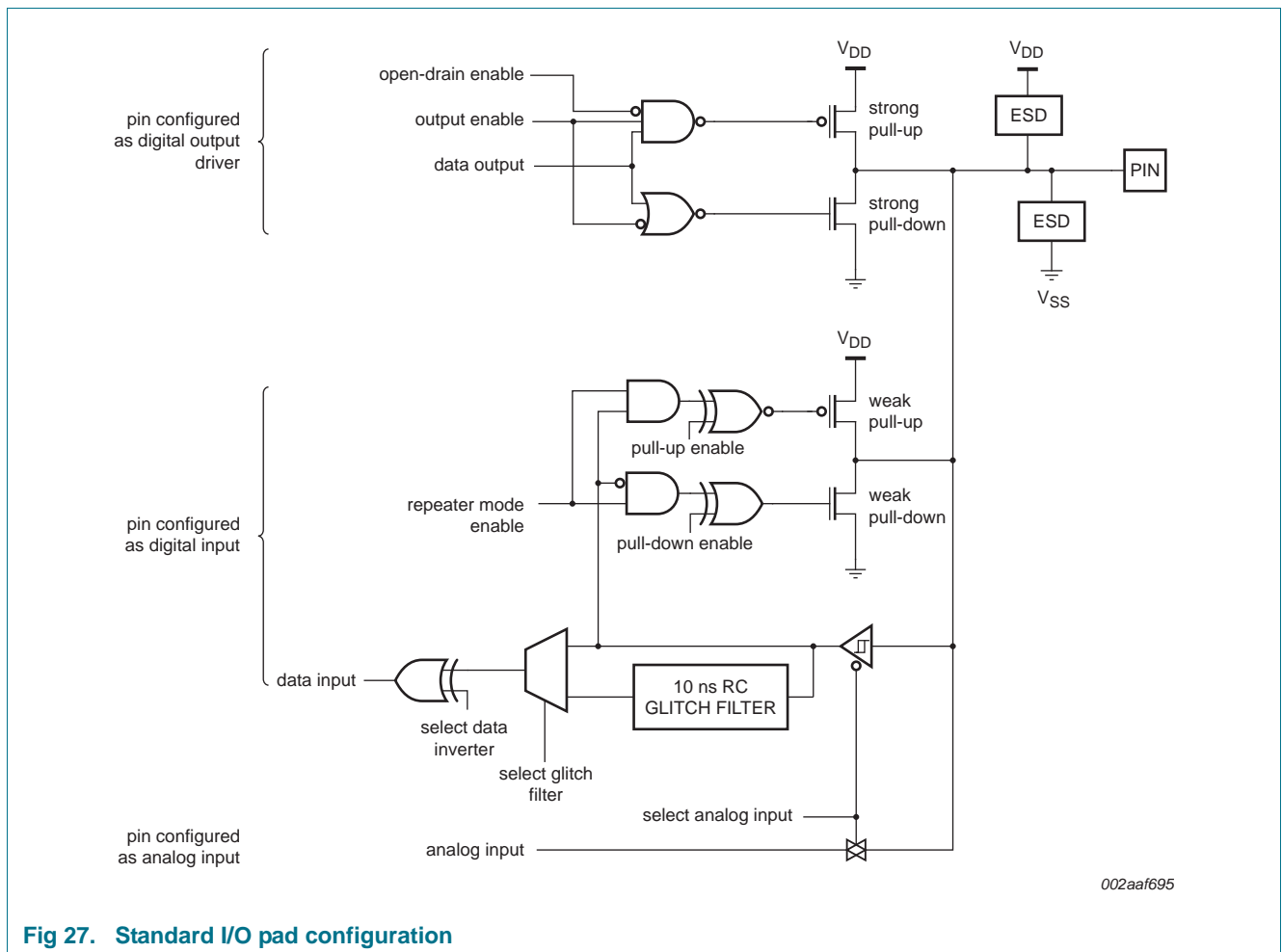


Fig 27. Standard I/O pad configuration

## 11.4 Reset pad configuration

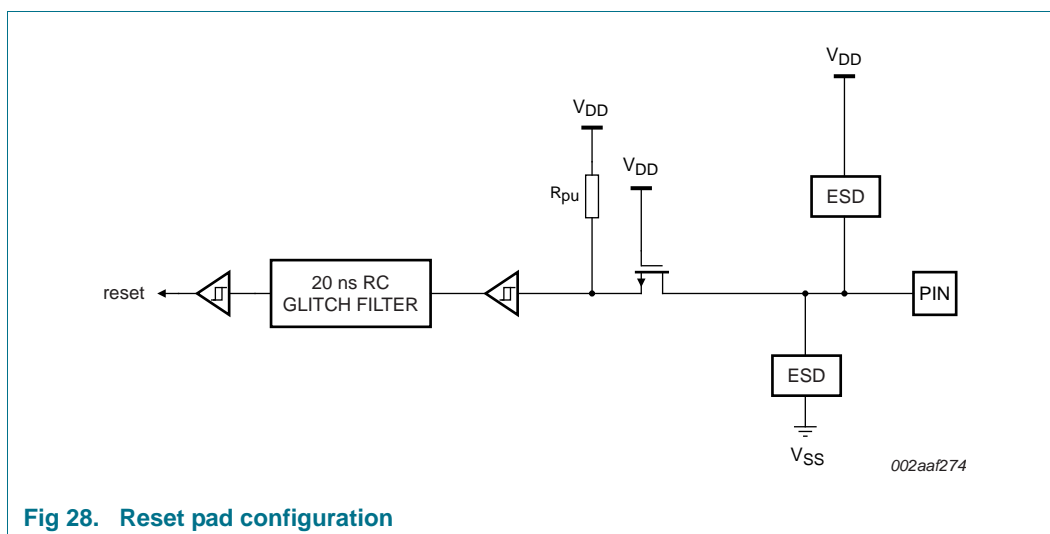


Fig 28. Reset pad configuration

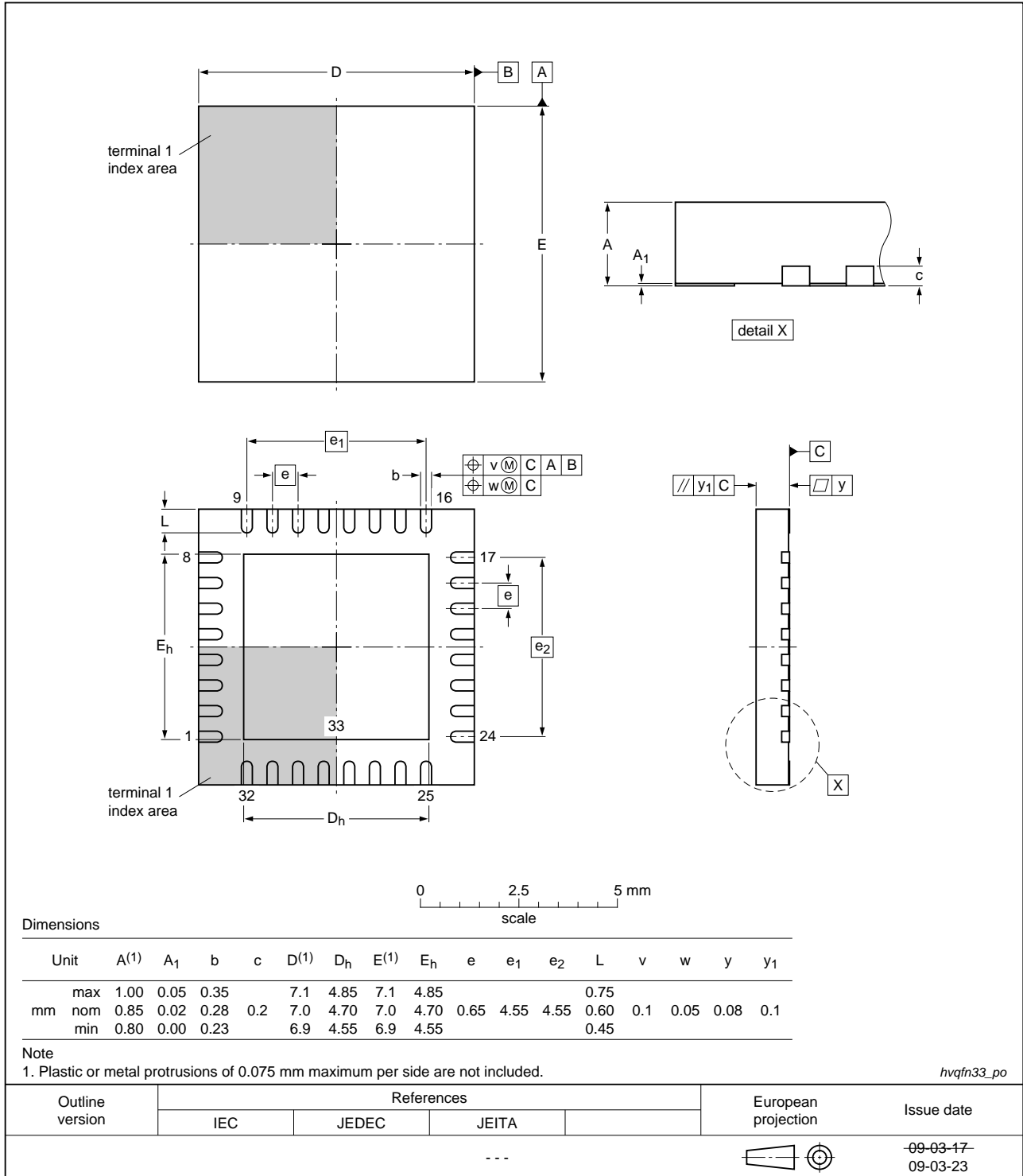
## 11.5 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in [Table 6](#):

- The ADC input trace must be short and as close as possible to the LPC11E3x chip.
- Shield The ADC input traces from fast switching digital signals and noisy power supply lines.
- The ADC and the digital core share the same power supply. Therefore, filter the power supply line adequately.
- To improve the ADC performance in a noisy environment, put the device in Sleep mode during the ADC conversion.

## 12. Package outline

**HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm**



**Fig 29. Package outline HVQFN33 (7 x 7 x 0.85 mm)**

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2

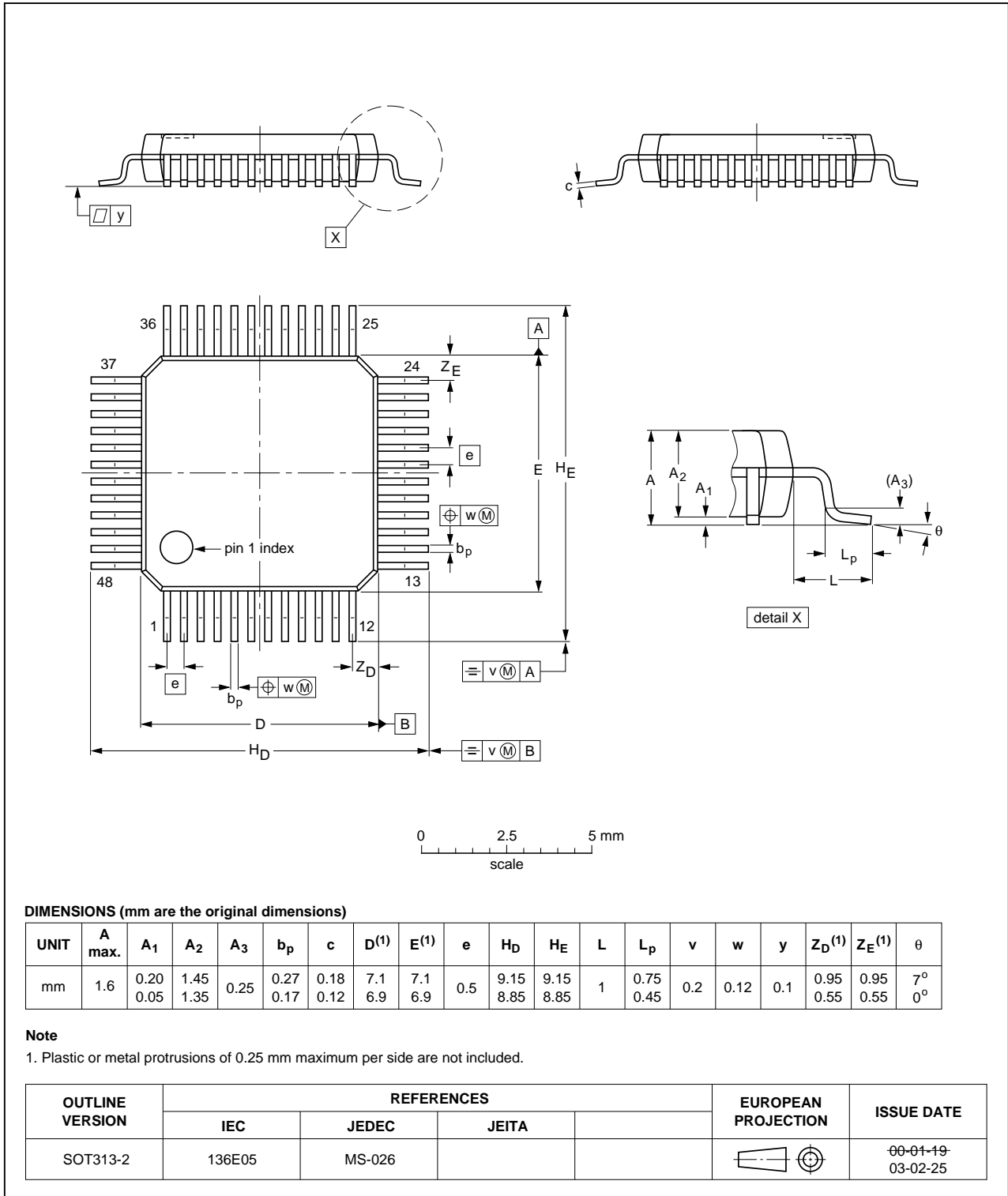


Fig 30. Package outline LQFP48 (SOT313-2)

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm

SOT314-2

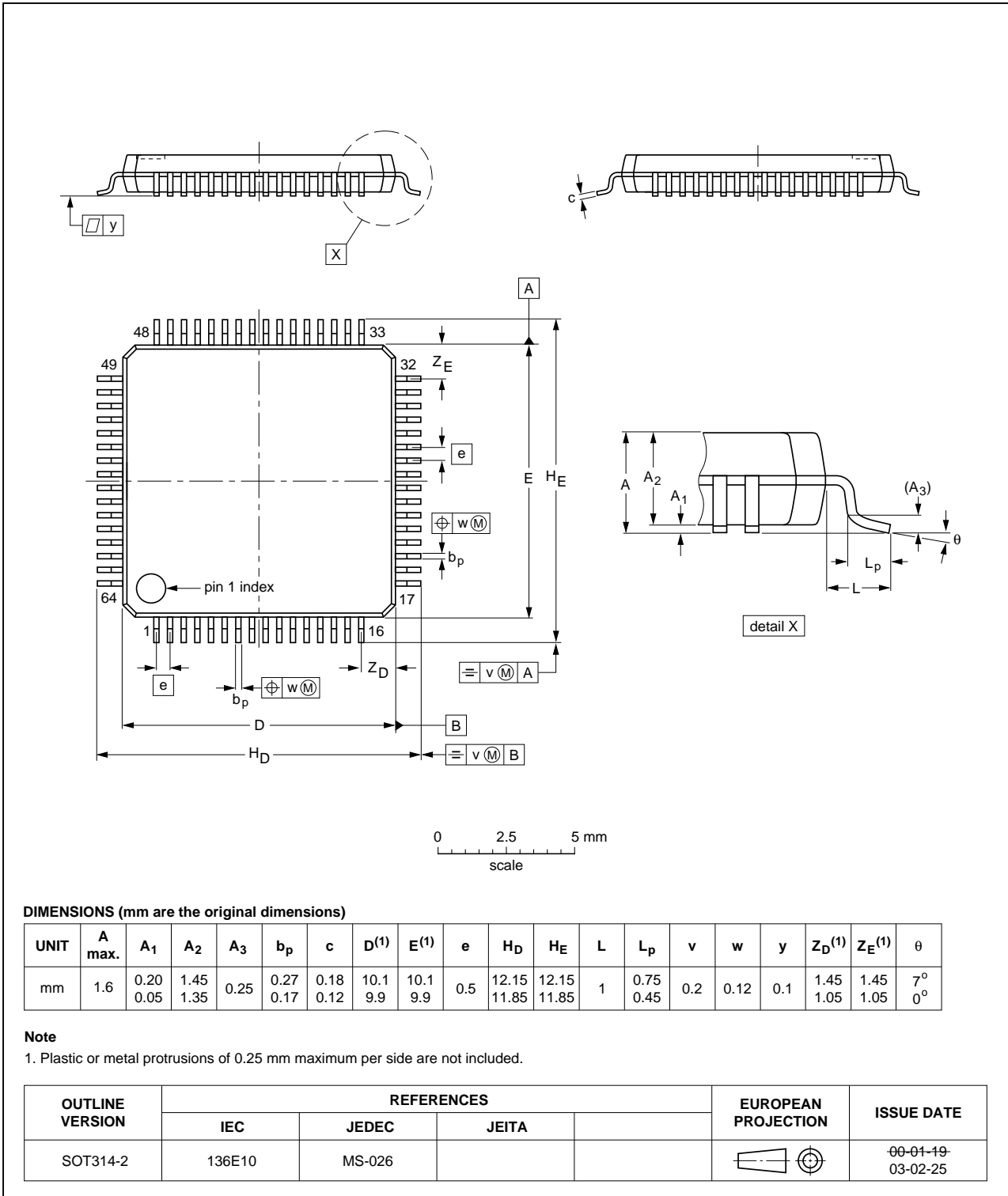
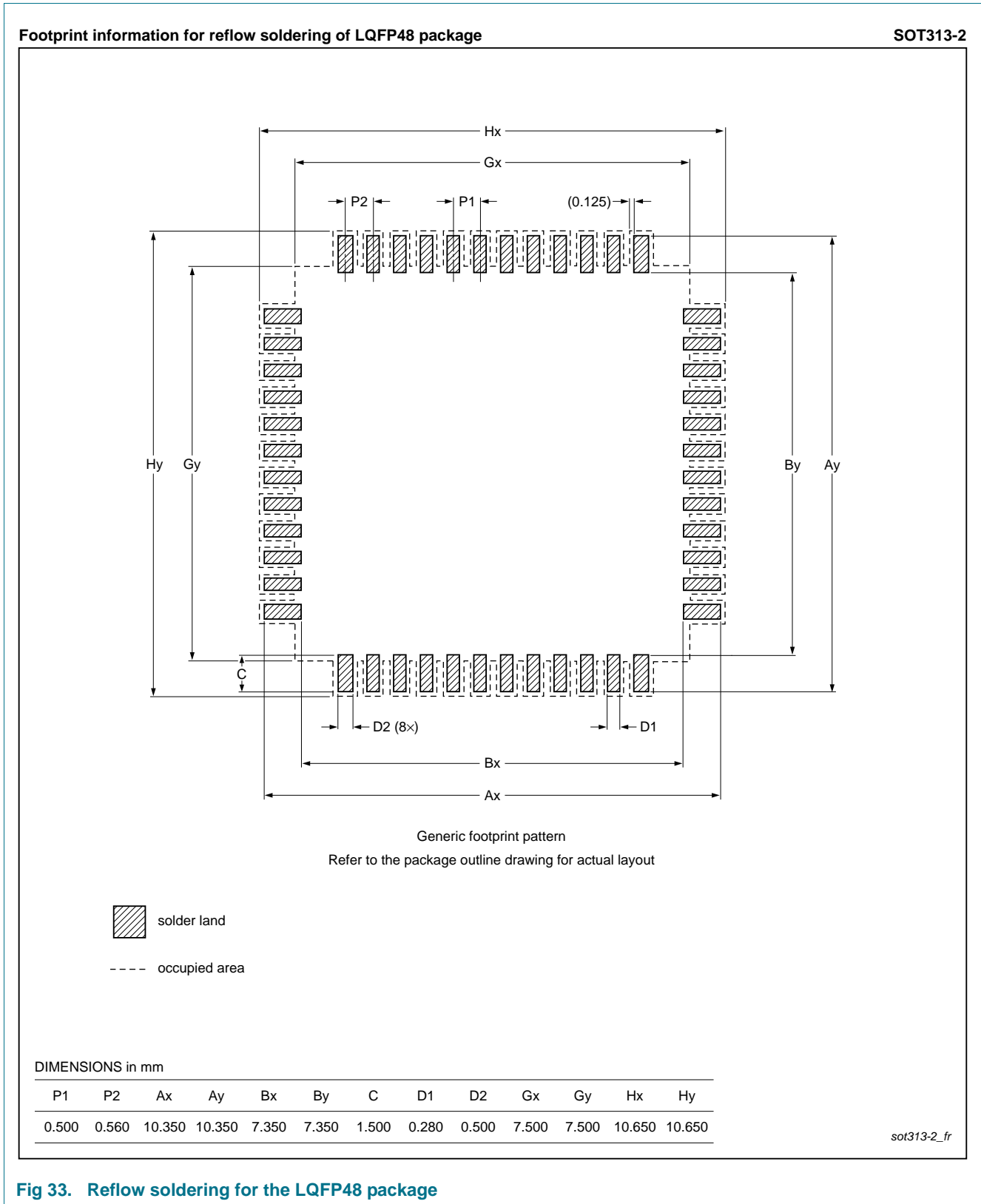
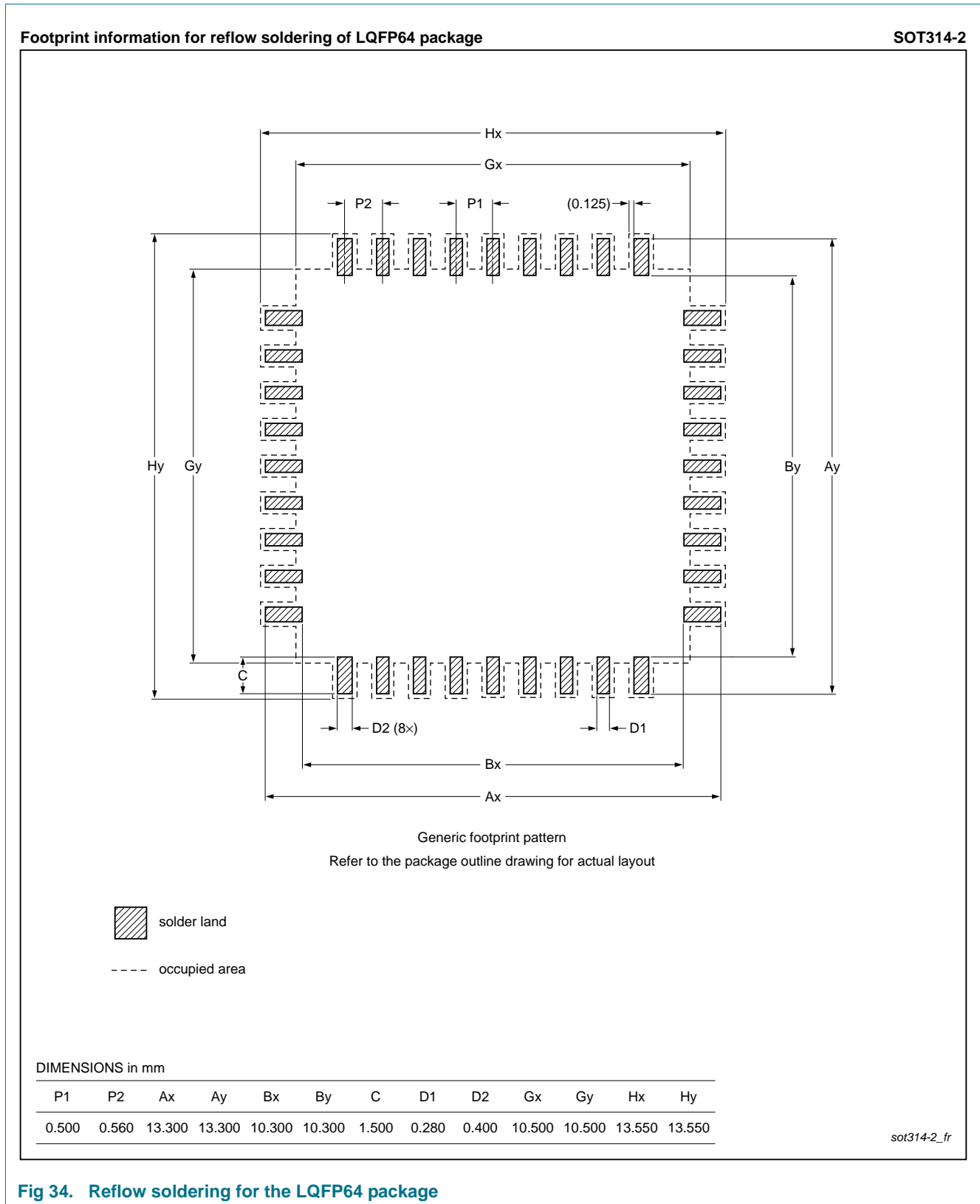


Fig 31. Package outline LQFP64 (SOT314-2)





**Fig 33. Reflow soldering for the LQFP48 package**



**Fig 34. Reflow soldering for the LQFP64 package**

## 14. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11E3X v.1	20121107	Objective data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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## 17. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>	7.16.5.3	Deep-sleep mode	24
<b>2</b>	<b>Features and benefits</b> . . . . .	<b>1</b>	7.16.5.4	Power-down mode	24
<b>3</b>	<b>Applications</b> . . . . .	<b>3</b>	7.16.5.5	Deep power-down mode	24
<b>4</b>	<b>Ordering information</b> . . . . .	<b>3</b>	7.16.6	System control	25
4.1	Ordering options	4	7.16.6.1	Reset	25
<b>5</b>	<b>Block diagram</b> . . . . .	<b>5</b>	7.16.6.2	Brownout detection	25
<b>6</b>	<b>Pinning information</b> . . . . .	<b>6</b>	7.16.6.3	Code security (Code Read Protection - CRP)	25
6.1	Pinning	6	7.16.6.4	APB interface	26
6.2	Pin description	9	7.16.6.5	AHBLite	26
<b>7</b>	<b>Functional description</b> . . . . .	<b>14</b>	7.16.6.6	External interrupt inputs	26
7.1	On-chip flash programming memory	14	7.17	Emulation and debugging	27
7.2	EEPROM	14	<b>8</b>	<b>Limiting values</b>	<b>28</b>
7.3	SRAM	14	<b>9</b>	<b>Static characteristics</b>	<b>29</b>
7.4	On-chip ROM	15	9.1	BOD static characteristics	34
7.5	Memory map	15	9.2	Power consumption	34
7.6	Nested Vectored Interrupt Controller (NVIC)	16	9.3	Peripheral power consumption	37
7.6.1	Features	16	9.4	Electrical pin characteristics	39
7.6.2	Interrupt sources	17	<b>10</b>	<b>Dynamic characteristics</b>	<b>42</b>
7.7	IOCON block	17	10.1	Flash memory	42
7.7.1	Features	17	10.2	External clock	42
7.8	General-Purpose Input/Output GPIO	17	10.3	Internal oscillators	43
7.8.1	Features	18	10.4	I/O pins	44
7.9	USART	18	10.5	I <sup>2</sup> C-bus	44
7.9.1	Features	18	10.6	SSP interface	46
7.10	SSP serial I/O controller	18	<b>11</b>	<b>Application information</b>	<b>49</b>
7.10.1	Features	18	11.1	XTAL input	49
7.11	I <sup>2</sup> C-bus serial I/O controller	19	11.2	XTAL Printed-Circuit Board (PCB) layout guidelines	50
7.11.1	Features	19	11.3	Standard I/O pad configuration	52
7.12	10-bit ADC	19	11.4	Reset pad configuration	53
7.12.1	Features	19	11.5	ADC usage notes	53
7.13	General purpose external event counter/timers	20	<b>12</b>	<b>Package outline</b>	<b>54</b>
7.13.1	Features	20	<b>13</b>	<b>Soldering</b>	<b>57</b>
7.14	System tick timer	20	<b>14</b>	<b>Revision history</b>	<b>60</b>
7.15	Windowed WatchDog Timer (WWDT)	20	<b>15</b>	<b>Legal information</b>	<b>61</b>
7.15.1	Features	20	15.1	Data sheet status	61
7.16	Clocking and power control	21	15.2	Definitions	61
7.16.1	Integrated oscillators	21	15.3	Disclaimers	61
7.16.1.1	Internal RC oscillator	22	15.4	Trademarks	62
7.16.1.2	System oscillator	22	<b>16</b>	<b>Contact information</b>	<b>62</b>
7.16.1.3	Watchdog oscillator	23	<b>17</b>	<b>Contents</b>	<b>63</b>
7.16.2	System PLL	23			
7.16.3	Clock output	23			
7.16.4	Wake-up process	23			
7.16.5	Power control	23			
7.16.5.1	Power profiles	23			
7.16.5.2	Sleep mode	24			

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