THE DATASHEET OF

1ED3323MC12NXUMA1

EiceDRIVER™ 1ED332xMC12N Enhanced (1ED-F3)

Datasheet

Single-channel 5.7 kV (rms) isolated gate driver IC with DESAT and soft-off

Features

- Single channel galvanically isolated coreless transformer (CT) gate driver
- Integrated protection features, such as short-circuit protection (DESAT), soft-off, active Miller Clamp and active shutdown
- For use with 600 V/650 V/1200 V/1700 V/2300 V IGBTs, Si and SiC MOSFETs
- Up to +6 A / -8.5 A typical peak output current
- 40 V absolute maximum output supply voltage *VCC2*
- High common-mode transient immunity CMTI > 300 kV/µs
- 85 ns short propagation delay (typ.)
- Tight IC-to-IC propagation delay matching (15 ns max.)
- 3.3 V and 5 V input supply voltage *VCC1*
- Suitable for operation at high ambient temperature and in fast switching applications
- DSO-16 wide body package with 8 mm creepage
- Safety certification:

  - UL 1577 (File E311313) with $V_{ISO,test}$ = 6840 V (rms) for 1 s, V_{ISO} = 5700 V (rms) for 60 s

  - Reinforced insulation according to IEC 60747-17 (Certificate no. 40055138) with V_{IORM} = 1767 V (peak, reinforced)

Potential applications

- Industrial motor drives - compact, standard, premium, servo drives
- Solar inverters, e.g., for 1500 V (DC) systems
- UPS systems
- High voltage DC-DC converter and DC-AC inverter
- Welding
- Commercial and agricultural vehicles (CAV)
- Commercial air-conditioning (CAC)
- High-voltage isolated DC-DC converters
- Isolated switch mode power supplies (SMPS)

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Device information

Product name	Gate drive current (typ.)	Outputs	UVLO (typ.)	Fault switch off	Package marking
1ED3320MC12N	+3.3 A / -6 A	*OUTH/OUTL*	12 V	Soft-off	1ED3320MC12
1ED3321MC12N	+6 A / -8.5 A	*OUTH/OUTL*	12 V	Soft-off	1ED3321MC12
1ED3322MC12N	+6 A / -8.5 A	*OUTH/OUTL*	13.6 V	Hard-off	1ED3322MC12
1ED3323MC12N	+6 A / -8.5 A	*OUT*	12 V	Hard-off	1ED3323MC12

Description

The 1ED332xMC12N (1ED-F3) is a EiceDRIVER™ Enhanced single channel galvanically isolated gate driver family with integrated protection features such as short circuit protection, active Miller Clamp and active shutdown for IGBT, MOSFET and SiC MOSFET in a DSO-16 wide body package. The products provide a typical output current up to +6 A / -8.5 A.

All logic pins are 3.3 V and 5 V CMOS-compatible and can be directly connected to a microcontroller. Data transfer across the galvanic isolation is realized by the integrated Coreless Transformer (CT) technology.

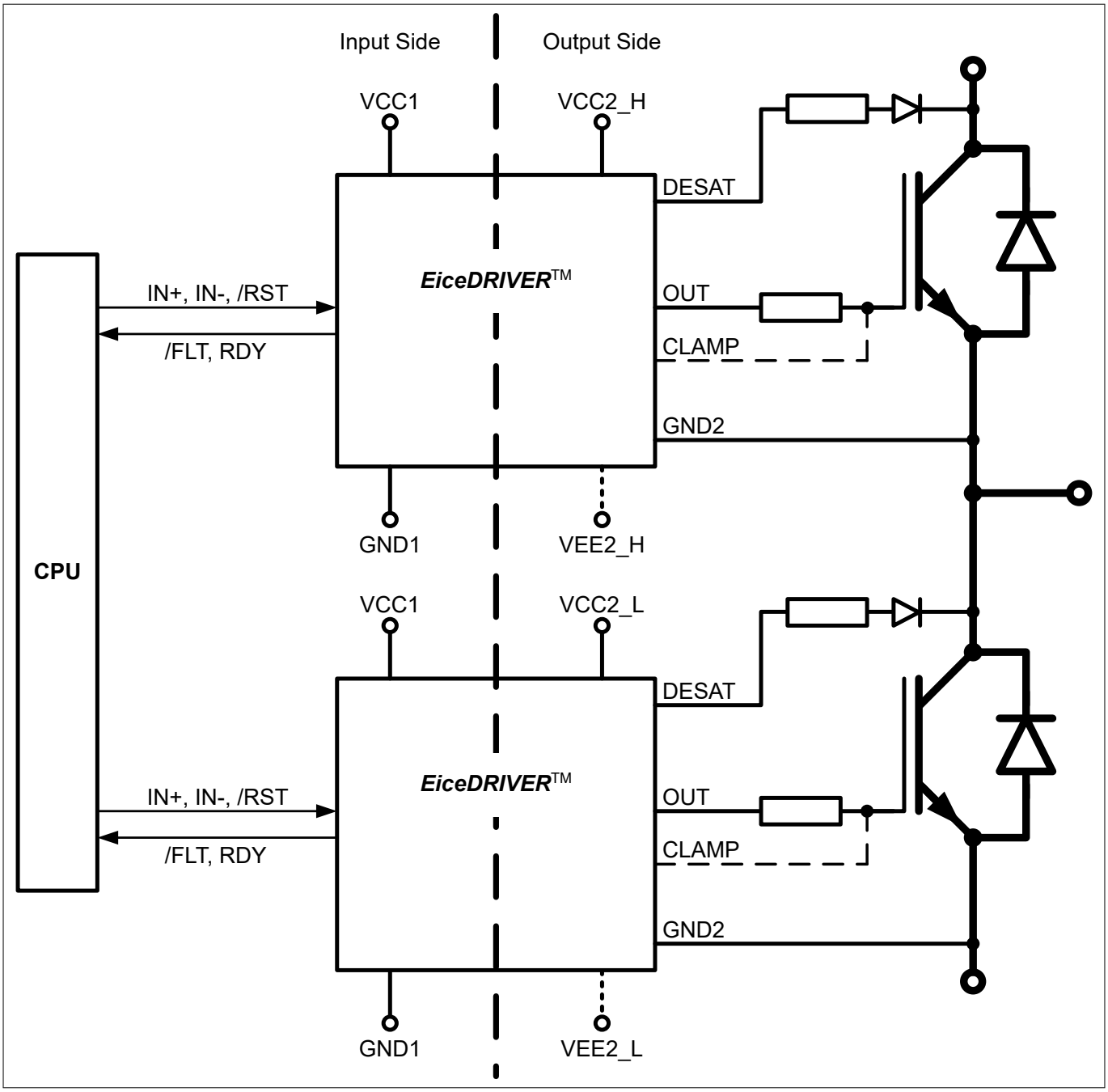

Figure 1 Typical application 1ED332xMC12N

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1 Block diagram

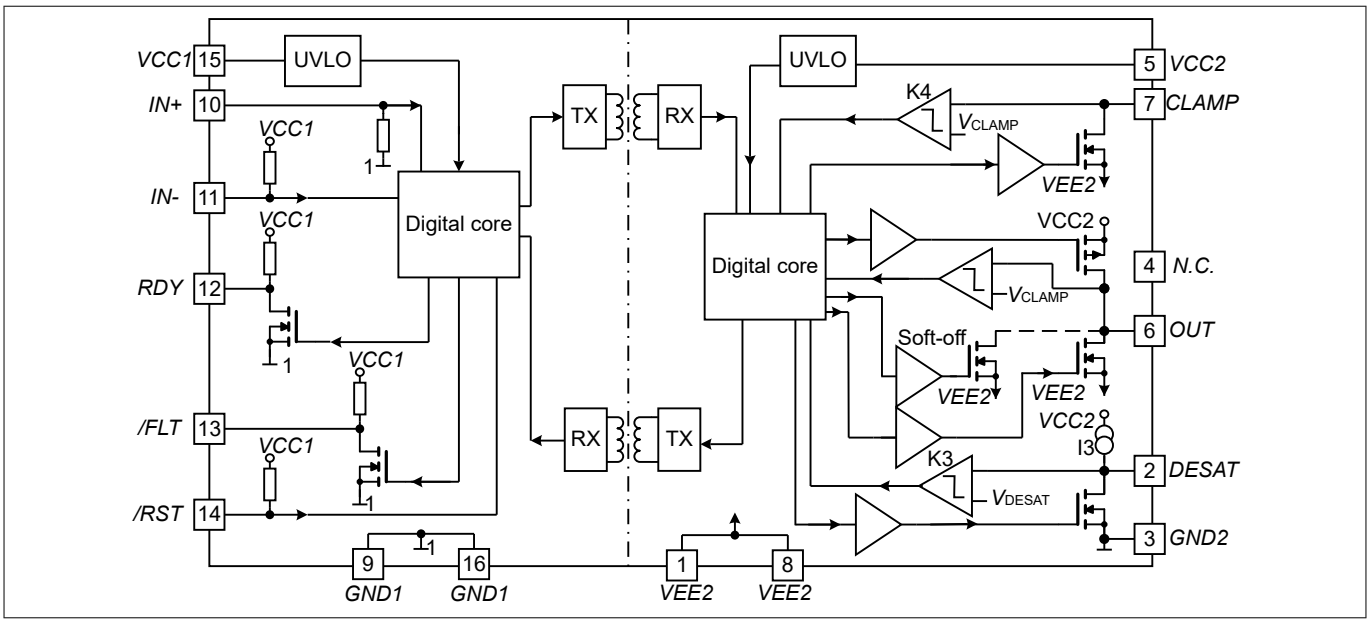

Figure 2 Block Diagram 1ED3323MC12N

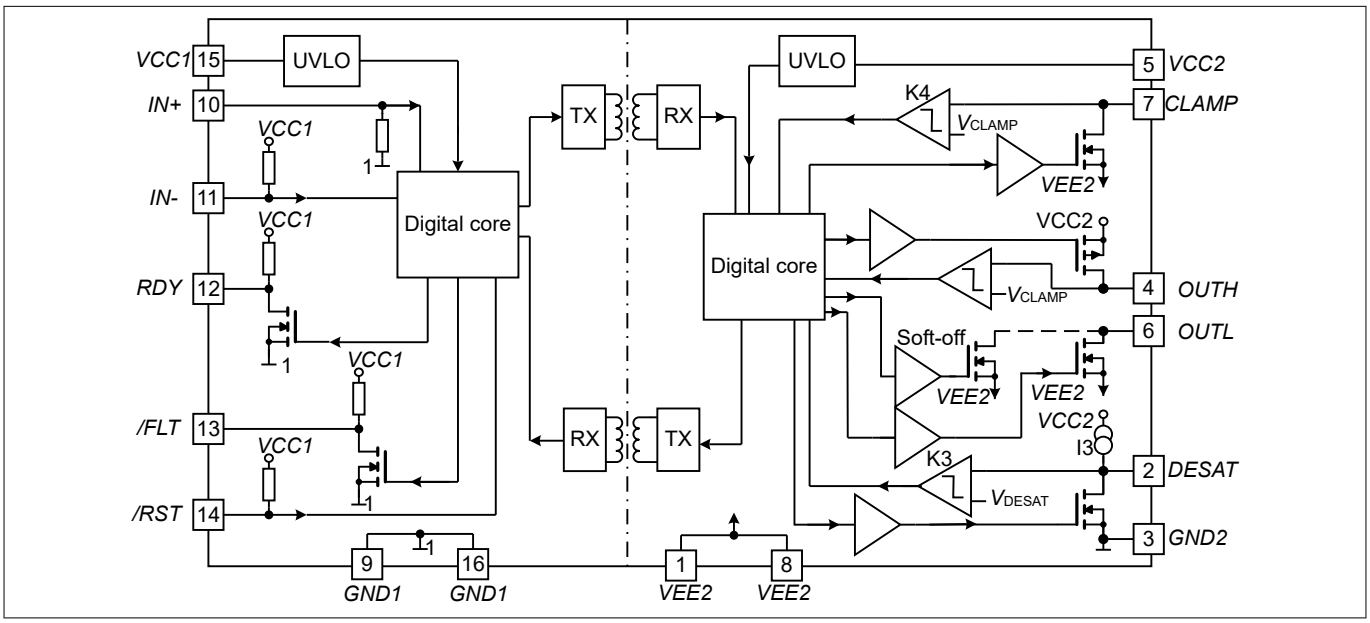

Figure 3 Block diagram 1ED3320MC12N, 1ED3321MC12N and 1ED3322MC12N

2 Related products

***Note**: Please consider the gate driver IC power dissipation and insulation requirements for the selected power switch and operating condition.*

Product group	Product name	Description
TRENCHSTOP™ IGBT Discrete	IKWH40N65WR6	650 V, 40 A IGBT with anti-parallel diode in TO-247-3-HCC
	IHW30N160R5	1600 V, 30 A IGBT Discrete with anti-parallel diode in TO-247
	IKW15N120CS7	1200 V IGBT7 S7, 15 A IGBT with anti-parallel diode in TO247
	IKQ75N120CS7	1200 V IGBT7 S7, 75 A IGBT with anti-parallel diode in TO247-3
CoolSiC™ SiC MOSFET Discrete	IMBF170R1K0M1	1700 V, 1000 mΩ SiC MOSFET in TO-263-7 with extended creepage
	IMZA120R040M1H	1200 V, 40 mΩ SiC MOSFET in TO247-4 package
	IMZA120R014M1H	1200 V, 14 mΩ SiC MOSFET in TO247-4 package
	IMBG120R030M1H	1200 V, 30 mΩ SiC MOSFET in TO-263-7 package
	IMYH200R012M1H	2000 V, 12 mΩ SiC MOSFET in TO-247-PLUS with high creepage and clearance
CoolSiC™ SiC MOSFET Module	FS33MR12W1M1H_B11	EasyPACK™ 1B 1200 V, 33 mΩ sixpack module
	FF17MR12W1M1H_B11	EasyDUAL™ 1B 1200 V, 17 mΩ half-bridge module
	FF4MR12W2M1H_B11	EasyDUAL™ 2B 1200 V, 4 mΩ half-bridge module
	F4-17MR12W1M1H_B11	EasyPACK™ 1B 1200 V, 17 mΩ fourpack module
TRENCHSTOP™ IGBT Modules	F4-100R17N3E4	EconoPACK™ 3 1700 V, 100 A fourpack IGBT module
	F4-200R17N3E4	EconoPACK™ 3 1700 V, 200 A fourpack IGBT module
	FP10R12W1T7_B11	EasyPIM™ 1B 1200 V, 10 A three phase input rectifier PIM IGBT module
	FS100R12W2T7_B11	EasyPACK™ 2B 1200 V, 100 A sixpack IGBT module
	FP150R12KT4_B11	EconoPIM™ 3 1200V three-phase PIM IGBT module
	FS200R12KT4R_B11	EconoPACK™ 3 1200 V, 200 A sixpack IGBT module

Table 1 Evaluation boards

Part number	Description
EVAL-1ED3321MC12N	Half-bridge evaluation board for 1ED3321MC12N

3 Pin configuration and functionality

3.1 Pin configuration

Table 2 Pin configuration common output 1ED3323MC12N

Pin No.	Name	Function
1	*VEE2*	Negative power supply output side
2	*DESAT*	Short circuit protection (Desaturation)
3	*GND2*	Signal ground output side
4	*NC*	Not connected
5	*VCC2*	Positive power supply output side
6	*OUT*	Driver charge / discharge output
7	*CLAMP*	Miller clamp
8	*VEE2*	Negative power supply output side
9	*GND1*	Ground input side
10	*IN+*	Non-inverting driver input
11	*IN-*	Inverting driver input
12	*RDY*	Ready output
13	*/FLT*	Fault output, low active
14	*/RST*	Reset input, low active
15	*VCC1*	Positive power supply input side
16	*GND1*	Ground input side

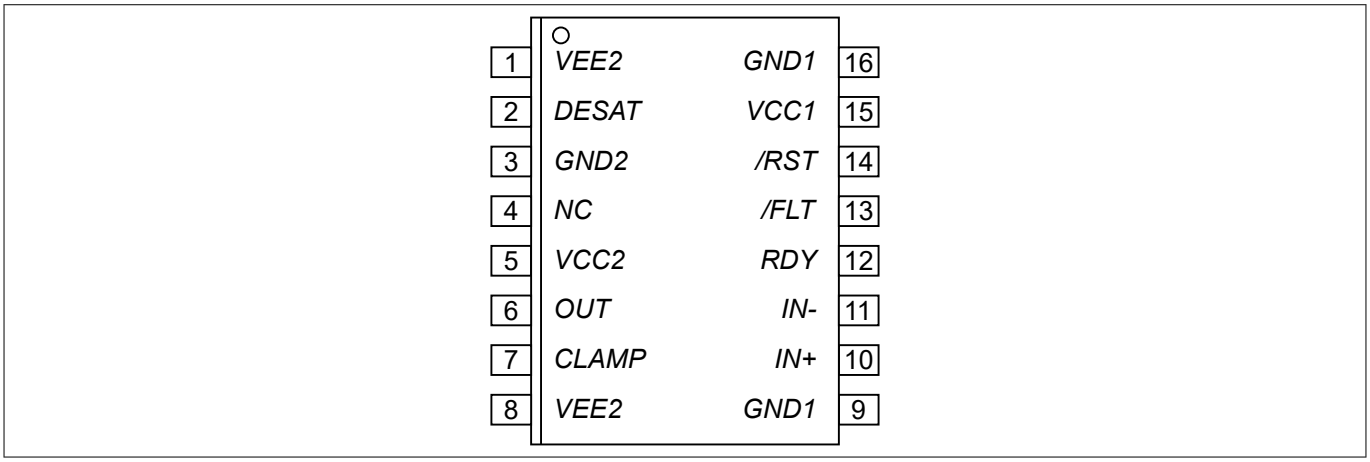

Figure 4 DSO-16 wide body (top view), 1ED3323MC12N

Table 3 Pin configuration separate outputs, 1ED3320MC12N, 1ED3321MC12N and 1ED3322MC12N

Pin No.	Name	Function
1	*VEE2*	Negative power supply output side

(table continues...)

Table 3 (continued) Pin configuration separate outputs, 1ED3320MC12N, 1ED3321MC12N and 1ED3322MC12N

Pin No.	Name	Function
2	*DESAT*	Short circuit protection (Desaturation)
3	*GND2*	Signal ground output side
4	*OUTH*	Driver charge output
5	*VCC2*	Positive power supply output side
6	*OUTL*	Driver discharge output
7	*CLAMP*	Miller clamp
8	*VEE2*	Negative power supply output side
9	*GND1*	Ground input side
10	*IN+*	Non-inverting driver input
11	*IN-*	Inverting driver input
12	*RDY*	Ready output
13	*/FLT*	Fault output, low active
14	*/RST*	Reset input, low active
15	*VCC1*	Positive power supply input side
16	*GND1*	Ground input side

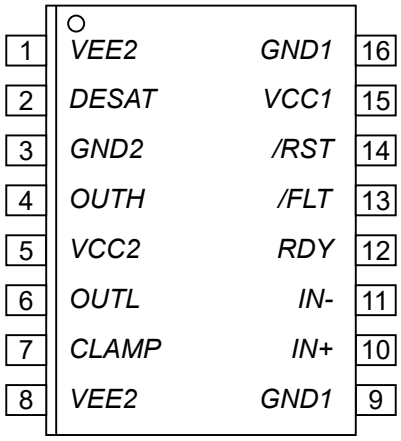

Figure 5 DSO-16 wide body (top view), 1ED3320MC12N, 1ED3321MC12N and 1ED3322MC12N

3.2 Pin functionality

GND1

Ground connection of the input side.

***IN+* non-inverting driver input**

IN+ control signal for the driver output if *IN-* is set to low. The power transistor is on if *IN+* = high and *IN-* = low. A minimum pulse width is defined to make the IC robust against glitches at *IN+*. An internal pull-down resistor ensuring the output is low.

IN- inverting driver input

IN- control signal for driver output if *IN+* is set to high. The power transistor is on if *IN-* = low and *IN+* = high.

A minimum pulse width is defined to make the IC robust against glitches at *IN-*. An internal pull-up resistor ensuring the output is low.

/RST reset input

Function 1: Enable/shutdown of the input chip. The power transistor is off if */RST* = low. A minimum pulse width is defined to make the IC robust against glitches at */RST*.

Function 2: Resets the DESAT-FAULT-state of the chip if */RST* is low for a time t_{RST}. An internal pull-up resistor is used to ensure */FLT* status output.

/FLT fault output

Open-drain output to report a desaturation fault of the power transistor, */FLT* is low if desaturation occurs.

RDY ready status

Open-drain output to report the correct operation of the device.*RDY* = high if both chips are above the UVLO level and the internal chip transmission is faultless.

VCC1

5 V or 3.3 V power supply of the input chip.

VEE2

Negative power supply pins of the output chip. If no negative supply voltage is available, all *VEE2* pins have to be connected to *GND2*.

DESAT desaturation detection input

Monitoring of the IGBT saturation voltage (V_{CE}) to detect desaturation caused by short circuits. If output *OUT* or *OUTH* is high, V_{CE} is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an external capacitor.

CLAMP Miller clamp

Ties the gate voltage to *VEE2* after the power transistor has been switched off. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below V_{CLAMP} (related to *VEE2*). The clamp is designed for a Miller current up to 2 A.

GND2 reference ground

Reference ground of the output chip.

OUTH driver output for 1ED3320MC12N, 1ED3321MC12N and 1ED3322MC12N

Output pin to charge the power transistor gate. The voltage is switched to *VCC2*. In normal operating mode *OUTH* is controlled by *IN+*, *IN-* and */RST*. During error mode (UVLO, internal error or *DESAT*) and OFF the *OUTH* is high impedance.

OUTL driver output for 1ED3320MC12N, 1ED3321MC12N and 1ED3322MC12N

Output pin to discharge the power transistor gate. The voltage is switched to *VEE2*. In normal operating mode *OUTL* is controlled by *IN+*, *IN-* and */RST*. During error mode (UVLO, internal error or *DESAT*). *OUTL* is tuned on.

OUT Driver Output for 1ED3323MC12N

Common output pin to charge and discharge the power transistor gate. The voltage is switched to *VEE2*. In normal operating mode *OUT* is controlled by *IN+*, *IN-* and */RST*. During error mode (UVLO, internal error or *DESAT*) and OFF mode *OUT* is low.

VCC2

Positive power supply pin of the output side.

4 Functional description

4.1 Introduction

The 1ED332xMC12N is an advanced IGBT gate driver that can be also used for driving power MOSFET devices. Control and protection functions are included to make possible the design of high reliability systems.

The device consists of two galvanic separated chips. The input chip can be directly connected to a standard 3.3 V or 5 V DSP or microcontroller with CMOS input/output and the output chip is connected to the high voltage side.

The rail-to-rail driver output enables the user to provide easy clamping of the power transistor gate voltage during short circuit of the power transistor. So, an increase of short circuit current due to the feedback via the Miller capacitance can be avoided. Further, the rail-to-rail output reduces power dissipation.

The device also includes IGBT short circuit protection (DESAT) with */FLT* status output.

The READY status output reports if the device is supplied and operates correctly.

4.2 Supply

The driver 1ED332xMC12N is designed to support two different supply configurations, bipolar supply and unipolar supply.

In bipolar supply the driver is typically supplied with a positive voltage of 15 V at *VCC2* and a negative voltage of -8 V at *VEE2*, please refer to Figure 6. Negative supply prevents a dynamic turn on. If an appropriate negative supply voltage is used, connecting *CLAMP* to IGBT gate is redundant and therefore typically not necessary.

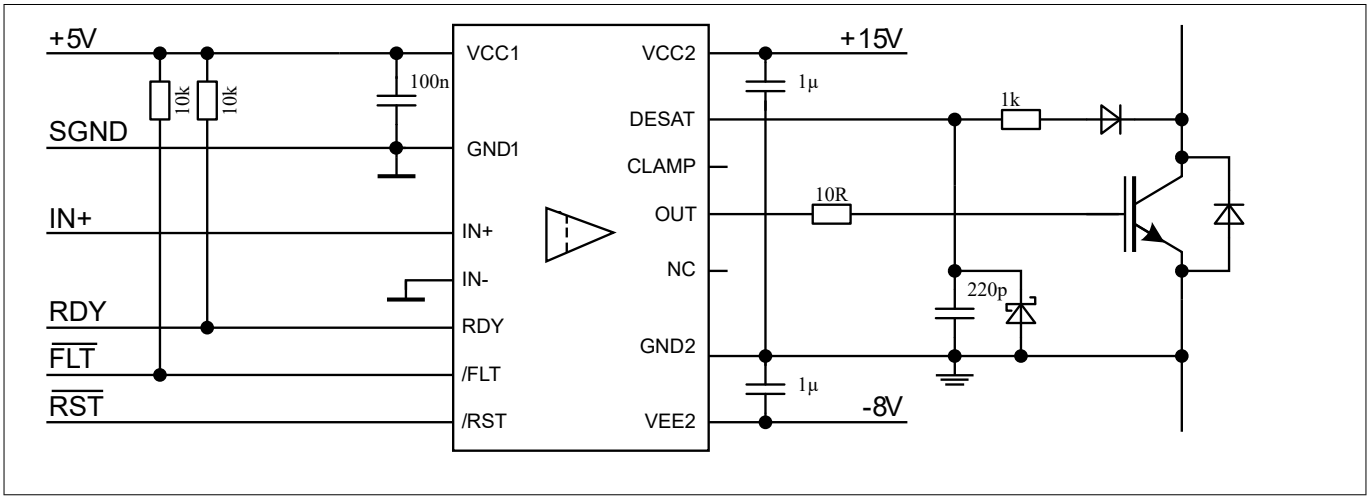

Figure 6 Application example bipolar supply

For unipolar supply configuration the driver is typically supplied with a positive voltage of 15 V at *VCC2*. *VEE2* is connected to *GND2*.

Erratic dynamic turn-on of the IGBT could be prevented with active Miller clamp function, so *CLAMP* output is directly connected to IGBT gate, please refer to Figure 7.

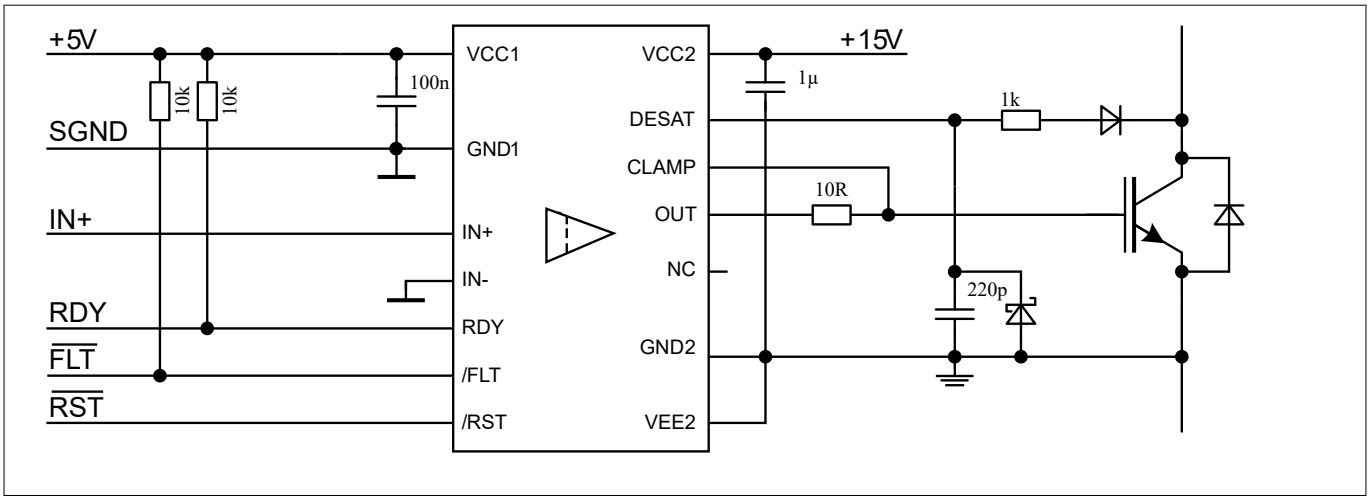

Figure 7 Application example unipolar supply

4.3 Internal protection features

4.3.1 Undervoltage lockout (UVLO)

To ensure correct switching of the power transistor the device is equipped with an undervoltage lockout for both chips, refer to the diagrams showing the undervoltage lockout function of *VCC1* Figure 8 and *VCC2* Figure 9.

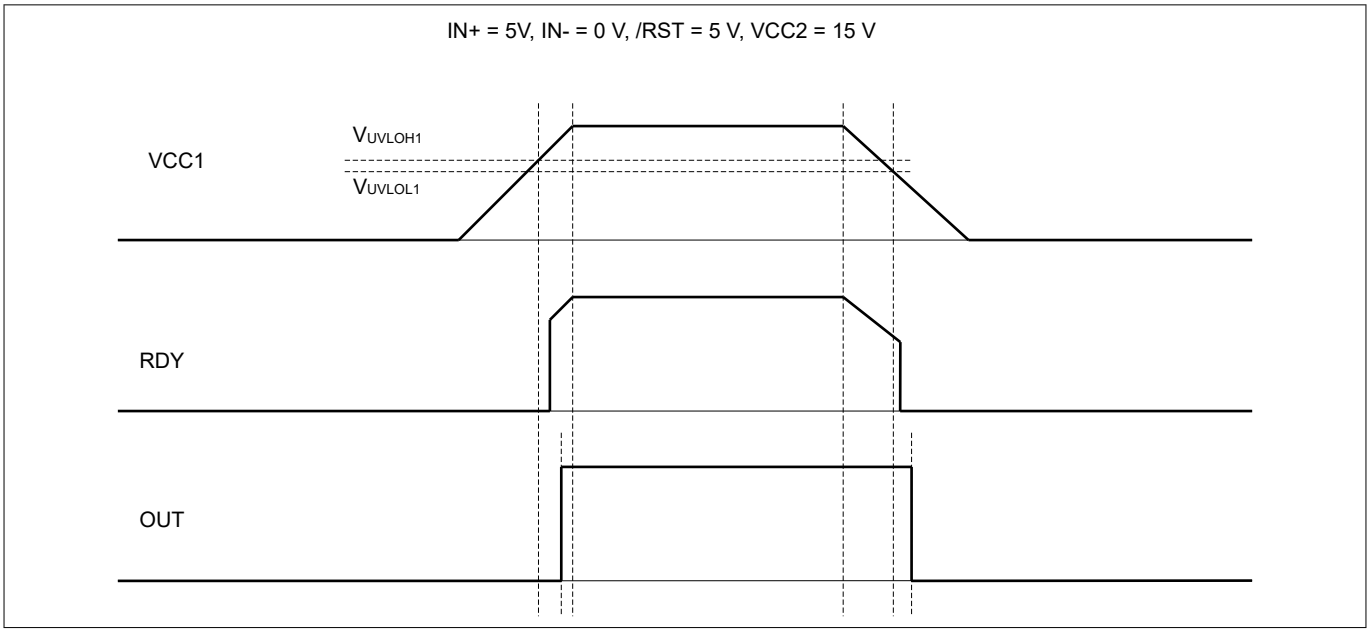

Figure 8 UVLO1

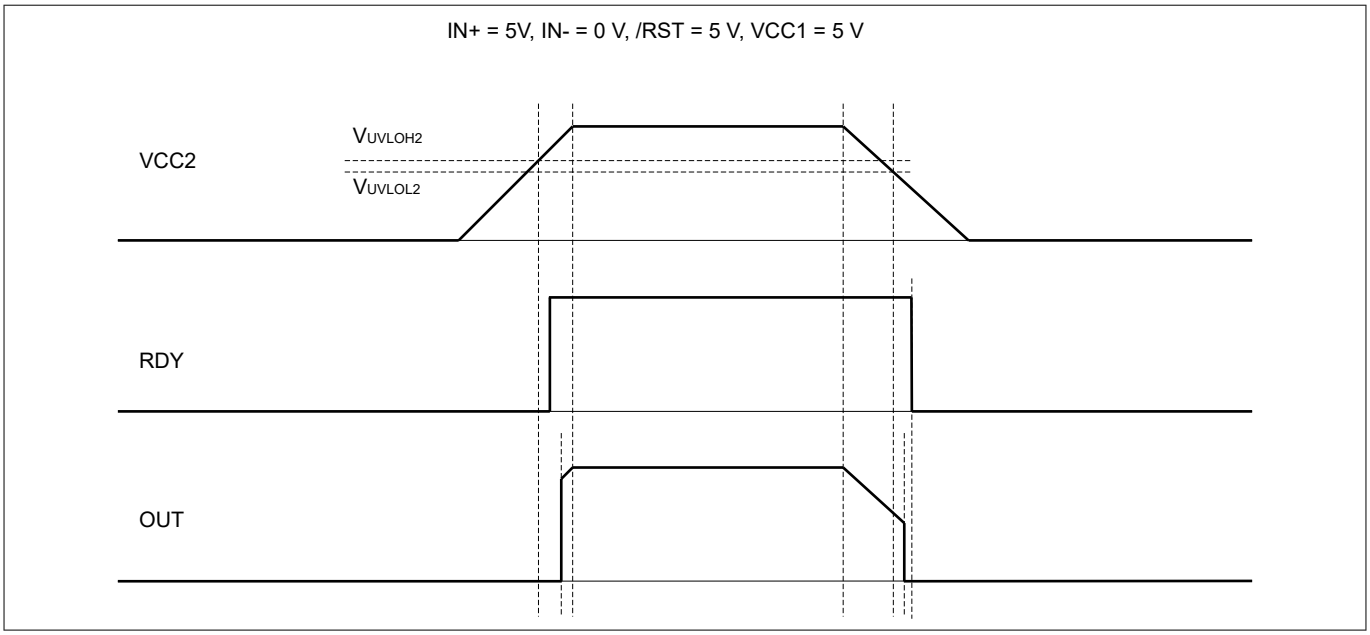

Figure 9 UVLO2

If the power supply voltage *VCC1* of the input chip drops below *VUVLOL1* a turn-off signal is sent to the output chip before the input chip powers down. The power transistor is switched off and the signals at *IN+* and *IN-* are ignored as long as *VCC1* is below the power-up voltage *VUVLOH1*.

If the power supply voltage *VCC2* of the output chip goes below *VUVLOL2* the power transistor is switched off and signals from the input chip are ignored as long as *VCC2* below the power-up voltage *VUVLOH2*. *VEE2* is not monitored, otherwise negative supply voltage range from 0 V to -12 V would not be possible.

4.3.2 READY status output *RDY*

The *RDY* output shows the status of three internal protection features:

- UVLO of the input chip
- UVLO of the output chip
- Internal signal transmission

It is not necessary to reset the *RDY* signal since its state only depends on the status of the former mentioned protection signals.

4.3.3 Watchdog timer

During normal operation the internal signal transmission is monitored by a watchdog timer. If the transmission fails for a given time, the IGBT is switched off and the *RDY* output reports an internal error.

4.3.4 Active shutdown

The active shut-down feature ensures a safe power transistor off-state if the output chip is not connected to the power supply. The power transistor gate is clamped by *OUT* or *OUTL* to *VEE2*.

4.4 Non-inverting and inverting inputs

There are two possible input modes to control the IGBT. In the non-inverting mode *IN+* controls the driver output while *IN-* is set to low. In the inverting mode *IN-* controls the driver output while *IN+* is set to high, is shown in Figure 10.

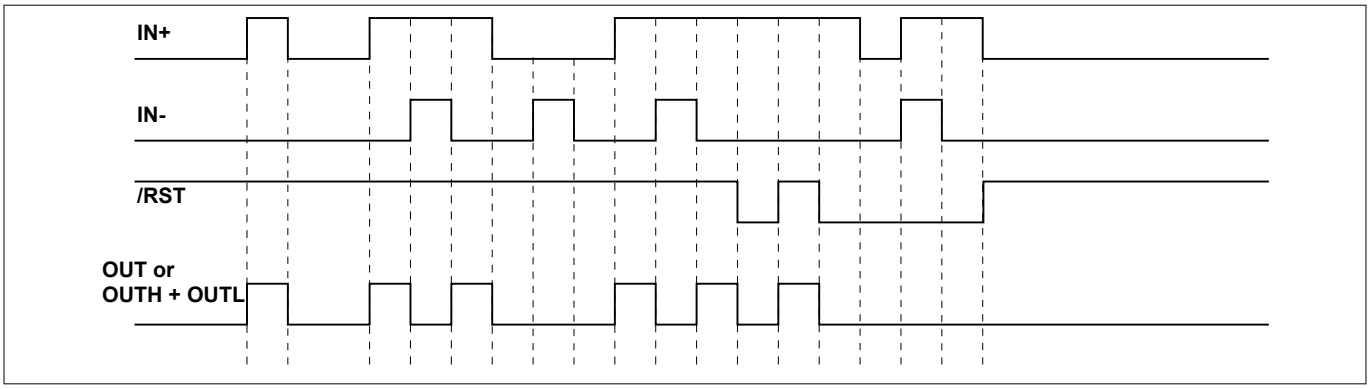

Figure 10 Typical switching behavior

A minimum input pulse width is defined to filter occasional glitches.

The output will react with the propagation delay time after change of the input signals. Figure 11 is showing the propagation delay time and the rise and fall time of the output voltage.

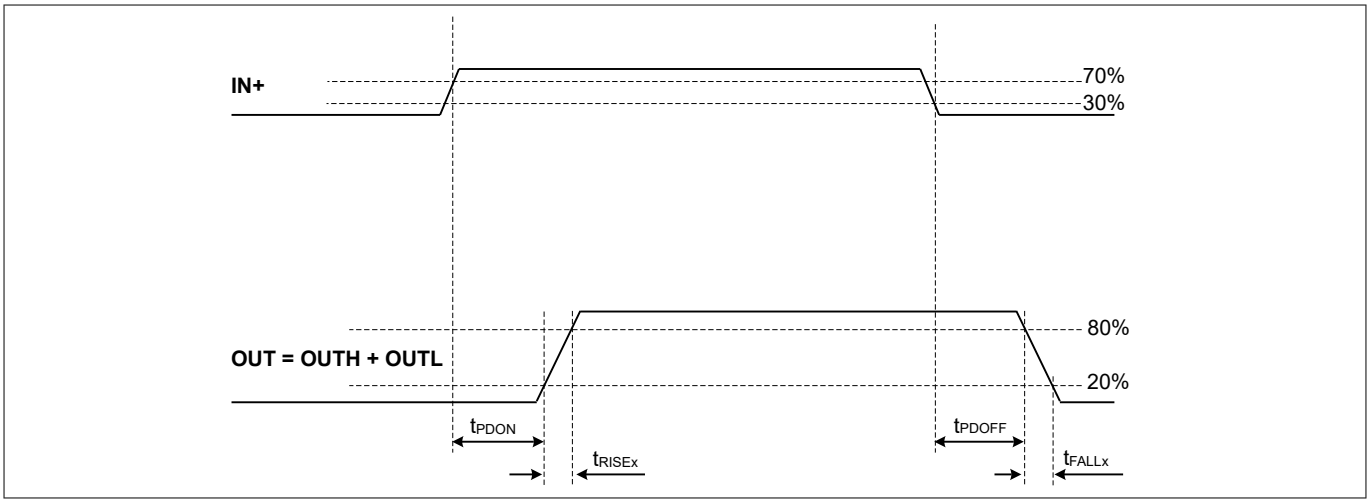

Figure 11 Propagation delay time

4.5 Driver output

The output driver sections uses only MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage, during on-state and short circuit, can be maintained as long as the drivers supply is stable. Due to the low internal voltage drop, switching behavior of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power dissipated by the driver.

4.6 External protection features

4.6.1 Short-circuit protection (DESAT)

A short circuit protection (DESAT) ensures the protection of the IGBT during short-circuit. When the *DESAT* voltage goes up and reaches 9 V, the output is driven low. Further, the */FLT* output is activated after *DESAT* to */FLT*off delay, see Figure 12 for the turn off after *DESAT* event.

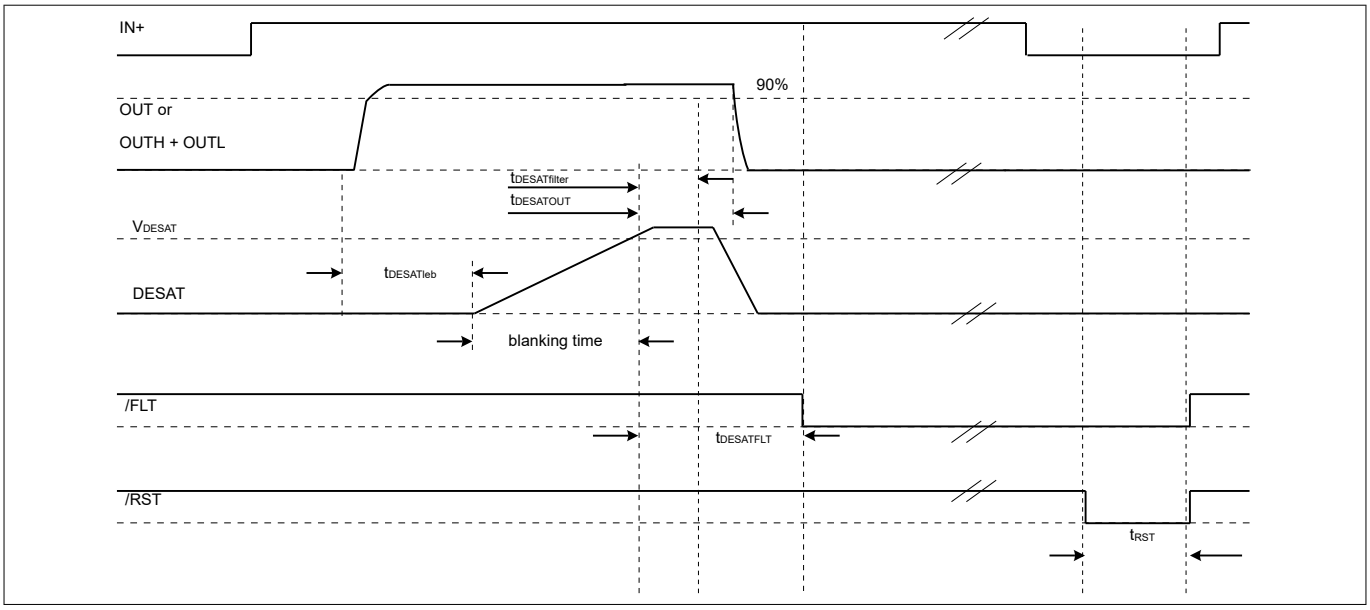

Figure 12 DESAT hard off behavior

The Figure 13 show the soft off behavior.

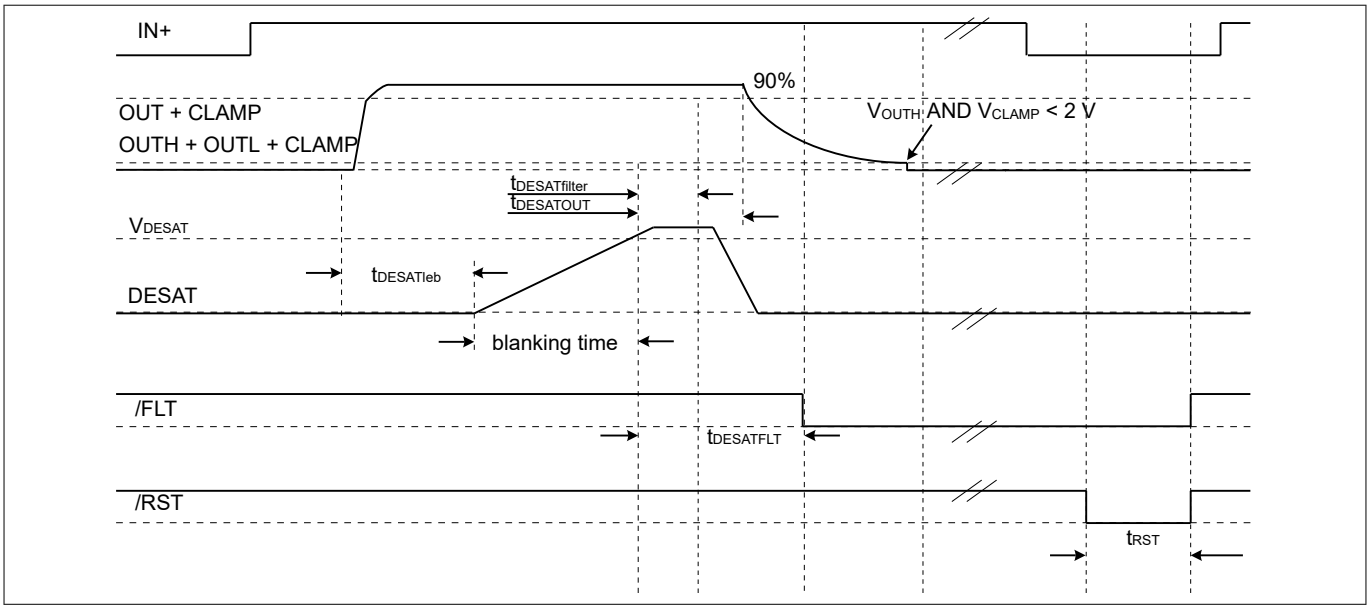

Figure 13 DESAT soft off behavior

A blanking time is used to allow enough time for IGBT saturation. The blanking time is provided by a highly precise internal current source and an external capacitor.

4.6.2 Active miller clamp

In a half bridge configuration the switched-off power transistor tends to dynamically turn on during turn on phase of the opposite power transistor. A Miller clamp allows sinking the Miller current across a low impedance path in this high dV/dt situation. Therefore in many applications, the use of a negative supply voltage can be avoided. During turn-off, the gate voltage is monitored and the *CLAMP* output is activated when the gate voltage goes below typical 2 V (related to *VEE2*). The *CLAMP* is designed for a Miller current up to 2 A.

4.6.3 Short-circuit clamping

During short-circuit the power transistor gate voltage tends to rise because of the feedback via the Miller capacitance. An additional internal protection circuit connected to OUT and CLAMP limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10 µs may be fed back to the supply through one of these paths. If higher currents are expected or a tighter clamping is desired external Schottky diodes may be added.

4.7 RESET

The reset inputs have two functions:

The reset */RST* is in charge of setting back the */FLT* output. If */RST* is low longer than a given time, */FLT* will be cleared at the rising edge of */RST*, refer to Figure 12 or Figure 13 otherwise, it will remain unchanged.

The reset (*/RST* = low for t_{RST}) after DESAT event should be performed only after the gate of the external power transistor is completely discharged and it is turned off.

The reset */RST* works as enable/shutdown of the input logic, refer to Figure 10.

5 Electrical parameters

5.1 Absolute maximum ratings

Table 4 Absolute maximum ratings

Absolute maximum ratings defined here may lead to destruction of the integrated circuit if the specified values are exceeded.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Positive power supply output side voltage	V_{VCC2}	- 0.3		40	V	1)
Negative power supply output side voltage	V_{VEE2}	- 22		0.3	V	1)
Maximum power supply voltage difference output side	V_{max2}	- 0.3		40	V	2)
Gate driver output voltage	V_{OUT}	V_{VEE2} - 0.3		V_{VCC2} + 0.3	V	1) , 1ED3323
Gate driver output voltage	V_{OUTH}, V_{OUTL}	V_{VEE2} - 0.3		V_{VCC2} + 0.3	V	1) , 1ED3320, 1ED3321, 1ED3322
Gate driver output difference	$V_{OUTH-OUTL}$	-40		40	V	1D3320, 1ED3321, 1ED3322
Gate driver output current	I_{OUT}	-9		9	A	3) , 4) , 1ED3323
Gate driver output current	I_{OUTH}, I_{OUTL}	-5		5	A	3) , 4) , 1ED3320
Gate driver output current	I_{OUTH}, I_{OUTL}	-9		9	A	3) , 4) , 1ED3321, 1ED3322
CLAMP voltage	V_{CLAMP}	V_{VEE2} - 0.3		V_{VCC2} + 0.3	V	1)
CLAMP to gate driver output difference	$V_{OUTH-CLAMP}$, $V_{OUTL-CLAMP}$	-40		40	V	1D3320, 1ED3321, 1ED3322
CLAMP to gate driver output difference	$V_{OUT-CLAMP}$	-40		40	V	1ED3323
CLAMP output current	I_{CLAMP}	-4.5		4.5	A	3) , 4)
Short circuit clamping time	t_{CPL}			10	µs	I_{CLAMP} = 0.5 A, V_{CLAMP} < 2 V, I_{OUT} = 0.5 A, V_{OUT} < 2 V, 4)
DESAT voltage	V_{DESAT}	- 0.3		V_{VCC2} + 0.3	V	1) , I_{DESAT} limited ≤ 5 mA , 4)
Positive power supply voltage input side	V_{VCC1}	- 0.3		7	V	5)
Logic input voltages IN+, IN-, /RST	$V_{LogicIN}$	- 0.3		V_{VCC1} + 0.3	V	5)
Open drain logic output voltage / FLT, RDY	V_{FLT}, V_{RDY}	- 0.3		V_{VCC1} + 0.3	V	open drain output in high state, 5)
Open drain output current /FLT, RDY	I_{FLT}, I_{RDY}			10	mA	open drain output in low state, output voltage <= V_{VCC1}

(table continues...)

Table 4 (continued) Absolute maximum ratings

Absolute maximum ratings defined here may lead to destruction of the integrated circuit if the specified values are exceeded.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output offset voltage	V_{OFFSET}	-		2300	V	$V_{VEE2,max}$ - $V_{VEE2,min}$ with $V_{VEE2,max} \geq V_{GND1} \geq V_{VEE2,min}$, 6)
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{ST}	-55		150	°C	
Power dissipation input part	P_{DIN}			100	mW	@ T_A = 85°C
Power dissipation output part DSO-16 wide body	$P_{DOUT-16}$			810	mW	@T_A = 85°C, JEDEC 2s2p no cooling, Package DSO-16 wide body
ESD capability HBM model	V_{ESDHBM}	-4		+4	kV	HBM model according ANSI/ ESDA/JEDEC JS-001 (discharge 100 pF capacitor through 1.5 kOhm series resistor)
ESD capability CDM model	*ESD_CDM*		TC 1500			Charged device model 7)
Maximum switching frequency	f_{SW}			1	MHz	

1) in respect to *GND2*
2) in respect to *VEE2*
3) *t* = 1 µs on, 5 µs period, limited by max. power dissipation
4) Parameter is not subject to production test - verified by design/characterization
5) in respect to *GND1*
6) for functional operation only
7) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)

5.2 Thermal parameter

Table 5 Thermal parameter

Thermal performance may change significantly with layout and heat dissipation of compontents in close proximity.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance junction to ambient DSO-16 wide body JEDEC 1s0p PCB with cooling	R_{THJAwc}		86.7		K/W	@T_A = 85 °C, P_{DIN} = 100 mW, P_{DOUT} = 650 mW, JEDEC 1s0p PCB, DSO-16 wide body with cooling
Thermal resistance junction to ambient DSO-16 wide body JEDEC 2s2p PCB no cooling	R_{THJAnc}		71.4		K/W	@T_A = 85 °C, P_{DIN} = 100 mW, P_{DOUT} = 810 mW, JEDEC 2s2p PCB, DSO-16 wide body no cooling

(table continues...)

Table 5 (continued) Thermal parameter

Thermal performance may change significantly with layout and heat dissipation of compontents in close proximity.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Characterization parameter junction to package DSO-16 wide body JEDEC 1s0p PCB with cooling	Ψ_{JTwc}		9.82		K/W	@T_A = 85 °C, P_{DIN} = 100 mW, P_{DOUT} = 650 mW, JEDEC 1s0p, DSO-16 wide body with cooling
Characterization parameter junction to package DSO-16 wide body JEDEC 2s2p PCB no cooling	Ψ_{JTnc}		9.93		K/W	@T_A = 85 °C, P_{DIN} = 100 mW, P_{DOUT} = 81 mW, JEDEC 2s2p PCB, DSO-16 wide body no cooling

5.3 Operating parameters

Table 6 Operating parameters

Within the operating range, the IC operates as described in the functional description and electrical characteristics.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Positive power supply output side	V_{VCC2}	V_{UVLOH2}		35	V	1)
Negative power supply output side	V_{VEE2}	-20		0	V	1)
Power supply difference output side	V_{max2}	2)		35	V	$V_{max2} = V_{VCC2} - V_{VEE2}$
Power supply input side	V_{VCC1}	V_{UVLOH1}		5.5	V	3)
Logic input voltages	$V_{LogicIN}$	-0.3		V_{VCC1}	V	3)
CLAMP voltage	V_{CLAMP}	V_{VEE2} - 0.3		V_{VCC2} + 0.3	V	1)
DESAT voltage	V_{DESAT}	-0.3		V_{VCC2} + 0.3	V	1)
Ambient temperature	T_A	-40		125	°C	
Operating junction temperature	T_{Jop}	-40		150	°C	
Common Mode Transient Immunity	*CMTI*	-300		300	kV/µs	@ V_{ISO} = 1.5 kV, 4)

1) in respect to *GND2*
2) $V_{UVLOH2}+(V_{GND2}-V_{VEE2})$
3) in respect to *GND1*
4) Parameter is not subject to production test - verified by design/characterization

5.4 Electrical characteristics

The electrical characteristics include the spread of values in supply voltages, load and junction temperatures T_{Jop} within the operating parameters and default parameter settings unless specified otherwise. Typical values represent the median values at T_A = 25°C.

5.4.1 Power supply

Table 7 Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UVLO threshold input side (on)	V_{UVLOH1}			3.1	V	V_{VCC1}-V_{GND1}
UVLO threshold input side (off)	V_{UVLOL1}	2.5			V	V_{VCC1}-V_{GND1}
UVLO hysteresis input side	V_{HYS1}	0.1	0.2		V	V_{UVLOH1}- V_{UVLOL1}
UVLO threshold output side (on)	V_{UVLOH2}		12.0	12.6	V	V_{VCC2}-V_{GND2}, 1D3320, 1ED3321, 1ED3323
UVLO threshold output side (on)	V_{ULVOH2}		13.6	14.2	V	V_{VCC2}-V_{GND2}, 1ED3322
UVLO threshold output side (off)	V_{UVLOL2}	10.4	11.0		V	V_{VCC2}-V_{GND2}, 1ED3320, 1ED3321, 1ED3323
UVLO threshold output side (off)	V_{UVLOL2}	11.9	12.6		V	V_{VCC2}-V_{GND2}, 1ED3322
UVLO hysteresis output side	V_{HYS2}	0.6	0.9		V	V_{UVLOH2}- V_{UVLOL2}
Quiescent current input side	I_{Q1}		1.1	3	mA	1)
Quiescent current output side	I_{Q2}		2	3	mA	1)

1) V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = - 8 V, *IN+* = High, *IN-* = Low, *OUT* = High, *RDY* = High, */FLT* = High, V_{DESAT} = 0 V

5.4.2 Logic input and output

Table 8 Logic input and output

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Digital input low threshold voltage IN+, IN-, /RST	V_{IN+L}, V_{IN-L}, V_{RST-L}	0.3 * V_{VCC1}			V	
Digital input high threshold voltage IN+, IN-, /RST	V_{IN+H}, V_{IN-H}, V_{RST-H}			0.7 * V_{VCC1}	V	
Digital input current IN-, /RST	I_{IN-}, I_{RST}	-200		-40	µA	V_{IN-} = *GND1*, V_{RST} = *GND1*
Digital input current IN+	I_{IN+}	40		200	µA	V_{IN+} = V_{VCC1}
Digital pull up current RDY, /FLT	I_{PRDY}, I_{PFLT}	-400	-100		µA	V_{RDY} = *GND1*, V_{FLT} = *GND1*
/FLT Low Voltage	V_{FLTL}			300	mV	$I_{SINK(FLT)}$ = 5 mA, 1)
RDY Low Voltage	V_{RDYL}			300	mV	$I_{SINK(RDY)}$ = 5 mA, 1)

1) The load capacitance connected to RDY or /FLT should be below 22 nF.

5.4.3 Gate driver

Table 9 Gate driver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High level output peak current	I_{OUTH}	4	6		A	[1] 1ED3321, 1ED3322, 1ED3323, [6]
High level output peak current	I_{OUTH}	2	3.3		A	[2] 1ED3320, [6]
High level output on resistance	$R_{DSON,H}$	0.5	0.79	1.3	Ω	I_{OUTH} = 0.1 A, 1ED3321, 1ED3322, 1ED3323
High level output on resistance	$R_{DSON,H}$	0.9	1.4	2.35	Ω	I_{OUTH} = 0.1 A, 1ED3320
High side sink current	$I_{OUT+,sink}$			30	µA	*IN+* = low or *IN-* = high, V_{VCC2} = 15 V, V_{VEE2} = -8 V, V_{OUTH} = 15 V, [3]
Low level output peak current	I_{OUTL}	4	8.5		A	[4] 1ED3321, 1ED3322, 1ED3323, [6]
Low level output peak current	I_{OUTL}	2	6		A	[5] 1ED3320, [6]
Low level output on resistance	$R_{DSON,L}$	0.35	0.51	0.85	Ω	I_{OUTL} = 0.1 A, 1ED3321, 1ED3322, 1ED3323
Low level output on resistance	$R_{DSON,L}$	0.6	0.89	1.4	Ω	I_{OUTL} = 0.1 A, 1ED3320
Soft-off sink current	I_{OUTLF}		230		mA	after DESAT detected, V_{OUTH} - V_{VEE2} > V_{CLAMP}
Soft-off watchdog time	$t_{WDSoftoff}$	5		9	µs	DESAT with soft-off activated, *OUTH* or *CLAMP* above miller clamp voltage
Short circuit clamp voltage OUTH / VCC2	V_{CLP_OUTH}		1	1.5	V	Path off, I_{OUTH} = 500 mA, t < 10 µs, 1D3320, 1ED3321, 1ED3322, [6]
Short circuit clamp voltage OUTL / VCC2	V_{CLP_OUTL}		1.6	2	V	Path off, I_{OUTL} = 500 mA, t < 10 µs, 1D3320, 1ED3321, 1ED3322, [6]
Short circuit clamp voltage OUT / VCC2	V_{CLP_OUT}		1	1.5	V	Path off, I_{OUT} = 500 mA, t < 10 µs, 1ED3323, [6]

1) *IN+* = High, *IN-* = Low, V_{OUT} = V_{VCC2} - 15 V, V_{VCC2} = 15 V, load condition C_L = 100 nF, R_L = 0.1 Ohm,
2) *IN+* = High, *IN-* = Low, V_{OUT} = V_{VCC2} - 15 V, V_{VCC2} = 15 V, load condition C_L = 100 nF, R_L = 0.1 Ohm,
3) in respect to *GND2*
4) *IN+* = Low, *IN-* = Low, *OUT* = V_{VEE2} + 15 V, V_{VCC2} = 15 V, load condition C_L = 100 nF, R_L = 0.1 Ohm
5) *IN+* = Low, *IN-* = Low, *OUT* = V_{VEE2} + 15 V, V_{VCC2} = 15 V, load condition C_L = 100 nF, R_L = 0.1 Ohm
6) Parameter is not subject to production test - verified by design/characterization

5.4.4 Active miller clamp

Table 10 Active miller clamp

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Low level clamp current	$I_{CLAMP,L}$	2	3		A	V_{CLAMP} = 1.5 V, V_{VCC2} = 15 V, V_{VEE2} = 0 V, R_g = 0.1 Ω, C_g = 1 µF, 1)
Low level clamp on resistance	$R_{DSON,CLP}$	0.4	0.6	1.0	Ω	I_{OUTL} = 0.1 A
Clamp threshold voltage	V_{CLAMP}	1.6	2.1	2.4	V	in respect to *VEE2*
Clamp activation time	t_{CLPDLY}			80	ns	$V_{CLAMP} \le V_{CLAMPth}$
Short circuit clamp voltage CLAMP / VCC2	V_{CLP}		1.8	2	V	Path off, I_{CLAMP} = 500 mA, t < 10 µs, 1)

1) Parameter is not subject to production test - verified by design/characterization

5.4.5 Dynamic characteristics

Table 11 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input IN+, IN-, /RST to output propagation delay on	t_{PDON}	74	80	84	ns	C_{LOAD} = 100 pF, V_{IN+} = 70 %, V_{OUT} = 20 %, T_A = 25 °C
Input IN+, IN-, /RST to output propagation delay off	t_{PDOFF}	81	86	92	ns	C_{LOAD} = 100 pF, V_{IN+} = 30 %, V_{OUT} = 80 %, T_A = 25 °C
Input IN+ to output propagation delay distortion	$\lvert t_{PDDISTO} \rvert$			11	ns	C_{LOAD} = 100 pF, T_A = 25 °C
Input IN-, /RST to output propagation delay distortion	$\lvert t_{PDDISTO} \rvert$			17	ns	C_{LOAD} = 100 pF, T_A = 25 °C
Input IN+, IN-, /RST pulse suppression time (filter time)	t_{INFLT}	29	35	41	ns	shorter pulses will not propagate to the output
Input IN+, IN-, /RST to output propagation delay on variation due to temperature	$\lvert t_{PDONt} \rvert$			15	ns	C_{LOAD} = 100 pF, 1)
Input IN+, IN-, /RST to output propagation delay off variation due to temperature	t_{PDOFFt}			15	ns	C_{LOAD} = 100 pF, 1)
Input IN+ to output propagation delay distortion variation due to temperature	$t_{PDISTOt}$			13	ns	C_{LOAD} = 100 pF, 1)
Input IN-, /RST to output propagation delay distortion variation due to temperature	$t_{PDISTOt}$			17	ns	C_{LOAD} = 100 pF, 1)

(table continues...)

Table 11 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input IN+, IN-, /RST to output propagation delay variation part to part	$\lvert t_{PD,P2P} \rvert$			15	ns	C_{LOAD} = 100 pF, Same T_A, slopes and supply voltages
Rise time 1	t_{rise1}		15	20	ns	C_{LOAD} = 1 nF, V_L 20 %, V_H 80 %, V_{VCC2} = 15 V, V_{VEE2} = *GND2* = 0 V
Rise time 2	t_{rise2}		10	15	ns	C_{LOAD} = 100 pF, V_L 20%, V_H 80%, V_{CCC2} = 15 V, V_{VEE2} = *GND2* = 0 V, [1)]
Rise time 3	t_{rise3}		300		ns	C_{LOAD} = 100 nF, 0.1 Ohm, V_L 20%, V_H 80%, V_{VCC2} = 15 V, V_{VEE2} = *GND2* = 0 V, 1ED3321, 1ED3322, 1ED3323, [1)]
Rise time 4	t_{rise4}		530		ns	C_{LOAD} = 100 nF, 0.1 Ohm, V_L 20%, V_H 80%, V_{VCC2} = 15 V, V_{VEE2} = *GND2* = 0 V, 1ED3320, [1)]
Fall time 1	t_{fall1}		15	20	ns	C_{LOAD} = 1 nF, V_L 20%, V_H 80%, V_{VCC2} = 15 V, V_{VEE2} = *GND2* = 0 V
Fall time 2	t_{fall2}		10	15	ns	C_{LOAD} = 100 pF, V_L 20%, V_H 80%, V_{VCC2} = 15 V, V_{VEE2} = *GND2* = 0 V, [1)]
Fall time 3	t_{fall3}		234		ns	C_{LOAD} = 100 nF, 0.1 Ohm, V_L 20%, V_H 80%, V_{VCC2} = 15 V, V_{VEE2} = *GND2* = 0 V, 1ED3321, 1ED3322, 1ED3323, [1)]
Fall time 4	t_{fall4}		370		ns	C_{LOAD} = 100 nF, 0.1 Ohm, V_L 20%, V_H 80%, V_{VCC2} = 15 V, V_{VEE2} = *GND2* = 0 V, 1ED3320, [1)]

1) Parameter is not subject to production test - verified by design/characterization

5.4.6 Desaturation protection

Table 12 Desaturation protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Blanking capacitor charge current	I_{DESATC}	438	510	582	µA	V_{VCC2} = 15 V, V_{VEE2} = *GND2*, V_{DESAT}-V_{GND2} = 2 V
Blanking capacitor discharge current	I_{DESATD}	90	150		mA	V_{VCC2} = 15 V, V_{VEE2} = *GND2*, V_{DESAT} - V_{GND2} = 6 V
Desaturation reference level	$V_{DESATth}$	8.5	9	9.5	V	V_{VCC2} = 15 V, in respect to *GND2*

(table continues...)

Table 12 (continued) Desaturation protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pulse suppression filter time	$t_{DESATfilter}$		250		ns	1)
Desaturation sense to out low delay	$t_{DESATOUT}$		350	430	ns	V_{OUT} = 90 %, C_{OUT} = 1 nF, *OUT* = *OUTH* + *OUTL* shorted, 1ED3322, 1ED3323
Desaturation sense to out low delay	$t_{DESATOUT\_SO}$		380	500	ns	V_{OUT} = 90 %, C_{OUT} = 1 nF, *OUT* = *OUTH* + *OUTL* shorted, 1ED3320, 1ED3321
Desaturation out slope with capacitive load	$t_{DESATOUT\_CL\_SO}$	1	3.5	6	us	V_{VCC2} = 15 V, V_{VEE2} = 0 V, V_{OUT} = 10 %, C_{OUT} = 47 nF, *OUTH* tied to *OUTL*, V_{CLAMP} = 5 V, 1ED3320, 1ED3321
Desaturation sense to flt low delay	$t_{DESATFLT}$			2.25	µs	V_{FLTL} = 10 %, I_{FLT} = 5 mA
Desaturation low voltage	V_{DESATL}	0.25	0.5	0.95	V	*IN+* = Low, *IN-* = Low, *OUT(H,L)* = Low, I_{DESAT} = 70 mA
Leading edge blanking	$t_{DESATleb}$	280	400	500	ns	
Pulse width /rst for resetting /flt	t_{RST}	800			ns	
Short circuit clamp voltage desat/ vcc2	V_{CLP_DESAT}		1.4	1.6	V	Path off, I_{DESAT} = 500 mA, t < 10 µs, 1)

1) Parameter is not subject to production test - verified by design/characterization

5.4.7 Active shutdown

Table 13 Active shutdown

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD}		2	2.6	V	I_{OUT} = 200 mA; V_{VCC2} = open

6 Insulation characteristics (IEC 60747-17, UL 1577) for DSO-16 wide body package

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 14 Insulation specification for DSO-16 wide body package

Description	Symbol	Characteristic	Unit
Safety limiting values			
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at T_A = 25°C[1)]	P_{SI}	100	mW
Maximum output-side power dissipation at T_A = 25°C[2)]	P_{SO}	810	mW
Package specific insulation characteristics			
External clearance	*CLR*	> 8	mm
External creepage	*CPG*	> 8	mm
Comparative tracking index	*CTI*	> 400	–
Isolation capacitance	C_{IO}	1.4	pF
Reinforced insulation according to IEC 60747-17 (Certificate no. 40055138)			
Installation classification per EN 60664-1, Table 1 for rated mains voltage ≤ 150 V (rms) for rated mains voltage ≤ 300 V (rms) for rated mains voltage ≤ 600 V (rms) for rated mains voltage ≤1000 V (rms)		 I-IV I-IV I-III I-II	–
Climatic classification		40/125/21	–
Pollution degree (EN 60664-1)		2	–
Apparent charge, method a $V_{pd(ini),a} = V_{IOTM}$, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_{ini} = 1 min, t_m = 10 s	q_{pd}	<5	pC
Apparent charge, method b $V_{pd(ini),b} = V_{IOTM} \times 1.2$, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_{ini} = 1 s, t_m = 1 s	q_{pd}	<5	pC
Isolation resistance at $T_{A,max}$; V_{IO} = 500 V_{DC}, T_A = 125 °C	R_{IO}	$>10^{11}$	Ω
Isolation resistance at T_S; V_{IO} = 500 V_{DC}, T_S = 150 °C	R_{IO_S}	$>10^{9}$	Ω
Maximum rated transient isolation voltage	V_{IOTM}	8000	V (peak)
Maximum repetitive isolation voltage	V_{IORM}	1767	V (peak)
Maximum working isolation voltage	V_{IOWM}	1249	V (rms)
Impulse voltage	V_{IMP}	8000	V (peak)
Maximum surge isolation voltage for reinforced isolation $V_{TEST} \geq V_{IMP} \times 1.3$	V_{IOSM}	11000	V (peak)
Recognized under UL 1577 (File E311313)			
Insulation withstand voltage (60 s)	V_{ISO}	5700	V (rms)
Insulation test voltage (1 s)	$V_{ISO,TEST}$	6840	V (rms)

1) IC input-side power dissipation is derated linearly at 11.53 mW/°C above 141 °C
2) IC output-side power dissipation is derated linearly at 8.98 mW/°C above 25 °C

7 Package outline

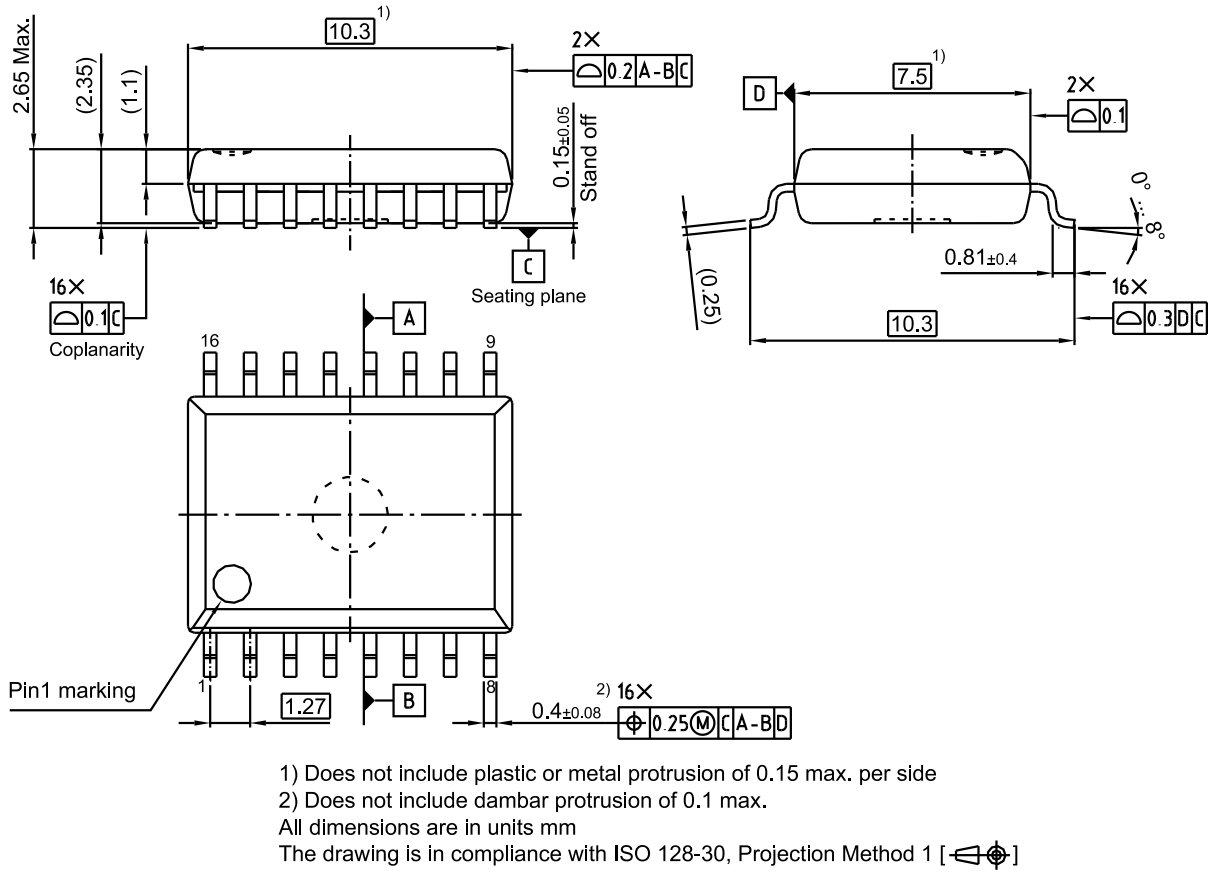

Figure 14 DSO-16 wide body (Plastic (green) dual small outline package)

7 Package outline

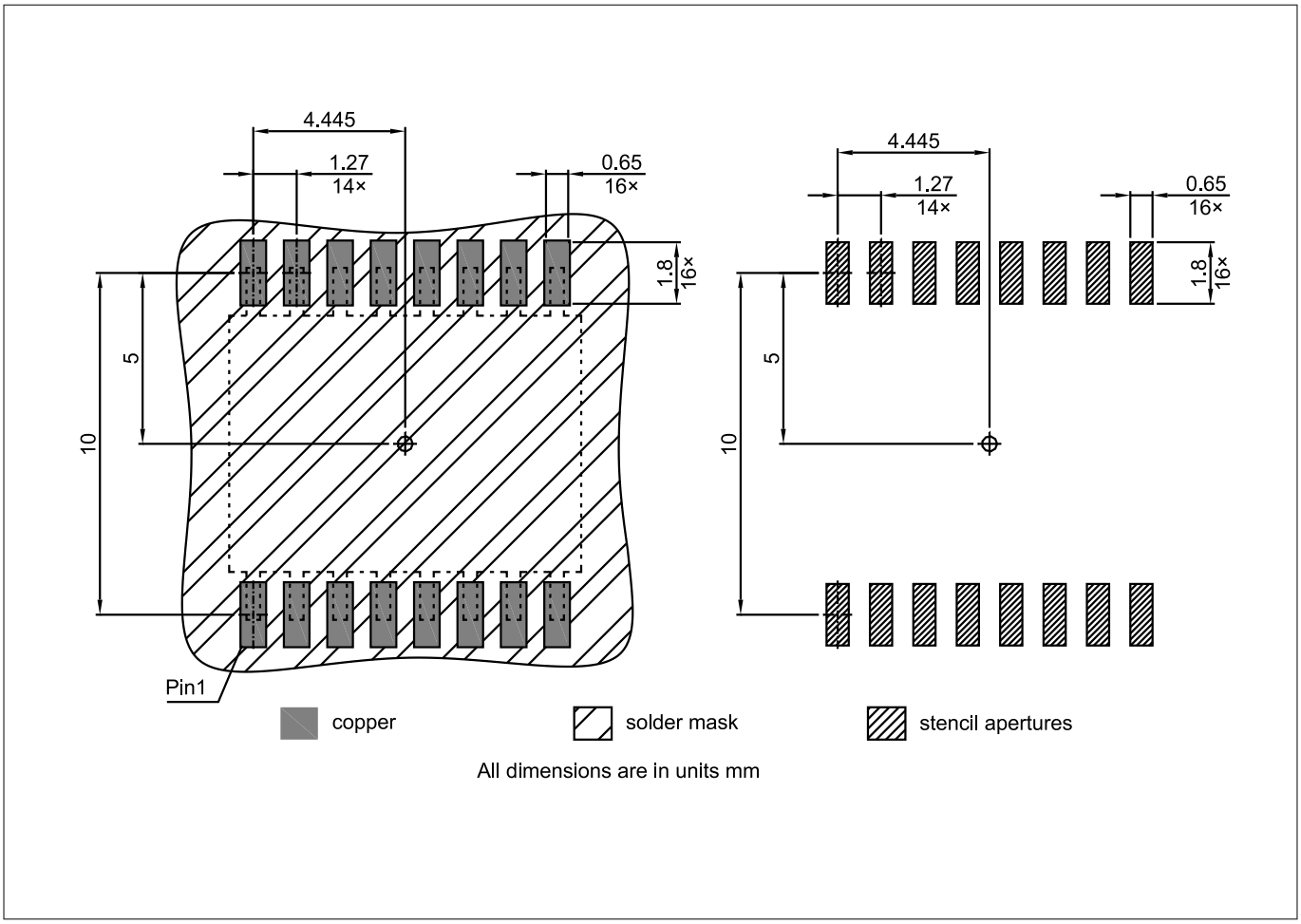

Figure 15 Footprint

8 Application notes

8.1 Reference layout for thermal data

The PCB layout shown in Figure 16 represents the reference layout used for the thermal characterisation. Pins 9 and 16 (*GND1*) and pins 1 and 8 (*VEE2*) require ground plane connections for achiving maximum power dissipation. The 1ED332xMC12N is conceived to dissipate most of the heat generated through this pins.

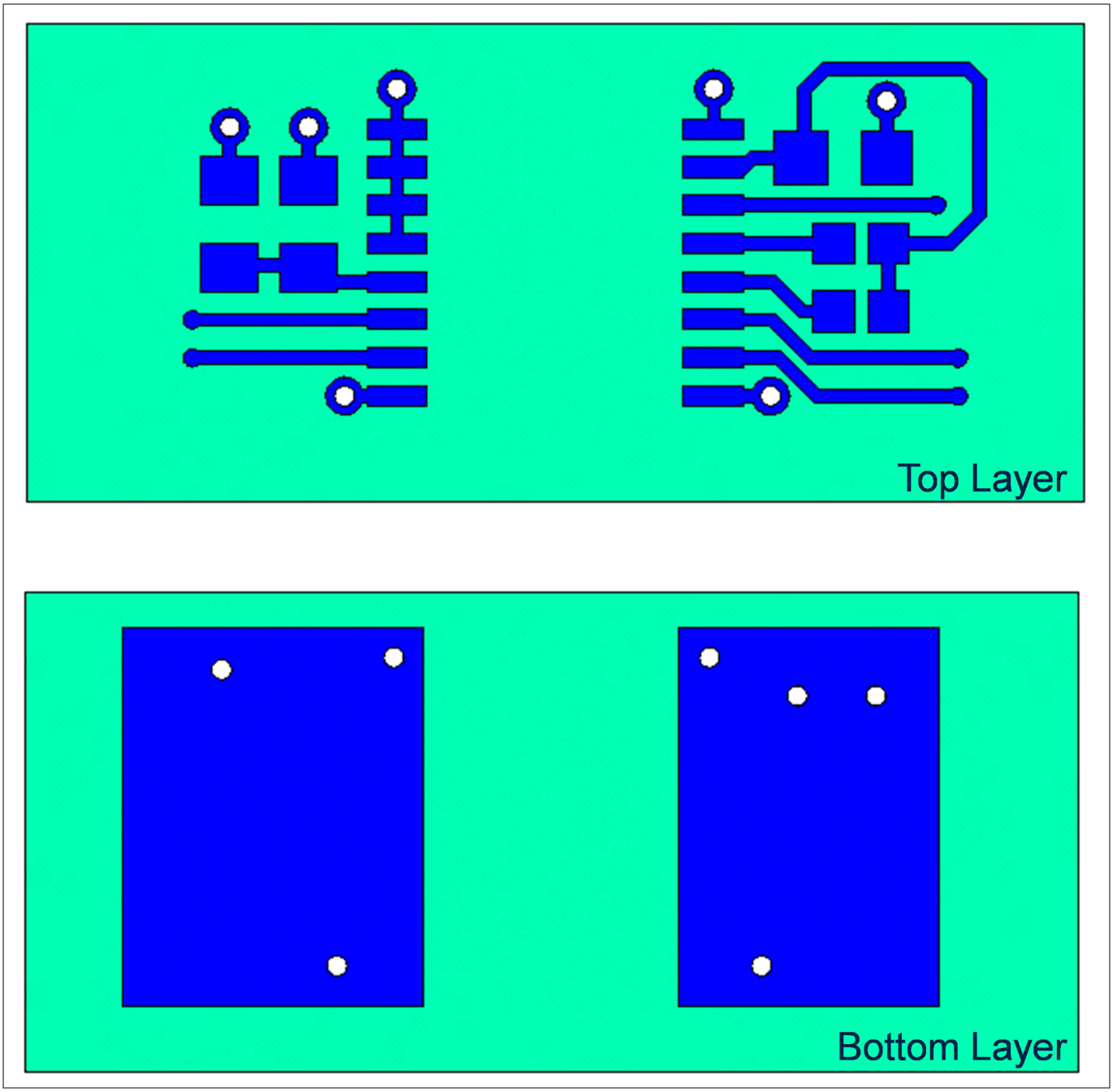

Figure 16 Reference layout for thermal data (Copper thickness 102 µm)

8.2 Printed circuit board guidelines

Following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.

8 Application notes

- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.
- The blocking cap should be placed as close as possible to *VEE2* and to *GND2* , pin 1 and 3.

9 Revision history

Revision history

Page or item	Subjects (major changes since previous revision)
Rev 1.00, 2021-11-18	
All	Initial version
Rev 1.01, 2021-12-14	
page 1, 2	update device information
Table 7	UVLO names updated
Rev 1.02, 2023-05-09	
page 1	Updated the VDE 0884-11 certificate information
page 7	Updated the related products
Table 15	Pending status of the VDE0884-11 certification deleted and added insulation capacitance parameter
Figure 10	Correction of OUTH parameter name
Figure 11	Correction of V_{IN+} threshold levels
Rev 1.03, 2024-04-17	
page 1	Updated the certification information
page 2	Updated the package marking information
page 26	Updated the certification information from VDE 0884-11 to IEC 60747-17

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