



THE DATASHEET OF ADM485ARM



FEATURES

- Meets EIA RS-485 standard
- 5 Mbps data rate
- Single 5 V supply
- 7 V to +12 V bus common-mode range
- High speed, low power BiCMOS
- Thermal shutdown protection
- Short-circuit protection
- Driver propagation delay: 10 ns typical
- Receiver propagation delay: 15 ns typical
- High-Z outputs with power off
- Superior upgrade for LTC485

APPLICATIONS

- Low power RS-485 systems
- DTE/DCE interface
- Packet switching
- Local area networks (LANs)
- Data concentration
- Data multiplexers
- Integrated services digital network (ISDN)

GENERAL DESCRIPTION

The ADM485 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced data transmission and complies with EIA standards RS-485 and RS-422. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver can be enabled independently. When disabled, the outputs are three-stated.

The ADM485 operates from a single 5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. If during fault conditions, a significant temperature increase is detected in the internal driver circuitry, this feature forces the driver output into a high impedance state.

Up to 32 transceivers can be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important, therefore, that the remaining disabled drivers do not load the bus. To ensure this, the ADM485 driver features high output impedance when disabled and when powered down, which minimizes the loading effect when the transceiver is not being used. The high impedance driver output is maintained over the common-mode voltage range of -7 V to +12 V.

Rev. F

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FUNCTIONAL BLOCK DIAGRAM

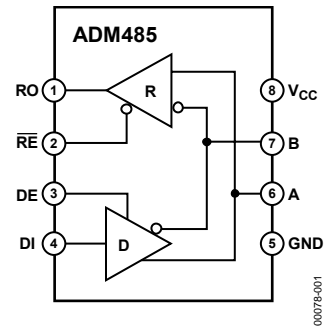


Figure 1.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM485 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.

The ADM485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at data rates up to 5 Mbps while low skew minimizes EMI interference.

The part is fully specified over the commercial and industrial temperature range and is available in 8-lead PDIP, 8-lead SOIC, and small footprint, 8-lead MSOP packages.

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REVISION HISTORY

04/08—Rev. E to Rev. F

Updated Format.....	Universal
Changes to Table 2.....	4
Updated Outline Dimension.....	13
Changes to Ordering Guide.....	14

10/03—Rev. D to Rev. E

Changes to Timing Specifications	2
Updated Ordering Guide.....	3

7/03—Rev. C to Rev. D

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1/03—Rev. B to Rev. C.

Change to Specifications	2
Change to Ordering Guide.....	3

12/02—Rev. A to Rev. B.

Deleted Q-8 Package	Universal
Edits to Features.....	1
Edits to General Description	1
Edits, additions to Specifications.....	2
Edits, additions to Absolute Maximum Ratings.....	3
Additions to Ordering Guide.....	3
TPCs Updated and Reformatted	5
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SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 5\%$, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}			5.0	V	$R = \infty$, see Figure 20
	2.0		5.0	V	$V_{CC} = 5\text{ V}$, $R = 50\ \Omega$ (RS-422), see Figure 20
	1.5		5.0	V	$R = 27\ \Omega$ (RS-485), see Figure 20
V_{OD3}	1.5		5.0	V	$V_{TST} = -7\text{ V}$ to $+12\text{ V}$, see Figure 21
$\Delta V_{OD} $ for Complementary Output States			0.2	V	$R = 27\ \Omega$ or $50\ \Omega$, see Figure 20
Common-Mode Output Voltage, V_{OC}			3	V	$R = 27\ \Omega$ or $50\ \Omega$, see Figure 20
$\Delta V_{OD} $ for Complementary Output States			0.2	V	$R = 27\ \Omega$ or $50\ \Omega$
Output Short-Circuit Current, $V_{OUT} = \text{High}$	35		250	mA	$-7\text{ V} \leq V_O \leq +12\text{ V}$
Output Short-Circuit Current, $V_{OUT} = \text{Low}$	35		250	mA	$-7\text{ V} \leq V_O \leq +12\text{ V}$
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0			V	
Logic Input Current (DE, DI)			± 1.0	μA	
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	-0.2		+0.2	V	$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$
Input Voltage Hysteresis, ΔV_{TH}		70		mV	$V_{CM} = 0\text{ V}$
Input Resistance	12			k Ω	$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$
Input Current (A, B)			1	mA	$V_{IN} = 12\text{ V}$
			-0.8	mA	$V_{IN} = -7\text{ V}$
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0			V	
Logic Enable Input Current (\overline{RE})			± 1	μA	
CMOS Output Voltage Low, V_{OL}			0.4	V	$I_{OUT} = 4.0\text{ mA}$
CMOS Output Voltage High, V_{OH}	4.0			V	$I_{OUT} = -4.0\text{ mA}$
Short-Circuit Output Current	7		85	mA	$V_{OUT} = \text{GND}$ or V_{CC}
Three-State Output Leakage Current			± 1.0	μA	$0.4\text{ V} \leq V_{OUT} \leq 2.4\text{ V}$
POWER SUPPLY CURRENT					
I_{CC} , Outputs Enabled		1.0	2.2	mA	Digital inputs = GND or V_{CC}
I_{CC} , Outputs Disabled		0.6	1	mA	Digital inputs = GND or V_{CC}

ADM485

TIMING SPECIFICATIONS

$V_{CC} = 5\text{ V} \pm 5\%$, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Propagation Delay Input to Output, t_{PLH} , t_{PHL}	2	10	15	ns	$R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 22
Driver Output to OUTPUT, t_{SKEW}		1	5	ns	$R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 22
Driver Rise/Fall Time, t_R , t_F		8	15	ns	$R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 22
Driver Enable to Output Valid		10	25	ns	$R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 23
Driver Disable Timing		10	25	ns	$R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 23
Matched Enable Switching $ t_{ZH} - t_{ZL} $		0	2	ns	$R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 23 ¹
Matched Disable Switching $ t_{HZ} - t_{LZ} $		0	2	ns	$R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 23 ¹
RECEIVER					
Propagation Delay Input to Output, t_{PLH} , t_{PHL}	8	15	30	ns	$C_L = 15\text{ pF}$, see Figure 24
Skew $ t_{PLH} - t_{PHL} $			5	ns	$C_L = 15\text{ pF}$, see Figure 24
Receiver Enable, t_{ZH} , t_{ZL}		5	20	ns	$C_L = 15\text{ pF}$, $R_L = 1\text{ k}\Omega$, see Figure 25
Receiver Disable, t_{HZ} , t_{LZ}		5	20	ns	$C_L = 15\text{ pF}$, $R_L = 1\text{ k}\Omega$, see Figure 25
Tx Pulse Width Distortion		1		ns	
Rx Pulse Width Distortion		1		ns	

¹ Guaranteed by characterization.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	-0.3 V to +7 V
Inputs	
Driver Input (DI)	-0.3 V to $V_{CC} + 0.3$ V
Control Inputs (DE, \overline{RE})	-0.3 V to $V_{CC} + 0.3$ V
Receiver Inputs (A, B)	-9 V to +14 V
Outputs	
Driver Outputs (A, B)	-9 V to +14 V
Receiver Output	-0.5 V to $V_{CC} + 0.5$ V
Power Dissipation 8-Lead MSOP	900 mW
θ_{JA} , Thermal Impedance	206°C/W
Power Dissipation 8-Lead PDIP	500 mW
θ_{JA} , Thermal Impedance	130°C/W
Power Dissipation 8-Lead SOIC	450 mW
θ_{JA} , Thermal Impedance	170°C/W
Operating Temperature Range	
Commercial Range (J Version)	0°C to 70°C
Industrial Range (A Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Transmitting

Inputs		Outputs	
DE	DI	B	A
1	1	0	1
1	0	1	0
0	X ¹	Z ²	Z ²

¹ X = don't care.

² Z = high impedance.

Table 5. Receiving

\overline{RE}	Input A – Input B	Output RO
0	$\geq +0.2$ V	1
0	≤ -0.2 V	0
0	Inputs open	1
1	X ¹	Z ²

¹ X = don't care.

² Z = high impedance.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADM485

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

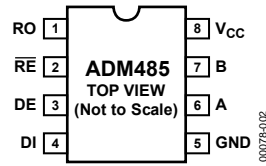


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	RO	Receiver Output. When enabled, if A is greater than B by 200 mV, RO is high. If A is less than B by 200 mV, RO is low.
2	\overline{RE}	Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state.
3	DE	Driver Output Enable. A high level enables the driver differential outputs, A and B. A low level places it in a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high, while a logic high on DI forces A high and B low.
5	GND	Ground Connection, 0 V.
6	A	Noninverting Receiver Input A/Driver Output A.
7	B	Inverting Receiver Input B/Driver Output B.
8	VCC	Power Supply, 5 V \pm 5%.

TYPICAL PERFORMANCE CHARACTERISTICS

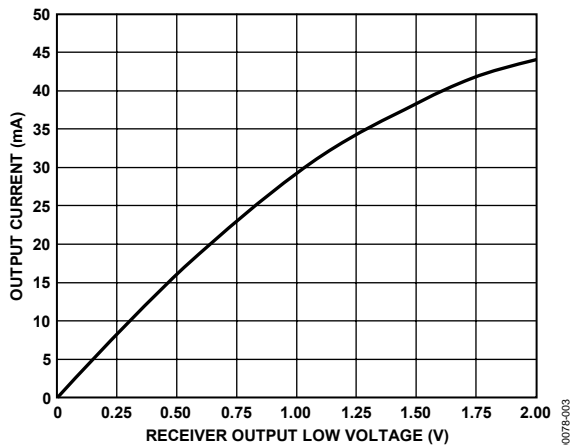


Figure 3. Output Current vs. Receiver Output Low Voltage

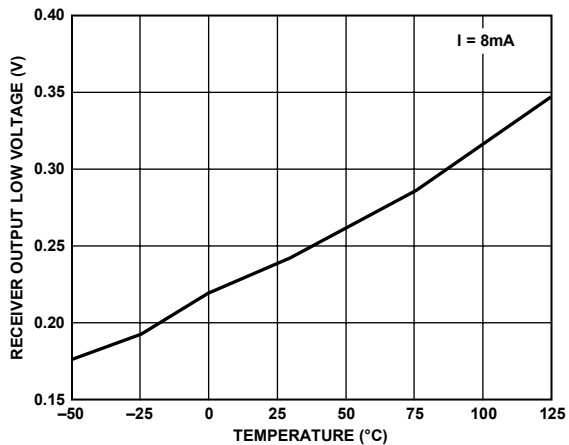


Figure 6. Receiver Output Low Voltage vs. Temperature

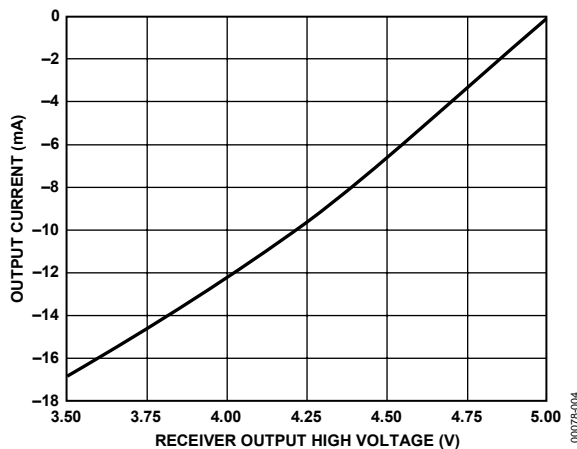


Figure 4. Output Current vs. Receiver Output High Voltage

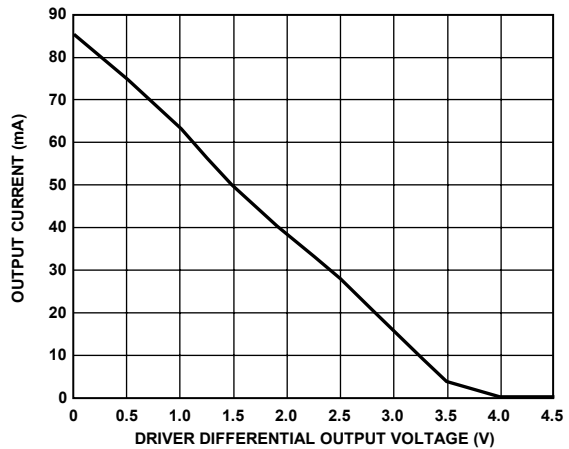


Figure 7. Output Current vs. Driver Differential Output Voltage

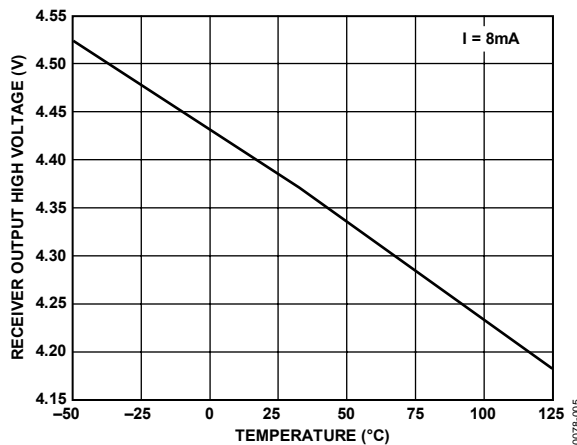


Figure 5. Receiver Output High Voltage vs. Temperature

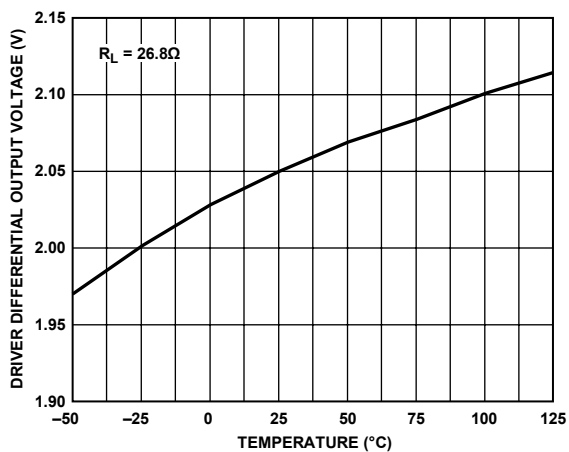


Figure 8. Driver Differential Output Voltage vs. Temperature

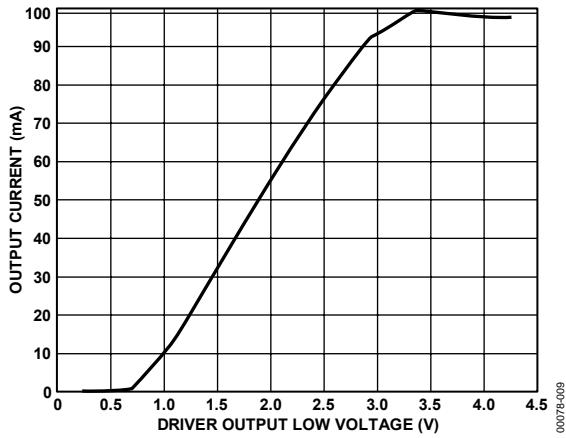


Figure 9. Output Current vs. Driver Output Low Voltage

00078-009

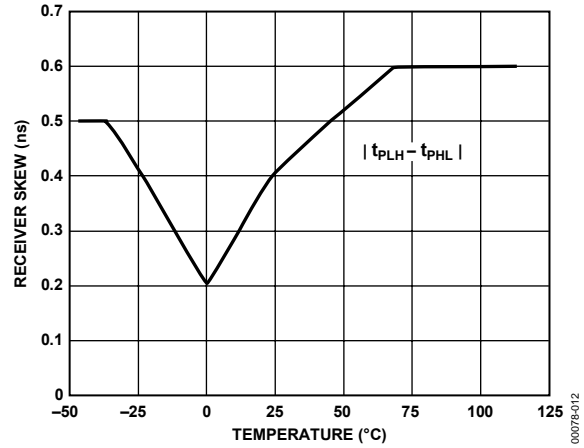


Figure 12. Receiver Skew vs. Temperature

00078-012

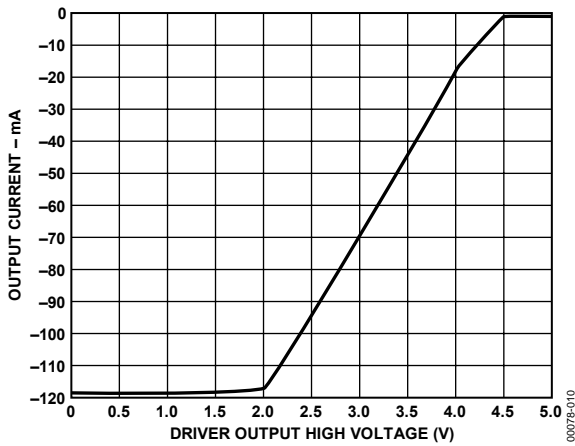


Figure 10. Output Current vs. Driver Output High Voltage

00078-010

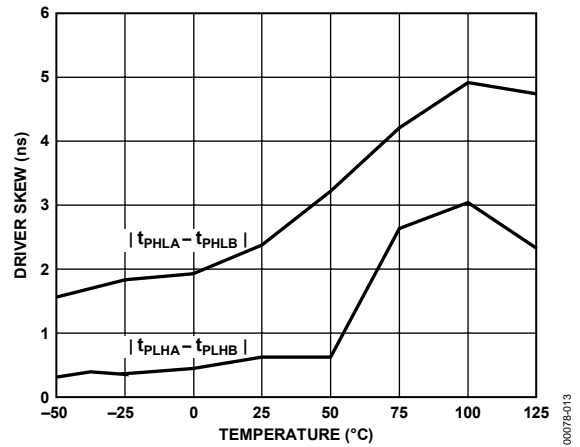


Figure 13. Driver Skew vs. Temperature

00078-013

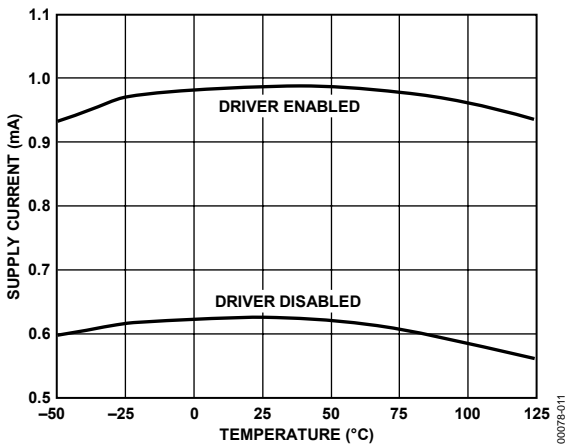


Figure 11. Supply Current vs. Temperature

00078-011

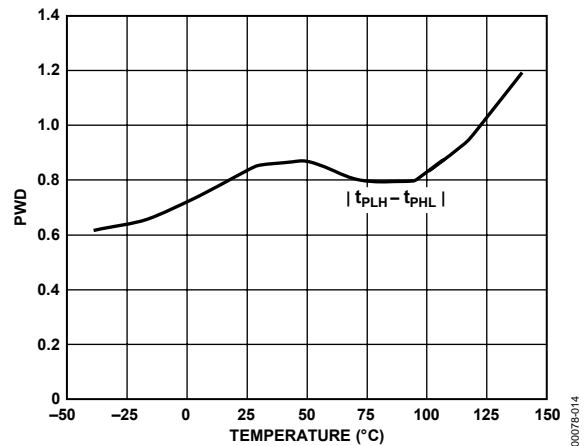


Figure 14. Driver Pulse Width Distortion (PWD) vs. Temperature

00078-014

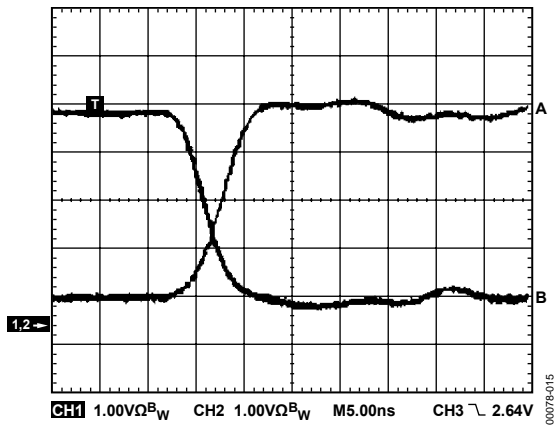


Figure 15. Unloaded Driver Differential Outputs

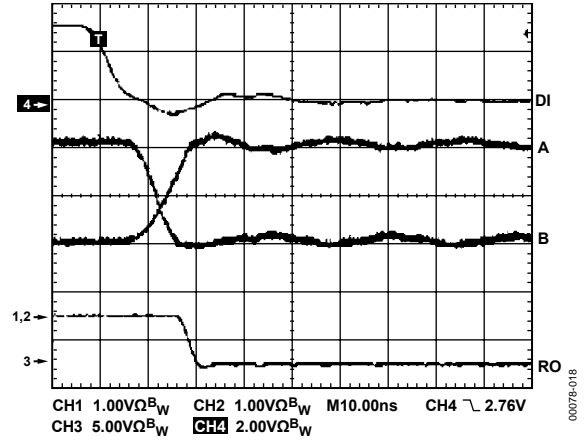


Figure 18. Driver/Receiver Propagation Delays, High to Low

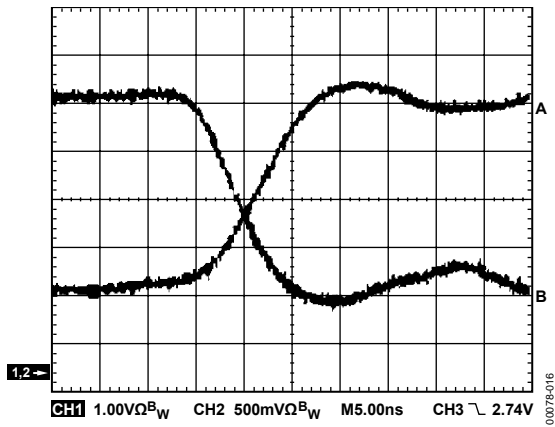


Figure 16. Loaded Driver Differential Outputs

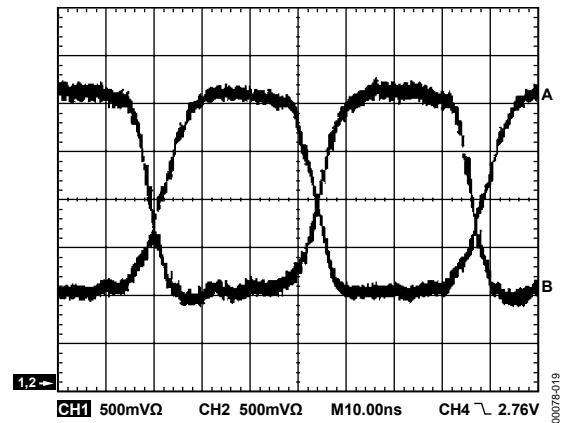


Figure 19. Driver Output at 30 Mbps

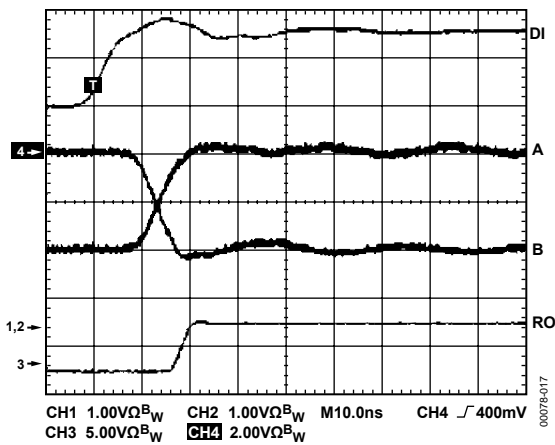


Figure 17. Driver/Receiver Propagation Delays, Low to High

TEST CIRCUITS

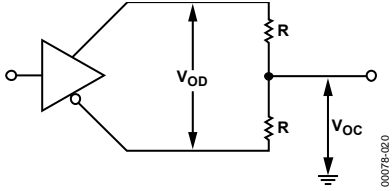


Figure 20. Driver Voltage Measurement

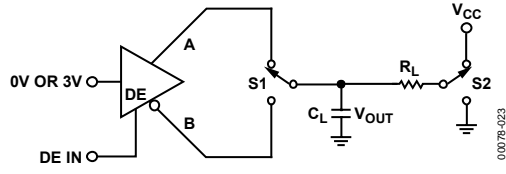


Figure 23. Driver Enable/Disable

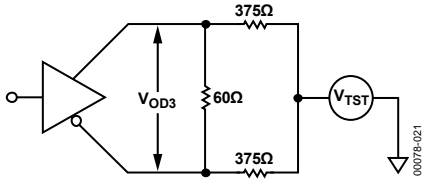


Figure 21. Driver Voltage Measurement

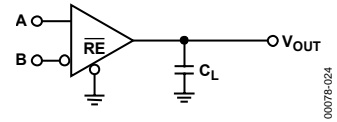


Figure 24. Receiver Propagation Delay

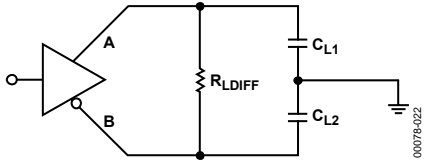


Figure 22. Driver Propagation Delay

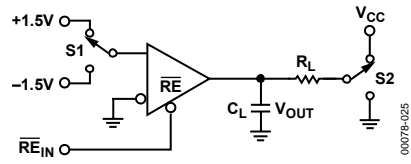
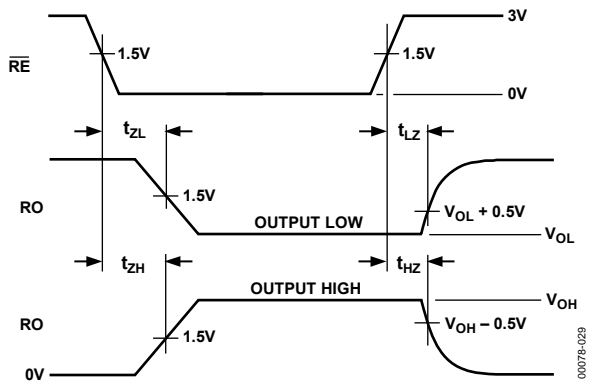
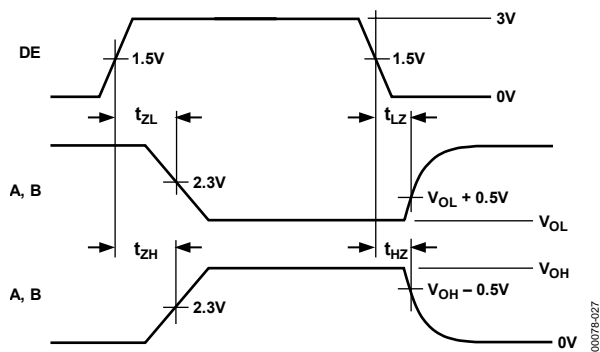
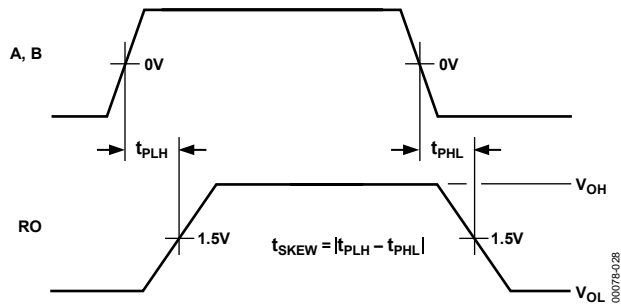
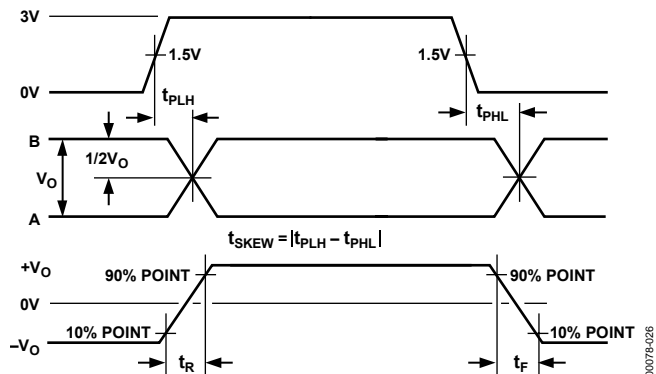


Figure 25. Receiver Enable/Disable

SWITCHING CHARACTERISTICS



APPLICATIONS INFORMATION

DIFFERENTIAL DATA TRANSMISSION

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line. There are two main standards approved by the EIA that specify the electrical characteristics of transceivers used in differential data transmission.

The RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

To cater to true multipoint communications, the RS-485 standard was defined. This standard meets or exceeds all the requirements of RS-422 but also allows for up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of -7 V to $+12\text{ V}$ is defined. The most significant difference between the RS-422 standard and the RS-485 standard is the fact that the drivers can be disabled, thereby allowing more than one (32 in fact) to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

Table 7. Comparison of RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	$\pm 2\text{ V}$	$\pm 1.5\text{ V}$
Driver Load Impedance	$100\ \Omega$	$54\ \Omega$
Receiver Input Resistance	$4\text{ k}\Omega$ min	$12\text{ k}\Omega$ min
Receiver Input Sensitivity	$\pm 200\text{ mV}$	$\pm 200\text{ mV}$
Receiver Input Voltage Range	-7 V to $+7\text{ V}$	-7 V to $+12\text{ V}$
No. of Drivers/Receivers per Line	1/10	32/32

CABLE AND DATA RATE

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM485 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 30. An RS-485 transmission line can have as many as 32 transceivers on the bus. Only one driver can transmit at a particular time, but multiple receivers can be enabled simultaneously.

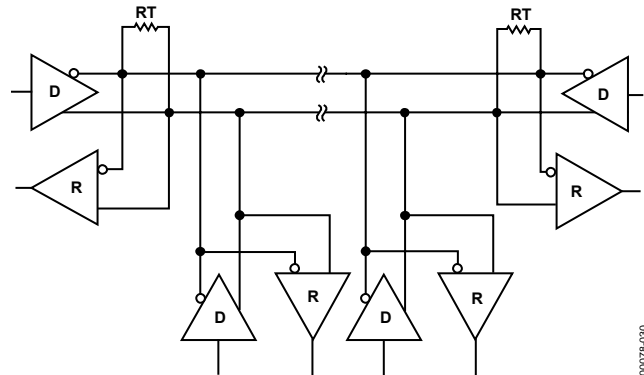


Figure 30. Typical RS-485 Network

As with any transmission line, it is important that reflections be minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

THERMAL SHUTDOWN

The ADM485 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature and disables the driver outputs. The thermal sensing circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at 140°C .

PROPAGATION DELAY

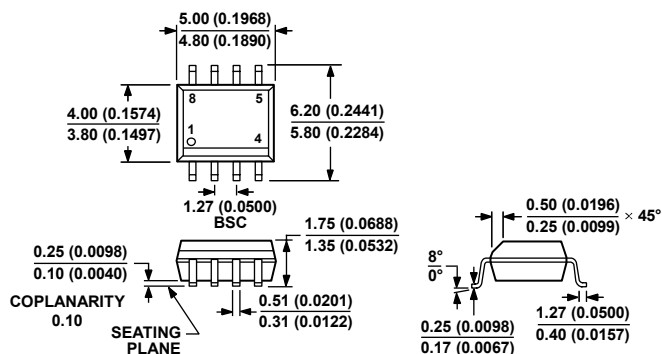
The ADM485 features very low propagation delay, ensuring maximum baud rate operation. The driver is well balanced, ensuring distortion free transmission.

Another important specification is a measure of the skew between the complementary outputs. Excessive skew impairs the noise immunity of the system and increases the amount of electromagnetic interference (EMI).

RECEIVER OPEN CIRCUIT, FAIL-SAFE

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.

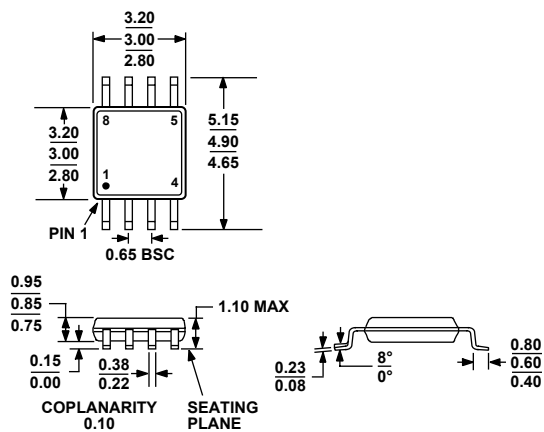
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

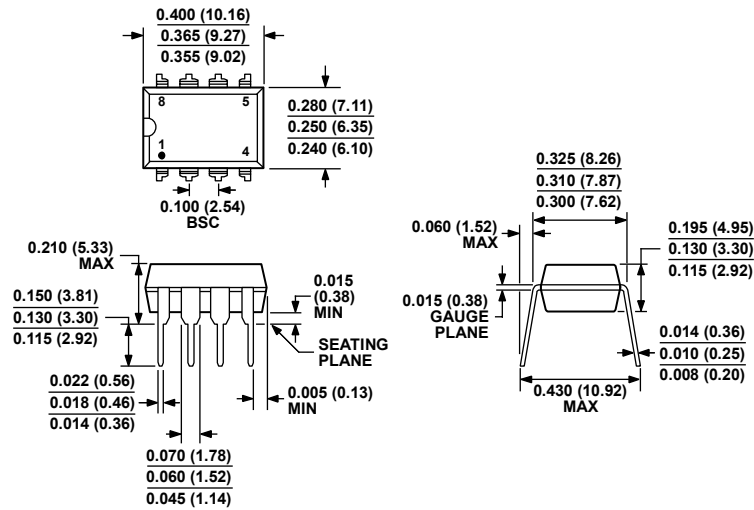
Figure 31. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body (R-8)
 Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 32. 8-Lead Mini Small Outline Package [MSOP]
 (RM-8)
 Dimensions shown in millimeters

ADM485



COMPLIANT TO JEDEC STANDARDS MS-001
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
 CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 33. 8-Lead Plastic Dual In-Line Package [PDIP]
 Narrow Body (N-8)
 Dimensions shown in inches and (millimeters)

070606-A

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADM485AN	-40°C to +85°C	8-Lead PDIP	N-8	
ADM485ANZ ¹	-40°C to +85°C	8-Lead PDIP	N-8	
ADM485AR	-40°C to +85°C	8-Lead SOIC_N	R-8	
ADM485AR-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8	
ADM485ARZ ¹	-40°C to +85°C	8-Lead SOIC_N	R-8	
ADM485ARZ-REEL ¹	-40°C to +85°C	8-Lead SOIC_N	R-8	
ADM485ARM	-40°C to +85°C	8-Lead MSOP	RM-8	M41
ADM485ARM-REEL	-40°C to +85°C	8-Lead MSOP	RM-8	M41
ADM485ARM-REEL7	-40°C to +85°C	8-Lead MSOP	RM-8	M41
ADM485ARMZ ¹	-40°C to +85°C	8-Lead MSOP	RM-8	M41#
ADM485ARMZ-REEL ¹	-40°C to +85°C	8-Lead MSOP	RM-8	M41#
ADM485ARMZ-REEL7 ¹	-40°C to +85°C	8-Lead MSOP	RM-8	M41#
ADM485JN	0°C to 70°C	8-Lead PDIP	N-8	
ADM485JNZ ¹	0°C to 70°C	8-Lead PDIP	N-8	
ADM485JR	0°C to 70°C	8-Lead SOIC_N	R-8	
ADM485JR-REEL	0°C to 70°C	8-Lead SOIC_N	R-8	
ADM485JR-REEL7	0°C to 70°C	8-Lead SOIC_N	R-8	
ADM485JRZ ¹	0°C to 70°C	8-Lead SOIC_N	R-8	
ADM485JRZ-REEL ¹	0°C to 70°C	8-Lead SOIC_N	R-8	
ADM485JRZ-REEL7 ¹	0°C to 70°C	8-Lead SOIC_N	R-8	

¹ Z = RoHS Compliant Part, # denotes RoHS compliant product may be top or bottom marked.

NOTES

ADM485

NOTES

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