



THE DATASHEET OF SL50N06D



N-Channel Enhancement Mode Power MOSFET

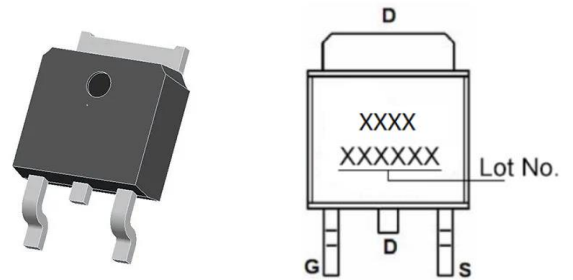
Description

The Power Device is produced using advanced TRENCH technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

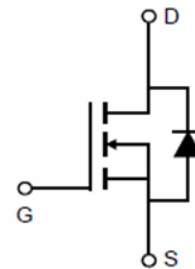
Features

- $V_{DS}=60V$, $I_D=50A$
- $R_{DS(ON)TYP} = 14m\Omega @ V_{GS} = 10V$
- Low gate charge (typical 33nC)
- High ruggedness
- Fast switching
- Good stability and uniformity with high EAS
- Improved dv/dt capability



TO252-2L TOP VIEW

Marking and Pin Assignment



Schematic diagram

Applications

- DC/DC Converters in Computing, Servers
- Isolated DC/DC Converters in Telecom and Industrial
- Uninterruptible Power Supply

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Package Marking and Ordering Information

Device	Marking	Package	Packing	Reel (pcs)
SL50N06D		TO-252	Reel	2500

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DS}	60	V
Gate-source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	50
		$T_C=100^\circ\text{C}$	30
Pulsed Drain Current($T_C=25^\circ\text{C}$, T_p Limited By T_{jmax}) ^(note1)	I_{DM}	200	A
Maximum Power Dissipation($T_C=25^\circ\text{C}$)	P_D	60	W
Avalanche energy , single Pulse($L=0.5\text{mH}$) ^(note2)	E_{AS}	450	mJ
Peak Diode Recovery dv/dt ^(note3)	dv/dt	4.5	V/ns
Operating Junction And Storage Temperature	T_j, T_{stg}	-55 To 175	$^\circ\text{C}$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	T_L	300	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Max	Unit
Junction-to-Case	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

Note:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. $I_{AS}=50\text{A}$, $V_{DD}=50\text{V}$, $R_g=25\Omega$,Starting $T_j=25^\circ\text{C}$.
3. $I_{SD} \leq 50\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_j = 25^\circ\text{C}$.
4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
5. Essentially independent of operating temperature.

Electrical Characteristic (TC=25°C unless otherwise noted)

Parameter	Symbol	Value			Unit	Test Condition
		Min.	Typ.	Max.		
Off Characteristic						
Drain-source breakdown voltage	BV_{DSS}	60	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=60V, V_{GS}=0V$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 25V, V_{DS}=0V$
On Characteristics						
Gate threshold voltage	$V_{GS(th)}$	1.0	1.6	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Drain-source on-state resistance	$R_{DS(on)}$	-	14	16	m Ω	$V_{GS}=10V, I_D=25A,$
Transconductance (note4)	G_{fs}	-	24	-	S	$V_{DS}=25V, I_D=25A$
Dynamic Characteristic						
Input Capacitance	C_{iss}	-	2800	-	PF	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$
Output Capacitance	C_{oss}	-	110	-		
Reverse Transfer Capacitance	C_{rss}	-	103	-		
Switching Characteristics						
Turn-on delay time	$t_{d(on)}$	-	15	-	nS	$V_{DD}=30V, I_D=25A,$ $R_G=25\Omega$ (note4,5)
Turn-on Rise time	t_r	-	105	-		
Turn-off delay time	$t_{d(off)}$	-	60	-		
Turn-off Fall time	t_f	-	65	-		
Gate Total Charge	Q_G	-	27	-	nC	$V_{GS}=4.5V, V_{DS}=30V, I_D=20A$ (note4,5)
Gate-Source Charge	Q_{gs}	-	14	-		
Gate-Drain Charge	Q_{gd}	-	6	-		
Drain-Source Diode Characteristics						
Body Diode Forward Voltage	V_{SD}	-	-	1.4	V	$V_{GS}=0V, I_{SD}=50A$
Body Diode Forward Current	I_S	-	-	50	A	-
Body Diode Reverse Recovery Time	T_{rr}	-	60	-	ns	$T_J=25^\circ C, I_{SD}=50A, V_{GS}=0V,$ $d_i/d_t=100A/\mu s$ (note4)
Body Diode Reverse Recovery Charge	Q_{rr}	-	80	-	nC	

N- Channel Typical Characteristics

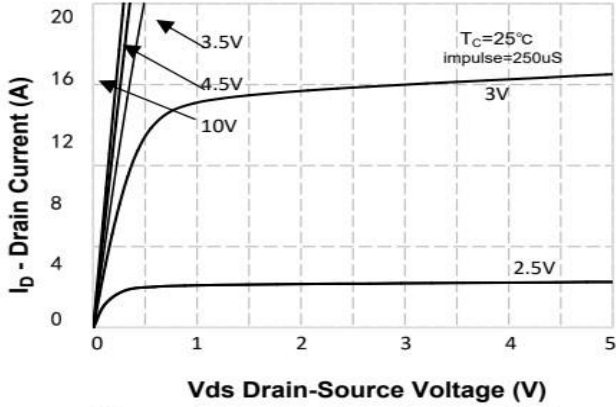


Figure 1. On-Region Characteristics

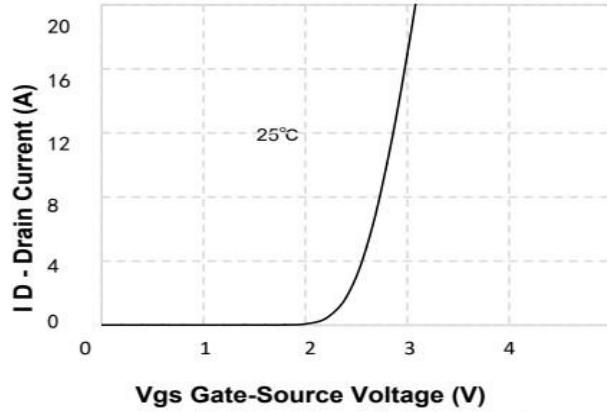


Figure 2. Transfer Characteristics

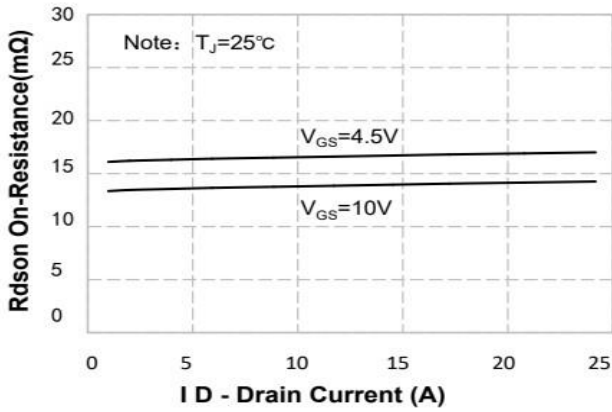


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

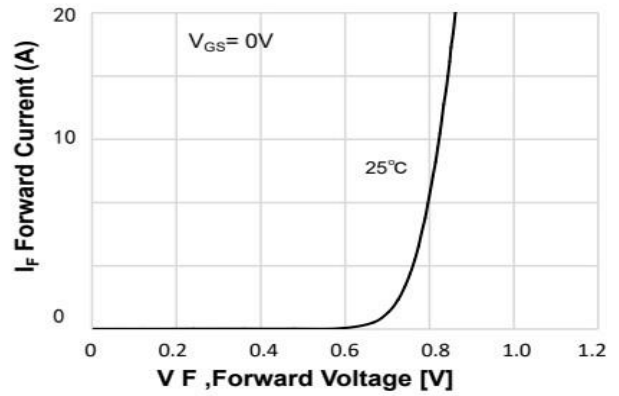


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

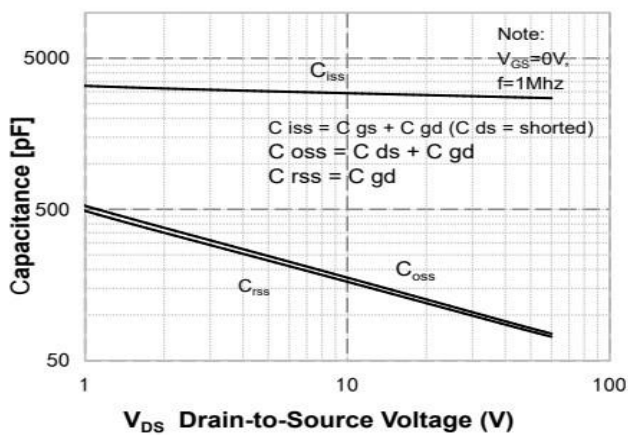


Figure 5. Capacitance Characteristics

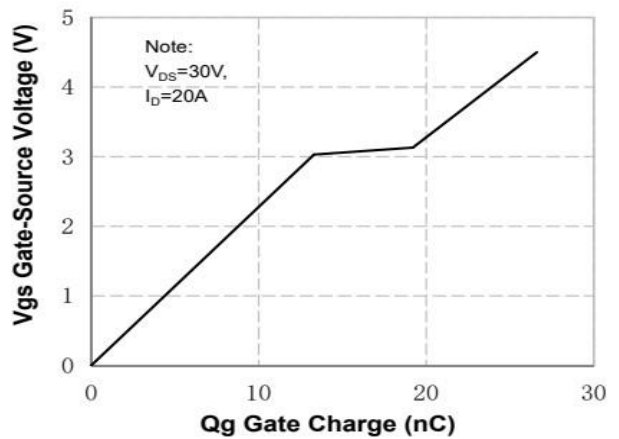


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

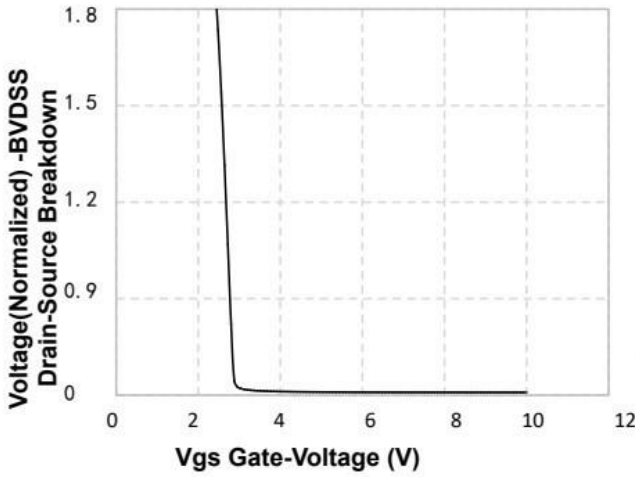


Figure 7. Breakdown Voltage Variation vs Gate-Voltage

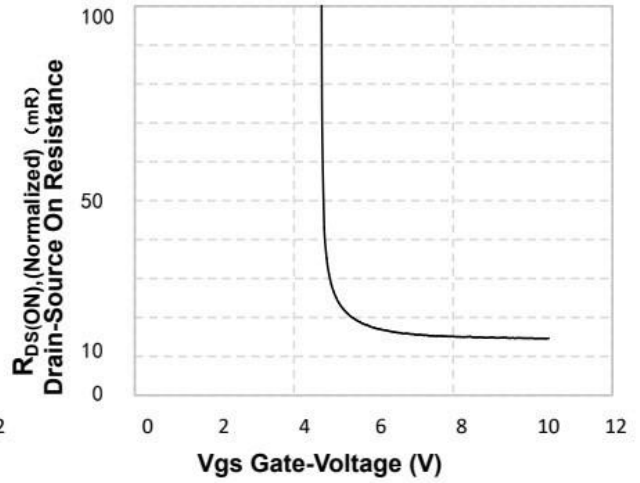


Figure 8. On-Resistance Variation vs Gate Voltage

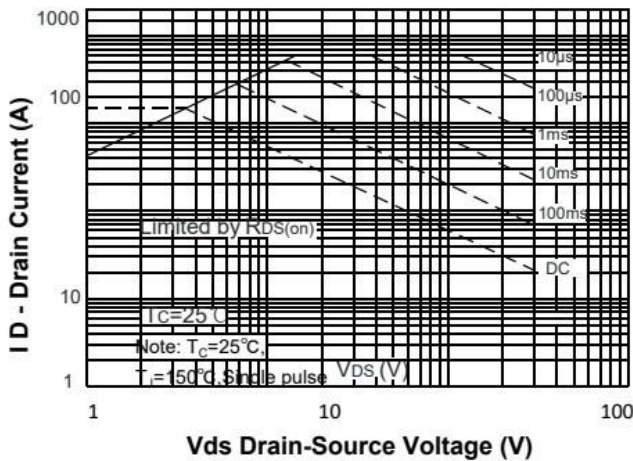


Figure 9. Maximum Safe Operating Area

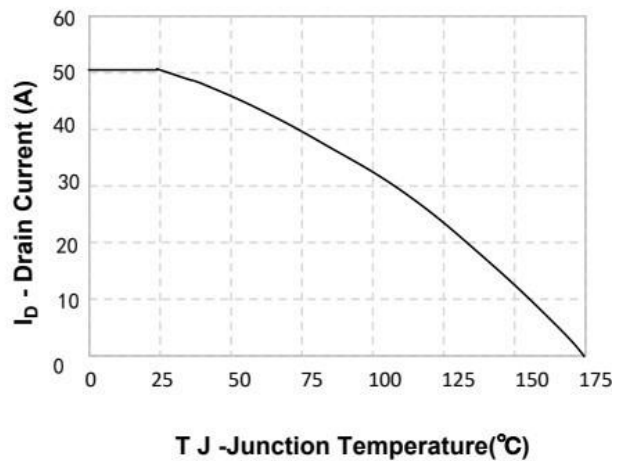


Figure 10. Maximum PContinuous Drain Current vs Case Temperature

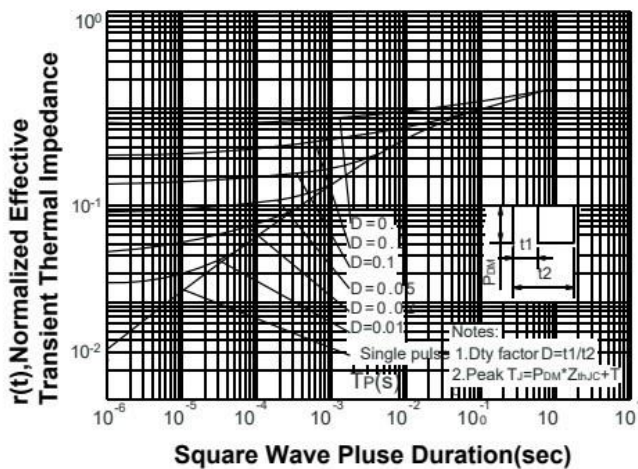
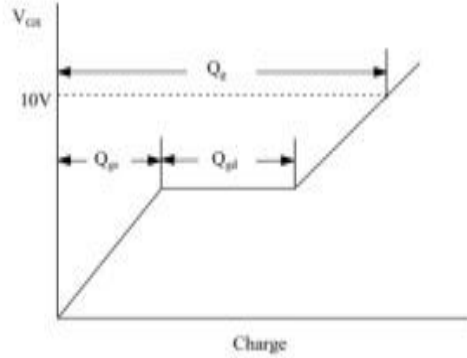
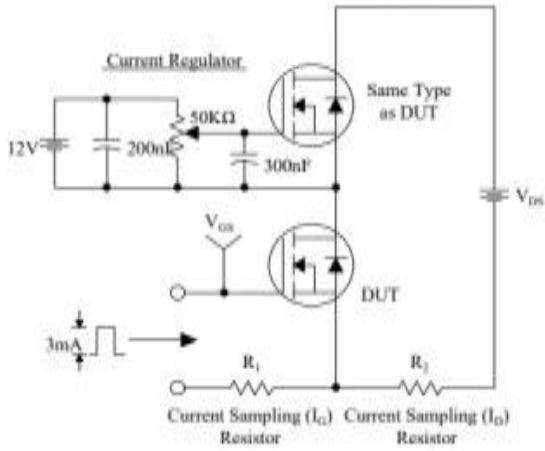
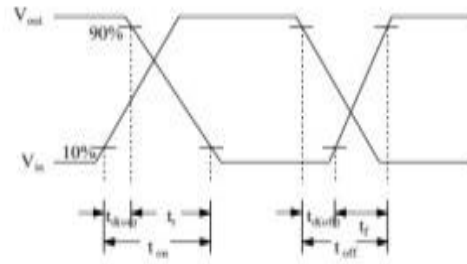
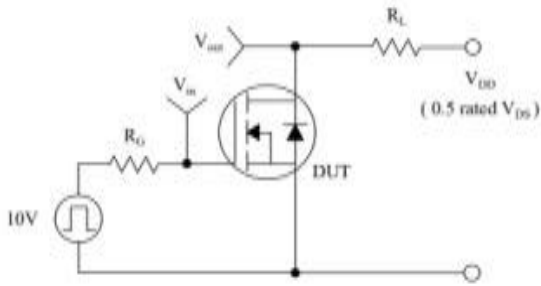


Figure 11. Transient Thermal Response Curve

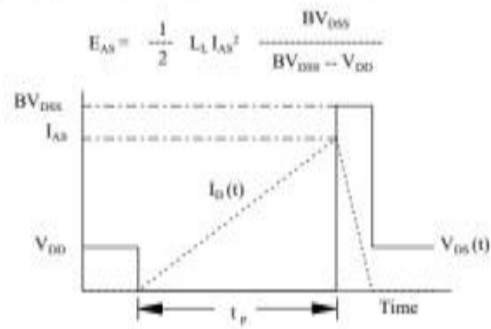
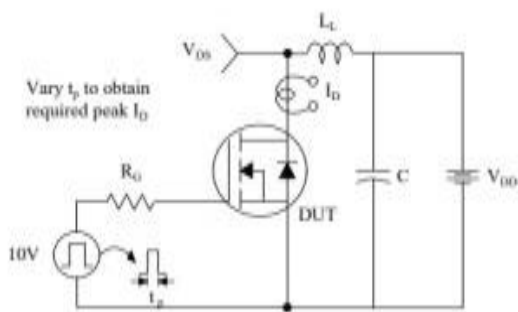
Gate Charge Test Circuit & Waveform



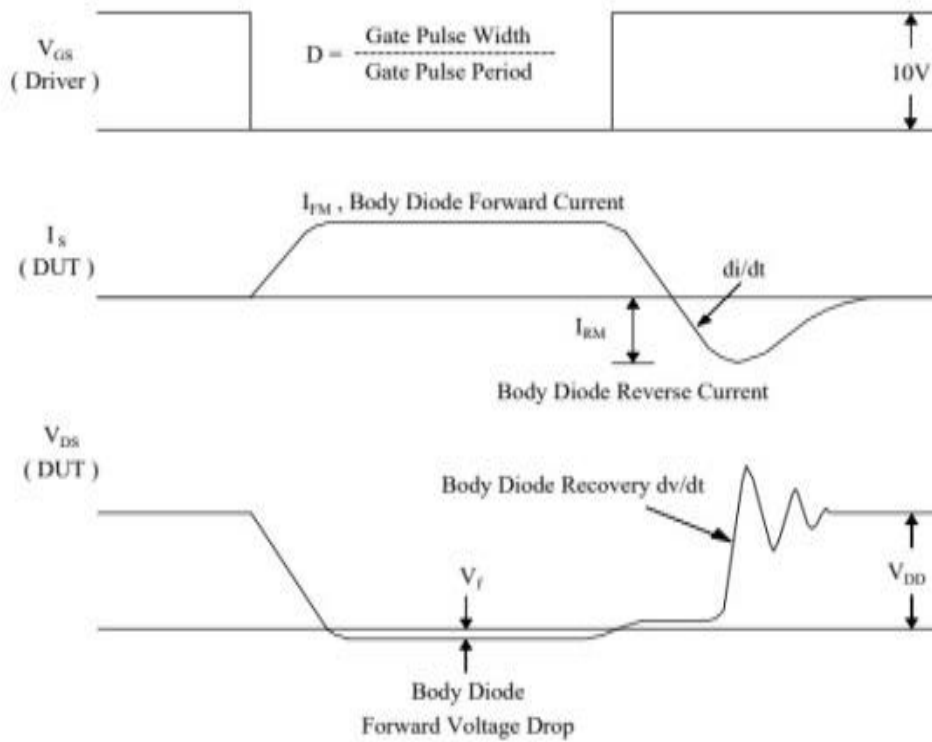
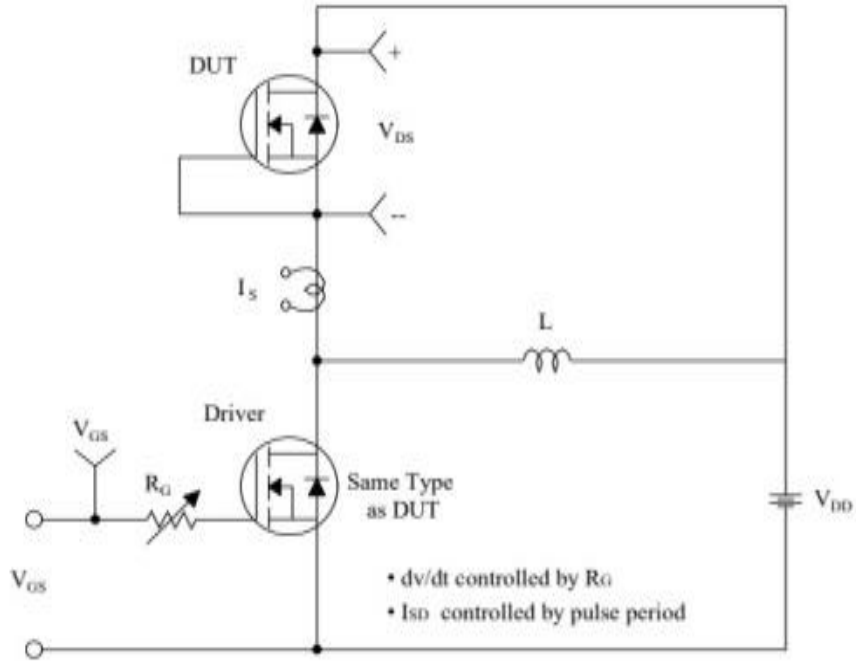
Resistive Switching Test Circuit & Waveforms

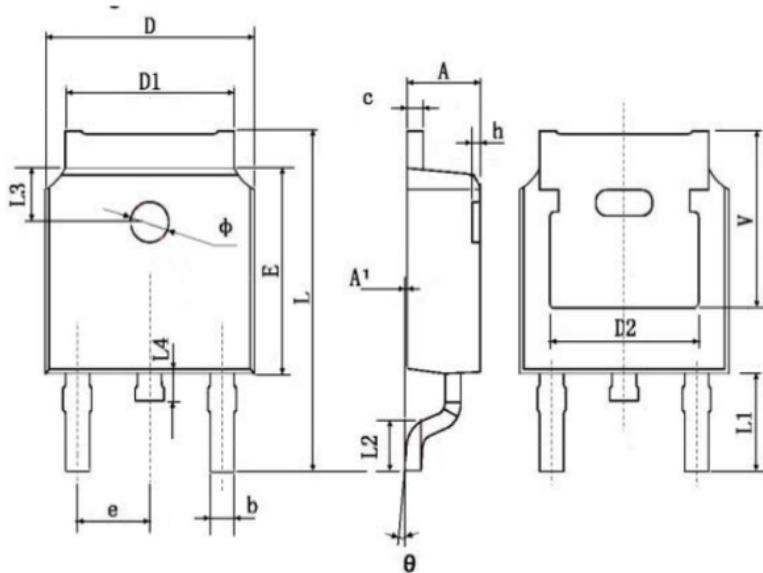


Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Information
TO-252 DPAK


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.250	2.350	0.089	0.093
A1	0.050	0.150	0.002	0.006
b	0.660	0.860	0.026	0.034
c	0.458	0.558	0.018	0.022
D	6.550	6.650	0.259	0.263
D1	5.234	5.434	0.207	0.215
D2	4.826 TYP.		0.191 TYP.	
E	6.050	6.150	0.239	0.243
e	2.236	2.336	0.088	0.092
L	9.820	10.220	0.388	0.404
L1	3.000 TYP.		0.119 TYP.	
L2	1.400	1.600	0.055	0.063
L3	1.800 TYP.		0.071 TYP.	
L4	0.700	0.900	0.028	0.036
φ	1.150	1.250	0.045	0.049
θ	0°	3°	0°	3°
h	0.000	0.300	0.000	0.012
V	5.399 TYP		0.213 TYP	

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