Freescale Semiconductor
Technical Data

Document Number: MHT2001N
Rev. 0, 6/2016

RF LDMOS Integrated Power Amplifier

This 175 W CW RF power integrated circuit is designed for consumer and commercial cooking applications operating in the 915 MHz ISM band.

Typical Performance: V_{DD} = 45 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 0 mA

Frequency (MHz)	Signal Type	G_{ps} (dB)	η_D 2nd Stage Eff. (%)	PAE (%)	P_{out} (W)
902	CW	33.8	73.4	65.1	206
915		33.9	73.0	64.8	191
928		33.8	72.8	64.0	181

Load Mismatch/Ruggedness

Frequency (MHz)	Signal Type	VSWR	P_{in} (dBm)	Test Voltage	Result
915	CW	> 10:1 at all Phase Angles	25 (3 dB Overdrive)	50	No Device Degradation

Features

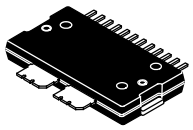
- Characterized with series equivalent large-signal impedance parameters and common source S-parameters
- Internally input matched
- Qualified for operation at 50 Vdc
- On-chip input and interstage matching (50 ohm input)
- Integrated quiescent current temperature compensation (1)
- Integrated ESD protection
- 150°C case operating temperature
- 225°C die temperature capability
- Integrated power and temperature sensors

Target Applications

- Consumer cooking
- Commercial cooking

MHT2001N

902–928 MHz, 175 W CW, 50 V RF LDMOS INTEGRATED POWER AMPLIFIER FOR CONSUMER AND COMMERCIAL COOKING



TO-270WB-14 PLASTIC

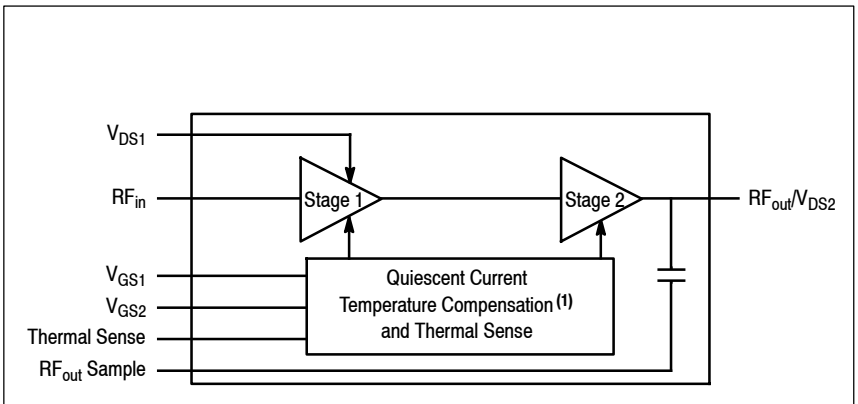
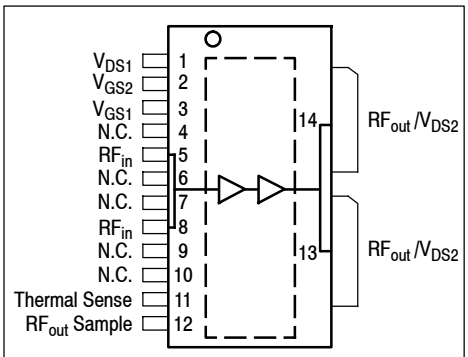


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate–Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
Input Power	P_{in}	25	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 88°C, 175 W CW, 915 MHz Stage 1, 50 Vdc, I_{DQ1} = 84 mA Stage 2, 50 Vdc, I_{DQ2} = 55 mA	$R_{\theta JC}$	 2.7 0.58	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	2, passes 2500 V
Machine Model (per EIA/JESD22–A115)	A, passes 150 V
Charge Device Model (per JESD22–C101)	II, passes 200 V

Table 4. Moisture Sensitivity Level (MSL)

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 — On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 53 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Stage 2 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 — On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 528 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.6 Adc)	$V_{DS(on)}$	0.1	0.25	0.5	Vdc
Dynamic Characteristics (1)					
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	42.4	—	pF

1. Part is input matched. Only output capacitance is measurable.

Table 6. Typical Performance

In Freescale Reference Circuit, 50 ohm system, V_{DD} = 45 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 0 mA, 902–928 MHz Bandwidth

Characteristic		Symbol	Min	Typ	Max	Unit
Power Gain		G_{ps}	—	33.8	—	dB
2nd Stage Drain Efficiency		η_D	—	72.8	—	%
Power Added Efficiency		PAE	—	64	—	%
P_{out} @ 1 dB Compression Point		P1dB	—	160	—	W
P_{out} @ 3 dB Compression Point		P3dB	—	181	—	W
Quiescent Current Accuracy over Temperature (1) with 2.2 kΩ Gate Feed Resistors (–20 to 95°C)	Stage 1 Stage 2	ΔI_{QT}	—	2.7 2.7	—	%
Gain Variation over Temperature (–20°C to +95°C)		ΔG	—	0.007	—	dB/°C
Output Power Variation over Temperature (–20°C to +95°C)		ΔP1dB	—	0.007	—	dB/°C

Table 7. Load Mismatch/Ruggedness

In Freescale Reference Circuit, 50 ohm system, I_{DQ1} = 80 mA, I_{DQ2} = 0 mA

Frequency (MHz)	Signal Type	VSWR	P_{in} (dBm)	Test Voltage, V_{DD}	Result
915	CW	> 10:1 at all Phase Angles	25 (3 dB Overdrive)	50	No Device Degradation

Table 8. Ordering Information

Device	Tape and Reel Information	Package
MHT2001NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-14

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

TYPICAL CHARACTERISTICS

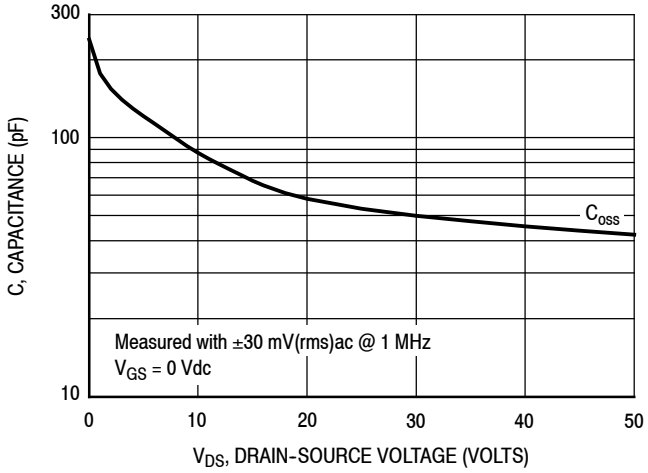


Figure 3. Capacitance versus Drain-Source Voltage (Second Stage Only)

Table 9. Load Pull Performance — Maximum Power Tuning

V_{DD} = 50 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 10 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power				
			P1dB				
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)
900	25.5 + j14.5	21.5 – j7.94	1.42 + j0.25	33.5	55.2	333	58.3
920	23.8 + j15.9	24.8 – j10.4	1.36 + j0.33	33.5	55.1	322	58.0
940	25.5 + j14.8	26.8 – j13.4	1.30 + j0.35	33.5	55.1	324	58.6

			Max Output Power				
			P3dB				
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)
900	25.5 + j14.5	23.8 – j10.6	1.42 + j0.20	31.4	55.5	354	56.4
920	23.8 + j15.9	26.4 – j14.2	1.33 + j0.28	31.4	55.3	339	55.4
940	25.5 + j14.8	27.3 – j17.7	1.32 + j0.30	31.4	55.3	340	57.1

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

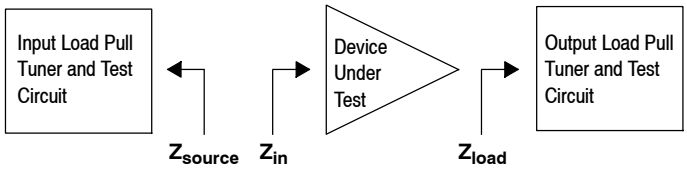
Table 10. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 50 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 10 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency				
			P1dB				
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)
900	25.5 + j14.5	24.0 – j7.30	1.51 + j2.08	34.4	52.7	184	72.6
920	23.8 + j15.9	27.7 – j10.5	1.36 + j1.97	34.4	52.5	178	72.9
940	25.5 + j14.8	29.5 – j14.5	1.34 + j1.86	34.3	52.8	188	73.1

			Max Drain Efficiency				
			P3dB				
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)
900	25.5 + j14.5	23.9 – j9.79	2.00 + j1.41	32.2	54.6	287	69.0
920	23.8 + j15.9	26.5 – j13.3	1.86 + j1.45	32.2	54.4	273	68.3
940	25.5 + j14.8	27.7 – j16.8	1.74 + j1.51	32.2	54.3	269	69.9

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P3dB – TYPICAL LOAD PULL CONTOURS — 920 MHz

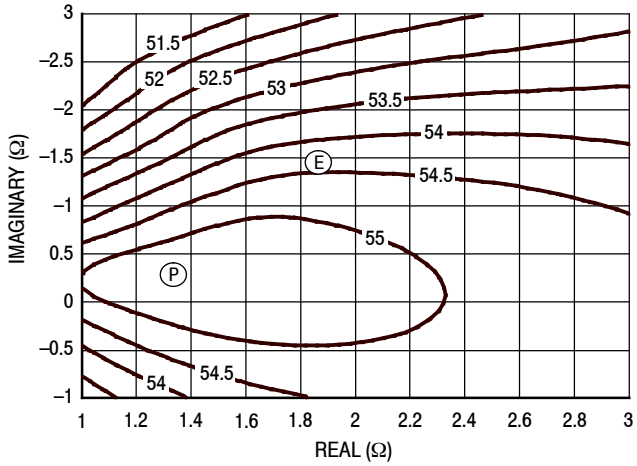


Figure 4. P3dB Load Pull Output Power Contours (dBm)

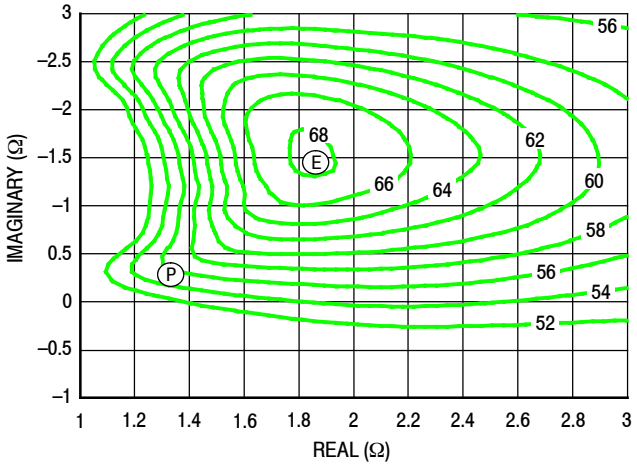


Figure 5. P3dB Load Pull Efficiency Contours (%)

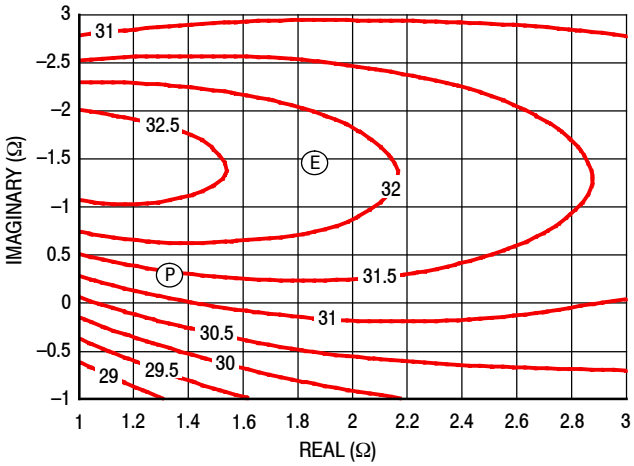


Figure 6. P3dB Load Pull Gain Contours (dB)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

915 MHz REFERENCE CIRCUIT — 3.2″ × 2.8″ (8.1″ cm × 7.1″ cm)

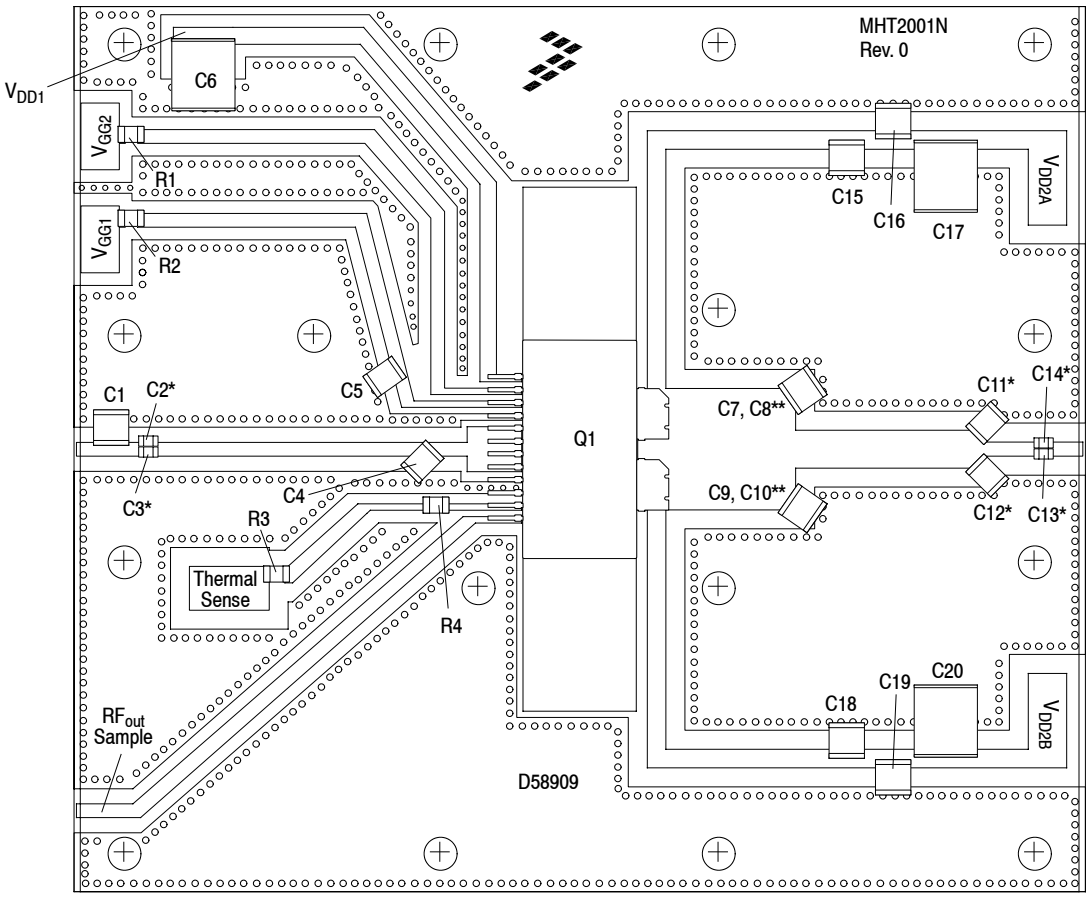
Table 11. 915 MHz Performance (In Freescale Reference Circuit, 50 ohm system)
V_{DD} = 45 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 0 mA, T_A = 25°C

Frequency (MHz)	P_{in} (dBm)	G_{ps} (dB)	η_D 2nd Stage Eff. (%)	PAE (%)	P_{out} (W)
902	22.3	33.8	73.4	65.1	206
915	21.9	33.9	73.0	64.8	191
928	21.8	33.8	72.8	64.0	181

Table 12. Load Mismatch/Ruggedness (In Freescale Reference Circuit)

Frequency (MHz)	Signal Type	VSWR	P_{in} (dBm)	Test Voltage, V_{DD}	Result
915	CW	> 10:1 at all Phase Angles	25 (3 dB Overdrive)	50	No Device Degradation

915 MHz REFERENCE CIRCUIT — 3.2″ × 2.8″ (8.1″ cm × 7.1″ cm)



*C2, C3, C11, C12, C13 and C14 are mounted vertically.
**C7 and C8, C9 and C10 are stacked.

Figure 7. MHT2001N Reference Circuit Component Layout — 915 MHz

Table 13. MHT2001N Reference Circuit Component Designations and Values — 915 MHz

Part	Description	Part Number	Manufacturer
C1	3.3 pF Chip Capacitor	ATC800B3R3BT500XT	ATC
C2, C3, C13, C14	47 pF Chip Capacitors	ATC600S470JT250XT	ATC
C4	1.1 pF Chip Capacitor	ATC800B1R1BT500XT	ATC
C5	1 μF Chip Capacitor	C3216X5R1H105K160AA	TDK
C6, C17, C20	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C7, C9	12 pF Chip Capacitors	ATC800B120JT500XT	ATC
C8, C10	1.7 pF Chip Capacitors	ATC800B1R7BT500XT	ATC
C11	6.8 pF Chip Capacitor	ATC800B6R8CT500XT	ATC
C12	1 pF Chip Capacitor	ATC800B1R0BT500XT	ATC
C15, C18	8.2 pF Chip Capacitors	ATC800B8R2BT500XT	ATC
C16, C19	47 pF Chip Capacitors	ATC800B470JT500XT	ATC
Q1	RF Power LDMOS Power Amplifier	MHT2001N	NXP
R1, R2	2.2 kΩ, 1/8 W Chip Resistors	WCR0805-2K2FI	Welwyn
R3	0 Ω, 1 A Chip Resistor	CWCR08050000Z0EA	Vishay
R4	1 kΩ, 1/4 W Chip Resistor	WCR0805-1KFI	Welwyn
PCB	Arlon TC350, 0.020″, ε_r = 3.5	D58909	MTL

TYPICAL CHARACTERISTICS — 915 MHz REFERENCE CIRCUIT

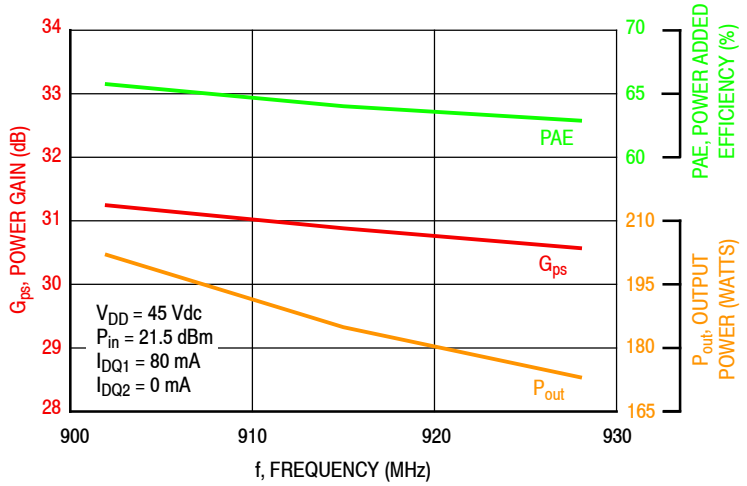


Figure 8. Power Gain, Power Added Efficiency and Output Power versus Frequency at a Constant Input Power

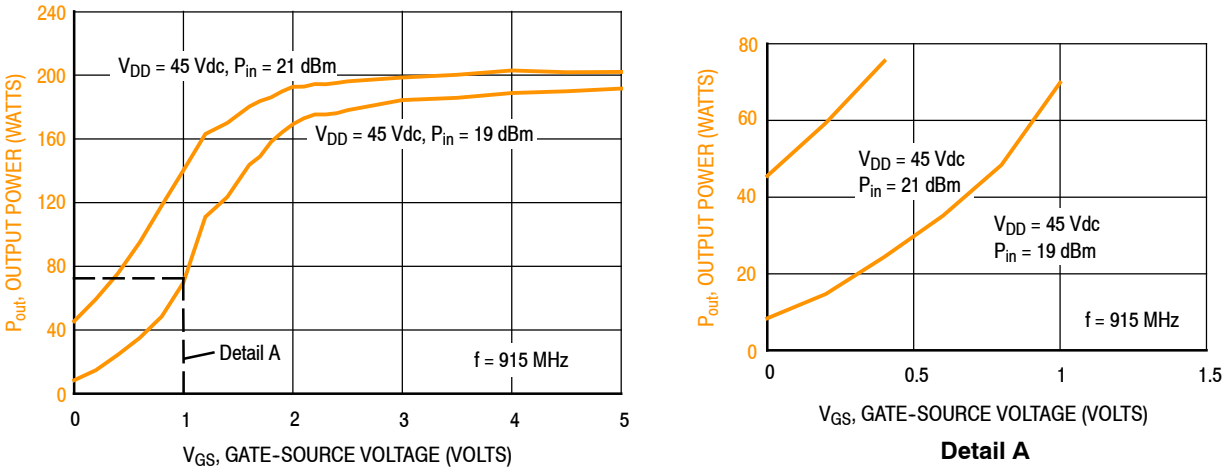


Figure 9. Output Power versus Gate-Source Voltage

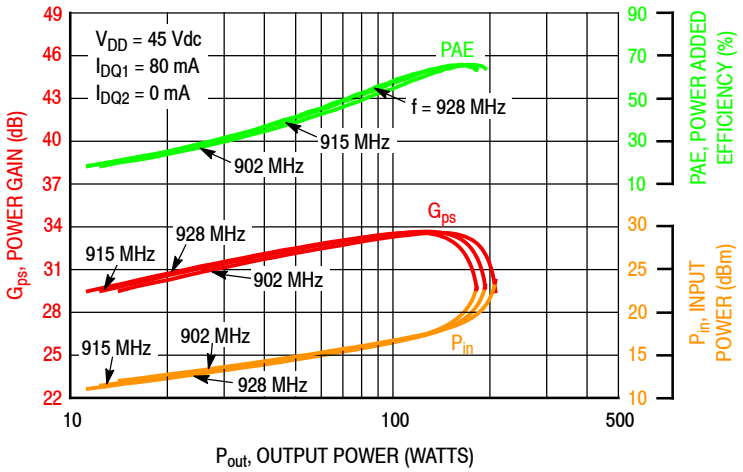


Figure 10. Power Gain, Power Added Efficiency and Input Power versus Output Power and Frequency

TYPICAL CHARACTERISTICS — 915 MHz REFERENCE CIRCUIT

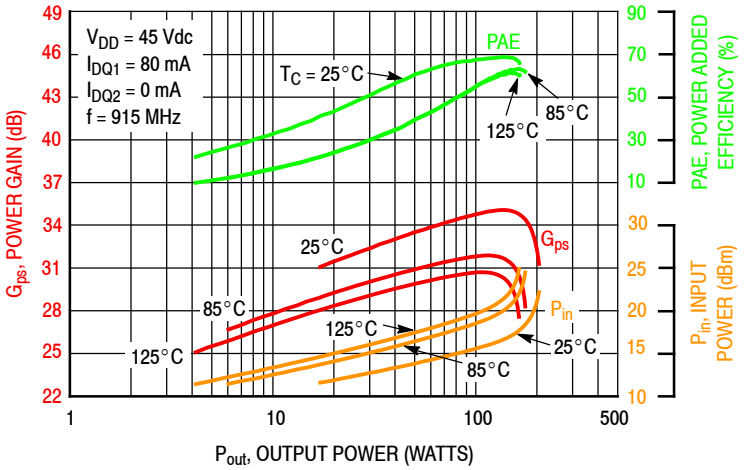
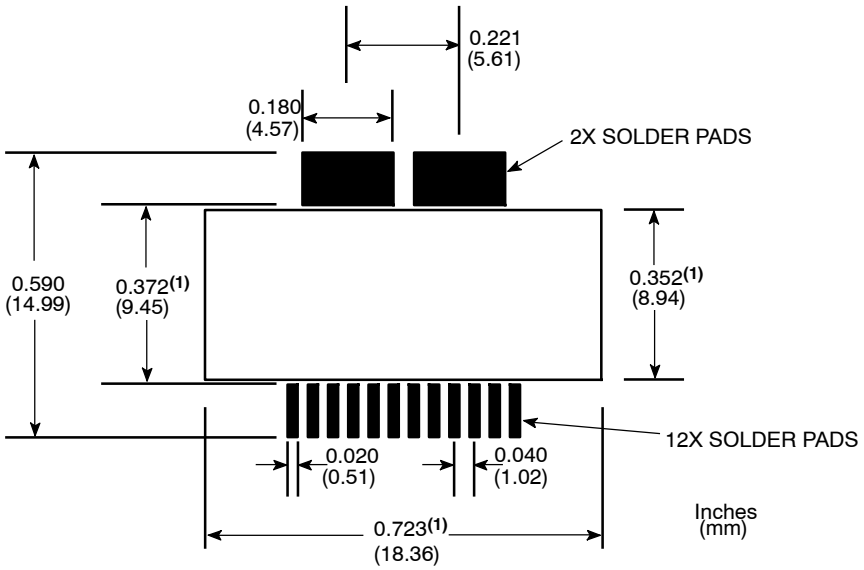


Figure 11. Power Gain, Power Added Efficiency and Input Power versus Output Power and Temperature

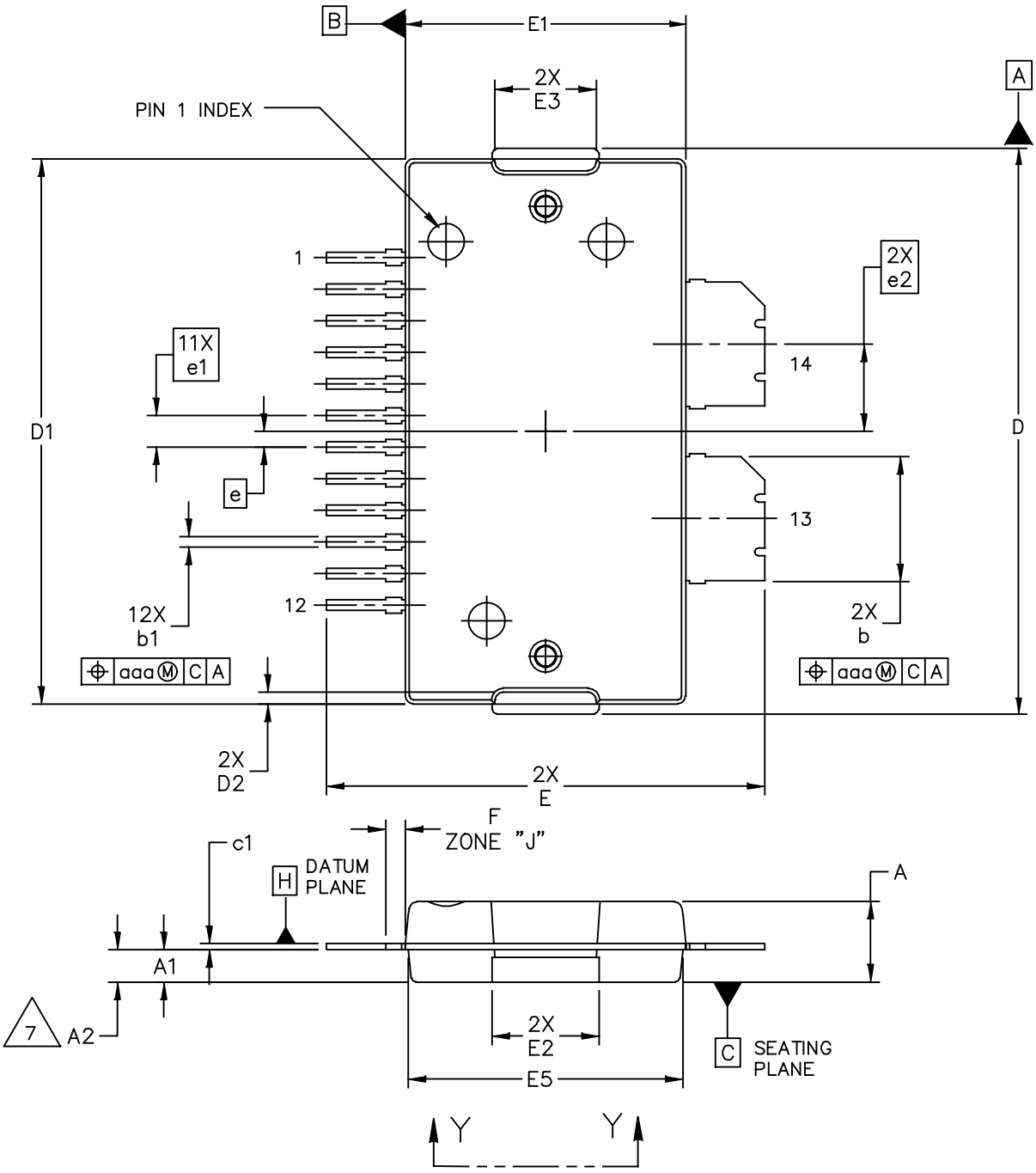


1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure 12. PCB Pad Layout for TO-270WB-14

Figure 13. Product Marking

PACKAGE DIMENSIONS



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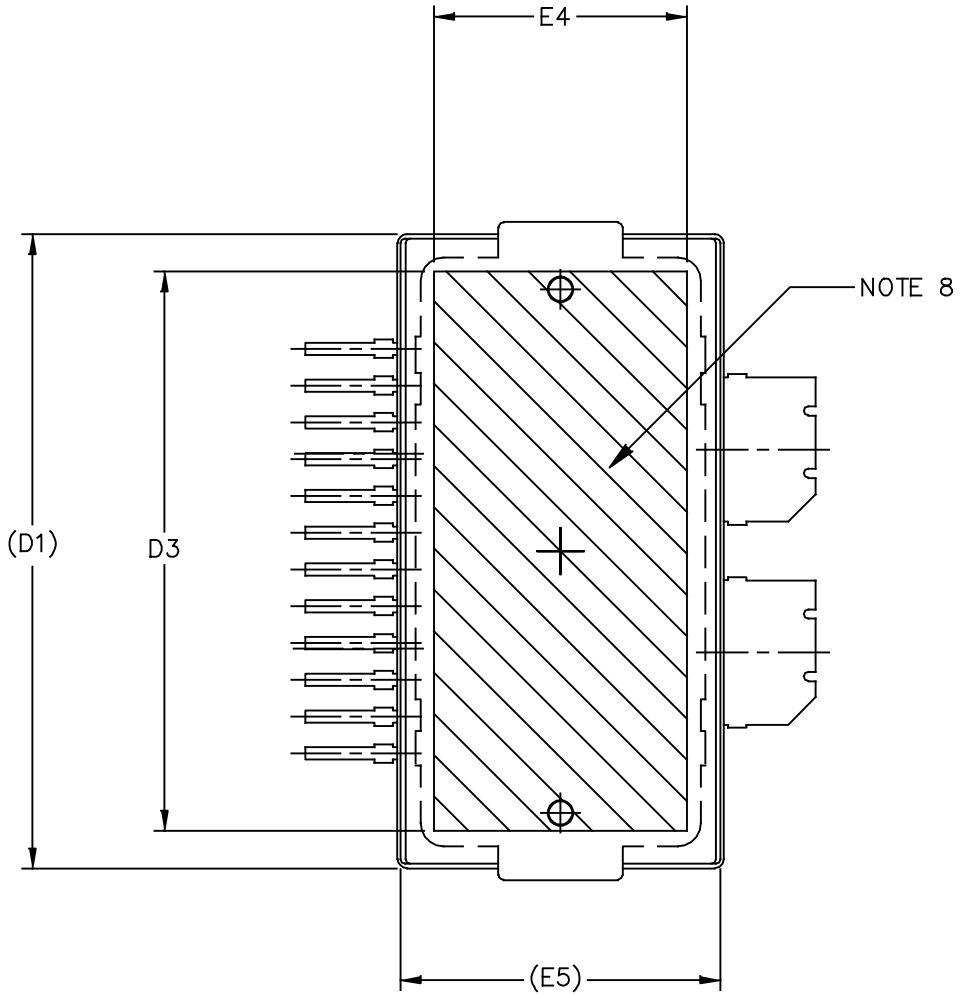
TITLE: TO-270 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10650D	REV: B
	STANDARD: NON-JEDEC	
	SOT1720-2	20 JAN 2016



VIEW Y–Y

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TITLE: TO–270 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10650D	REV: B
	STANDARD: NON–JEDEC	
	SOT1720–2	20 JAN 2016

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	---	15.24	---	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:
TO–270 WIDE BODY
14 LEAD

DOCUMENT NO: 98ASA10650D REV: B

STANDARD: NON–JEDEC

SOT1720–2 20 JAN 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	June 2016	• Initial Release of Data Sheet

How to Reach Us:

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freescale.com

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freescale.com/support

Document Number: MHT2001N
Rev. 0, 6/2016

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Click below to explore more details on WIN SOURCE:

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Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management