

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +150	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 81°C, 12.5 W, 2450 MHz Stage 1, 28 Vdc, $I_{DQ1} = 12$ mA Stage 2, 28 Vdc, $I_{DQ2} = 72$ mA	$R_{\theta JC}$	14 4.3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	1B, passes 500 V
Charge Device Model (per JS-002-2014)	C3, passes 1000 V

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 - Off Characteristics					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	500	nAdc
Gate-Source Leakage Current ($V_{GS} = 0.9$ Vdc, $V_{DS} = 0$ Vdc)	I_{GSS}	—	—	200	nAdc
Stage 1 - On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 3$ μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Fixture Gate Quiescent Voltage (4) ($V_{DS} = 28$ Vdc, $I_{DQ1} = 12$ mAdc)	$V_{GG(Q)}$	—	4.9	—	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.nxp.com/RF/calculators>.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.
4. Data measured in NXP test fixture with 4.7 k Ω resistor in series with V_{GS1} and V_{GS2} pins.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 2 - Off Characteristics					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	$\mu\text{A dc}$
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	500	nA dc
Gate-Source Leakage Current ($V_{GS} = 0.9\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	200	nA dc
Stage 2 - On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 14\ \mu\text{A dc}$)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Fixture Gate Quiescent Voltage (1) ($V_{DS} = 28\text{ Vdc}$, $I_{DQ2} = 72\text{ mA dc}$)	$V_{GG(Q)}$	—	4.8	—	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 140\text{ mA dc}$)	$V_{DS(on)}$	0.05	0.14	0.20	Vdc

Table 6. Typical Performance

In NXP Reference Circuit, 50 ohm system, $V_{DD} = 28\text{ Vdc}$, $I_{DQ1} = 15\text{ mA}$, $I_{DQ2} = 75\text{ mA}$, 2400–2500 MHz Bandwidth

Power Gain	G_{ps}	—	29.7	—	dB
Power Added Efficiency	PAE	—	50.5	—	%
P_{out} @ 1 dB Compression Point, CW	P1dB	—	11.7	—	W
P_{out} @ 3 dB Compression Point, CW	P3dB	—	14	—	W
Gain Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔG	—	0.036	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature (-30°C to $+85^\circ\text{C}$)	$\Delta P1dB$	—	0.004	—	dB/ $^\circ\text{C}$

Table 7. Load Mismatch/Ruggedness

In NXP Reference Circuit, 50 ohm system, $I_{DQ1} = 12\text{ mA}$, $I_{DQ2} = 72\text{ mA}$

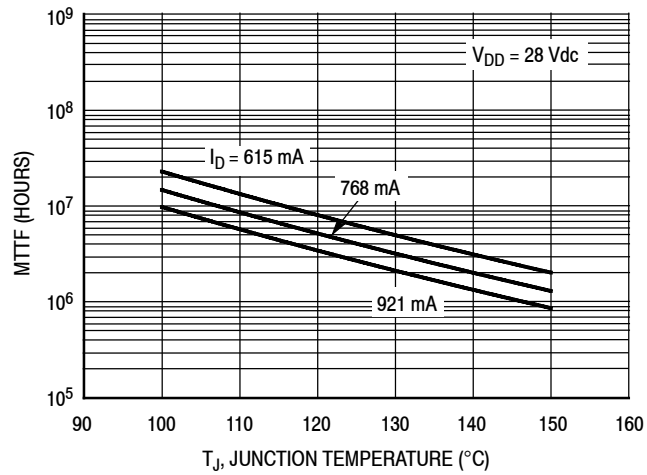
Frequency (MHz)	Signal Type	VSWR	P_{in} (dBm)	Test Voltage, V_{DD}	Result
2450	CW	10:1 at all Phase Angles	14 (3 dB Overdrive)	32	No Device Degradation

Table 8. Ordering Information

Device	Tape and Reel Information	Package
MHT2012NT1	T1 Suffix = 1000 Units, 16 mm Tape Width, 13-inch Reel	PQFN 8 × 8

1. Data measured in NXP test fixture with 4.7 k Ω resistor in series with V_{GS1} and V_{GS2} pins.

TYPICAL CHARACTERISTICS



Note: MTTF value represents the total cumulative operating time under indicated test conditions.

MTTF calculator available at <http://www.nxp.com/RF/calculators>.

Figure 3. MTTF versus Junction Temperature – CW

Table 9. Load Pull Performance — Maximum Power Tuning

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ1} = 12 \text{ mA}$, $I_{DQ2} = 73 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec(ON)}$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	40.9 + j23.6	48.3 – j23.1	7.22 – j4.32	30.0	42.2	17	49.8	49.7
2450	38.1 + j30.8	47.3 – j30.9	7.06 – j3.92	29.9	42.3	17	51.9	51.8
2500	32.9 + j30.7	40.4 – j32.8	6.76 – j3.83	30.0	42.4	18	52.6	52.5

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	40.9 + j23.6	42.8 – j26.8	7.50 – j4.46	27.9	42.8	19	49.4	49.3
2450	38.1 + j30.8	40.4 – j32.0	7.20 – j4.35	27.8	43.0	20	50.8	50.7
2500	32.9 + j30.7	33.9 – j32.4	7.05 – j4.26	27.9	43.0	20	51.2	51.1

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.

Table 10. Load Pull Performance — Maximum Efficiency Tuning

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ1} = 12 \text{ mA}$, $I_{DQ2} = 73 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec(ON)}$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	40.9 + j23.6	58.6 – j22.8	4.19 – j1.25	30.5	40.9	12	56.2	56.1
2450	38.1 + j30.8	56.8 – j34.4	4.01 – j1.06	30.2	41.0	13	56.8	56.7
2500	32.9 + j30.7	48.5 – j37.7	3.63 – j1.34	30.4	41.1	13	59.5	59.4

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	40.9 + j23.6	51.9 – j26.8	4.28 – j1.45	28.5	41.6	15	54.3	54.2
2450	38.1 + j30.8	48.5 – j35.0	4.19 – j1.50	28.2	41.9	15	55.2	55.1
2500	32.9 + j30.7	40.4 – j36.5	3.94 – j1.74	28.4	42.0	16	57.0	56.9

(1) Load impedance for optimum P1dB efficiency.

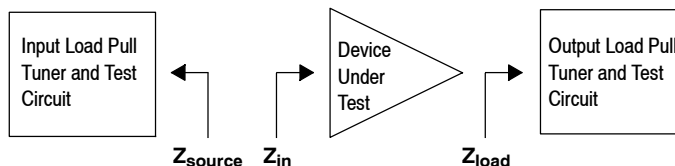
(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Note: Measurement made on a per side basis.



P3dB – TYPICAL LOAD PULL CONTOURS — 2450 MHz

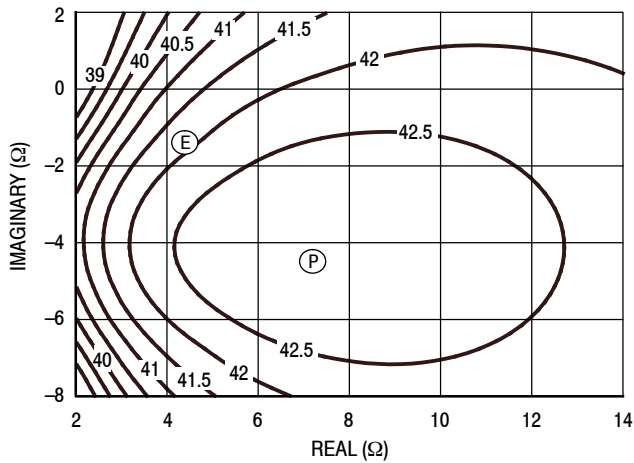


Figure 4. P3dB Load Pull Output Power Contours (dBm)

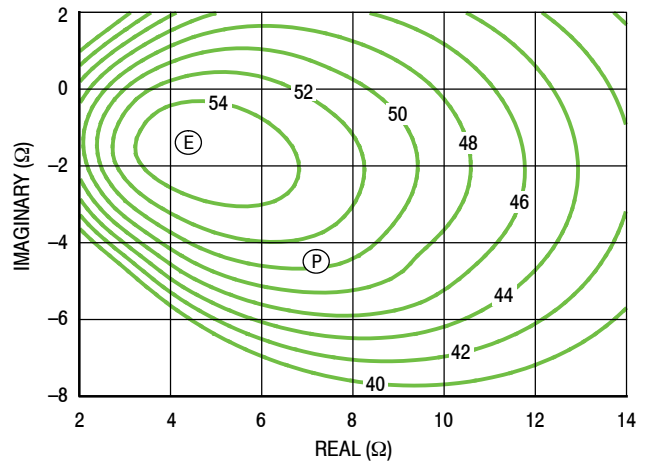


Figure 5. P3dB Load Pull Efficiency Contours (%)

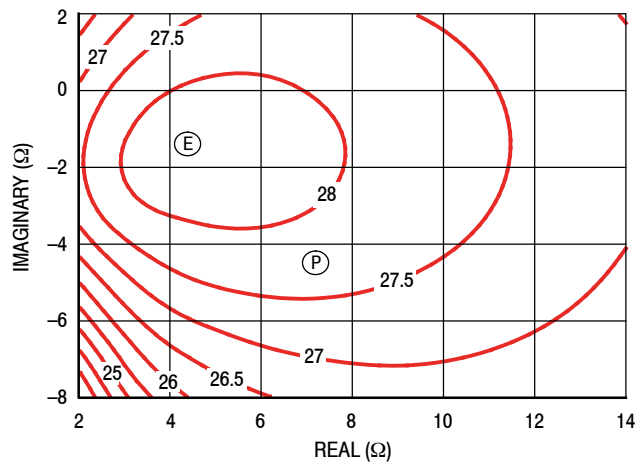


Figure 6. P3dB Load Pull Gain Contours (dB)

NOTE: (P) = Maximum Output Power
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

2400–2500 MHz REFERENCE CIRCUIT — 2" × 3" (5.1 cm × 7.6 cm)

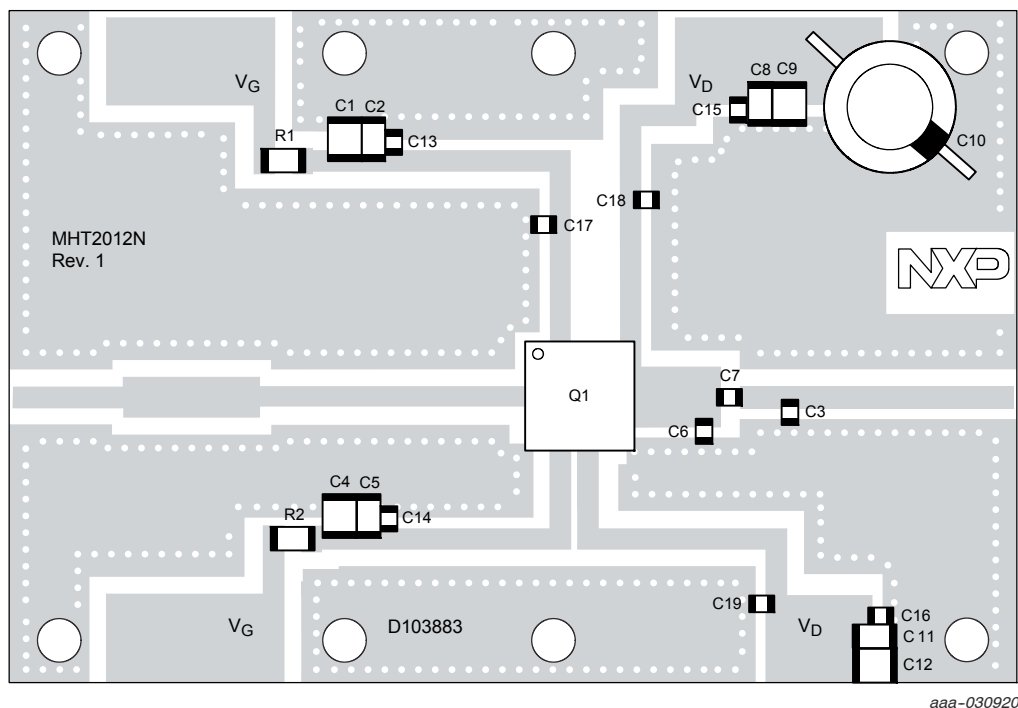


Figure 7. MHT2012N Reference Circuit Component Layout — 2400–2500 MHz

Table 11. MHT2012N Reference Circuit Component Designations and Values — 2400–2500 MHz

Part	Description	Part Number	Manufacturer
C1, C4, C9, C12	10 μ F Chip Capacitor	GRM32ER61H106KA12L	Murata
C2, C5, C8, C11	0.1 μ F Chip Capacitor	GRM32NR72A104KA01B	Murata
C3	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C6	1.6 pF Chip Capacitor	ATC600F1R6BT250XT	ATC
C7	4.7 pF Chip Capacitor	ATC600F4R7BT250XT	ATC
C10	220 μ F, 50 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
C13, C14, C15, C16, C17, C18, C19	5.6 pF Chip Capacitor	ATC600F5R6BT250XT	ATC
Q1	RF Power LDMOS Transistor	MHT2012N	NXP
R1, R2	4.7 k Ω , 1/4 W Chip Resistor	CRCW12064K70FKEA	Vishay
PCB	Rogers RT6035HTC, 0.030", $\epsilon_r = 3.5$	D103883	MTL

TYPICAL CHARACTERISTICS — 2400–2500 MHz REFERENCE CIRCUIT

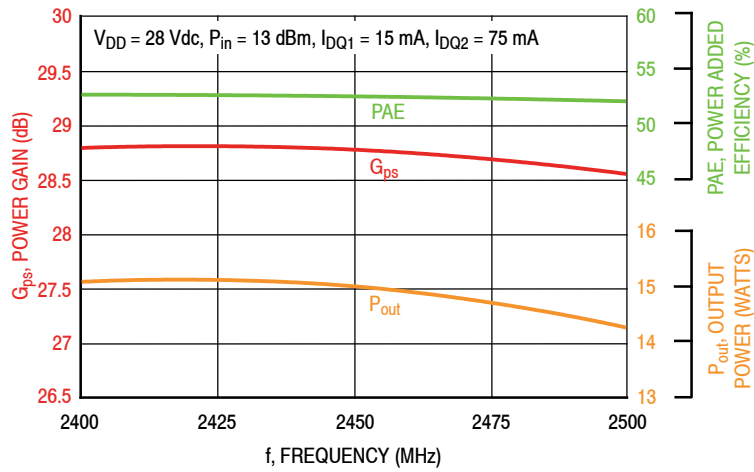


Figure 8. Power Gain, Power Added Efficiency and CW Output Power versus Frequency at a Constant Input Power

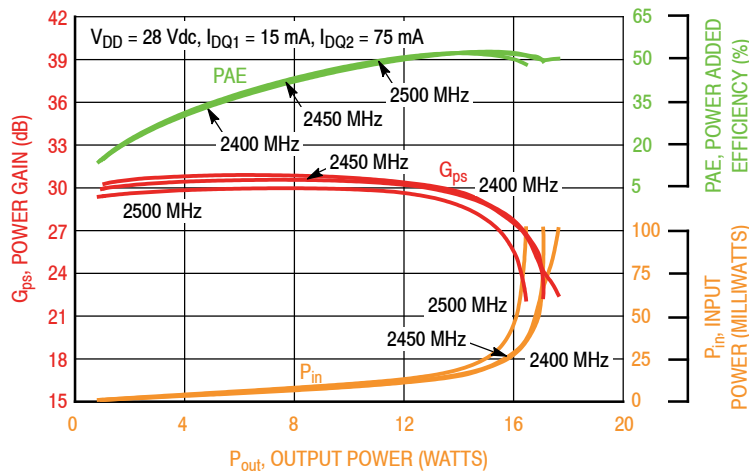


Figure 9. Power Gain, Power Added Efficiency and Input Power versus CW Output Power and Frequency

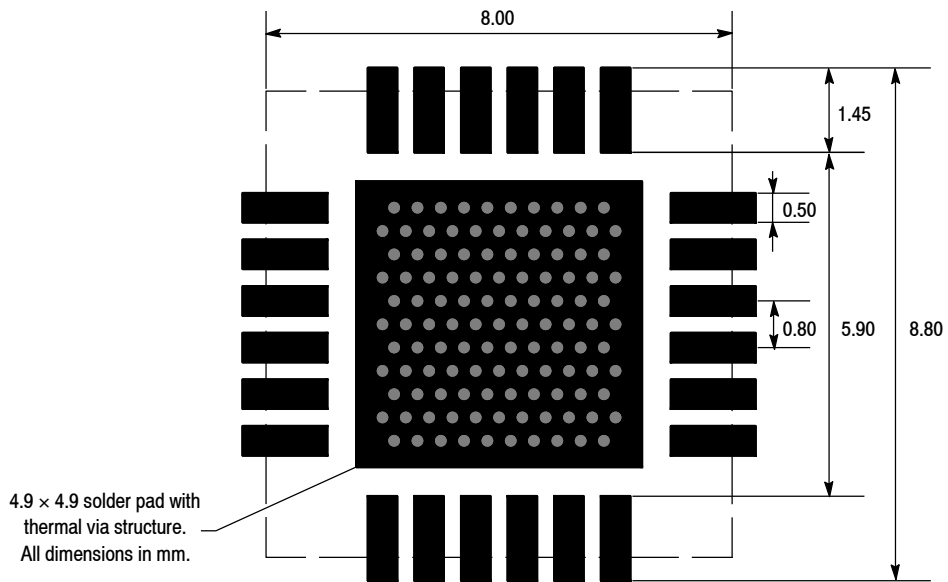
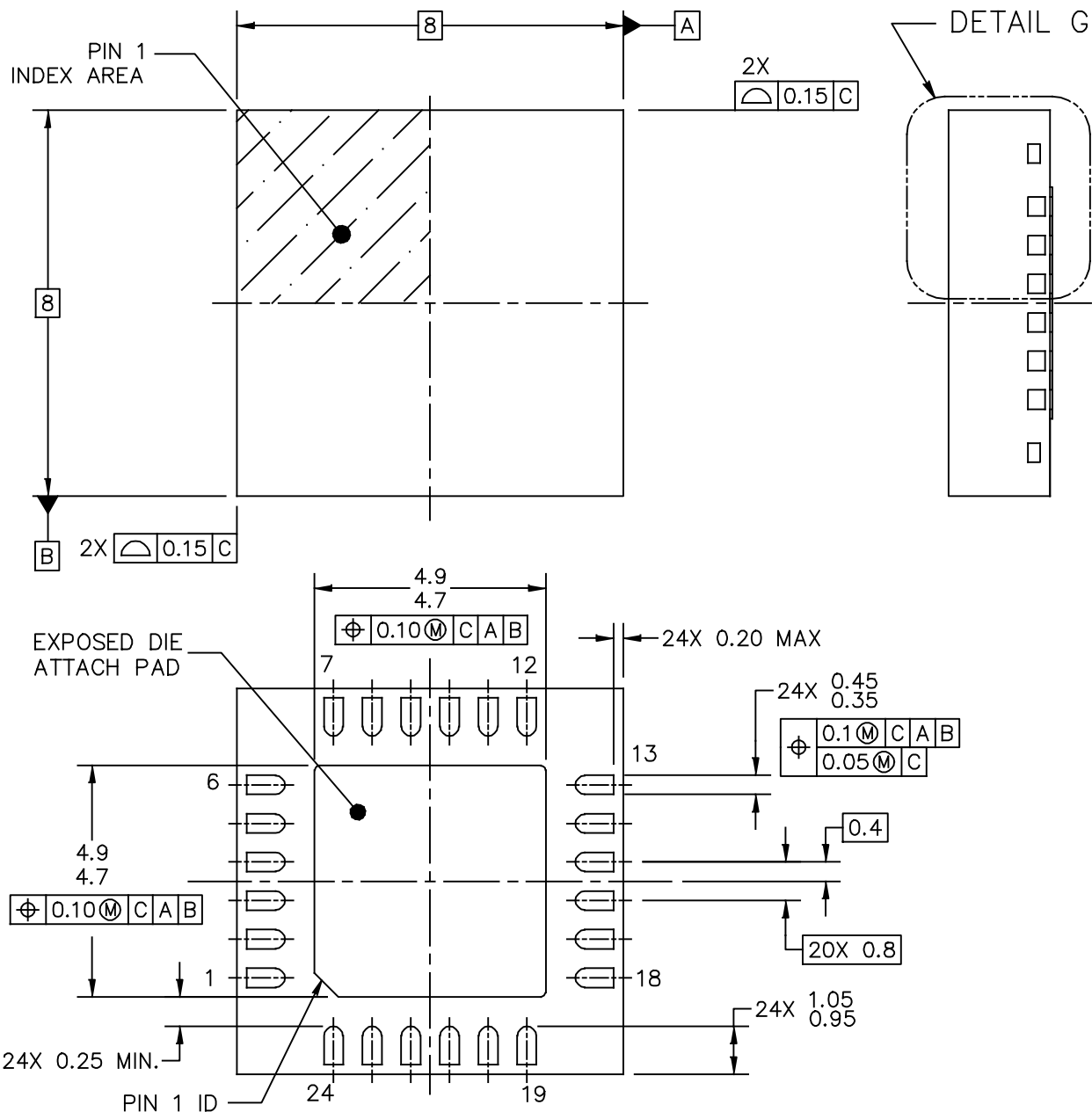


Figure 10. PCB Pad Layout for 24-Lead PQFN 8 × 8

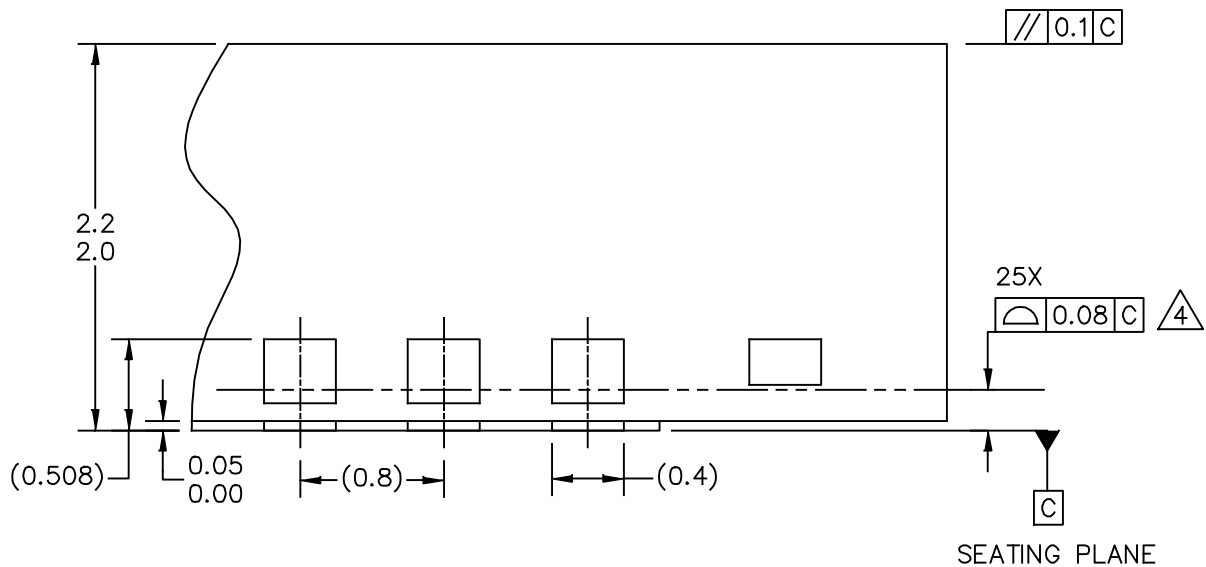


Figure 11. Product Marking

PACKAGE DIMENSIONS



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	STANDARD: NON-JEDEC	
	SOT1664-1	11 MAR 2016



DETAIL G
VIEW ROTATED 90° CW

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NOTES:

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2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
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		STANDARD: NON-JEDEC	
		SOT1664-1	11 MAR 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to <http://www.nxp.com/RF>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2018	<ul style="list-style-type: none">• Initial release of data sheet

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