

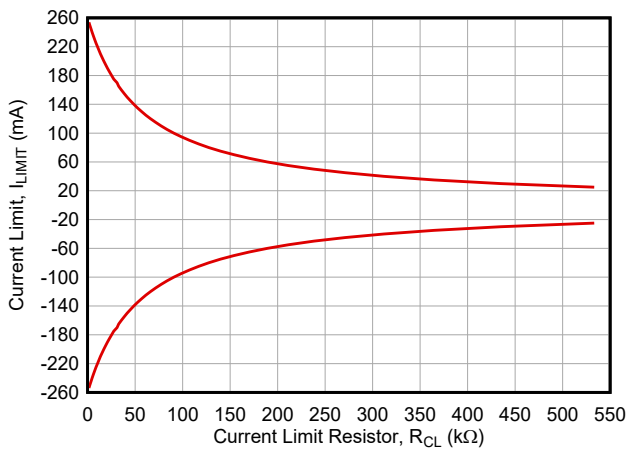
OPA593 85-V, 250-mA Output Current, Precision, Power Op Amp

1 Features

- Wide power-supply range:
 - 8 V (± 4 V) to 85 V (± 42.5 V)
- Low offset voltage: ± 20 μ V
- Low offset voltage drift: ± 0.4 μ V/ $^{\circ}$ C
- High output current: 250 mA
- Wide gain bandwidth: 10 MHz
- High slew rate: 45 V/ μ s, rising
- Low noise: 7 nV/ $\sqrt{\text{Hz}}$ at 10 kHz
- Mux-friendly inputs
- Rail-to-rail output
- Quiescent current:
 - Enabled: 3.25 mA
 - Disabled: 250 μ A
- Specified current limit accuracy
- Overtemperature and overcurrent flags
- Temperature range: -40° C to $+125^{\circ}$ C
- Package: 12-pin WSON

2 Applications

- [Semiconductor test](#)
- [Semiconductor manufacturing](#)
- [Programmable DC power supply](#)
- [LCD test](#)
- [CT and PET scanner](#)



Output Current vs Current-Limit Resistor Configuration

3 Description

The OPA593 is a high-voltage (85 V), high-precision, wide-bandwidth (10 MHz), high-output-current (250 mA), unity-gain-stable, power op amp.

The OPA593 uses a laser trimming technique to improve the offset voltage (20 μ V, typical) and offset voltage drift (0.4 μ V/ $^{\circ}$ C, typical), and thus avoids the need for calibration. This device features *mux-friendly* inputs that enable differential input voltage range to the supply rails and help improve settling performance in multichannel systems.

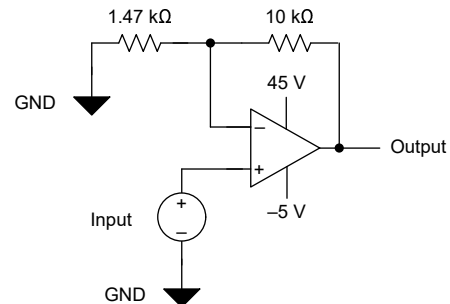
An external resistor can be used to limit the current with specified accuracy, and thus provide more precise measurements. In case of an overcurrent or overtemperature condition, the device indicates erroneous operation through a status flag. An included disable feature is used to shutdown the device, saving power and placing the output into a high-impedance state.

The device is unity-gain stable, enabling operation as a high-impedance buffer. The wide bandwidth and high slew enable high signal gains. The high output current and capacitive drive allow the device to drive external field-effect transistors (FETs) used to provide higher system currents, such as in a digital power supply.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
OPA593	DNT (WSON, 12)	4.00 mm \times 4.00 mm

- (1) For all available packages, see the package option addendum at the end of the data sheet.



Output Driver Configured With a Gain of 8



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2022) to Revision C (November 2022)	Page
• Changed from advanced information (preview) to production data (active).....	1

5 Pin Configuration and Functions

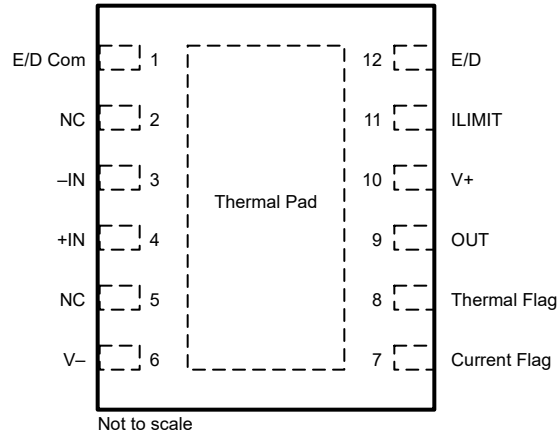


Figure 5-1. DNT (12-Pin WSON) Package, Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Current Flag	7	Output	Overcurrent status flag
E/D	12	Input	Enable and disable
E/D Com	1	Input	Enable and disable common
ILIMIT	11	Input	Current limit
+IN	4	Input	Noninverting input
-IN	3	Input	Inverting input
NC	2, 5	—	No internal connection
OUT	9	Output	Output
Thermal Flag	8	Output	Overtemperature status flag
Thermal Pad	Thermal pad	—	The thermal pad is internally connected to V-. The thermal pad must be soldered to a printed-circuit board (PCB) connected to V-, even with applications that have low power dissipation.
V+	10	Power	Positive (highest) power supply
V-	6	Power	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _S	Supply voltage, V _S = (V+) – (V–)		93	V
	Signal input pin voltage ⁽²⁾	(V–) – 0.3	(V+) + 0.3	V
	Status flag and E/D pin voltage ⁽³⁾		E/D Com + 7	V
	ILIMIT pin voltage	V–	(V–) + 3.35	V
	Status flag pins current ⁽³⁾		3	mA
	Input current, all pins ⁽²⁾		±10	mA
	Output short circuit current ⁽⁴⁾		Continuous	
T _J	Junction temperature	–55	150	°C
T _{STG}	Storage temperature	–65	150	°C

- Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- Input, E/D Com, and output pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to less than 10 mA.
- Status flag and E/D pins are diode clamped to E/D Com – 0.3 V and E/D Com + 7 V. Pullup signals must be current-limited to < 3 mA.
- Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _S	Supply voltage, V _S = (V+) – (V–)	Single supply voltage	8		85	V
		Dual supply voltage	±4		±42.5	
V _{E/D}	E/D pin voltage ⁽¹⁾				5.5	V
	Status flag pin voltage ⁽¹⁾				5.5	V
I _{LIMIT}	Current limit set		±25		±250	mA
T _A	Operating temperature		–40		125	°C

- Recommended voltage must be current limited to below the listed value in the *Absolute Maximum Ratings*.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA593	UNIT
		DNT (WSN)	
		12 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	40.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	30.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	17.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	17.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	4.3	°C/W

- For information on traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $V_S = 85\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to mid-supply, I_{OUT} limit set to 100 mA, and $V_{CM} = V_{OUT} = \text{mid-supply}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				± 20	± 100	μV
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 0.4	± 2	$\mu\text{V}/^\circ\text{C}$
PSRR	Power supply rejection ratio	$V_S = \pm 4\text{ V}$ to $\pm 42.5\text{ V}$			0.1	1	$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT							
I_B	Input bias current				± 1	± 10	pA
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				± 350	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$					± 5
I_{OS}	Input offset current				± 1	± 5	pA
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				± 250	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$					± 1
NOISE							
	Input voltage noise	$f = 0.1\text{ Hz}$ to 10 Hz			2.9		μV_{PP}
e_n	Input voltage noise density	$f = 10\text{ Hz}$			75		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$			10		
		$f = 10\text{ kHz}$			7		
i_n	Current noise density	$f = 1\text{ kHz}$			12		fA/ $\sqrt{\text{Hz}}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	Linear operation		$(V-) - 0.1$		$(V+) - 3.5$	V
CMRR	Common-mode rejection	$(V-) \leq V_{CM} \leq (V+) - 3.5\text{ V}$		124	140		dB
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	108	124		
INPUT IMPEDANCE							
	Differential				$10^{13} \parallel 0.3$		$\Omega \parallel \text{pF}$
	Common-mode				$10^{13} \parallel 9.4$		$\Omega \parallel \text{pF}$
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	$(V-) + 0.3\text{ V} < V_O < (V+) - 0.3\text{ V}$, $R_L = 10\text{ k}\Omega$		134	140		dB
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	130	140		
		$(V-) + 1\text{ V} < V_O < (V+) - 1\text{ V}$, $R_L = 2\text{ k}\Omega$		132	140		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	130	135		
		$(V-) + 2.5\text{ V} < V_O < (V+) - 2.5\text{ V}$, $R_L = 600\ \Omega$		130	135		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	125	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				10		MHz
SR	Slew rate	Gain = ± 1 , $V_{OUT} = 70\text{-V}$ step	Rising		45		V/ μs
			Falling		35		
t_s	Settling time	To $\pm 0.01\%$, gain = -1 , $V_{OUT} = 70\text{-V}$ step, $C_L = 100\text{ pF}$			2.9		μs
THD+N	Total harmonic distortion + noise	Gain = $+1$, $V_{OUT} = 70\text{ V}_{PP}$, $f = 1\text{ kHz}$	$R_L = 600\ \Omega$		-105		dB
			$R_L = 2\text{ k}\Omega$		-110		
OUTPUT							
V_O	Voltage output swing from rail	$R_{CL} = 0\ \Omega$ connected to $V-$	No load		10	25	mV
			$I_{OUT} = 50\text{ mA}$		50	125	
			$I_{OUT} = 100\text{ mA}$		400	750	
			$I_{OUT} = 250\text{ mA}$		1.2	2	

6.5 Electrical Characteristics (continued)

at $V_S = 85\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to mid-supply, I_{OUT} limit set to 100 mA, and $V_{CM} = V_{OUT} = \text{mid-supply}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Continuous output current, dc	$V_S = 85\text{ V}$, $R_{CL} = 2.29\text{ k}\Omega$, $I_{LIMIT} = 250\text{ mA}$			± 250		mA
C_{LOAD}	Capacitive load drive			See typical curves			pF
Z_O	Open-loop output impedance			See typical curves			Ω
	Output impedance	Output disabled, $V_- < V_{OUT} < V_+$			100		M Ω
	Output capacitance	Output disabled			56		pF
CURRENT LIMIT							
I_{LIMIT}	Current limit			± 25		± 250	mA
	Current limit accuracy ⁽³⁾	Sourcing, $R_L = 10\text{ }\Omega$ to mid-supply	$I_{LIMIT} = 25\text{ mA}$, $V_{LIMIT} = 3.33\text{ V}$	17		29	mA
			$I_{LIMIT} = 50\text{ mA}$, $V_{LIMIT} = 2.98\text{ V}$	42		55	
			$I_{LIMIT} = 100\text{ mA}$, $V_{LIMIT} = 2.27\text{ V}$	94		107	
			$I_{LIMIT} = 250\text{ mA}$, $V_{LIMIT} = 0.14\text{ V}$	237		263	
		Sinking, $R_L = 10\text{ }\Omega$ to mid-supply	$I_{LIMIT} = 25\text{ mA}$, $V_{LIMIT} = 3.33\text{ V}$	10		45	
			$I_{LIMIT} = 50\text{ mA}$, $V_{LIMIT} = 2.98\text{ V}$	35		68	
			$I_{LIMIT} = 100\text{ mA}$, $V_{LIMIT} = 2.27\text{ V}$	85		115	
			$I_{LIMIT} = 250\text{ mA}$, $V_{LIMIT} = 0.14\text{ V}$	235		275	
	Current limit equation	Resistor set, R_{CL} connected between I_{LIMIT} pin and V_-		$(3.687\text{ V} \times 4000) / (56.7\text{ k}\Omega + R_{CL})$			mA
		Voltage set, V_{LIMIT} connected to I_{LIMIT} pin and referenced to V_-		$4000 \times (3.687\text{ V} - V_{LIMIT}) / 56.7\text{ k}\Omega$			
STATUS FLAG PIN (Referenced to E/D Com)							
	Status flag delay	Overcurrent delay			10		μs
		Overcurrent recovery delay			10		
	Thermal shutdown	Alarm (status flag high)			170		$^\circ\text{C}$
		Return to normal operation (status flag low)			150		
	Status flag output voltage	Normal operation		See typical curves			
E/D PIN							
$V_{E/D}$	E/D voltage ⁽¹⁾	Enable, pin open or forced high ⁽²⁾		E/D Com + 1.5		E/D Com + 5.5	V
		Disable, pin forced low ⁽²⁾		E/D Com		E/D Com + 0.5	
$I_{E/D}$	E/D input current				50		μA
	Output disable time				12		μs
	Output enable time				18		μs
E/D COM PIN							
	E/D Com voltage			(V_-)		(V_+) – 6	V
POWER SUPPLY							
I_Q	Quiescent current				3.25	3.75	mA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$				4	
		Output disabled			0.25		

(1) For information on the output enable and disable feature see [Section 7.3.4](#).

(2) Enable and disable voltage thresholds can vary near the maximum temperature range; see [Figure 6-67](#).

(3) Proper output swing headroom is necessary to maintain current limit accuracy; see [Figure 6-19](#) to [Figure 6-34](#).

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{\text{LIMIT}} = 100\text{ mA}$, $V_{\text{CM}} = V_{\text{OUT}} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

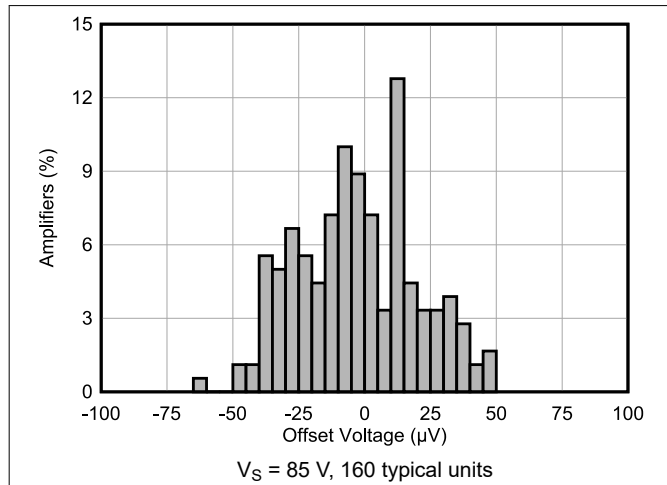


Figure 6-1. Input Offset Production Distribution

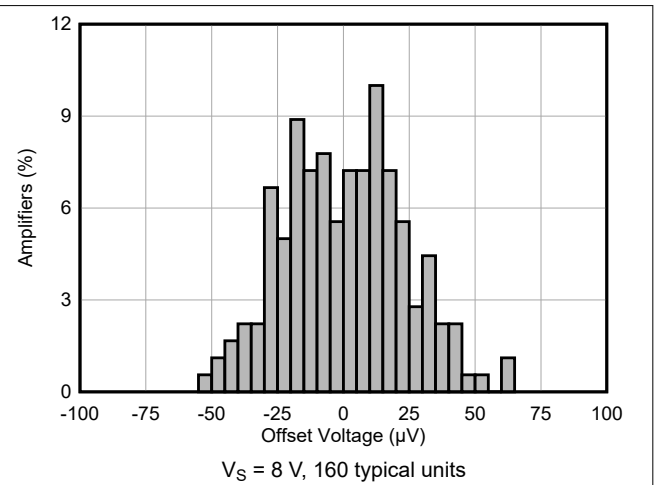


Figure 6-2. Input Offset Production Distribution

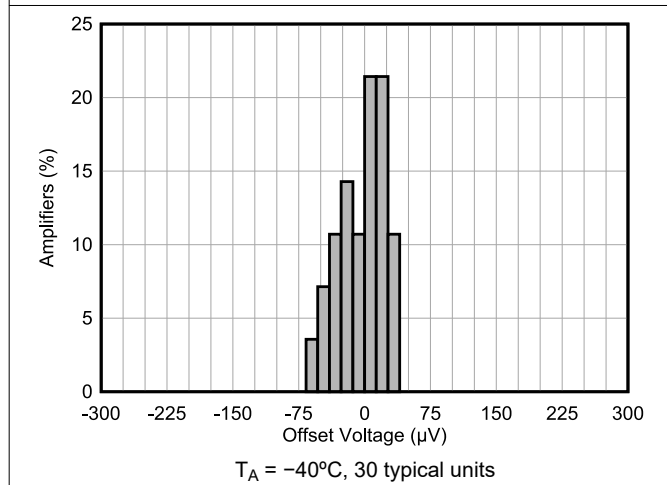


Figure 6-3. Input Offset Production Distribution

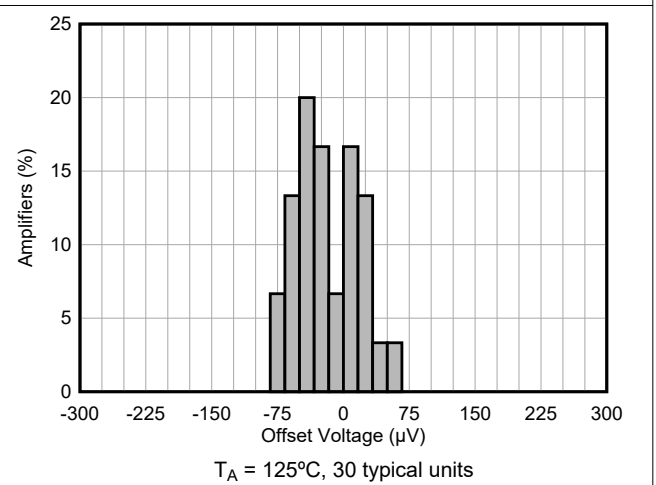


Figure 6-4. Input Offset Production Distribution

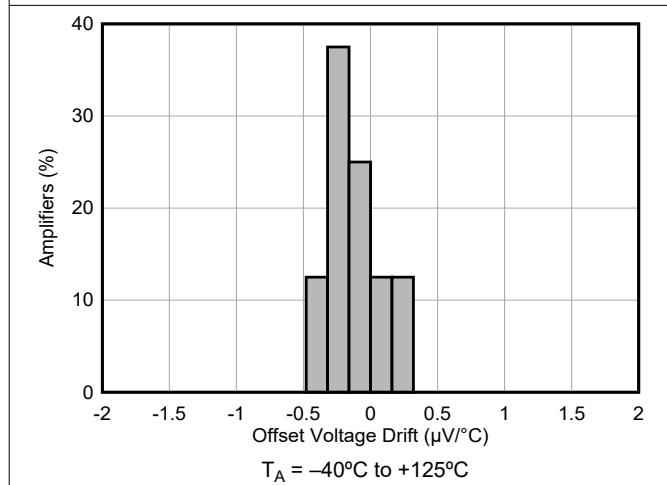


Figure 6-5. Input Offset Voltage Drift Distribution

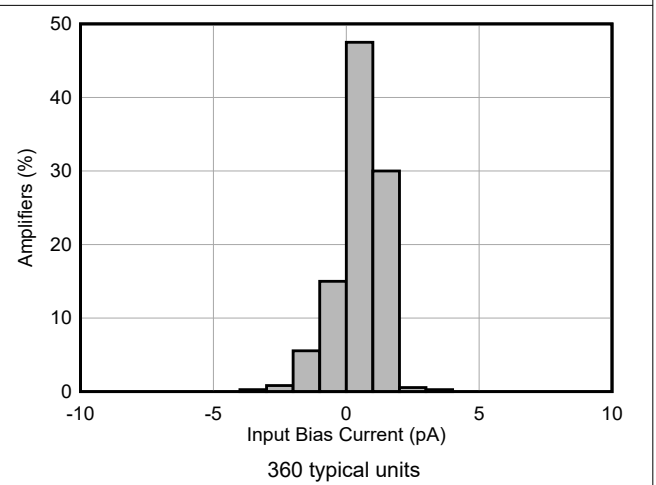


Figure 6-6. Input Bias Current Production Distribution

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{\text{LIMIT}} = 100\text{ mA}$, $V_{\text{CM}} = V_{\text{OUT}} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

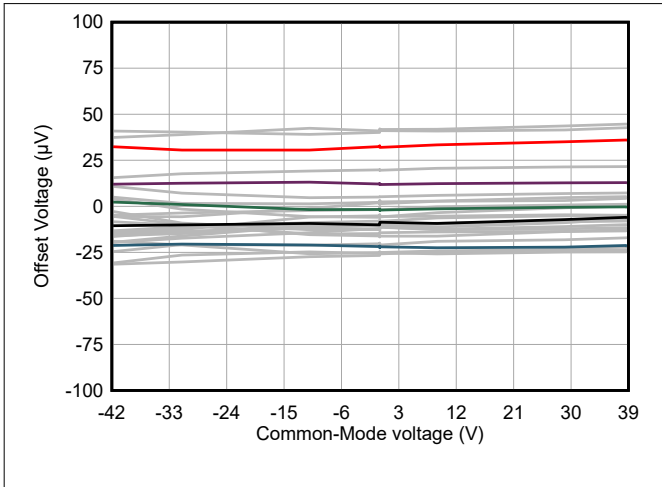


Figure 6-7. Input Offset Voltage vs Common-Mode Voltage

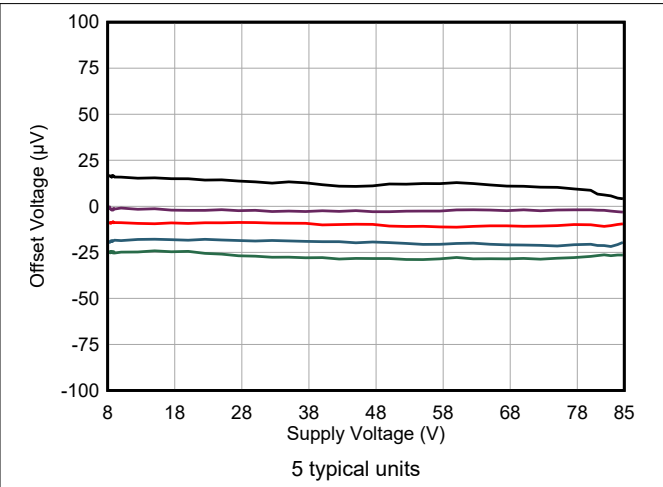


Figure 6-8. Input Offset Voltage vs Supply Voltage

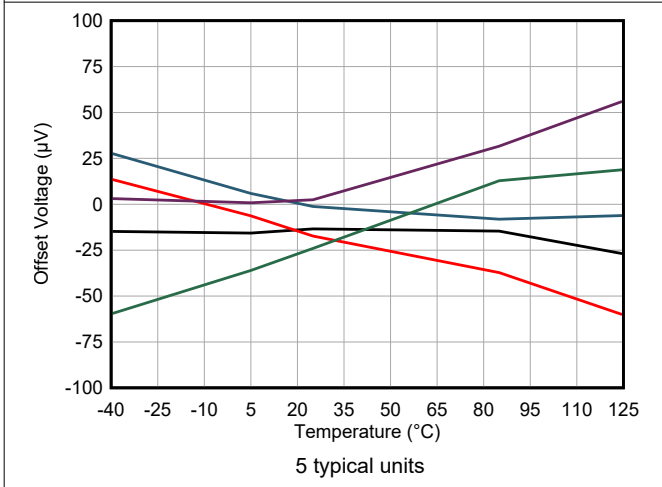


Figure 6-9. Input Offset Voltage vs Temperature

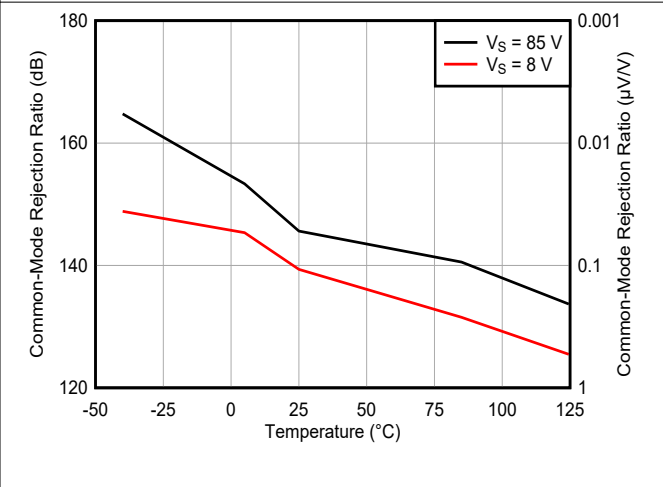


Figure 6-10. CMRR vs Temperature

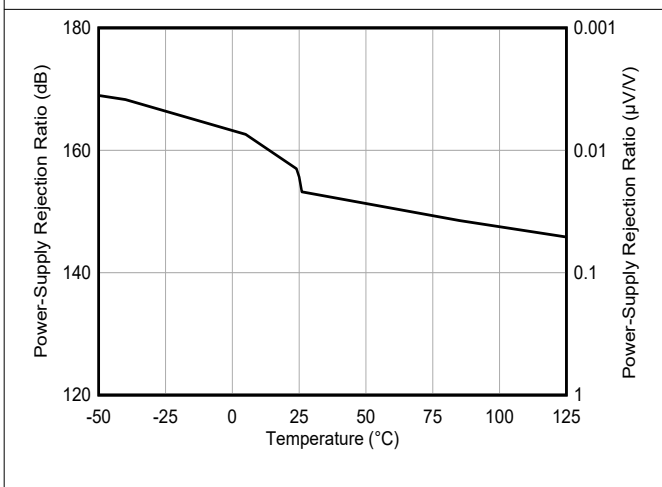


Figure 6-11. PSRR vs Temperature

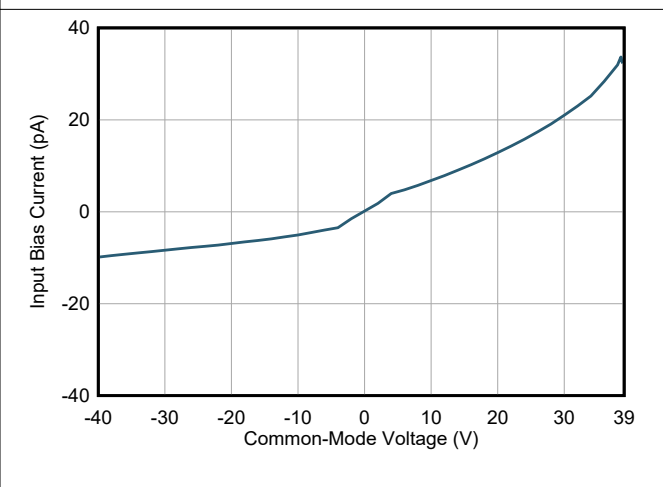


Figure 6-12. Input Bias Current vs Common-Mode Voltage

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{\text{LIMIT}} = 100\text{ mA}$, $V_{\text{CM}} = V_{\text{OUT}} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

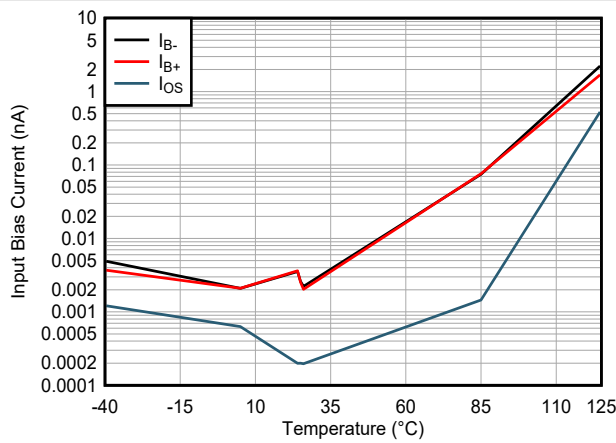


Figure 6-13. Input Bias Current and Current Offset vs Temperature

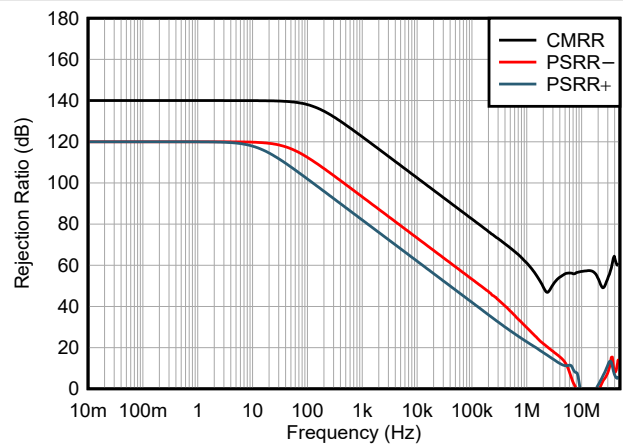


Figure 6-14. PSRR and CMRR vs Frequency

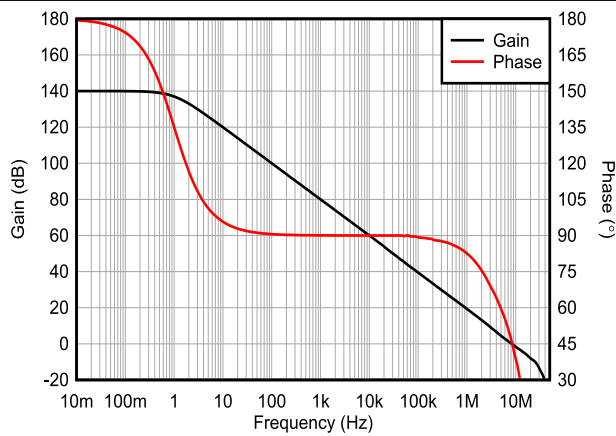


Figure 6-15. Open-Loop Gain and Phase vs Frequency

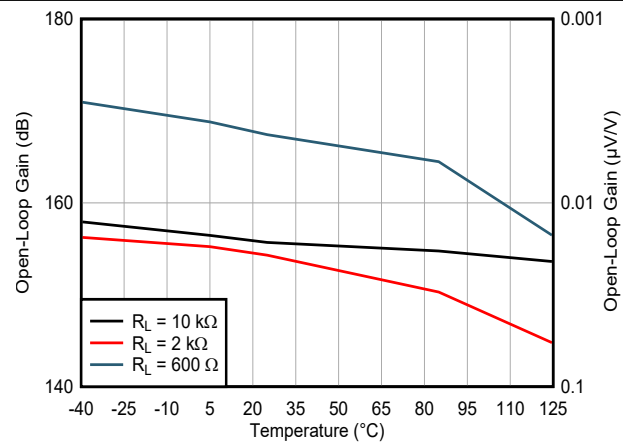


Figure 6-16. Open Loop Gain vs Temperature

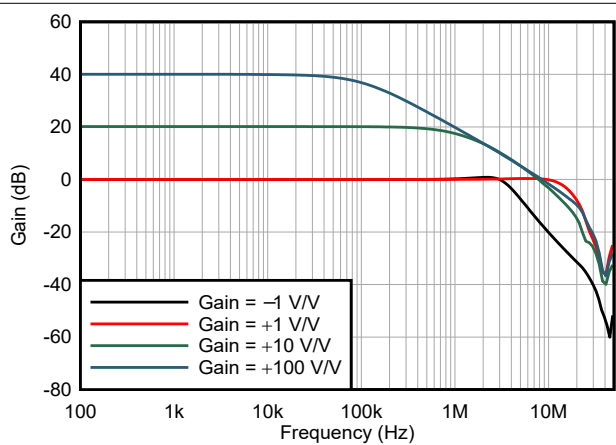


Figure 6-17. Closed-Loop Gain vs Frequency

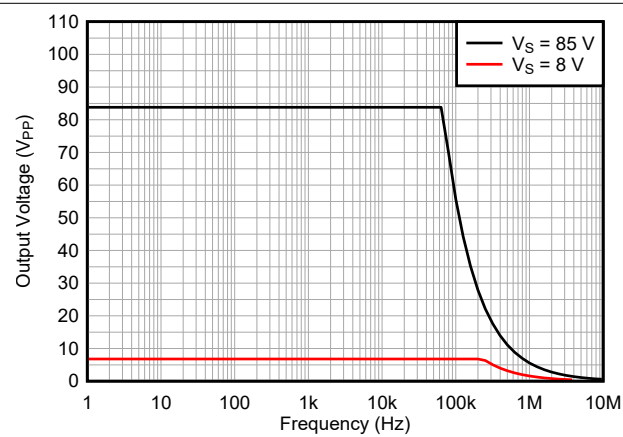


Figure 6-18. Maximum Output Voltage vs Frequency

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{\text{LIMIT}} = 100\text{ mA}$, $V_{\text{CM}} = V_{\text{OUT}} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

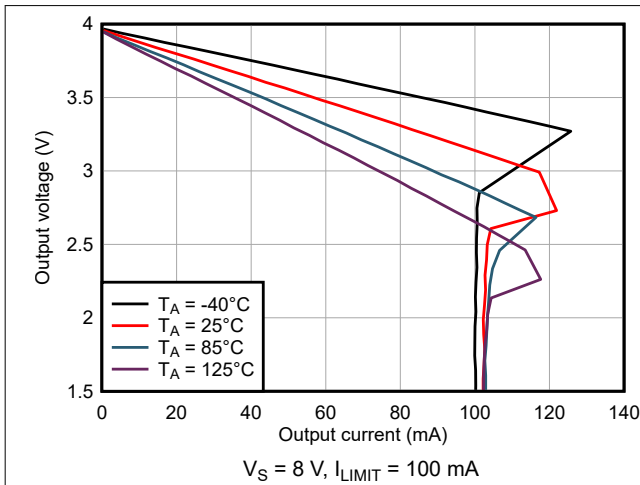


Figure 6-19. Output Voltage vs Output Sourcing Current

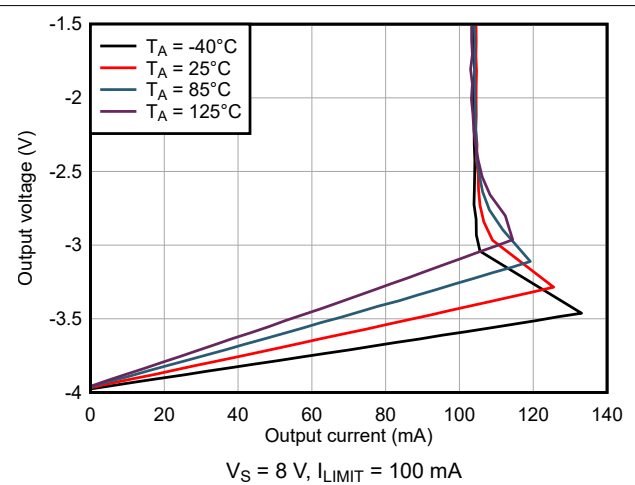


Figure 6-20. Output Voltage vs Output Sinking Current

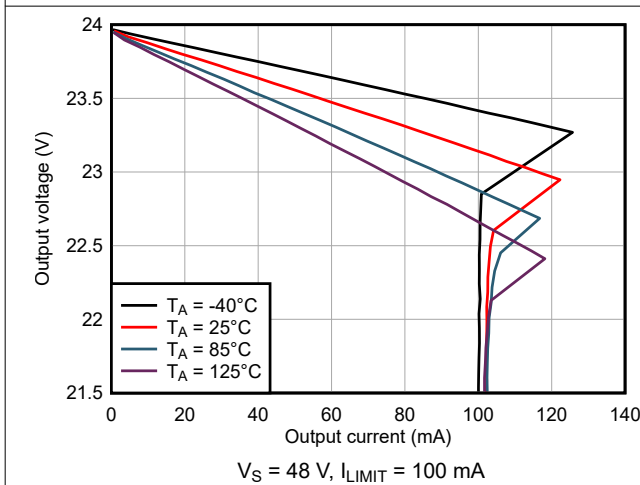


Figure 6-21. Output Voltage vs Output Sourcing Current

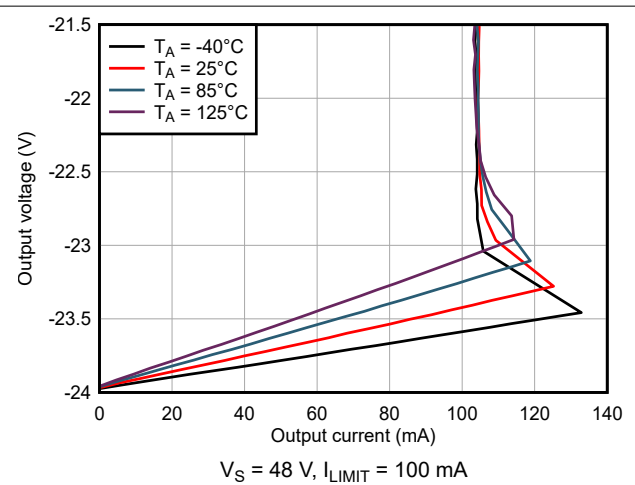


Figure 6-22. Output Voltage vs Output Sinking Current

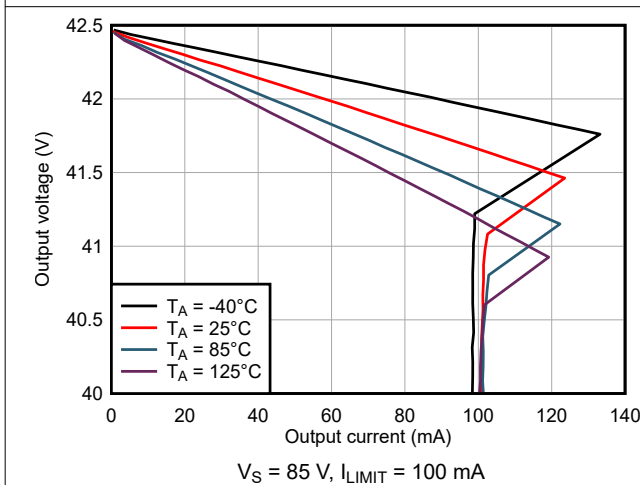


Figure 6-23. Output Voltage vs Output Sourcing Current

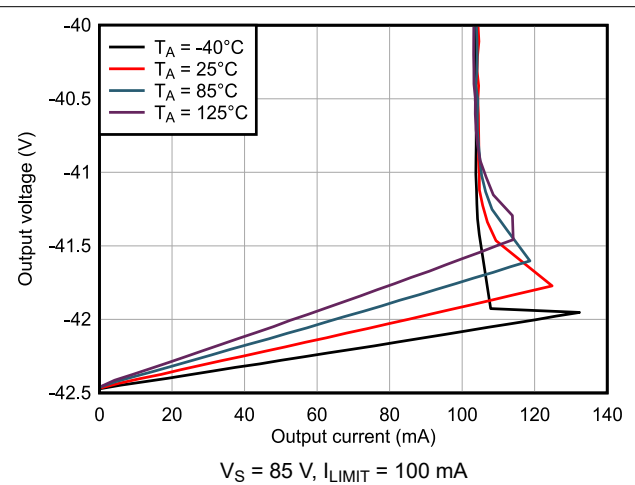


Figure 6-24. Output Voltage vs Output Sinking Current

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{LIMIT} = 100\text{ mA}$, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

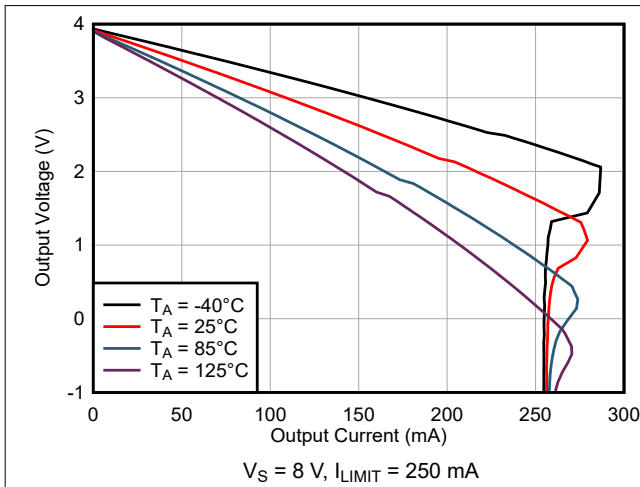


Figure 6-25. Output Voltage vs Output Sourcing Current

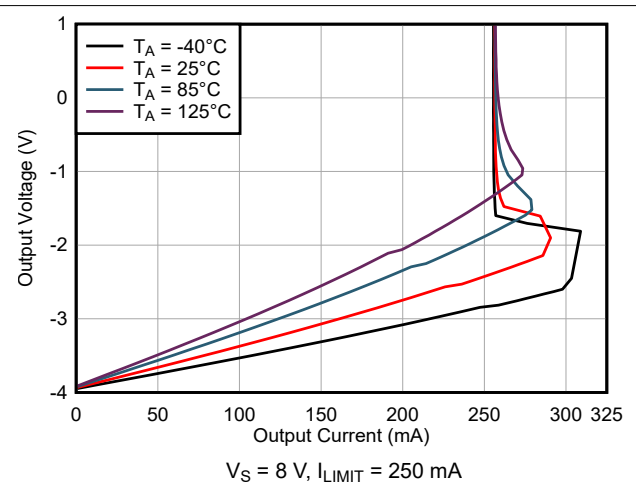


Figure 6-26. Output Voltage vs Output Sinking Current

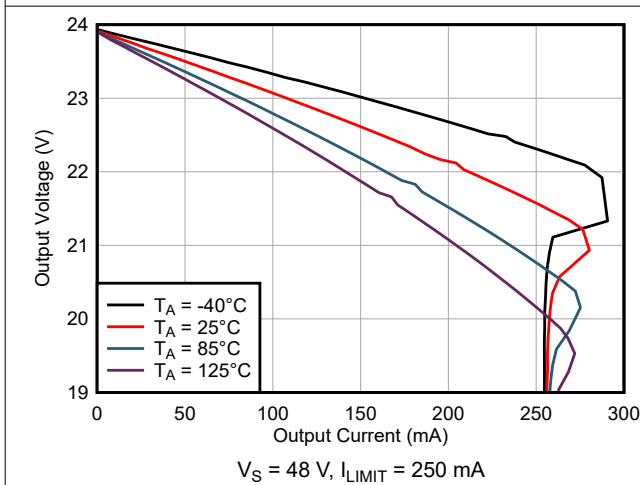


Figure 6-27. Output Voltage vs Output Sourcing Current

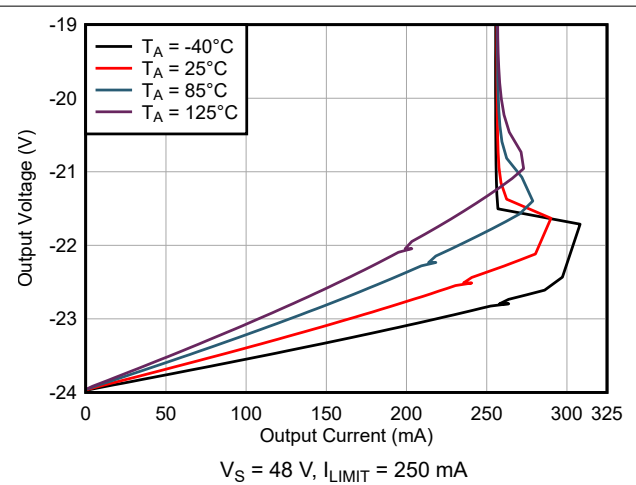


Figure 6-28. Output Voltage vs Output Sinking Current

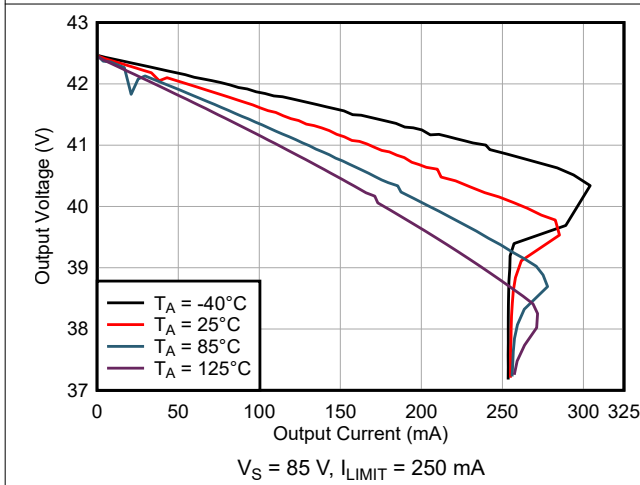


Figure 6-29. Output Voltage vs Output Sourcing Current

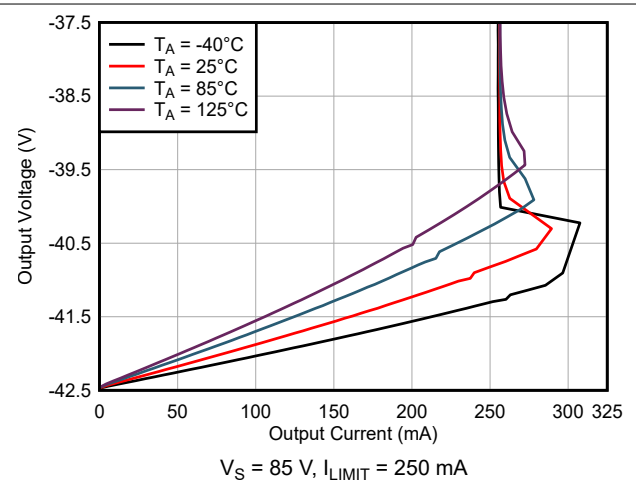


Figure 6-30. Output Voltage vs Output Sinking Current

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{LIMIT} = 100\text{ mA}$, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

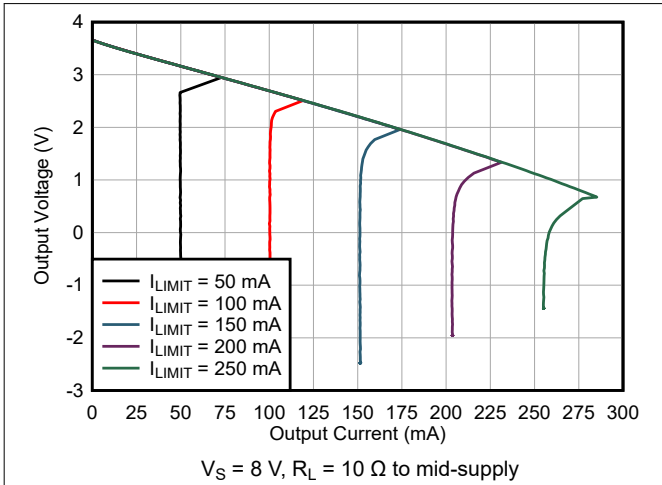


Figure 6-31. Output Voltage vs Current Limit Set

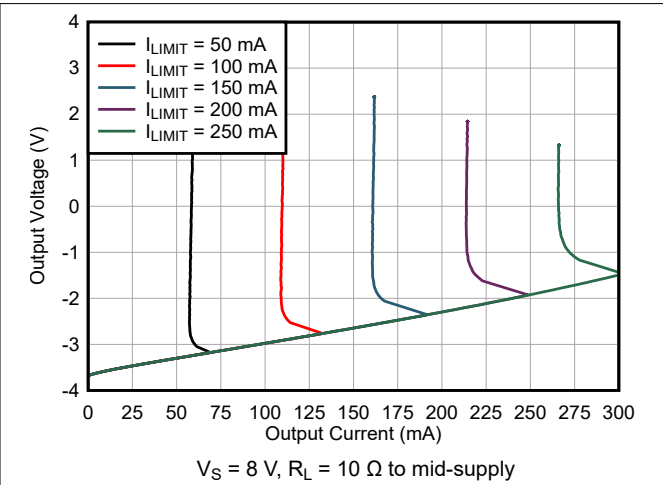


Figure 6-32. Output Voltage vs Current Limit Set

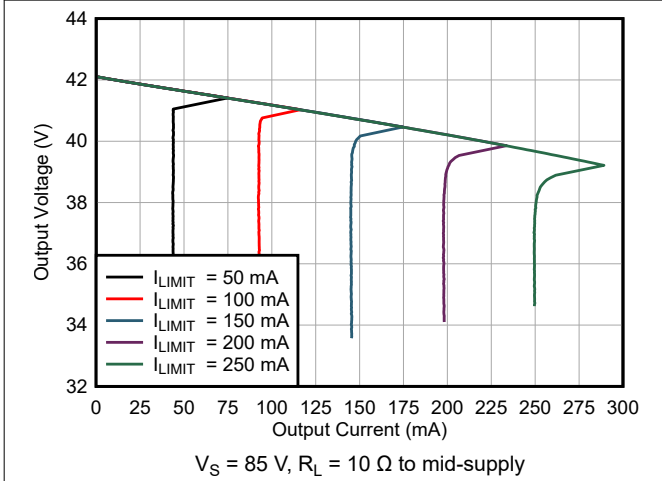


Figure 6-33. Output Voltage vs Output Sourcing Current

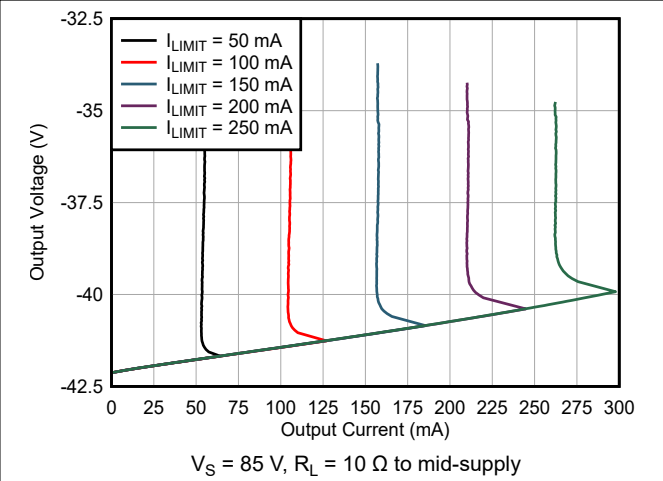


Figure 6-34. Output Voltage vs Output Sinking Current

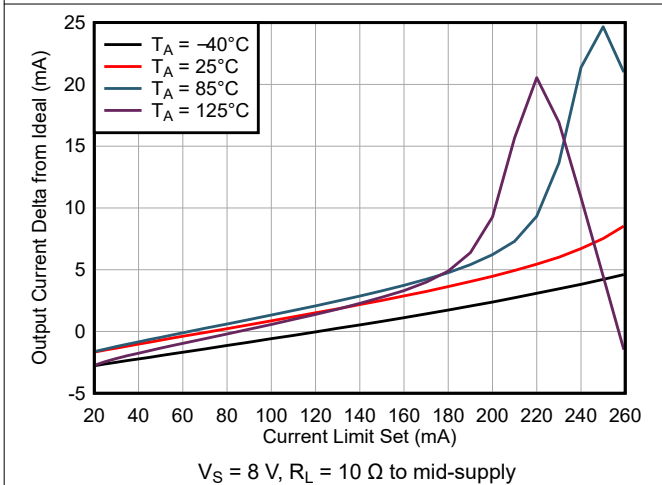


Figure 6-35. Output Sourcing Current Error vs Current Limit Set

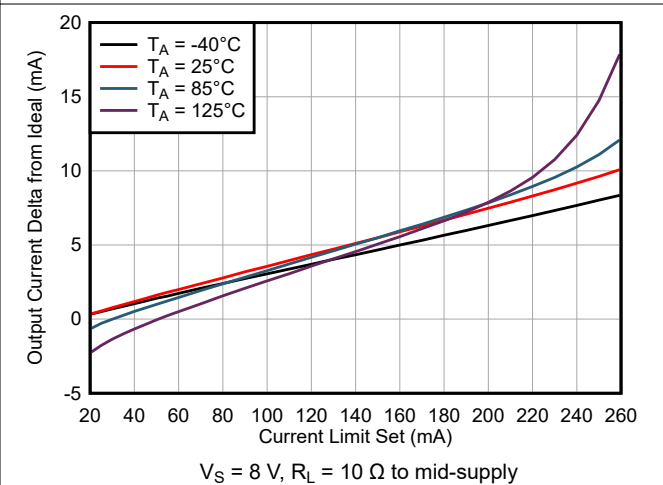


Figure 6-36. Output Sinking Current Error vs Current Limit Set

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{\text{LIMIT}} = 100\text{ mA}$, $V_{\text{CM}} = V_{\text{OUT}} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

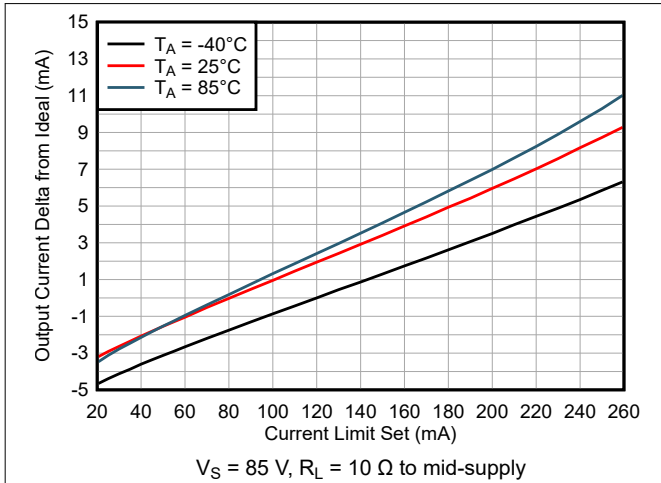


Figure 6-37. Output Sourcing Current Error vs Current Limit Set

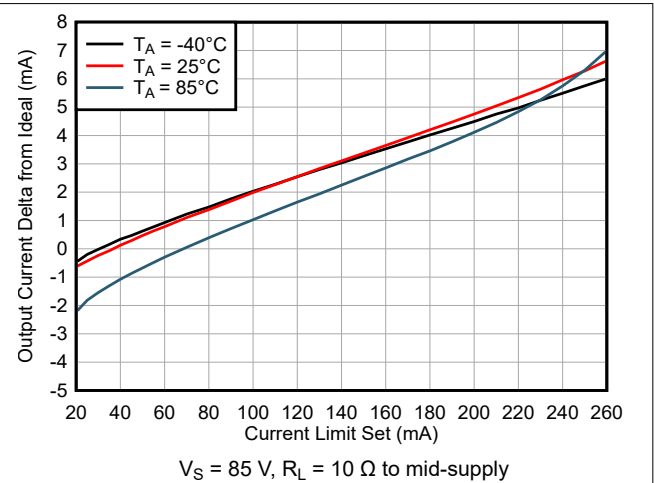


Figure 6-38. Output Sinking Current Error vs Current Limit Set

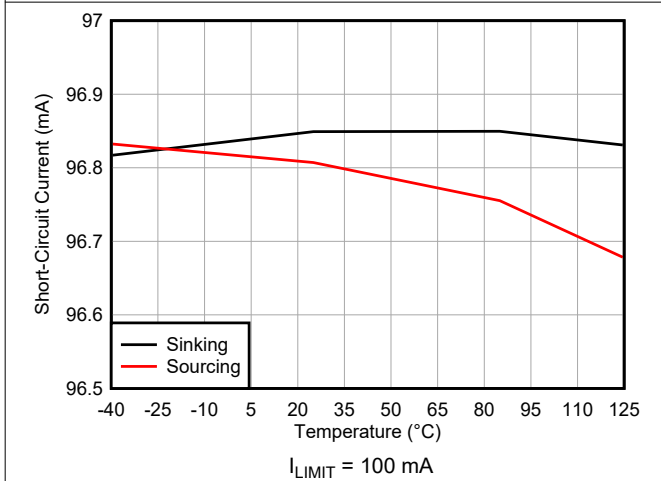


Figure 6-39. Short Circuit Current vs Temperature

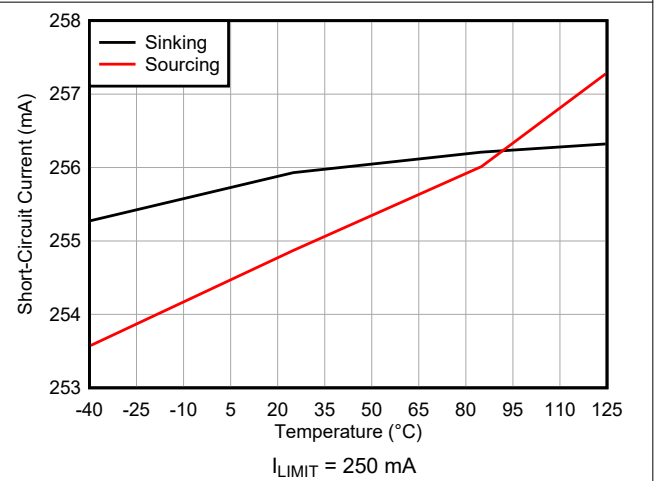


Figure 6-40. Short Circuit Current vs Temperature

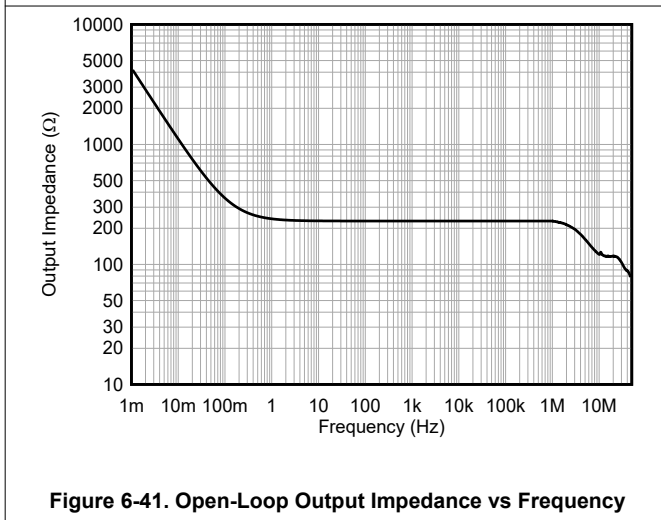


Figure 6-41. Open-Loop Output Impedance vs Frequency

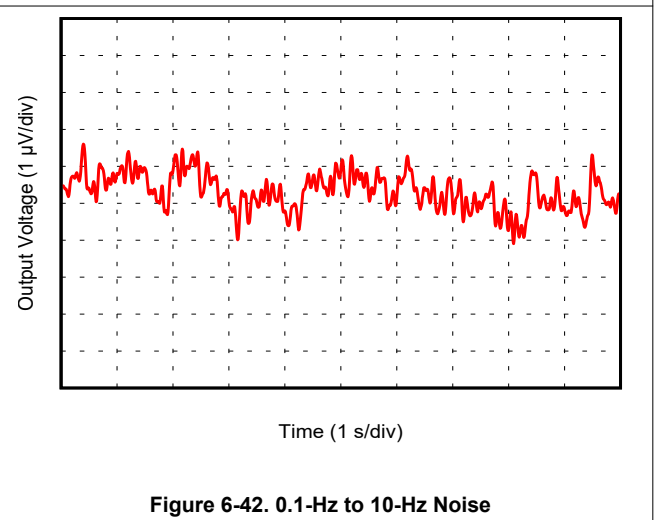


Figure 6-42. 0.1-Hz to 10-Hz Noise

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{\text{LIMIT}} = 100\text{ mA}$, $V_{\text{CM}} = V_{\text{OUT}} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

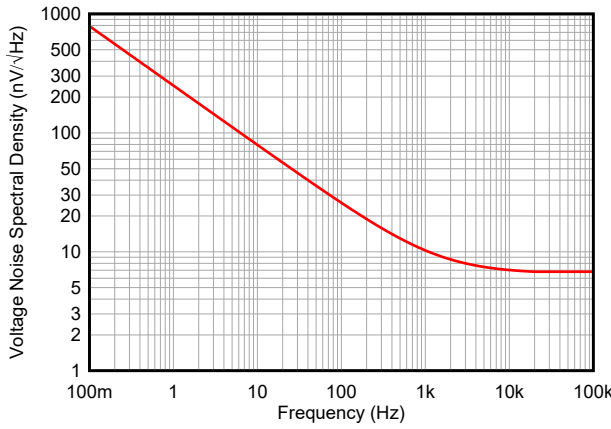


Figure 6-43. Input Voltage Noise Spectral Density

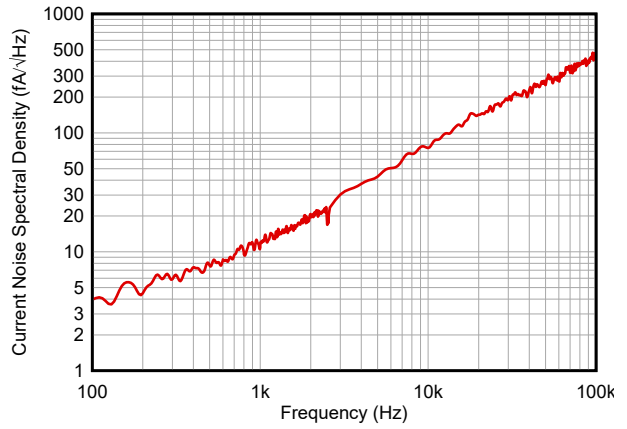


Figure 6-44. Input Current Noise Spectral Density

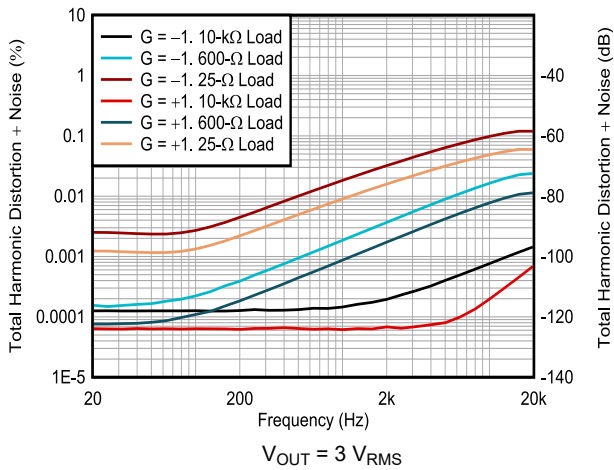


Figure 6-45. Total Harmonic Distortion + Noise vs Frequency

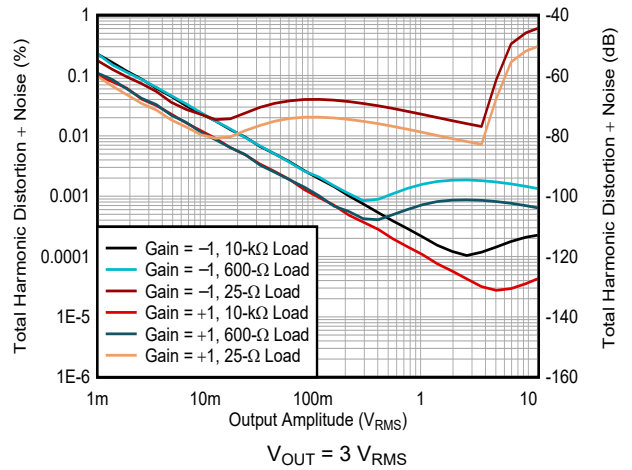


Figure 6-46. Total Harmonic Distortion + Noise vs Amplitude

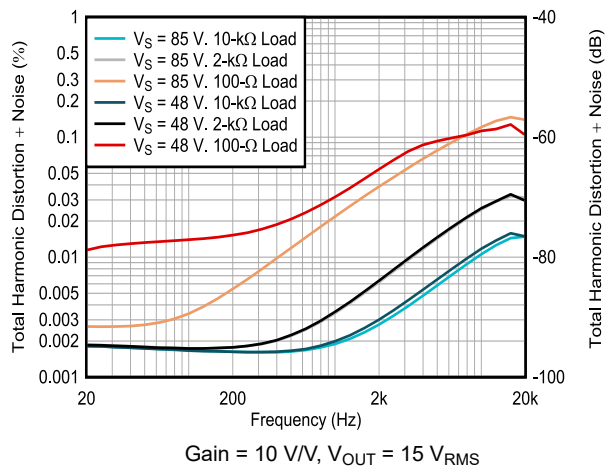


Figure 6-47. Total Harmonic Distortion + Noise vs Frequency

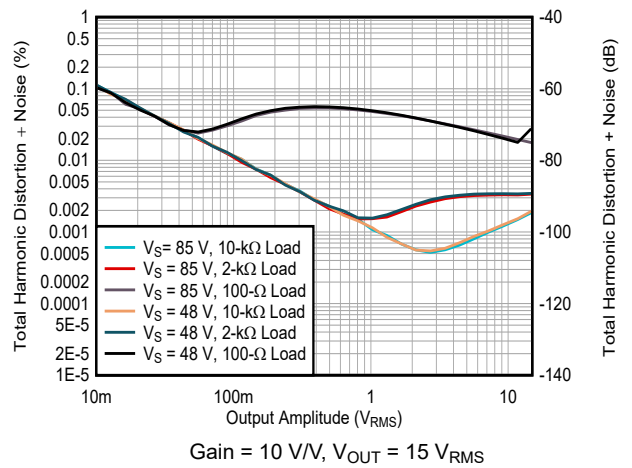


Figure 6-48. Total Harmonic Distortion + Noise vs Amplitude

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{\text{LIMIT}} = 100\text{ mA}$, $V_{\text{CM}} = V_{\text{OUT}} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

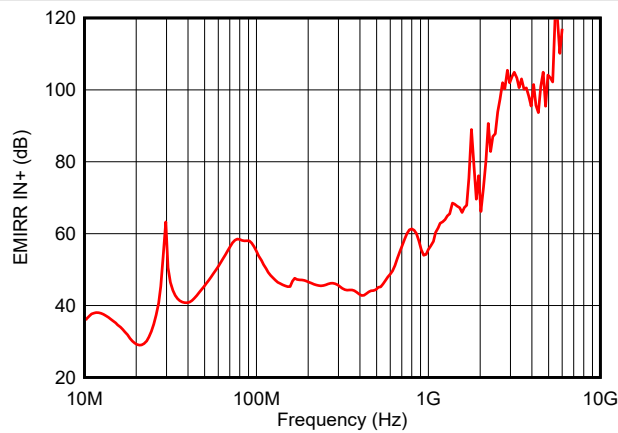


Figure 6-49. EMIRR vs Frequency

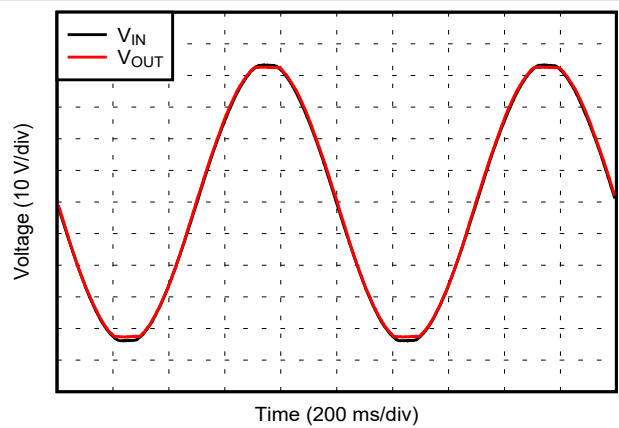


Figure 6-50. No Phase Reversal

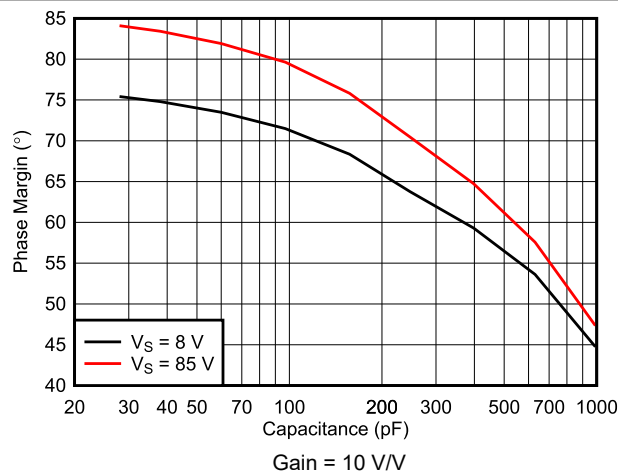


Figure 6-51. Phase Margin vs Capacitive Load

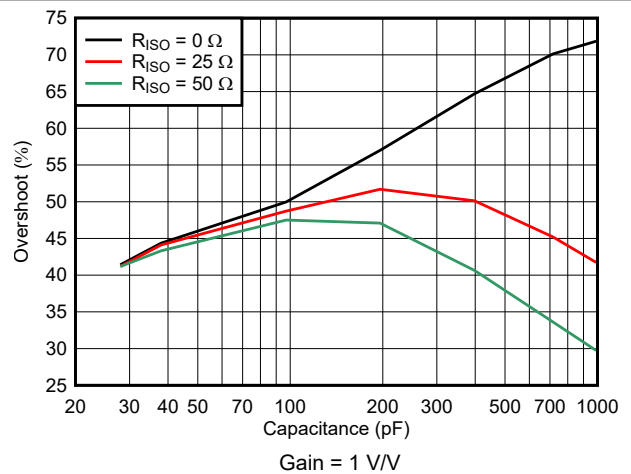


Figure 6-52. Small-Signal Overshoot vs Capacitive Load

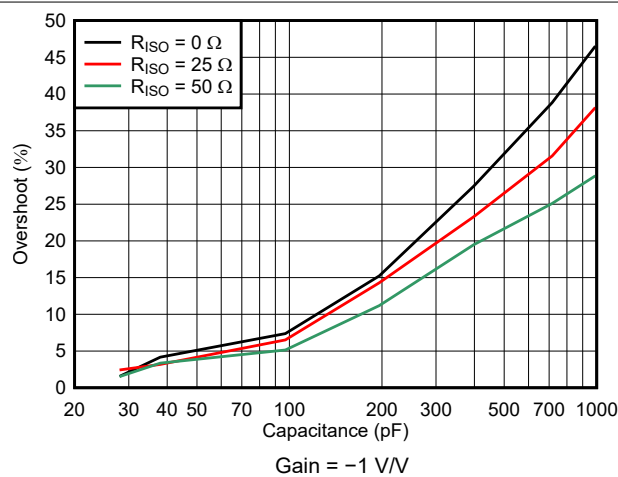


Figure 6-53. Small-Signal Overshoot vs Capacitive Load

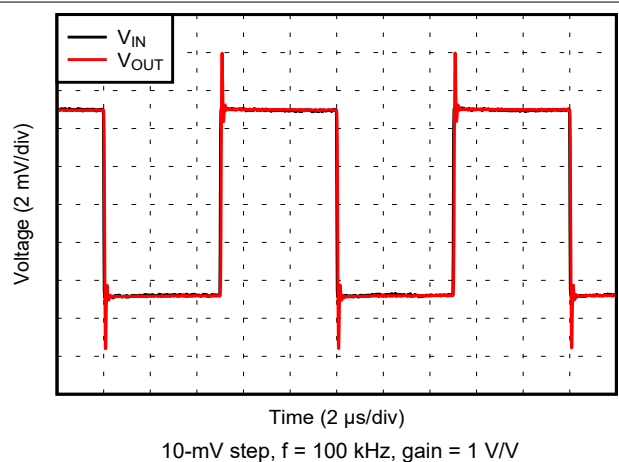
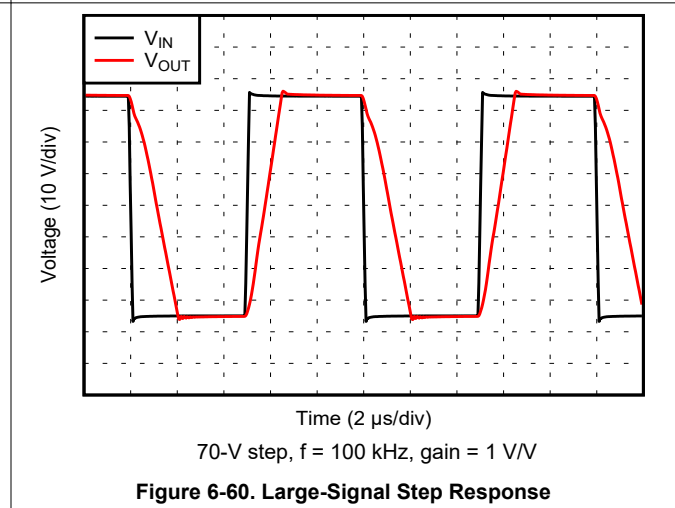
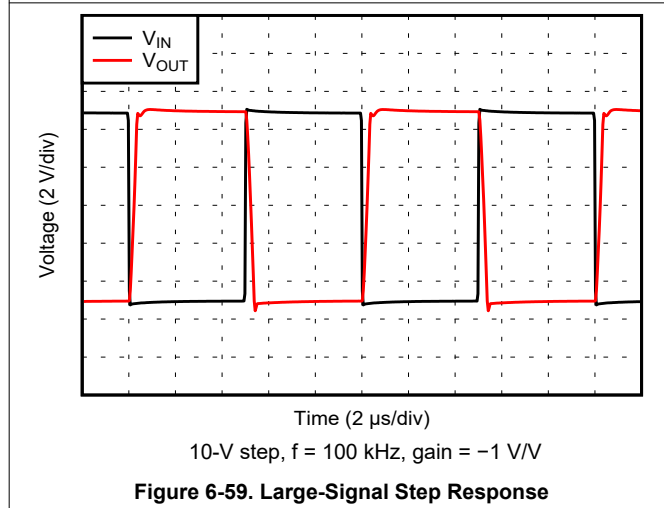
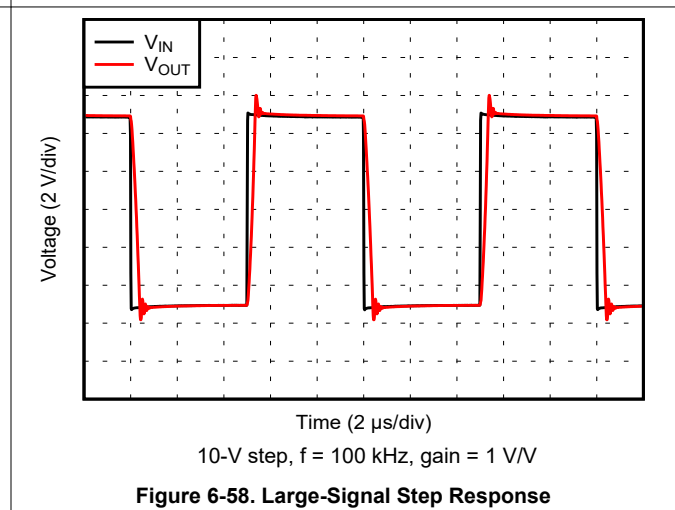
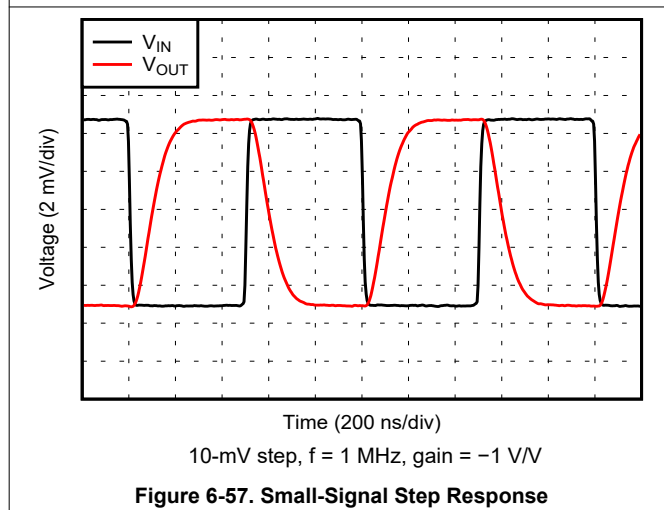
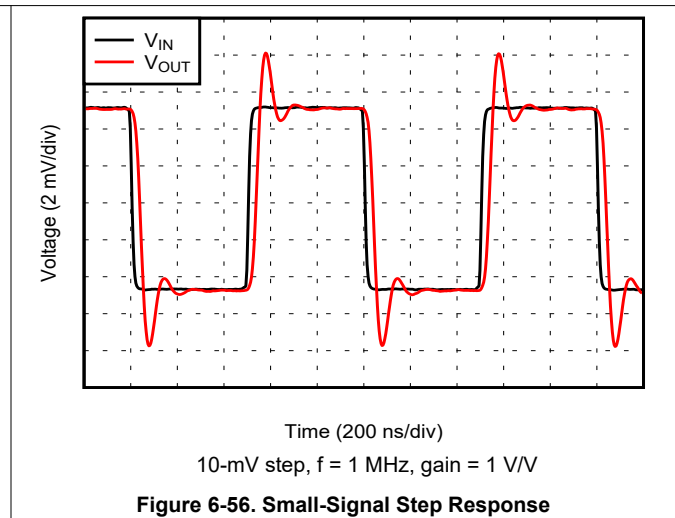
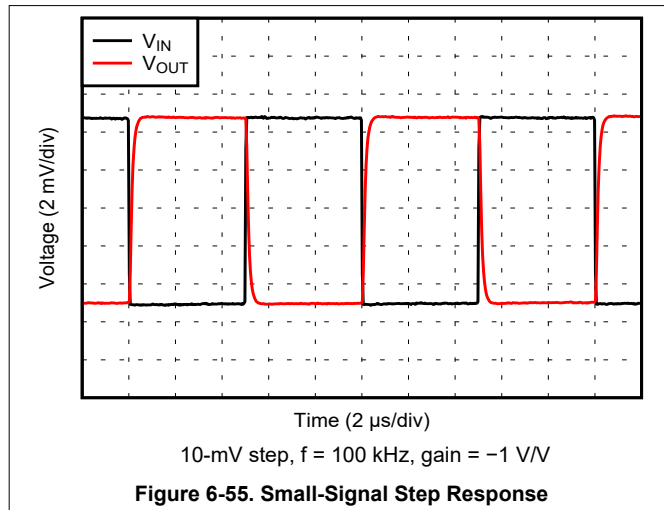


Figure 6-54. Small-Signal Step Response

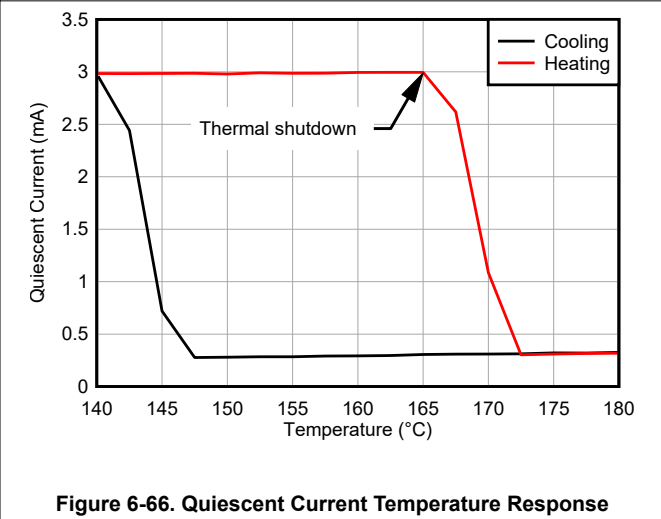
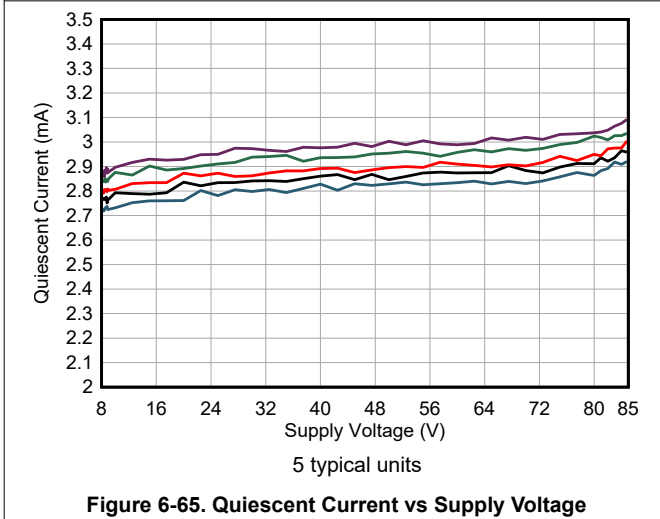
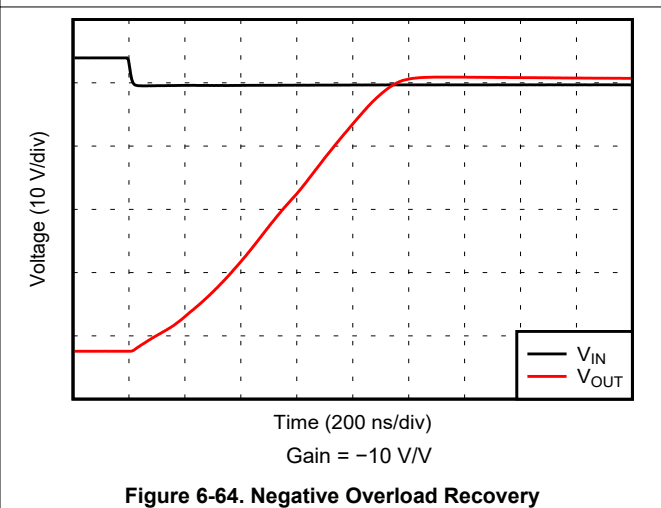
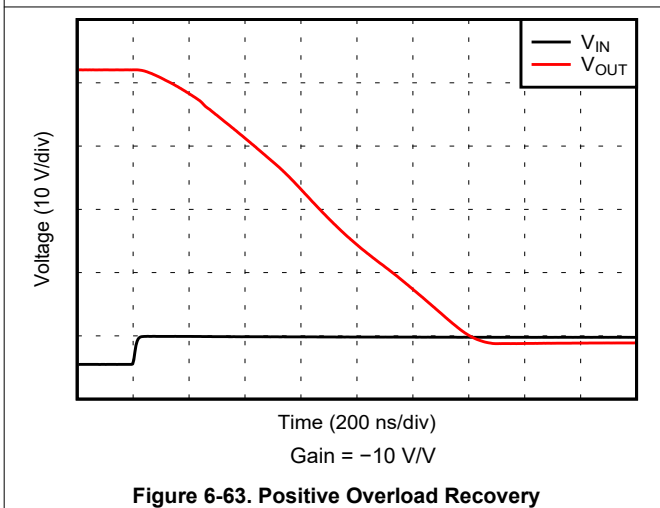
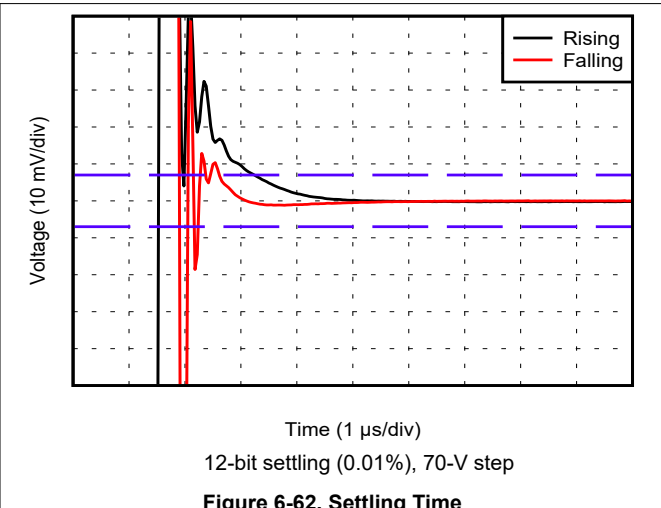
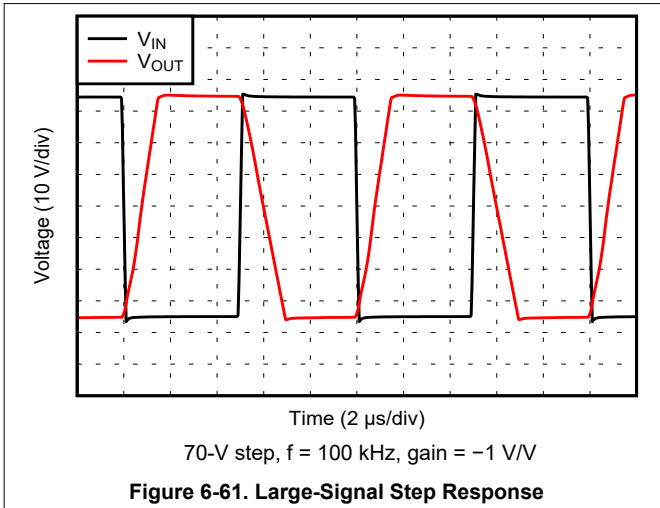
6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{\text{LIMIT}} = 100\text{ mA}$, $V_{\text{CM}} = V_{\text{OUT}} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)



6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{\text{LIMIT}} = 100\text{ mA}$, $V_{\text{CM}} = V_{\text{OUT}} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)



6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{LIMIT} = 100\text{ mA}$, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

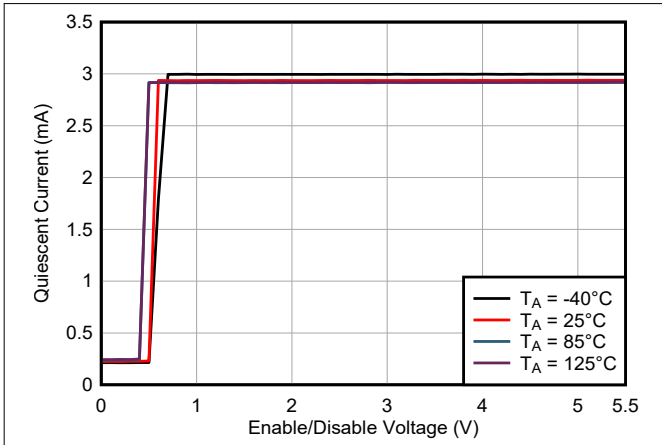


Figure 6-67. Quiescent Current vs Enable Voltage

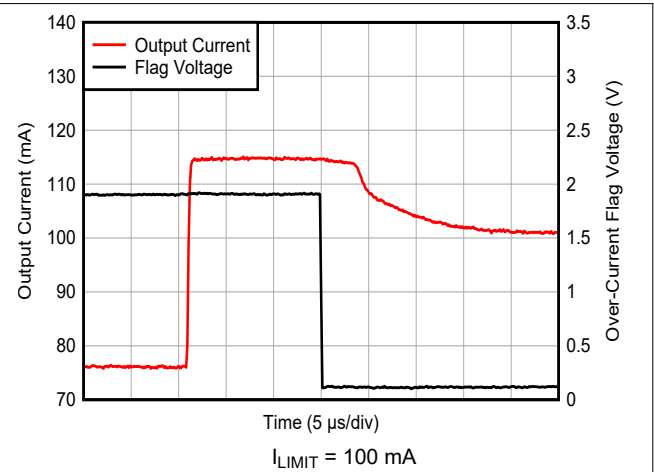


Figure 6-68. Current Limit Response

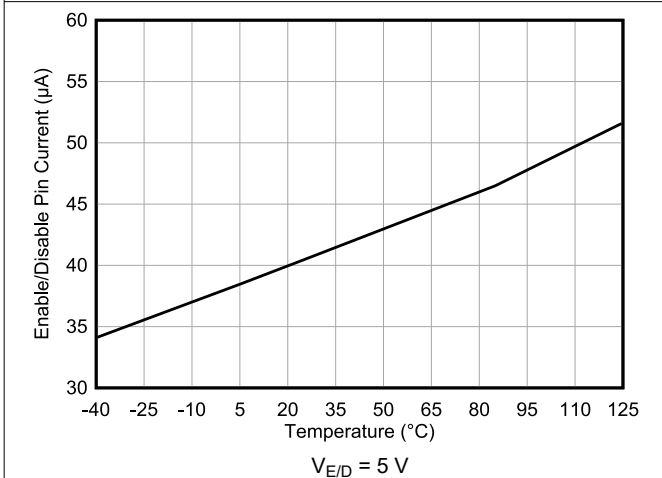


Figure 6-69. Enable/Disable Pin Current vs Temperature

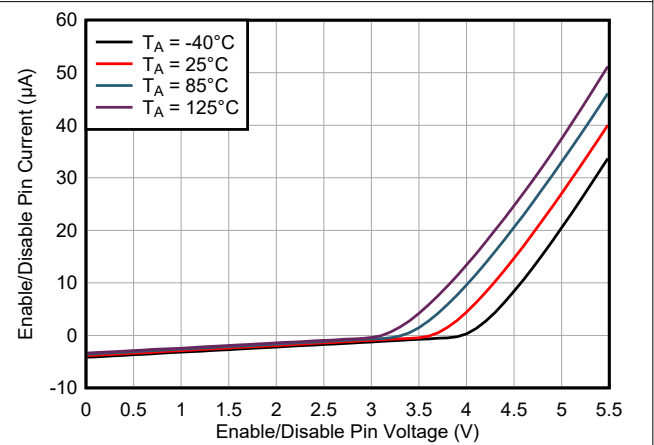


Figure 6-70. Enable Pin Current vs Enable Pin Voltage

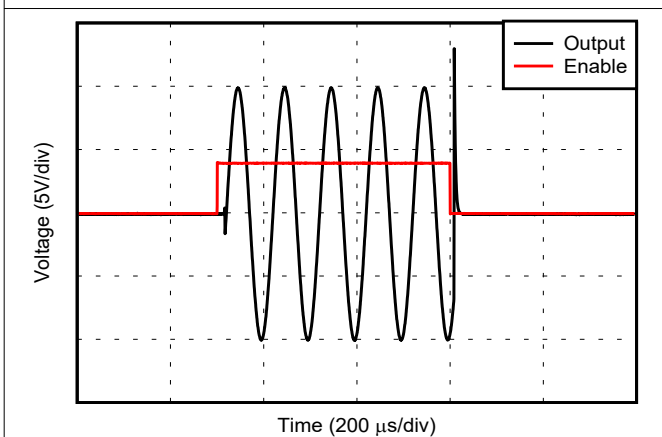


Figure 6-71. Enable Response

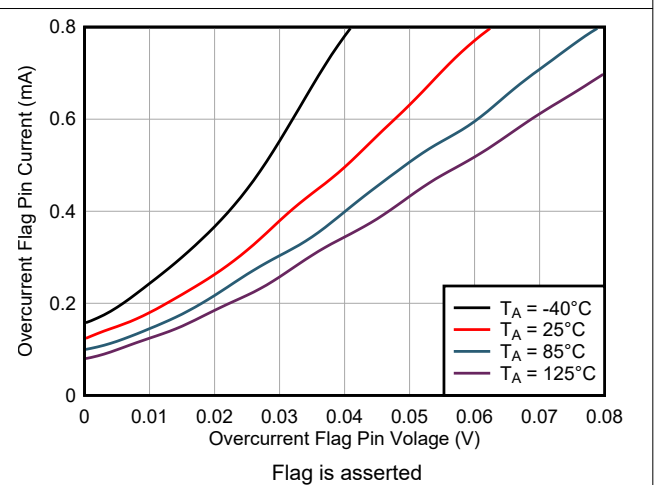
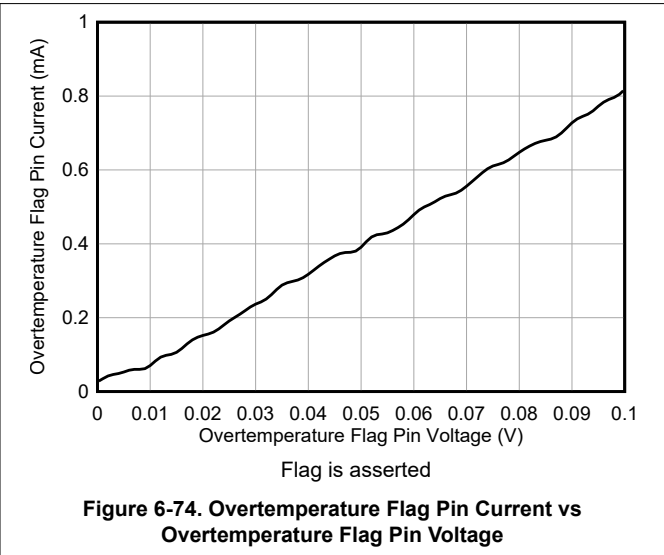
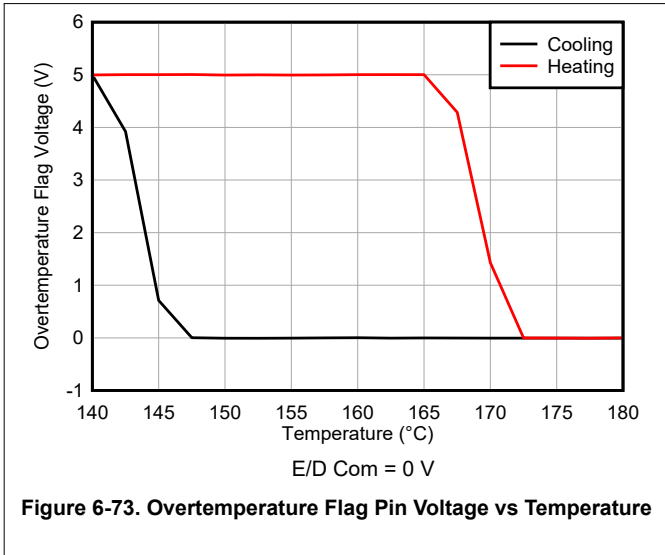


Figure 6-72. Current-Limit Flag Pin vs Current-Limit Flag Pin Voltage

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = (V+) - (V-) = 85\text{ V}$, $I_{LIMIT} = 100\text{ mA}$, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)



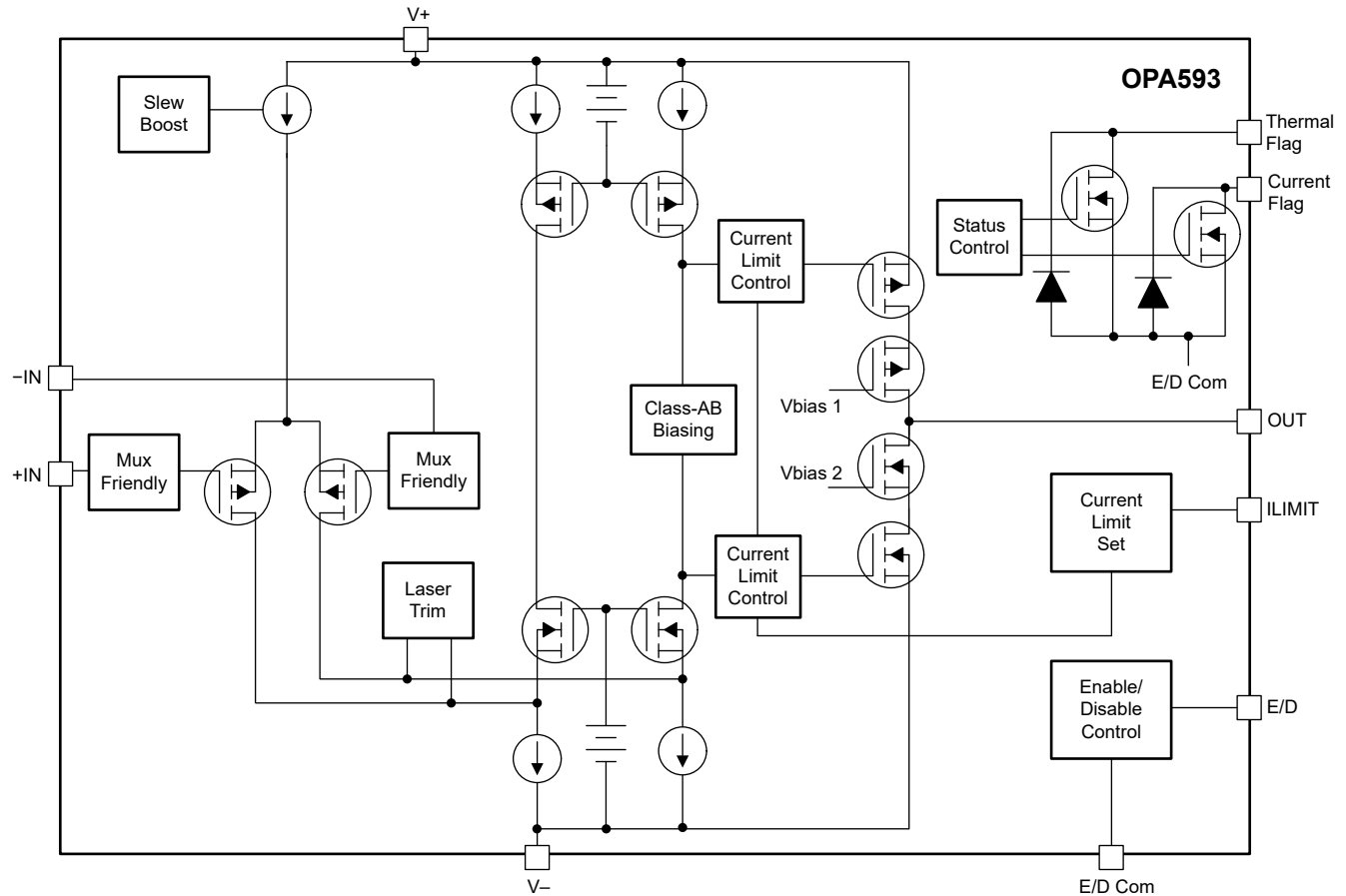
7 Detailed Description

7.1 Overview

The OPA593 is a precision, high-voltage (85 V), wide bandwidth (10 MHz), power operational amplifier (op amp) with a high output current drive of ± 250 mA. The device features a current limit that helps protect the system in the event of an output short to ground. Unlike other power op amps, the current limit is specified for specific current ranges from ± 25 mA to ± 250 mA. Additionally, the device has two flags that indicate an overcurrent fault condition (beyond the configured limit) and an overtemperature fault condition (when the output stage shuts down to protect the device from overheating). Lastly, the output can be disabled to save system power and reduce thermal dissipation.

The unity-gain stable OPA593 has no phase inversion, a common-mode voltage range that includes the negative rail, a wide output swing range, and high dc precision. All these features make the OPA593 an excellent choice as an output driver for a device under test (DUT) in automated test equipment (ATE) systems, or for signal processing in industrial systems using signals greater than 36 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Current Limit

The OPA593 current limit is set through the I_{LIMIT} pin and is programmable from ±25 mA to ±250 mA, typical. The device is specified and tested for current limits of ±25 mA, ±50 mA, ±100 mA, ±250 mA. A resistor can be used to limit the current to a fixed value or a digital-to-analog converter (DAC) can be used to vary the current limit during operation. Figure 7-1 shows a simplified diagram of the current-limit mirror configurations, as well as common resistor or DAC settings and the respective output current limit.

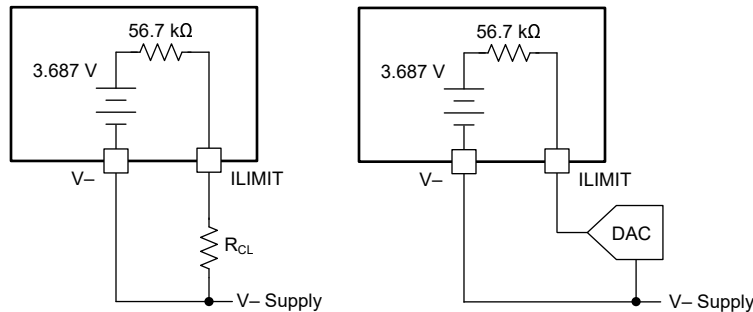


Figure 7-1. OPA593 Internal Current Limit Configurations

The most common configuration is to set the current limit using a resistor (R_{CL}) connected between the I_{LIMIT} pin and the negative supply (V_{-}). With this configuration, Equation 1 and Equation 2 are used to calculate the current limit based on the external resistor value or the resistor needed given the desired current limit value:

$$I_{LIMIT} = \frac{3.687\text{ V} \times 4000}{56.7\text{ k}\Omega + R_{CL}} \quad (1)$$

$$R_{CL} = \frac{3.687\text{ V} \times 4000}{I_{LIMIT}} - 56.7\text{ k}\Omega \quad (2)$$

An alternative to fixing the current limit to a single value using an external resistor is to use a source measure unit (SMU) or digital-to-analog converter (DAC), which enables a variable current limit.

CAUTION

With this configuration, the output of the SMU or DAC must not exceed the I_{LIMIT} specification in Section 6.1 to avoid reverse biasing the internal current limit circuitry and potentially damaging the device.

Use Equation 3 to set the current limit when a DAC is used ($V_{LIMIT} = \text{DAC output voltage}$):

$$V_{LIMIT} = 3.687\text{ V} - \frac{I_{LIMIT} \times 56.7\text{ k}\Omega}{4000} \quad (3)$$

Be aware that the SMU or DAC output voltage must be referenced to the negative supply of the OPA593. Several nominal current-limit values along with the respective external resistor values and DAC output voltages are listed in Table 7-1.

Table 7-1. Nominal Current-Limit Values

CURRENT LIMIT, I_{LIMIT} (mA)	RESISTOR, R_{CL} (k Ω)	DAC VOLTAGE, V_{LIMIT} (V) ⁽¹⁾
25	536	3.33
50	237	2.98
100	90.9	2.27
200	16.9	0.85
250	2.29	0.14

(1) Voltages are referenced to the negative supply, V_{-}

While the current limit tolerance of the OPA593 is specified for specific current limit levels, any resistor, SMU, or DAC inaccuracies add to the listed tolerance. To achieve the desired system level accuracy, take care when selecting these external components. Figure 7-2 shows a correlation between the ideal or calculated output current limit and the actual current limit as measured on the OPA593.

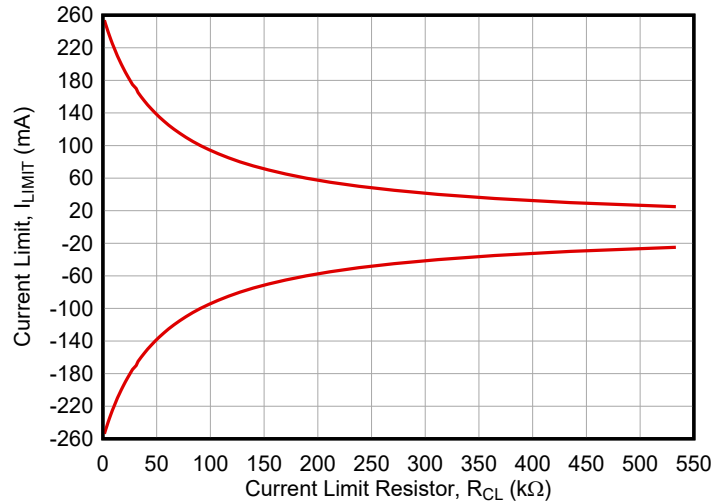


Figure 7-2. Typical Output Current vs Current-Limit Resistor Value

7.3.2 Overcurrent Flag

The OPA593 features an overcurrent flag (Current Flag pin) that indicates a condition where the output current exceeds the limit established by the ILIMIT pin. For example, in an output short-to-ground fault condition, the overcurrent flag asserts, which pulls the flag pin low to E/D Com, and the output current is limited to the value set by ILIMIT. This flag is an open-drain output compatible with standard low-voltage logic circuitry, such as a microcontroller (MCU). Use a 5-k Ω to 10-k Ω pullup resistor to limit the input current when the flag is asserted. If this feature is not used, leave this pin floating.

7.3.3 Overtemperature Flag

The OPA593 has internal thermal protection. When the junction temperature reaches approximately 170°C, the op amp output stage disables and the overtemperature flag (Thermal Flag pin) is asserted, which pulls the flag pin low to E/D Com. When the junction temperature cools to a safe operating temperature, approximately 150°C, the output stage is enabled, and the op amp resumes normal operation. This flag is an open-drain output compatible with standard low-voltage logic circuitry, such as an MCU. Use a 5-k Ω to 10-k Ω pullup resistor to limit the input current when the flag is asserted. If this feature is not used, leave this pin floating.

7.3.4 Output Enable and Disable

The OPA593 incorporates an enable and disable feature that uses the E/D pin to disable the output stage of the amplifier, which reduces the power consumption of the op amp and switches the output to a high-impedance state.

The E/D pin is referenced to the E/D Com pin. If left floating, the E/D pin is internally pulled up to enable the device. If externally controlled, the E/D pin must be supplied with a voltage between 1.5 V and 5.5 V greater than the E/D Com pin voltage. Even though the OPA593 output is enabled with a floating E/D pin, a moderately fast, negative-going signal capacitively coupled to the E/D pin can overpower the internal pullup and cause device shutdown. If the enable function is not used, a conservative and recommended approach is to connect E/D through a 47-pF capacitor to E/D Com. [Figure 7-3](#) shows different ways to connect the E/D and E/D Com pins.

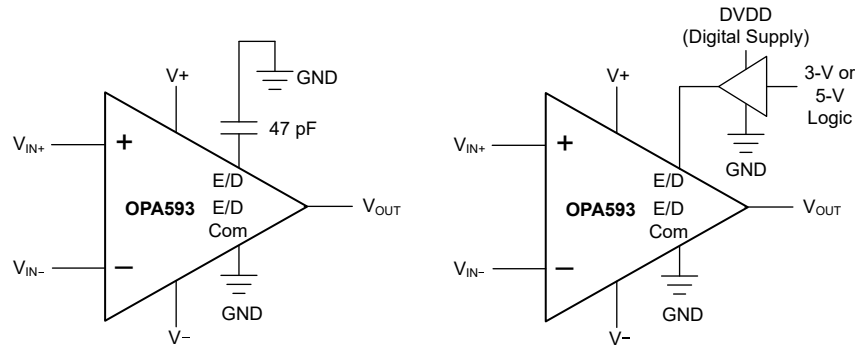


Figure 7-3. E/D and E/D Com Pin Connections

When the E/D pin is dropped to a voltage between 0 V and 0.5 V greater than the E/D Com pin voltage, the output of the OPA593 is disabled. When disabled, the output of the OPA593 is set to a high-impedance state.

7.3.5 Mux-Friendly Inputs

The OPA593 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in [Figure 7-4](#) can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in [Figure 7-5](#). For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current, resulting in extended settling time.

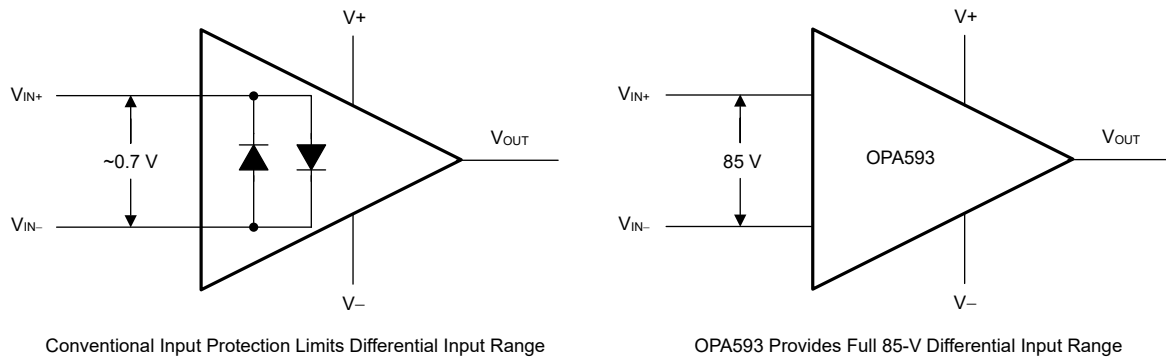


Figure 7-4. OPA593 Input Protection Does Not Limit Differential Input Capability

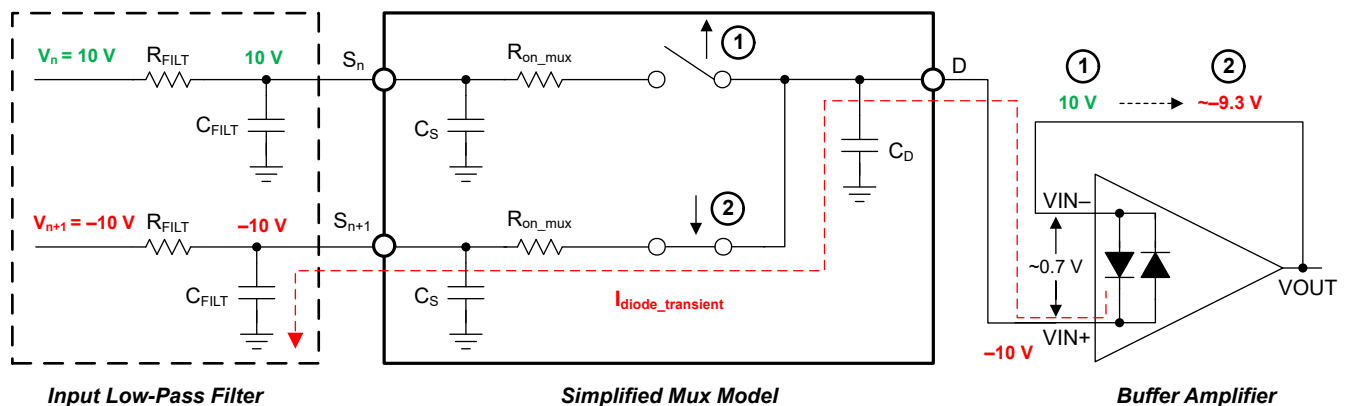


Figure 7-5. Back-to-Back Diodes Create Settling Issues

The OPA593 a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making this device an excellent choice for multichannel, high-switched, input applications. The OPA593 tolerates a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 85 V, making this device a great choice for use as a comparator or in applications with fast-ramping or switched input signals.

7.4 Device Functional Modes

The OPA593 has two modes of operation. The first mode is normal operation where the amplifier is enabled, either by supplying a voltage to the enable-disable (E/D) pin that is between 2.5 V and 5 V greater than the E/D Com pin or by leaving the E/D pin floating. The second mode of operation is a low-power, disabled state where the E/D pin is driven between 0 V and 0.65 V greater than the E/D Com pin. In this state, the amplifier output is disabled and enters a high-output-impedance state.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPA593 is a precision, high-voltage, high-output-current op amp. The device is capable of operating with supplies as low as ± 4 V (8 V) and as high as ± 42.5 V (85 V). The current limit feature limits the output current, up to ± 250 mA, to a specified accuracy. With a small size, high operating voltage range, output current, and high dc precision, the device is designed to operate as a high-gain stage, capable of driving heavy loads and condition large signals. The additional features of the OPA593, including the current limit, overcurrent and overtemperature flags, thermal protection, output disable, and mux-friendly inputs, help protect both the op amp and the system from potential damage due to various fault conditions.

8.2 Typical Application

8.2.1 Output Driver

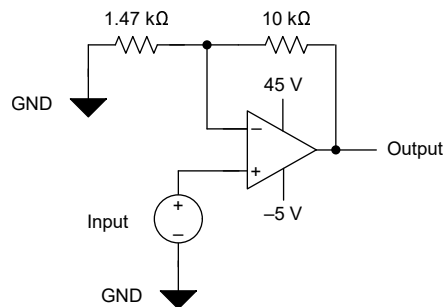


Figure 8-1. Output Driver Configured With a Gain of 8

8.2.1.1 Design Requirements

The OPA593 is designed for use as an output driver stage with gain and provides a wide supply voltage and high output current with programmable current limit. Combined with the small size of the 4-mm \times 4-mm WSON package, these features make this device a great choice for high-channel density systems, such as semiconductor test and manufacturing platforms where many channels are present. In this design example, the OPA593 is configured for a gain of 8 V/V. A small negative supply is provided if the application requires a small output voltage. For example, in the case of a device under test (DUT) continuity check, the amplifier is able to provide the output without being limited by the negative rail (that is, saturating the output).

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage	+45 V, -5 V
Input voltage	0 V to 5 V
Output voltage	0 V to 40 V
System gain	8
Output current	Up to 250 mA

8.2.1.2 Detailed Design Procedure

In this design example, the OPA593 is configured as both a gain stage and output driver. The input signal to the amplifier is 0 V to 5 V, and the device is configured with a positive gain of 8. This configuration results in an output voltage of 0 V to 40 V. Select supply voltages that provide adequate headroom so that the amplifier can sink or source up to 250 mA without *slamming* the output into the rail. Minimize the swing from the supply to the output to minimize the thermal dissipation of the device.

This simple design example is common in many systems that use a DAC to provide the input signal and require a wide output signal with high output current. Such systems include test and measurement platforms and power supplies.

Figure 8-2 shows the input and output signal of this OPA593 circuit.

8.2.1.3 Application Curve

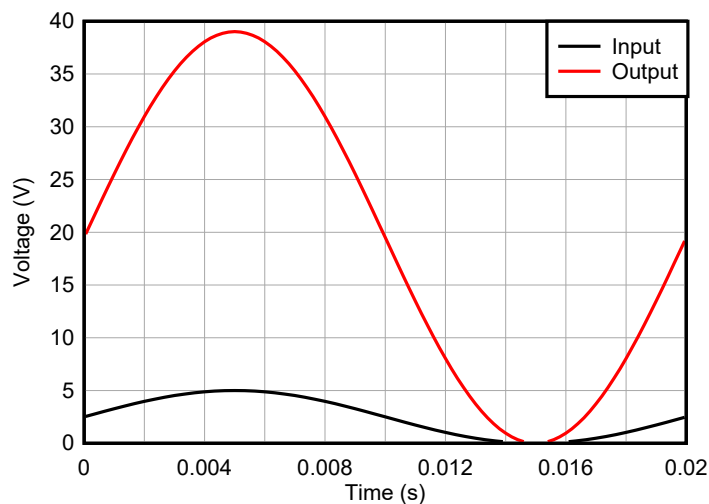


Figure 8-2. OPA593 Output Driver Circuit, Input and Output Signals

8.2.2 High Voltage 2:1 Multiplexer With Unity Gain

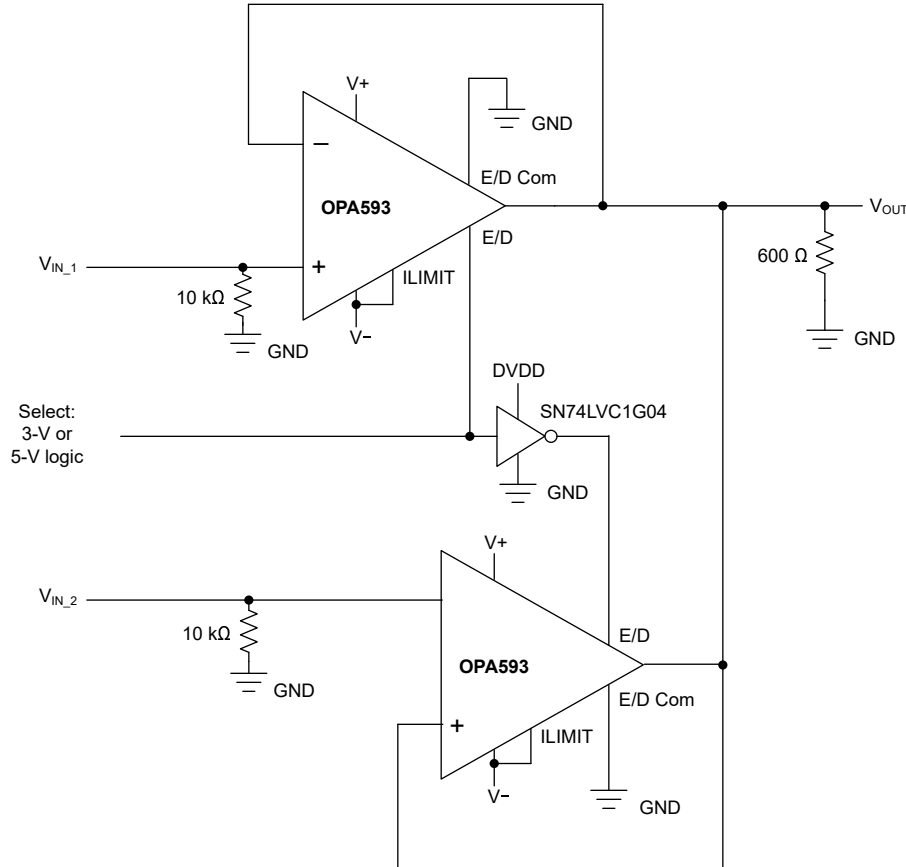


Figure 8-3. High Voltage 2:1 Multiplexer With Unity Gain

8.2.2.1 Design Requirements

The OPA593 operates on high-voltage supplies up to 85 V and is used to create a high voltage multiplexer (MUX) with a gain of 1 or higher. This design example uses two OPA593 op amps and makes use of the disable function. The high-impedance state of the output while the amplifier is disabled allows for the outputs of two OPA593 op amps to be connected together.

8.2.2.2 Detailed Design Procedure

In this design example, two OPA593 precision op amps are configured as a unity gain buffers powered with a ± 42.5 -V dual supply. The input signal to either amplifier can range from -40 V to $+39$ V to remain in linear operation. The output of the amplifiers are connected together and a 3-V or 5-V logic signal, serving as the output select, is used to toggle between the enable and disable modes of operation. The logic control signal is directly applied to one OPA593 E/D pin, and an inverter gate is used to drive the other OPA593 E/D pin. [Figure 8-3](#) shows a simplified representation of this circuit.

A clear benefit of this design is the high-voltage capability, along with the thermal protection, overcurrent protection, and current-limit features. The *mux-friendly* input of the OPA593 provides a full input differential range, avoiding the pitfalls of other amplifiers with traditional back-to-back diodes in this configuration. This design can also be reconfigured to include signal gain, but careful selection of the input and feedback resistors is required to minimize current leakage paths.

8.3 Power Supply Recommendations

The OPA593 operates from power supplies up to ± 42.5 V, or a total of 85 V, with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. A power-supply bypass capacitor of at least 0.1 μ F is required for proper operation. Make sure that the capacitor voltage is rated for high voltage across the full operating temperature range. Parameters that vary significantly with operating voltage are shown in [Section 6.6](#).

Some applications do not require an equal positive and negative output voltage swing. Power-supply voltages do not have to be equal. The OPA593 operates with as little as 8 V between the supplies, and with up to 85 V between the supplies.

8.4 Layout

8.4.1 Layout Guidelines

During the surface-mount solder operation (when the pins are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat is conducted away from the package into a V- plane. Always solder the thermal pad to the PCB, even with applications that have low power dissipation. Follow these steps to attach the device to the PCB:

1. Connect the thermal pad to the most negative supply voltage on the device, V-.
2. Prepare the PCB with a top-side pattern. There must be patterning for the pins and thermal pad.
3. Thermal vias improve heat dissipation, but are not required.
4. Place recommended vias in the area of the thermal pad. Recommended thermal land size and thermal via patterns for the SON-12 DNT package are shown in the thermal land pattern mechanical drawing appended at the end of this document. Keep the vias small, so that solder wicking through the vias is not a problem during reflow. Use a 0.2-mm size via with a minimum of five connected directly below the thermal pad.
5. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA593 device. These additional vias can be larger than the vias directly under the thermal pad because the additional vias are not in the thermal pad area to be soldered; thus, wicking is not a problem.
6. Connect all vias to the internal power plane of the correct voltage potential, V-.
7. When connecting these vias to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the vias under the OPA593 WSON package must make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
8. The top-side solder mask must leave the pins of the package and the thermal pad area exposed. The bottom-side solder mask must cover the vias of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
9. Apply solder paste to the exposed thermal pad area and all of the device pins.
10. With these preparatory steps in place, simply place the device in position, and run through the solder reflow operation as with any standard surface-mount component.

8.4.1.1 Thermal Considerations

Through normal operation, the OPA593 self-heats. Self-heating is a natural increase in the die junction temperature that occurs in every amplifier. The maximum allowed junction temperature sets the maximum allowed internal power dissipation (P_D) as described in the following paragraph. Design efforts should be made to prevent T_J from exceeding the maximum temperature listed in the *Absolute Maximum Ratings* table.

Operating junction temperature (T_J) is determined by the ambient temperature (T_A), the internal P_D under the operating conditions, and the junction-to-ambient thermal resistance ($R_{\theta JA}$). This relationship is given by $T_A + (P_D \times R_{\theta JA})$. P_D is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) when delivering power to the load. P_{DQ} is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load, but for a grounded resistive load the P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for balanced bipolar supplies, $V+$ and $V-$). Under this condition $P_{DL} = (V+)^2 / (4 \times R_L)$, where R_L includes feedback network loading.

The power in the output stage and not into the load determines internal power dissipation.

As a worst-case example, compute the maximum T_J using the OPA593 in the circuit of [Figure 8-1](#) operating at a maximum specified temperature of 125°C and driving a grounded 600-Ω load.

$$P_D = P_{DQ} + P_{DL} \quad (4)$$

$$P_D = (50\text{ V} \times 4\text{ mA}) + \frac{22.5^2\text{ V}}{(4 \times 600\ \Omega \parallel 11.47\text{ k}\Omega)} \quad (5)$$

$$T_J(\text{max}) = 125^\circ\text{C} + (0.422\text{ W} \times 40.8^\circ\text{C/W}) = 142.2^\circ\text{C} \quad (6)$$

To enhance semiconductor long-term operating life, minimize T_J . Take proper measures to provide maximum heat removal through both heat conduction and radiation to help keep T_J to the lowest possible level. These proper measures include maximizing the PCB copper area to which the package thermal pad is soldered. The copper area serves as the traditional heat sink. The top layer copper is often easiest to route and is most often exposed to open air. PCB internal planes and the exposed bottom plane can also be used as heat sinks, but the connections are made with vias having higher thermal resistance. The [OPA593EVM](#) uses a board design that provides a highly effective thermal layout. The board design encompasses a large top-side copper area, and has heat conduction paths to other planes on the board. Additionally, other higher power-dissipating components are kept physically distant from the OPA593 to better accommodate heat removal by radiation.

8.4.2 Layout Example

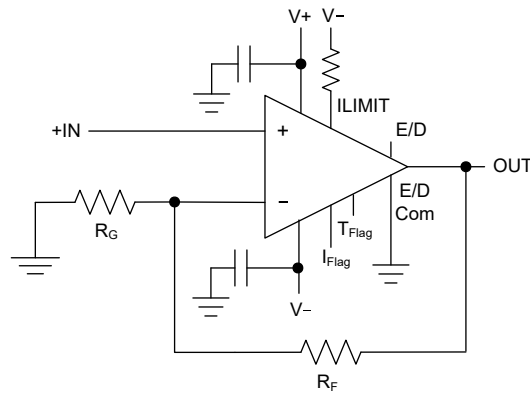


Figure 8-4. Schematic Representation

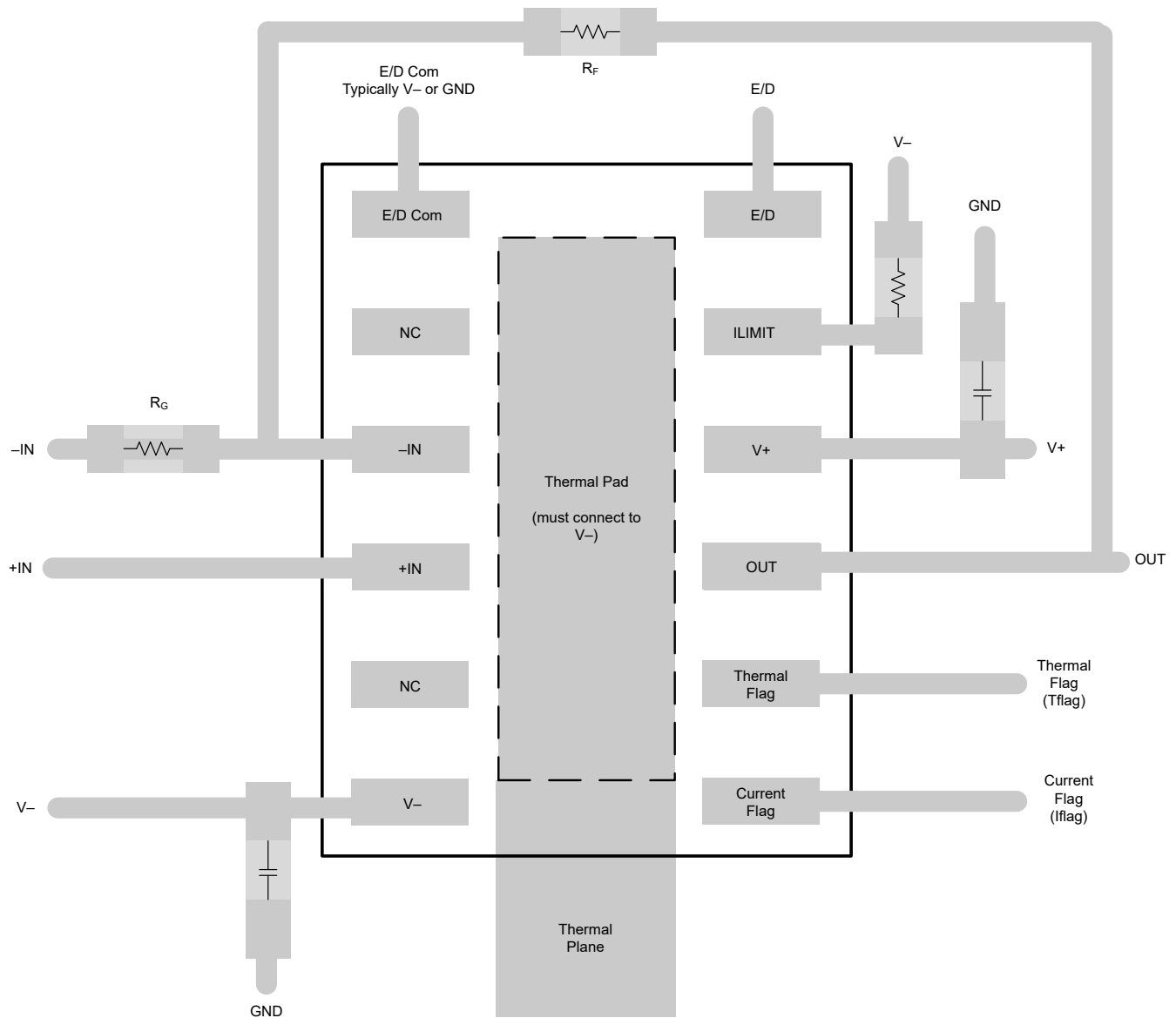


Figure 8-5. OPA593 Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the [Design tools and simulation](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA593DNTR	Active	Production	WSON (DNT) 12	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA593
OPA593DNTT	Active	Production	WSON (DNT) 12	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA593

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA593DNTR	WSO	DNT	12	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA593DNTR	WSO	DNT	12	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

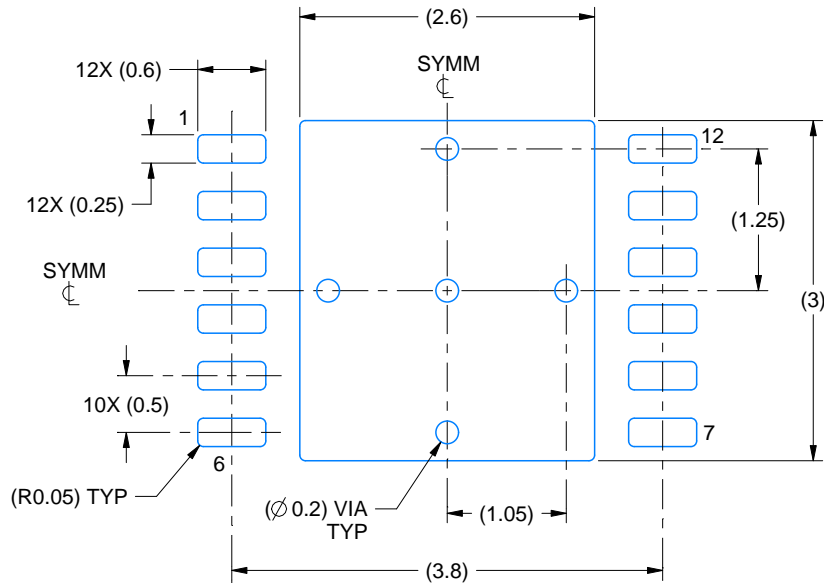
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA593DNTR	WSON	DNT	12	5000	367.0	367.0	35.0
OPA593DNTR	WSON	DNT	12	250	210.0	185.0	35.0

EXAMPLE BOARD LAYOUT

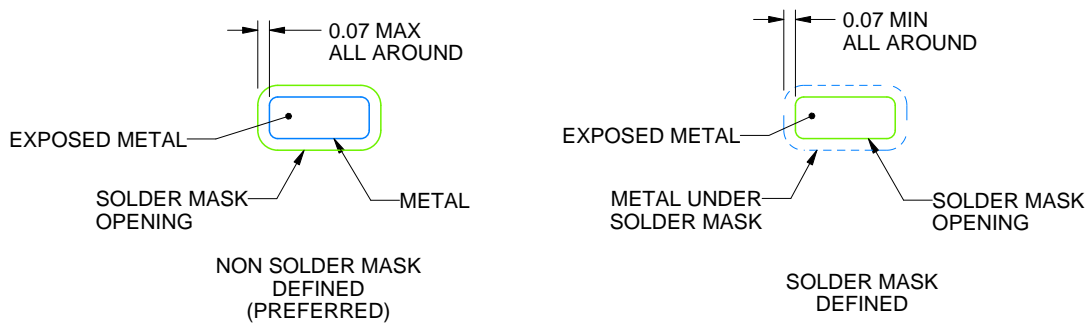
DNT0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

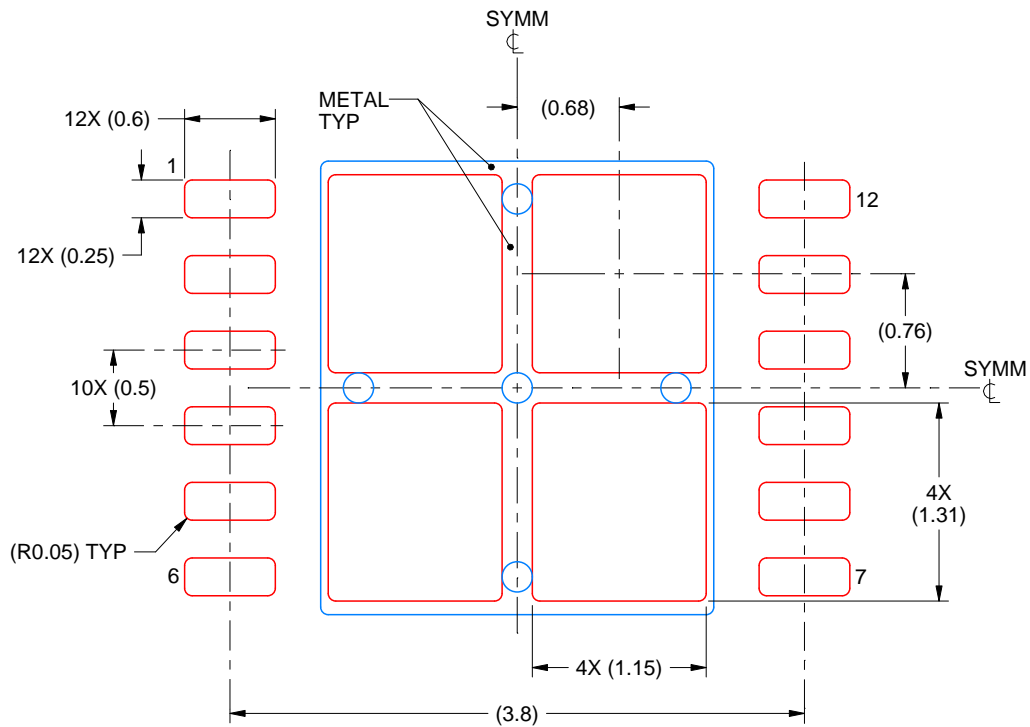
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DNT0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management