



**THE DATASHEET OF
MF4SAM3HN/9BA659Z**



MF4SAM3X_SDS

MIFARE SAM AV3 secure access module

Rev. 3.2 — 5 March 2024

Product short data sheet

1 General description

The NXP MIFARE SAM AV3 secure hardware solution is the ideal add-on for reader devices offering additional security services. Supporting DES, TDEA, AES and RSA capabilities, it offers secure storage and secure communication in various infrastructures.

Unlike other products in the field, MIFARE SAM AV3 has proven interoperability with all broad card and RFID product portfolio of NXP, (MIFARE, NTAG DNA, ICODE DNA, UCODE DNA and SmartMX product families), making it the most versatile and secure SAM solution on the market today.

The MIFARE SAM AV3 is built on the SmartMX2 P60 secure smart card controller with CC EAL6+ certification of NXP. Its software implementation is evaluated and composite certified by the MIFARE Security Evaluation Scheme. Similar to the hardware CC evaluation, the MIFARE Scheme also evaluates against high attack potential. Hence, systems using MIFARE SAM AV3 are reassured with the state-of-the-art security measures adopted by the industry.

Programmable Logic

The MIFARE SAM AV3 is equipped with a new Programmable Logic functionality which allows customers to flexibly create their business logic on the SAM. This new functionality opens up many new possibilities with the creation of project-specific customization such as a new key diversification algorithm, a new secure messaging, or a new secure storage.

X-mode communication

When used in combination with a reader IC supporting innovative "X" features, MIFARE SAM AV3 provides a significant boost in performance to the reader along with faster communication between reader and module. The "X" feature is a new way to use the SAM in a system, with SAM connected to the microcontroller and the reader IC simultaneously.

Secured communication

The connection between the SAM and the reader is performed using security protocols based on either AES symmetric cryptography or PKI RSA asymmetric cryptography. The protocols comply with the state-of-art standards and thereby ensure data confidentiality and integrity.

2 Features and benefits

2.1 Cryptography

- Supports MIFARE Crypto1, DES, TDEA (112 bits and 168 bits), AES (128 bits, 192 bits and 256 bits), RSA (up to 2048 bits) and ECC (up to 256 bits) cryptography
- Supported NXP products:
 - MIFARE DESFire EV3, EV2, EV1, and Light
 - MIFARE Plus EV2, EV1, X, S, and SE
 - MIFARE Classic EV1
 - MIFARE Ultralight AES, C and EV1



- NTAG, ICODE, and UCODE DNA
- Secure storage and updating of keys
 - 128 key entries for symmetric cryptography
 - 3 RSA key entries for asymmetric cryptography
 - 8 ECC public key entries for signature verification
 - 4 ECC curves entries
 - 48 EMV CA public key entries (supports 8 RID minimum)
- SHA-1, SHA-224 and SHA-256 hashing computation
- TDEA and AES-based key diversification
- Generic cryptography commands for user-defined schemes
- Supports EMVCo terminal functionality
- True random number generator (TRNG) compliant to AIS-31

2.2 Communication

- ISO/IEC 7816 (part 2 and 3) contact interface
 - Support Class A, B and C operating condition
 - Support ISO/IEC 7816 baud rates
 - Support high-speed baud rates up to 1.5 Mbit/s
- Optional I²C Target mode host interface (only available on HVQFN package)
- Communication protocol compliant with ISO/IEC 7816-3 T=1 protocol
- Up to four logical channels; simultaneous multiple card support
- Support for MIFARE DESFire and MIFARE Plus authentication (with related secure messaging and session key generation)
- Secure Host to SAM and back end to SAM communication with symmetric cryptography including 3-pass authentication for confidentiality and integrity
- Secure Host to SAM and back end to SAM communication with RSA-based cryptography for key updating
- X-mode direct interface with NXP's contactless reader ICs (RC663, RC52x, PN512)

2.3 Programmable logic (restricted feature) ²

- Up to 32 kB of code and data in EEPROM for user customized functionality
- 1 kB of RAM for user's dynamic data
- Internal Host access to all MIFARE SAM AV3 commands

2.4 Security evaluation and certification

- CC EAL6+ certified hardware platform (based on NXP's SmartMX2 P6022y VB)
- Composite certified with MIFARE Security Evaluation Scheme (Equivalent to EMVCo Security Evaluation) (Evaluation lab: TÜViT, Certification lab: UL)
- FIPS 140-2 CAVP certified

2.5 New features

This section gives an overview of the new features compared to MIFARE SAM AV2. Please see [\[1\]](#) for details.

- All new features from MIFARE DESFire EV2 requiring cryptographic operations. This includes EV2 secure messaging and Transaction MAC support (incl CommitReaderID).
- All new features from MIFARE Plus EV1 requiring cryptographic operations. This includes EV1 secure messaging, Transaction MAC support (incl CommitReaderID) and Sector Security Level Switching.
- New Virtual Card Selection and Proximity Check protocols.
- Post-Delivery Configuration support.
- MIFARE Ultralight EV1 password authentication.
- AES authentication according to ISO/IEC 29167-10 for UCODE and ICODE support.
- LRP support for DESFire secure messaging, as supported by DESFire Light and NTAG42x(TT) and for Offline Crypto operations.
- ECC originality signature verification as supported by all recent MIFARE products.
- Generic CMAC-based key derivation for a.o. Transaction MAC session key generation and (e.g. UCODE) key diversification.
- Fine-grained key access control.
- EMV terminal support for certificate verification, offline authentication and pin code verification.
- Programmable Logic feature to allow customized business logic and a.o. key diversifications to be run within the SAM.
- Personalization SAM feature to generate cryptogram to export keys for injection in another SAM for AES variant and for RSA variant.
- AES-256 support for Offline Crypto and SAM-Host protection.
- RSA OAEP encryption and decryption.
- ATR configuration.
- I²C target interface in addition to ISO/IEC 7816 interface (for HVQFN only).

² Note: The PL code uploading functionality is only available to a limited set of customers.

3 Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-------------------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------|----------|
| | Name | Description | Version |
| MF4SAM3U15/9BA659 | wafer unbumped | 150 µm thickness sawn wafer on film frame carrier (FFC) | NAU000 |
| MF4SAM3HN/9BA659 | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm; reel pack; minimum order quantity: 6.000 | SOT617-3 |
| MF4SAM3X84/9BA659 | PCM1.5 ^[1] | contact chip card module (super 35 mm tape format, 8 contact), minimum order quantity: 11.900 | SOT658-1 |

[1] NXP Semiconductors is ending the internal PCM1.5 manufacturing of 8-pin contact modules. For more information please contact your sales representative.

4 Block diagram

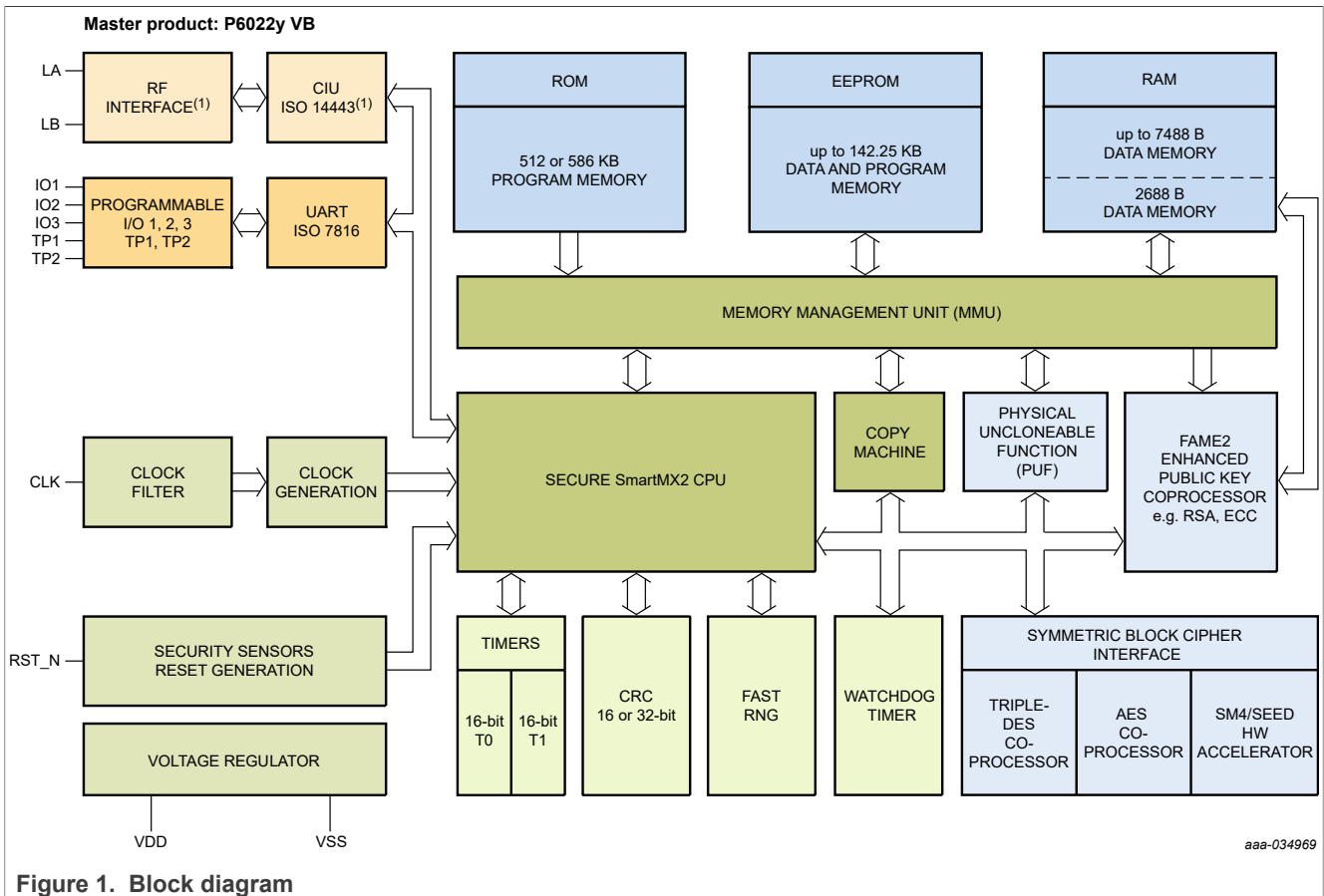


Figure 1. Block diagram

Table 3. Pin description HVQFN32 MIFARE SAM AV3

| Pad | Symbol | Description |
|-----|-----------------|-----------------------------------------------------------------------------------------------------------------|
| 1 | GND | ground (reference voltage) input |
| 3 | IO3 | used for I ² C communication to RC (SCL) |
| 5 | IO1 | input/output for serial data (ISO7816 or SDA_Target for I ² C host communication) |
| 7 | IO2 | used for I ² C communication to RC (SDA) |
| 24 | V _{CC} | power supply voltage input |
| 22 | RST_N | reset input, active LOW |
| 18 | CLK_N | clock input |
| 29 | TP2 | SCL_Target: used for I ² C communication to Host when I ² C host communication is enabled |
| 30 | TP1 | I2C_Enable: enable I ² C host communication when high |

6 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to VSS (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------------|---------------------------------------|----------------------------------------------------------|---------|-------------------------|------|
| V _{DD(AMR)} | supply voltage | | -0.5 | 6 | V |
| V _{I(AMR)} | input voltage | any signal pad | -0.5 | V _{DD} + 0.5 V | V |
| I _{I(AMR)} | input current | pads IO1, IO2, IO3 and TP1, TP2 | [1] - | ± 15 | mA |
| I _O | output current | pads IO1, IO2, IO3 and TP1, TP2 | [1] - | ± 15 | mA |
| I _{lu} | latch-up current | V _I < 0 V or V _I > V _{DD} | - | ± 100 | mA |
| V _{esd} | electrostatic discharge voltage (HBM) | pads VDD, VSS, CLK, RST_N, IO1, IO2, IO3 | [2] - | ± 4 | kV |
| | | TP1, TP2 | [3] - | ± 2 | kV |
| | electrostatic discharge voltage (CDM) | all pads | [4] - | ± 500 | V |
| P _{tot} | total power dissipation | | [5] - | 1 | W |
| T _{stg} | storage temperature | | [6] -55 | 125 | °C |

[1] If IO2 and IO3 are available.

[2] In accordance with ANSI/ESDA/JEDEC JS-001-2011, ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level.

[3] Only available if enabled via OEF setting.

[4] In accordance with JEDEC JESD22-C101 for Charged-Device Model (CDM).

[5] Depending on appropriate thermal resistance of the package.

[6] Depending on delivery type, refer to *NXP Semiconductors General Specification for 12" Wafers* (15) and to *NXP Semiconductors Contact & Dual Interface Chip Card Module Specification* (16).

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

7 Recommended operating conditions

Table 5. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|---------------------------------------------------------|-----------------------------------------------------------------|------|-----|-----------------|------|
| V _{DD} (5) | supply voltage ^[1] | Class A/5 V nominal supply voltage contact interface operation | 4.5 | 5 | 5.5 | V |
| V _{DD} (3) | | Class B/3 V nominal supply voltage contact interface operation | 2.7 | 3 | 3.3 | V |
| V _{DD} (1.8) | | Class C/1.8V nominal supply voltage contact interface operation | 1.62 | 1.8 | 1.98 | V |
| V _I | DC input voltage on digital inputs and digital I/O pads | - | 0 | - | V _{DD} | V |
| T _{amb} | operating ambient temperature ^[2] | | -25 | - | 85 | °C |

[1] All described supply voltages according to ISO/IEC 7816-3.

[2] All product properties and values specified within this data sheet are only valid within the operating ambient temperature range.

The supported operating supply voltage ranges limited by exception sensors covers the whole range of classes A, B and C. The Product Name devices operate within the full voltage range described in [Figure 4](#).

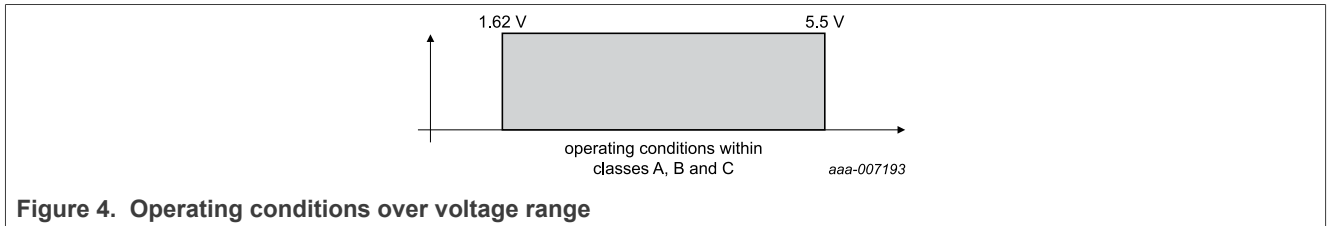


Figure 4. Operating conditions over voltage range

8 Static characteristics

8.1 Measurement conventions

Testing measurements are performed at the contact pads of the device under test. All voltages are defined with respect to the ground contact pad VSS. All currents flowing into the Smart Card IC are considered positive.

8.2 Levels and currents

Table 6. Electrical DC characteristics of Input/Output: IO1, IO2 and IO3

Conditions: $V_{DD} = 1.62\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|----------------------|---------------|
| V_{IH} | HIGH-level input voltage | | $0.7 \times V_{DD}$ | - | $V_{DD} + 0.3$ | V |
| V_{IL} | LOW-level input voltage | | -0.3 | - | $0.25 \times V_{DD}$ | V |
| I_{IH} | HIGH-level input current in "weak pull-up" input mode | $0.7 V_{DD} \leq V_I \leq V_{DD}$; Test conditions for the maximum absolute value: $I_{IH(max)}: V_I = 0.7 V_{DD}$, $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C | 0 | - | -20 | μA |
| I_{IL} | LOW-level input current | $0\text{ V} \leq V_I \leq 0.3 V_{DD}$; Test conditions for the maximum absolute value: $I_{IL(max)}: V_I = 0\text{ V}$, $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C | - | - | -50 | μA |
| I_{TL} | HIGH-to-LOW transition input current (only in "quasi-bidirectional" mode) | $0.3 V_{DD} < V_I \leq V_{DD}$; Test conditions for the maximum absolute value: $V_I = 0.5 V_{DD}$, $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C ^[1] | | | | |
| | | Class A | - | - | -300 | μA |
| | | Class B | - | - | -250 | μA |
| | | Class C | - | - | -200 | μA |
| I_I | input current in "weak pull-up" input mode | $0\text{ V} \leq V_I \leq V_{DD}$; Test conditions for the maximum absolute value: $I_{I(max)}: V_I = 0\text{ V}$, $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C | 0 | - | -50 | μA |
| I_{ILIH} | leakage input current at input voltage beyond V_{DD} in "weak pull-up" input mode | $V_{DD} < V_I \leq V_{DD} + 0.3\text{ V}$; $-25\text{ }^{\circ}\text{C} \leq T_{amb} \leq 85\text{ }^{\circ}\text{C}$; Test conditions: $V_I = V_{DD} + 0.3\text{ V}$; $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C; $T_{amb} = 85\text{ }^{\circ}\text{C}$ | - | - | 20 | μA |

Table 6. Electrical DC characteristics of Input/Output: IO1, IO2 and IO3...continued

Conditions: $V_{DD} = 1.62\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ °C to }85\text{ °C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|----------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-----|------------------------|------|
| I _{LIL} | leakage input current at input voltage below V _{SS} in "weak pull-up" input mode | -0.3 V ≤ V _I < 0 V; -25 °C ≤ T _{amb} ≤ 30 °C Test conditions: V _I = -0.3 V; V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C; T _{amb} = 30 °C | - | - | -50 | µA |
| | | -0.3 V ≤ V _I < 0 V; 30 °C < T _{amb} ≤ 85 °C Test conditions: V _I = -0.3 V; V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C; T _{amb} = 85 °C | - | - | -275 | µA |
| I _{LIHQ} | leakage input current at input voltage beyond V _{DD} (only in "quasi-bidirectional" mode) | V _{DD} < V _I ≤ V _{DD} + 0.3 V; -25 °C ≤ T _{amb} ≤ 85 °C Test conditions: V _I = V _{DD} + 0.3 V; V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C; T _{amb} = 85 °C | - | - | 100 | µA |
| I _{LILQ} | leakage input current at input voltage below V _{SS} (only in "quasi-bidirectional" mode) | -0.3 V ≤ V _I < 0 V; -25 °C ≤ T _{amb} ≤ 30 °C Test conditions: V _I = -0.3 V; V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C; T _{amb} = 30 °C | - | - | -75 | µA |
| | | -0.3 V ≤ V _I < 0 V; 30 °C < T _{amb} ≤ 85 °C Test conditions: V _I = -0.3 V; V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C; T _{amb} = 85 °C | - | - | -300 | µA |
| V _{OH} | HIGH-level output voltage | I _{OH} = -20 µA; Class A condition ^[2] | 3.8 0.7 × V _{DD} | - | - | V |
| | | I _{OH} = -20 µA; Class B or C condition ^[2] | 0.7 × V _{DD} | - | - | V |
| V _{OL} | LOW-level output voltage | Class A or B condition; I _{OL} = 1 mA | - | - | 0.3 | V |
| | | Class C condition; | | | | |
| | | I _{OL} = 1 mA | - | - | 0.3 | V |
| | | I _{OL} = 0.5 mA | - | - | 0.15 × V _{DD} | V |

[1] IO1, IO2 and IO3 source a transition current when being externally driven from HIGH to LOW. This transition current (I_{TL}) reaches its maximum value when the input voltage V_I is approximately 0.5 V_{DD}. Input current I_{TL} is tested at input voltage V_I = 0.5 V_{DD}. Current I_L is tested at input voltage V_I = 0.3 V. Figure 5 shows the input characteristic of this quasi-bidirectional port mode.

[2] External pull-up resistor 20 kΩ to V_{DD} assumed. The worst case test condition for parameter V_{OH} is present at minimum V_{DD}. For class A supply voltage conditions V_{DD} = 4.5 V is the worst case with respect to the fix specification limit V_{OHmin} = 3.8 V (0.844 V_{DD}). The supply voltage-related limit "0.7 V_{DD}" is a stricter requirement than the fix value 3.8 V at high V_{DD} values (0.7 V_{DD} = 3.85 V at V_{DD} = 5.5 V). So, in the V_{DD} range 4.5 V to 5.5 V, V_{OHmin} is specified

as "the larger value of 0.7 V_{DD} and 3.8 V, respectively". The V_{OHmin} value (0.7 V_{DD}) cannot be guaranteed in "quasi-bidirectional" mode at an output current of I_{OH} = -20 μA - the strong output drive mode must be used.

Table 7. Electrical DC characteristics of Inputs CLK and RST_N^{[1][2]}

Conditions: V_{DD} = 1.62 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -25 °C to 85 °C, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------------------------------------|---------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----|------------------------|------|
| Inputs CLK (when the IC is not in reset) and RST_N | | | | | | |
| V _{IH1} | HIGH-level input voltage | | 0.7 × V _{DD} | - | V _{DD} + 0.3 | V |
| V _{IL1} | LOW-level input voltage | | -0.3 | - | 0.25 × V _{DD} | V |
| I _{IH1} | HIGH-level input current (weak pull-down is on) | 0.7 V _{DD} ≤ V _I ≤ V _{DD} ; Test conditions for the maximum absolute value: I _{IH1(max)} : V _I = V _{DD} , V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C | - | - | 20 | μA |
| I _{IL1} | LOW-level input current (weak pull-down is on) | 0 V ≤ V _I ≤ 0.3 V _{DD} ; Test conditions for the maximum absolute value: I _{IL1(max)} : V _I = 0.3 V _{DD} , V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C | 0 | - | 20 | μA |
| I _{I1} | input current (weak pull-down is on) | 0 V ≤ V _I ≤ V _{DD} ; Test conditions for the maximum absolute value: I _{I1(max)} : V _I = V _{DD} , V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C | 0 | - | 20 | μA |
| I _{ILIH1} | leakage input current at input voltage beyond V _{DD} | V _{DD} < V _I ≤ V _{DD} + 0.3 V; -25 °C ≤ T _{amb} ≤ 85 °C Test conditions: V _I = V _{DD} + 0.3 V; V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C; T _{amb} = 85 °C | - | - | 20 | μA |
| I _{ILIL1} | leakage input current at input voltage below V _{SS} | -0.3 V ≤ V _I < 0 V; -25 °C ≤ T _{amb} ≤ 30 °C Test conditions: V _I = -0.3 V; V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C; T _{amb} = 30 °C | - | - | -50 | μA |
| | | -0.3 V ≤ V _I < 0 V; 30 °C < T _{amb} ≤ 85 °C Test conditions: V _I = -0.3 V; V _{DD} = V _{DD(max)} of the respective supply voltage class A, B or C; T _{amb} = 85 °C | - | - | -200 | μA |

Table 7. Electrical DC characteristics of Inputs CLK and RST_N^{[1][2]}...continued

Conditions: $V_{DD} = 1.62\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ °C to }85\text{ °C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------|--------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|----------------------|---------------|
| Input CLK (during IC reset) | | | | | | |
| V_{IH2} | HIGH-level input voltage | | $0.7 \times V_{DD}$ | - | $V_{DD} + 0.3$ | V |
| V_{IL2} | LOW-level input voltage | | -0.3 | - | $0.25 \times V_{DD}$ | V |
| I_{IH2} | HIGH-level input current (weak pull-up is on) | $0.7 V_{DD} \leq V_I \leq V_{DD}$; Test conditions for the maximum absolute value: $I_{IH2(max)}: V_I = 0.7 V_{DD}$, $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C | 0 | - | -20 | μA |
| I_{IL2} | HIGH-level input current (weak pull-up is on) | $0\text{ V} \leq V_I \leq 0.3 V_{DD}$; Test conditions for the maximum absolute value: $I_{IL2(max)}: V_I = 0\text{ V}$, $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C | - | - | -20 | μA |
| I_{I2} | input current (weak pull-up is on) | $0\text{ V} \leq V_I \leq V_{DD}$; Test conditions for the maximum absolute value: $I_{I2(max)}: V_I = 0\text{ V}$, $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C | 0 | - | -20 | μA |
| I_{ILIH2} | leakage input current at input voltage beyond V_{DD} | $V_{DD} < V_I \leq V_{DD} + 0.3\text{ V}$; $-25\text{ °C} \leq T_{amb} \leq 85\text{ °C}$ Test conditions: $V_I = V_{DD} + 0.3\text{ V}$; $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C; $T_{amb} = 85\text{ °C}$ | - | - | 20 | μA |
| I_{ILIL2} | leakage input current at input voltage below V_{SS} | $-0.3\text{ V} \leq V_I < 0\text{ V}$; $-25\text{ °C} \leq T_{amb} \leq 30\text{ °C}$ Test conditions: $V_I = -0.3\text{ V}$; $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C; $T_{amb} = 30\text{ °C}$ | - | - | -50 | μA |
| | | $-0.3\text{ V} \leq V_I < 0\text{ V}$; $30\text{ °C} < T_{amb} \leq 85\text{ °C}$ Test conditions: $V_I = -0.3\text{ V}$; $V_{DD} = V_{DD(max)}$ of the respective supply voltage class A, B or C; $T_{amb} = 85\text{ °C}$ | - | - | -200 | μA |

[1] The active low RST_N input and outside reset state also the CLK input internally activate a resistive pull-down device to VSS. Accordingly a current is flowing into the pad at voltages above 0 V. Figure 7 shows this input characteristic. In CLOCKSTOP mode the preferred electrical state on CLK is a LOW level, in order to minimize the power consumption.

[2] The CLK input internally has a resistive pull-up device to VDD activated during IC reset. Accordingly a current is flowing out of the pad at voltages below V_{DD} . Figure 8 shows this input characteristic.

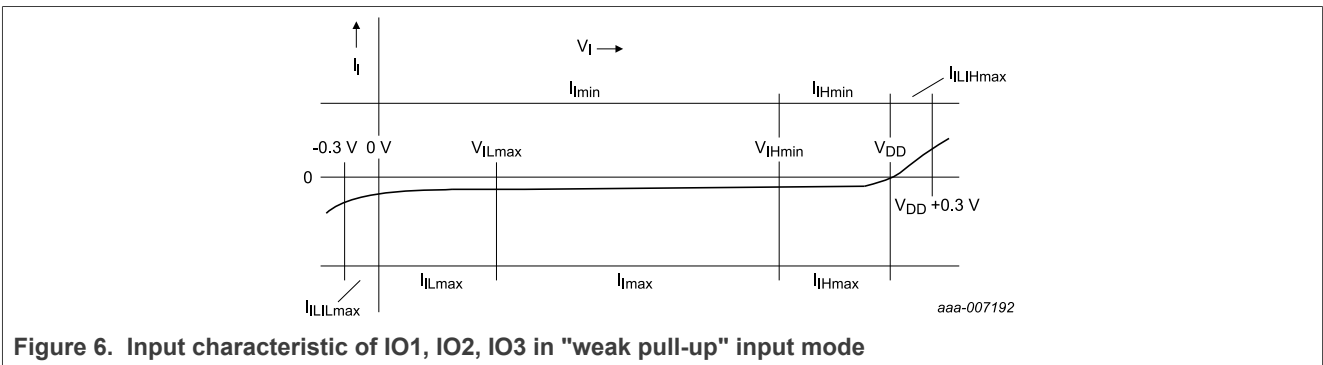
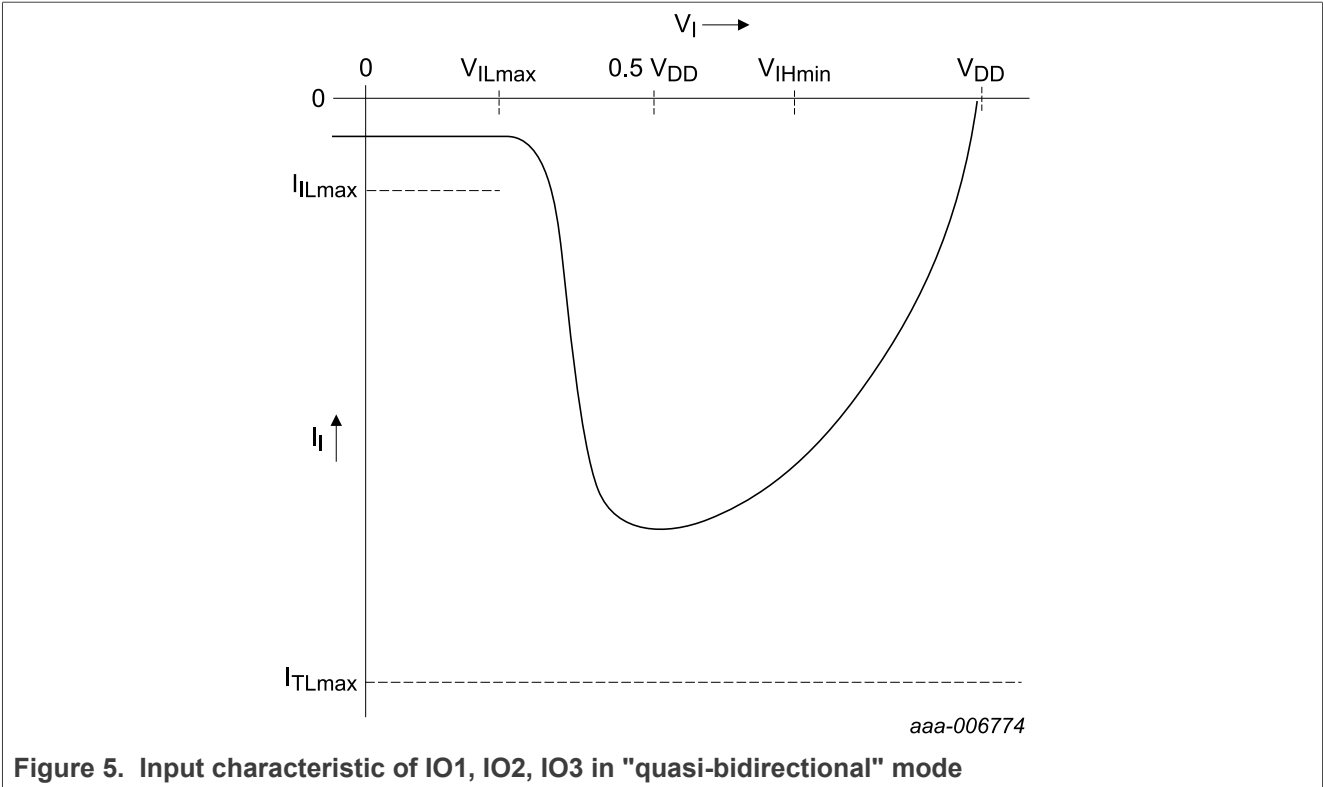
Table 8. Electrical DC characteristics of TP1 and TP2

Conditions: (A) $V_{DD} = 1.62\text{ V to }1.98\text{ V}$; $V_{DDAE} = V_{DD}$;

(B) $V_{DD} = 2.2\text{ V to }5.5\text{ V}$ (that is outside Class C supply range); $V_{DDAE(NOM)} = 1.8\text{ V}$;

$V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ }^\circ\text{C to }85\text{ }^\circ\text{C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|-----|---------------------------|---------------|
| V_{IHT} | HIGH-level input voltage | | $0.7 \times V_{DDAE}$ | - | $V_{DDAE} + 0.3\text{ V}$ | V |
| V_{ILT} | LOW-level input voltage | | -0.3 | - | $0.25 \times V_{DDAE}$ | V |
| I_{IHD} | HIGH-level input current maximum (resistive pull-down is on) | $0.7 V_{DDAE} \leq V_I \leq V_{DDAE}$; Test conditions for the maximum absolute value: $V_I = V_{DDAE}$; $V_{DDAE} = V_{DDAE(max)}$; for the minimum absolute value: $V_I = 0.7 V_{DDAE}$; $V_{DDAE} = V_{DDAE(min)}$ | 10 | - | 100 | μA |
| I_{ILD} | LOW-level input current maximum (resistive pull-down is on) | $0\text{ V} \leq V_I \leq 0.3 V_{DDAE}$; Test conditions for the maximum absolute value: $V_I = 0.3 V_{DDAE}$; $V_{DDAE} = V_{DDAE(max)}$; | 0 | - | 20 | μA |
| I_{ILIH3} | leakage input current at input voltage beyond V_{DDAE} (resistive pull-down is on) | $V_{DDAE} < V_I \leq V_{DDAE} + 0.3\text{ V}$; $-25\text{ }^\circ\text{C} \leq T_{amb} \leq 85\text{ }^\circ\text{C}$; Test conditions: $V_I = 2.3\text{ V}$; $T_{amb} = 85\text{ }^\circ\text{C}$ | - | - | 150 | μA |
| I_{ILIL3} | leakage input current at input voltage beyond V_{SS} (resistive pull-down is on) | $-0.3\text{ V} \leq V_I < 0\text{ V}$; $-25\text{ }^\circ\text{C} \leq T_{amb} \leq 30\text{ }^\circ\text{C}$; Test conditions: $V_I = -0.3\text{ V}$; $T_{amb} = 30\text{ }^\circ\text{C}$ | 0 | - | -150 | μA |
| | | $-0.3\text{ V} \leq V_I < 0\text{ V}$; $30\text{ }^\circ\text{C} < T_{amb} \leq 85\text{ }^\circ\text{C}$; Test conditions: $V_I = -0.3\text{ V}$; $T_{amb} = 85\text{ }^\circ\text{C}$ | - | - | -300 | μA |
| V_{OH2} | HIGH-level output voltage | $I_{OH2} = -0.1\text{ }\mu\text{A}$ | $V_{DDAE} - 0.3\text{ V}$ | - | - | V |
| V_{OL2} | LOW-level output voltage | $I_{OL2} = 1.2\text{ }\mu\text{A}$ | - | - | 0.3 | V |



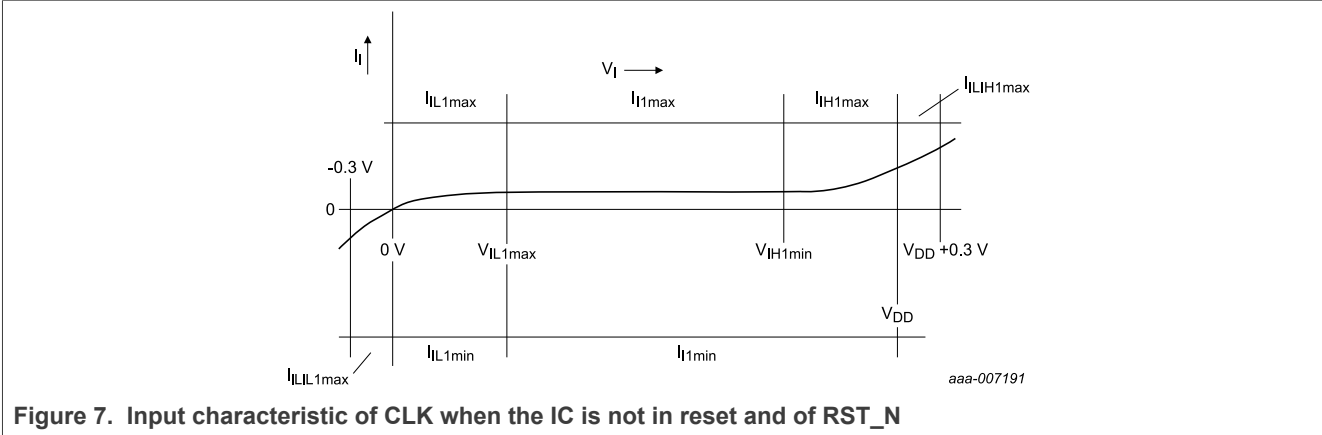


Figure 7. Input characteristic of CLK when the IC is not in reset and of RST_N

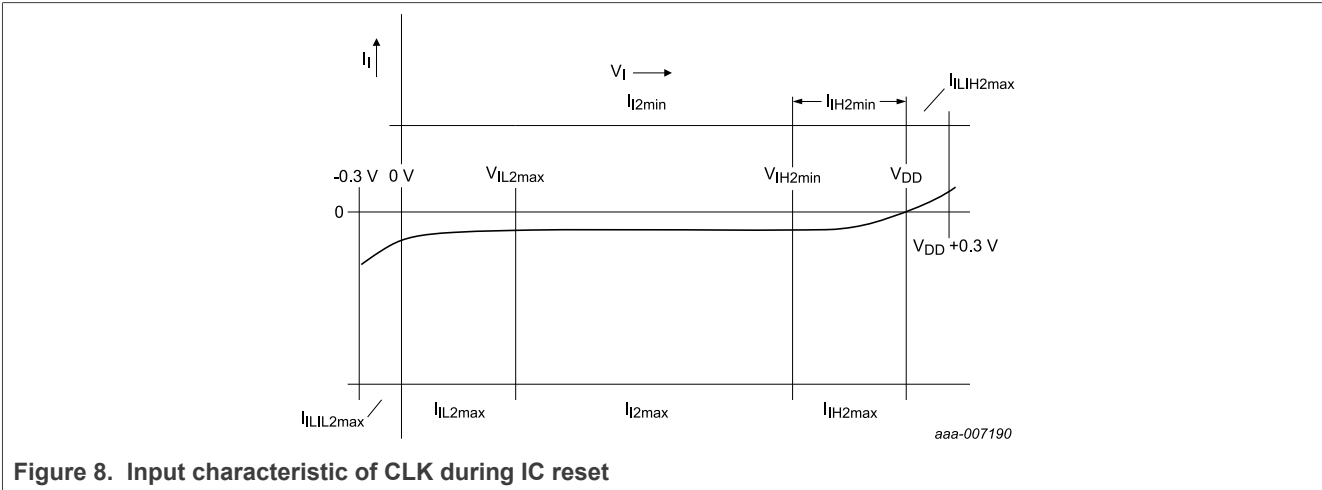


Figure 8. Input characteristic of CLK during IC reset

8.3 General and ISO/IEC 7816 I/O interface at ISO/IEC 7816-3: A/5 V, class B/3 V or class C/1.8 V class operation

Table 9. Electrical characteristics of IC supply current^[1]

Conditions: $V_{DD} = 1.62\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Supply voltage class | Min | Typ | Max | Unit |
|------------------------------------|-------------------------------|-----------------------------------------|----------------------|------|-----|------|------|
| Supply | | | | | | | |
| V_{DD} | supply voltage range | Class A: 5 V range | A (5 V) | 4.5 | 5 | 5.5 | V |
| | | Class B: 3 V range | B (3 V) | 2.7 | 3 | 3.3 | V |
| | | Class C: 1.8 V range | C (1.8 V) | 1.62 | 1.8 | 1.98 | V |
| operating mode: Reset State | | | | | | | |
| I_{DD} | supply current operating mode | $f_{CLK} = 10\text{ MHz}$, RESET state | A (5 V) | - | 1.2 | 4 | mA |
| | | | B (3 V) C (1.8 V) | | | | |
| operating mode: typical CPU | | | | | | | |

Table 9. Electrical characteristics of IC supply current^[1] ...continued

Conditions: $V_{DD} = 1.62\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ °C to }85\text{ °C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Supply voltage class | Min | Typ | Max | Unit |
|---------------|----------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|-----|------|------|---------------|
| | no coprocessor active | $f_{CLK} = 10\text{ MHz}$, CPU at f_{CLK} | A (5 V) B (3 V) C (1.8 V) | - | 1.6 | 4 | mA |
| | no coprocessor active | $f_{CLK} = 10\text{ MHz}$, CPU in free running mode | A (5 V) B (3 V) C (1.8 V) | - | 2.5 | 4 | mA |
| | DES coprocessor active (DES int. 32 MHz) | $f_{CLK} = 10\text{ MHz}$, CPU at int. 4 MHz | A (5 V) B (3 V) C (1.8 V) | - | 4 | 6 | mA |
| | DES coprocessor active (DES int. 96 MHz) | $f_{CLK} = 10\text{ MHz}$, CPU at int. 4 MHz | A (5 V) B (3 V) C (1.8 V) | - | 8.6 | 10.5 | mA |
| | AES coprocessor active (AES int. 32 MHz) | $f_{CLK} = 10\text{ MHz}$, CPU at int. 4 MHz | A (5 V) B (3 V) C (1.8 V) | - | 3.1 | 5 | mA |
| | AES coprocessor active (AES int. 96 MHz) | $f_{CLK} = 10\text{ MHz}$, CPU at int. 4 MHz | A (5 V) B (3 V) C (1.8 V) | - | 5.6 | 8 | mA |
| | Fame2 coprocessor active (Fame2 clock = 16 MHz, double multiplier mode) | $f_{CLK} = 10\text{ MHz}$, CPU at int. 4 MHz | A (5 V) B (3 V) C (1.8 V) | - | 3.9 | 6.5 | mA |
| | Fame2 coprocessor active (Fame2 clock = 48 MHz, double multiplier mode) | $f_{CLK} = 10\text{ MHz}$, CPU at int. 4 MHz | A (5 V) B (3 V) C (1.8 V) | - | 5.4 | 8.5 | mA |
| | Fame2 coprocessor active (Fame2 clock = free running, double multiplier mode) | $f_{CLK} = 10\text{ MHz}$, CPU at int. 4 MHz | A (5 V) B (3 V) C (1.8 V) | - | 5.4 | 10.5 | mA |
| $I_{DD(ID)}$ | supply current CPU IDLE mode (this parameter should not be mixed-up with the ETSI "idle state") | $f_{CLK} = 10\text{ MHz}$, $T_{amb} = 25\text{ °C}$ | A (5 V) B (3 V) C (1.8 V) | - | 0.8 | 1.5 | mA |
| $I_{DD(SLP)}$ | supply current SLEEP mode (this parameter should not be mixed-up with the ETSI "idle state") | $f_{CLK} = 10\text{ MHz}$, $T_{amb} = 25\text{ °C}$ (VDDCO power domain switched off) | A (5 V) | - | 175. | 200 | μA |
| | | | B (3 V) | - | 150 | | μA |
| | | | C (1.8 V) | | | | |
| $I_{DD(PD)}$ | supply current CLO CKSTOP mode | $V_{DDmin} \leq V_{DD} \leq V_{DDmax}$; Clock to input CLK stopped, $T_{amb} = 25\text{ °C}$ (VDDCO power domain and CLIF switched off) | A (5 V) | - | 80 | 200 | μA |
| | | | B (3 V) | - | 60 | 100 | μA |
| | | | C (1.8 V) | | | | |

[1] Typical values are only referenced for information. They are subject to change without notice.

9 Dynamic characteristics

Remark: The P6022y VB only supports one single IO1.

9.1 General, ISO/IEC 7816 I/O and ISO/IEC 14443 I/O interfaces

Table 10. Electrical AC characteristics of IO1, IO2, IO3, CLK and RST_N

Conditions: $V_{DD} = 1.62\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit | |
|------------------------------------------|--------------------------------------------------------------------------|----------------------------------------------------------------|-----|--------------------|-----------------------------|---------------|---------------|
| Input/Output: IO1, IO2 and IO3 | | | | | | | |
| $t_{r(i)}$ | Input rise time | Input/reception mode | [2] | - | 1 | μs | |
| | | | [3] | - | $0.25 \times t_{IOWx_min}$ | μs | |
| $t_{f(i)}$ | Input fall time | Input/reception mode | [2] | - | 1 | μs | |
| | | | [3] | - | $0.25 \times t_{IOWx_min}$ | μs | |
| $t_{r(o)}$ | Output rise time | Output/transmission mode; $C_L = 30\text{ pF}$ | - | - | 0.1 | μs | |
| $t_{f(o)}$ | Output fall time | Output/transmission mode; $C_L = 30\text{ pF}$ | - | - | 0.1 | μs | |
| Inputs: CLK and RST_N | | | | | | | |
| f_{CLK} | External clock frequency in ISO/IEC 7816 UART applications | t_{CLKW} , T_{amb} and V_{DD} in their spec'd limits | [4] | 0.85 | - | 11.5 | MHz |
| t_{CLKW} | Clock pulse width i.r.t. clock period (positive pulse duty cycle of CLK) | | [5] | 40 | - | 60 | % |
| $t_{r(i)CLK}$ | CLK input rise time | | [6] | - | - | see [6] | |
| $t_{f(i)CLK}$ | CLK input fall time | | [6] | - | - | see [6] | |
| $t_{r(i)RST}$ | RST_N input rise time | | [7] | - | - | 400 | μs |
| $t_{f(i)RST}$ | RST_N input fall time | | [7] | - | - | 400 | μs |
| t_{RW} | Reset pulse width (RST_N low) | | | 40 | - | - | μs |
| t_{WKP} | Wake-up time from SLEEP mode | $f_{CLKmin} \leq f_{CLK} \leq f_{CLKmax}$ | | - | 17 | 20 | μs |
| t_{WKPIO} | I/Ox LOW time for wake-up from SLEEP mode | level triggered ext.int. | | - | 20 | - | μs |
| | | edge triggered ext.int. | | - | 20 | - | μs |
| t_{WKPRST} | RST_N LOW time for wake-up from SLEEP mode | | | 40 | - | - | μs |
| Inputs: CLK, RST_N, IO1, IO2, IO3 | | | | | | | |
| C_{PIN} | Pin capacitances CLK, RST_N, IO1, IO2, IO3 | Test frequency = 1 MHz; $T_{amb} = 25\text{ }^{\circ}\text{C}$ | | - | - | 10 | pF |

[1] Typical values are only referenced for information. They are subject to change without notice.

[2] At minimum IOx input signal HIGH or LOW level voltage pulse width of 3.2 μs . This timing specification applies to ISO7816 configurations down to a minimum etu duration of 16 CLK cycles at a maximum CLK frequency of 5 MHz ($TA1 = 0x96$, $(Fi/Di) = (512/32)$), for example.

[3] At minimum IOx input signal HIGH or LOW level voltage pulse width of less than 3.2 μs . This timing specification applies to ISO7816 configurations beyond the conditions listed in note [2], down to a minimum etu duration of 8 CLK cycles at a maximum CLK frequency of 5 MHz ($TA1=0x97$, $(Fi/$

- $D_i)=(512/64))$, for example. An 8 CLKs/etu at $f_{clk} = 5$ MHz configuration results in $t_{IO_{Wx_min}} = 1.6 \mu s$, and in a time of 400 ns for t_{rIO_max} and t_{fIO_max} , matching the $(F_i/D_i)=(512/64)$ speed enhancement requirements of ETSI TS 102 221.
- [4] ISO/IEC 7816 I/O applications have to supply a clock signal to input CLK in the frequency range of 1 MHz to 10 MHz nominal. A $\pm 15\%$ tolerance range yields the allowed limits of 0.85 MHz and 11.5 MHz.
 - [5] During AC testing the inputs CLK, RST_N, IO1, IO2 and IO3 are driven at 0 V to 0.3 V for a LOW input level and at $V_{DD} - 0.3$ V to V_{DD} for a HIGH input level. Clock period and signal pulse (duty cycle) timing is measured at 50 % of V_{DD} (see Figure 9).
 - [6] The maximum CLK rise and fall time are 10 % of the CLK period $1/f_{CLK}$ - with the following exception: In the CLK frequency range of 1 MHz to 5 MHz the maximum allowed CLK rise and fall time is 50 ns, if 10 % of the CLK period is shorter than 50 ns.
 - [7] The ETSI TS102 221/GSM 11.1x specifications specify a maximum reset signal (RST_N) rise time and fall time of 400,000 μs , respectively.

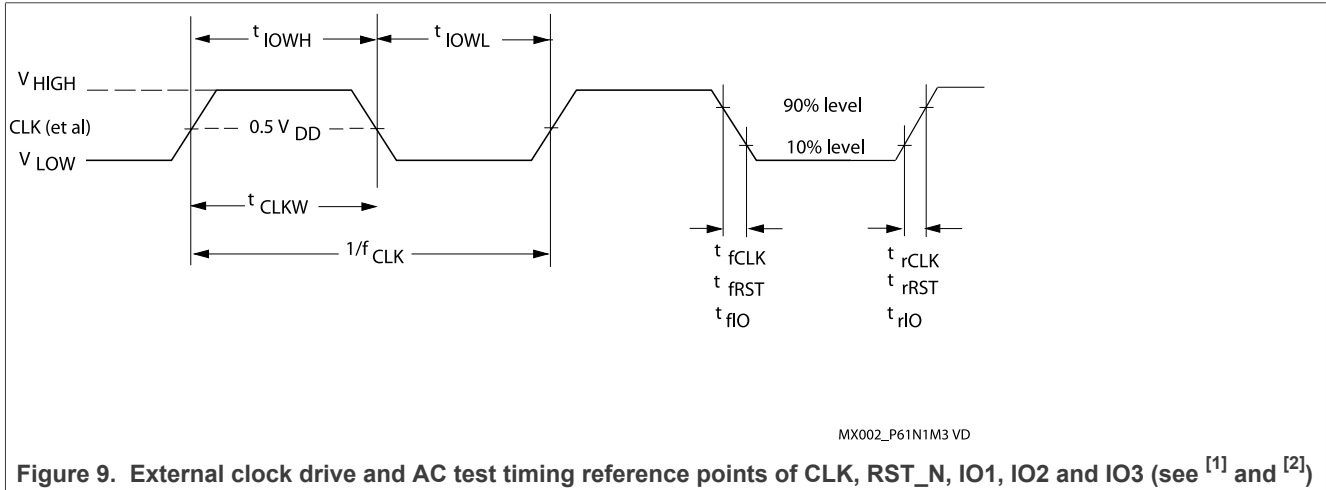


Figure 9. External clock drive and AC test timing reference points of CLK, RST_N, IO1, IO2 and IO3 (see [1] and [2])

- [1] During AC testing the inputs CLK, RST_N, IO1, IO2 and IO3 are driven at 0 V to 0.3 V for a LOW input level and at $V_{DD} - 0.3$ V to V_{DD} for a HIGH input level. Clock period and signal pulse (duty cycle) timing is measured at 50 % of V_{DD} .
- [2] t_r is defined as rise time between 10 % and 90 % of the signal amplitude.
 t_f is defined as fall time between 90 % and 10 % of the signal amplitude.

Table 11. Electrical AC characteristics of TP1 and TP2

Conditions: (A) $V_{DD} = 1.62$ V to 1.98 V; $V_{DDAE} = V_{DD}$; (B) $V_{DD} = 2.2$ V to 5.5 V (that is outside Class C supply range): $V_{DDAE}(nom) = 1.8$ V; $V_{SS} = 0$ V; $T_{amb} = -25$ °C to 85 °C, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|------------------------------|-----------------------------------------------|-----|-----|-----|---------|
| t_{rTP} | TP input rise time | Input/reception mode | - | - | 1 | μs |
| t_{fTP} | TP input fall time | Input/reception mode | - | - | 1 | μs |
| t_{rOTP} | TP output rise time | Output/transmission mode; $C_L = 30$ pF | - | - | 50 | ns |
| t_{fOTP} | TP output fall time | Output/transmission mode; $C_L = 30$ pF | - | - | 50 | ns |
| C_{iTP} | Pin characteristics TP1, TP2 | Test frequency = 1 MHz; $T_{amb} = -25$ °C | - | - | 15 | pF |

9.2 Non-Volatile memory

Table 12. Non-volatile memory characteristics

Conditions: $V_{DD} = 1.62\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--------------------|-------------------------------------------------------------------------------------------|--------------------------|----------------------|-----------------------|-----|--------|
| t _{EEP} | EEPROM erase/program time | [2] | - | 2 | - | ms |
| t _{EEE} | EEPROM erase time | | - | 1.25 | - | ms |
| t _{EEW} | EEPROM program time | | - | 0.75 | - | ms |
| t _{EEER} | EEPROM data retention time | T _{amb} = 55 °C | 25 | - | - | years |
| N _{EEEC} | EEPROM endurance (number of programming cycles) | | 5 × 10 ⁵ | - | - | cycles |
| N _{EEECM} | EEPROM endurance (maximum number of programming cycles applied to the whole memory block) | | 20 × 10 ⁶ | 100 × 10 ⁶ | - | cycles |

[1] Typical values are only referenced for information. They are subject to change without notice.

[2] Given value specifies physical access times of EEPROM memory only.

9.3 I²C Target interface bus timing

Table 13. Non-volatile memory characteristics

Conditions: $V_{DD} = 1.62\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -25\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|--------------------------------------------------|-------------------------------------------------------|------|------|------|
| f _{SCL} | SCL clock frequency | | 0 | 350 | kHz |
| t _{HD,STA} | hold time (repeated) START condition | after this period, the first clock pulse is generated | 4000 | - | ns |
| t _{SU,STA} | set-up time for a repeated START condition | | 4700 | - | ns |
| t _{SU,STO} | set-up time for STOP condition | | 4000 | - | ns |
| t _{LOW} | LOW period of the SCL clock | | 1400 | - | ns |
| t _{HIGH} | HIGH period of the SCL clock | | 1400 | - | ns |
| t _{HD,DAT} | data hold time | | 300 | 3450 | ns |
| t _{SU,DAT} | data set-up time | | 250 | - | ns |
| t _{VD,DAT} | data valid time | | - | 3450 | ns |
| t _{VD,ACK} | data valid acknowledge | | - | 3450 | ns |
| t _r | rise time | SDA and SCL signals | - | 1000 | ns |
| t _f | fall time | SDA and SCL signals | - | 300 | ns |
| t _{BUF} | bus free time between a STOP and START condition | | 4700 | - | ns |

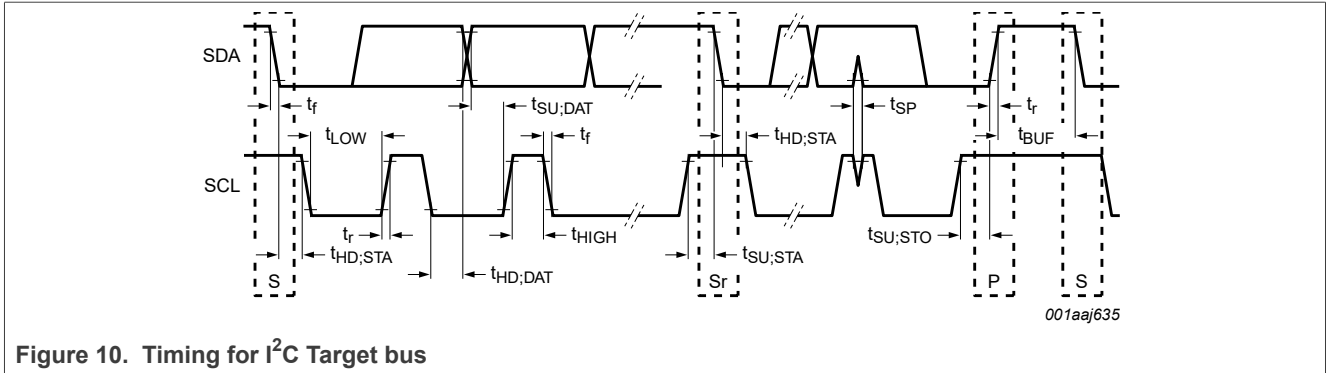


Figure 10. Timing for I²C Target bus

10 Package outline

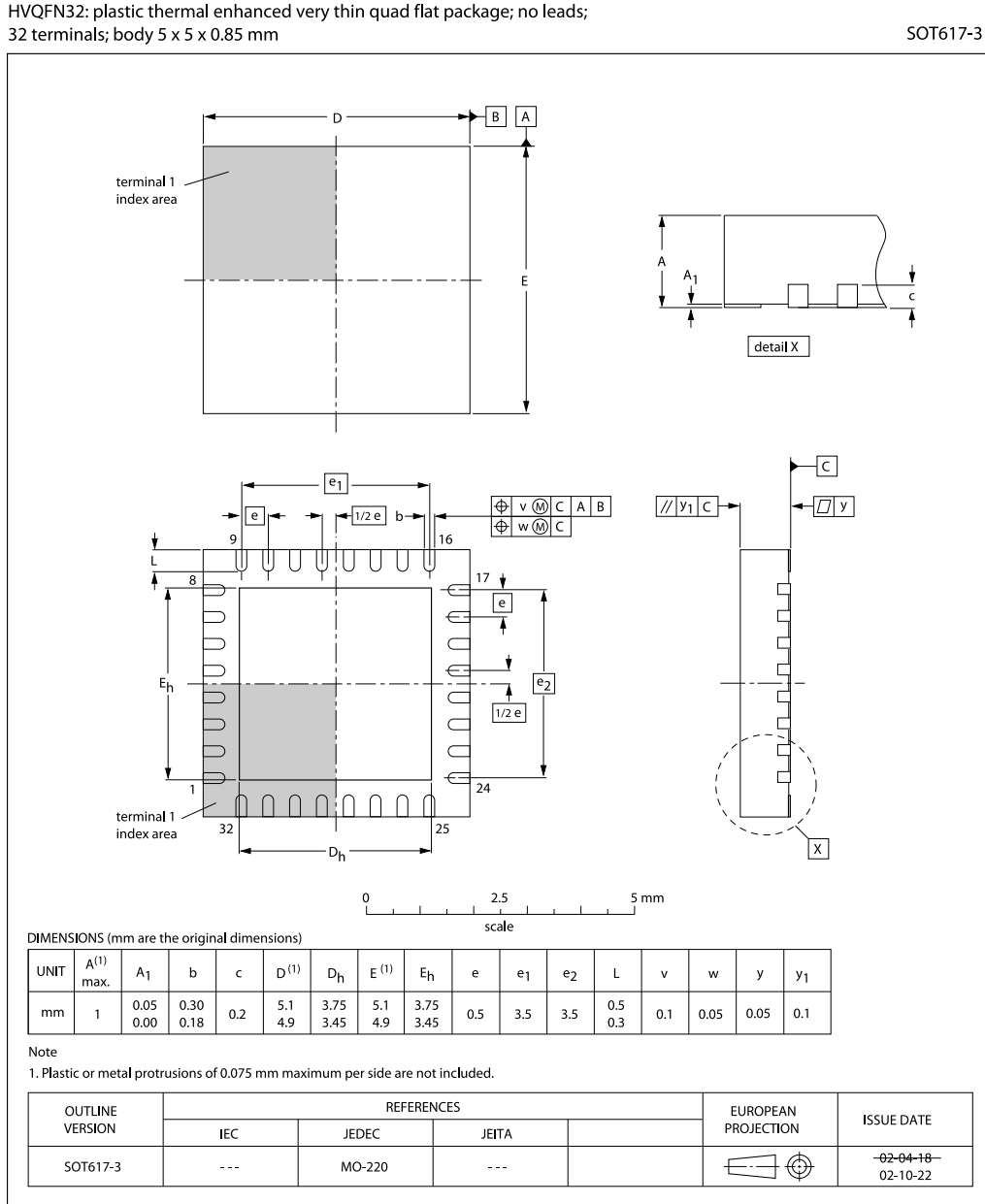
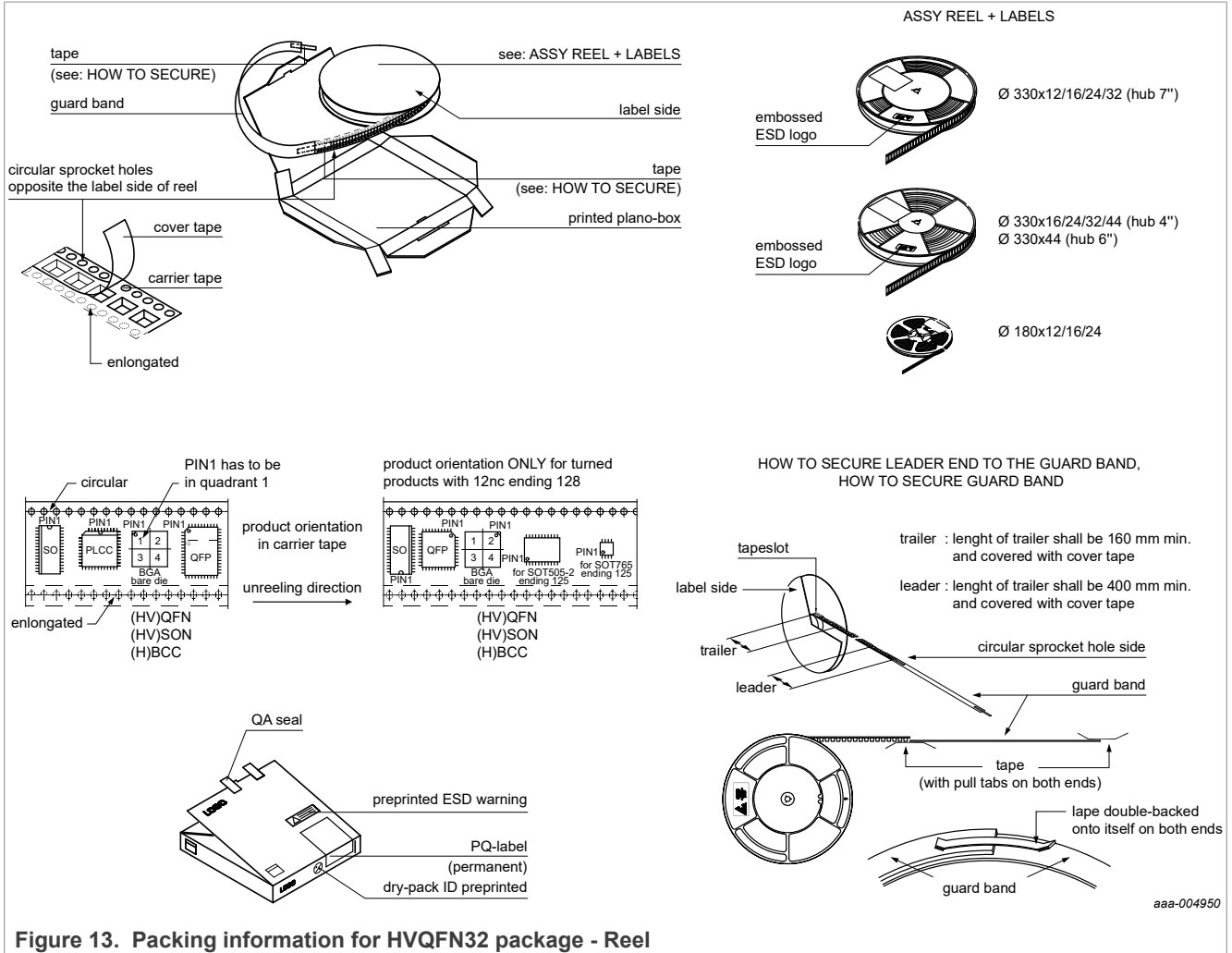


Figure 11. Package outline SOT617-3

11 Packing information



12 References

- [1] Data sheet — MF4SAM3 MIFARE SAM AV3 secure access module, Product data sheet, Doc No. 3235**³

3 ** denote the document version number

13 Revision history

Table 14. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|---------------|-------------------|
| MF4SAM3X_SDS v.3.2 | 05 March 2024 | Product short data sheet | - | MF4SAM3_SDS v.3.1 |
| Modifications: | <ul style="list-style-type: none"> • updated Legal information • Updated the terms "master/slave" to "controller/target" throughout to align with MIPI I3C specification and NXP's Inclusive Language Project • corrected the notation of I²C throughout the document • updated the list of supported NXP products at Section 2.1 | | | |
| MF4SAM3X_SDS v.3.1 | 01 July 2023 | Product short data sheet | - | MF4SAM3_SDS v.3.0 |
| Modifications: | <ul style="list-style-type: none"> • Type number updated in the Section 3 "Ordering information" improving the product robustness in handling unstable power supply operating condition. No functional changes. All features as specified in the data sheet are the same. | | | |
| MF4SAM3_SDS v.3.0 | 02 August 2019 | Product short data sheet | - | -- |
| Modifications: | <ul style="list-style-type: none"> • Initial released version | | | |

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| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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