THE DATASHEET OF

ESD200B1CSP0201XTSA1

ESD200-B1-CSP0201

Protection device

TVS (transient voltage suppressor)
Bi-directional, 5.5 V, 6.5 pF, 0201, RoHS and halogen free compliant

Feature list

- ESD/transient protection of data lines according to:
  - IEC61000-4-2 (ESD): ±19 kV (air), ±17 kV (contact discharge)
  - IEC61000-4-4 (EFT): ±2 kV/±40 A (5/50 ns)
  - IEC61000-4-5 (Surge): ±3 A (8/20 µs)
- Bi-directional working voltage up to: V_{RWM} = ±5.5 V
- Line capacitance: C_L = 6.5 pF (typical) at f = 1 MHz
- Clamping voltage: V_{CL} = 13 V (typical) at I_{TLP} = 16 A with R_{DYN} = 0.2 Ω (typical)
- Very low reverse current: I_R < 1 nA (typical)
- Minimized clamping overshoot due to extremely low parasitic inductance
- Small form factor SMD size 0201, low profile (0.58 mm x 0.28 mm x 0.15 mm) ***[3]***
- Bi-directional and symmetric I/V characteristic for optimized design and assembly, recommendations for PCB assembly see ***[2]***

Potential applications

- ESD protection of highly susceptible IC/ASICs in audio, headset and human digital interfaces

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

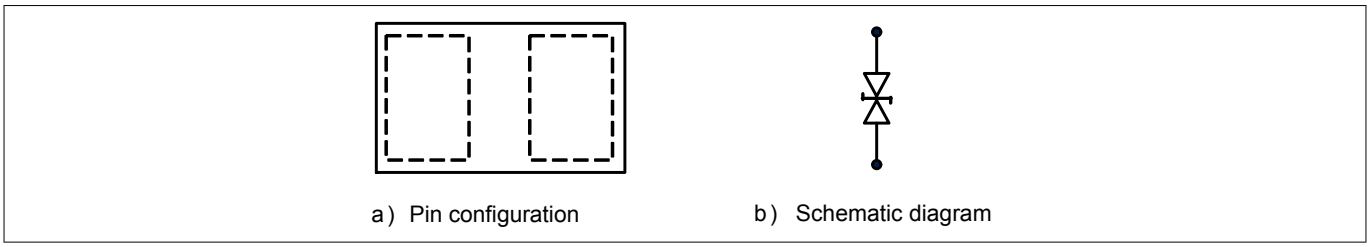

Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
ESD200-B1-CSP0201	WLL-2-1	1 line, bi-directional	A [1)]

1 The device has no marking code on the device backside. The marking code is on pad side.

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1 Maximum ratings

Note: T_A = 25 °C, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values	Unit
Reverse working voltage	V_{RWM}	±5.5	V
ESD discharge [1)]	V_{ESD} (contact)	±17	kV
	V_{ESD} (air)	±19	
Peak pulse power [2)]	P_{PK}	45	W
Peak pulse current [2)]	I_{PP}	±3	A
Operating temperature range	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

Attention: ***Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.***

1 V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF discharge network)
2 Stress pulse: 8/20 µs current waveform according to IEC61000-4-5

2 Electrical characteristics

Note: *T_A = 25 °C, unless otherwise specified. Device is electrically symmetrical.*

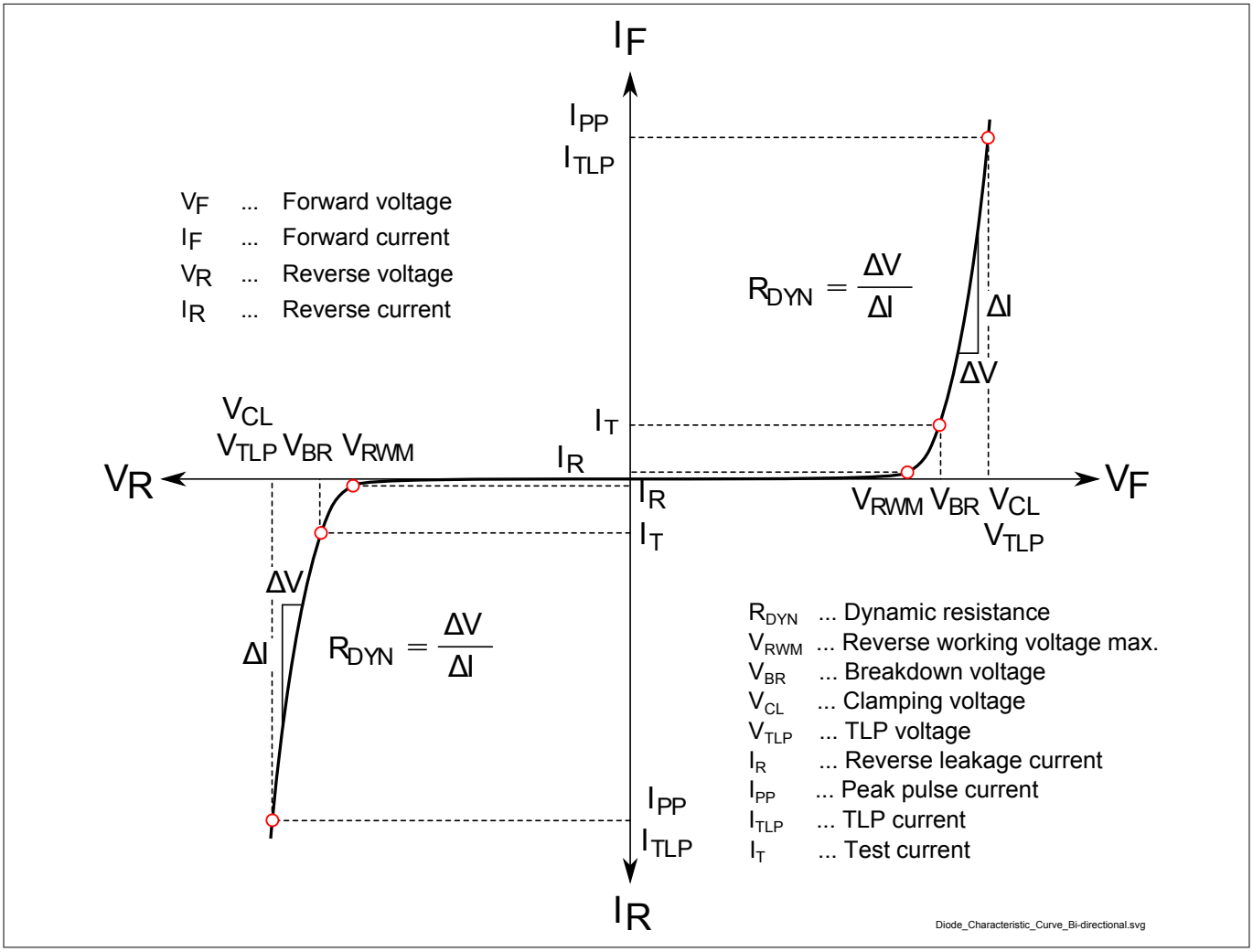

Figure 2 Definitions of electrical characteristics

Electrical characteristics

Table 3 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Breakdown voltage	V_{BR}	6	–	10	V	I_T = 1 mA
Reverse current	I_R	–	0.1	100	nA	V_R = 5.5 V

Table 4 AC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	6.5	–	pF	V_R = 0 V, f = 1 MHz
		–	6.5	–		V_R = 0 V, f = 1 GHz

Table 5 ESD and Surge characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Clamping voltage [1)]	V_{CL}	–	12	–	V	V_{ESD} = 8 kV, contact discharge
Clamping voltage[2)]		–	10	–		I_{TLP} = 1 A, t_p = 100 ns
		–	13	–		I_{TLP} = 16 A, t_p = 100 ns
Clamping voltage [3)]		–	10	–		I_{PP} = 1 A, t_p = 8/20 µs
		–	12.5	–		I_{PP} = 3 A, t_p = 8/20 µs
Dynamic resistance [2)]	R_{DYN}	–	0.2	–	Ω	t_p = 100 ns

1 V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF discharge network)
2 Please refer to application note AN210 *[1]*, TLP parameters: Z_0 = 50 Ω , t_p = 100 ns, t_r = 0.6 ns
3 Stress pulse: 8/20 µs current waveform according to IEC61000-4-5

3 Typical characteristic diagrams

Note: $T_A = 25$ °C, *unless otherwise specified.*

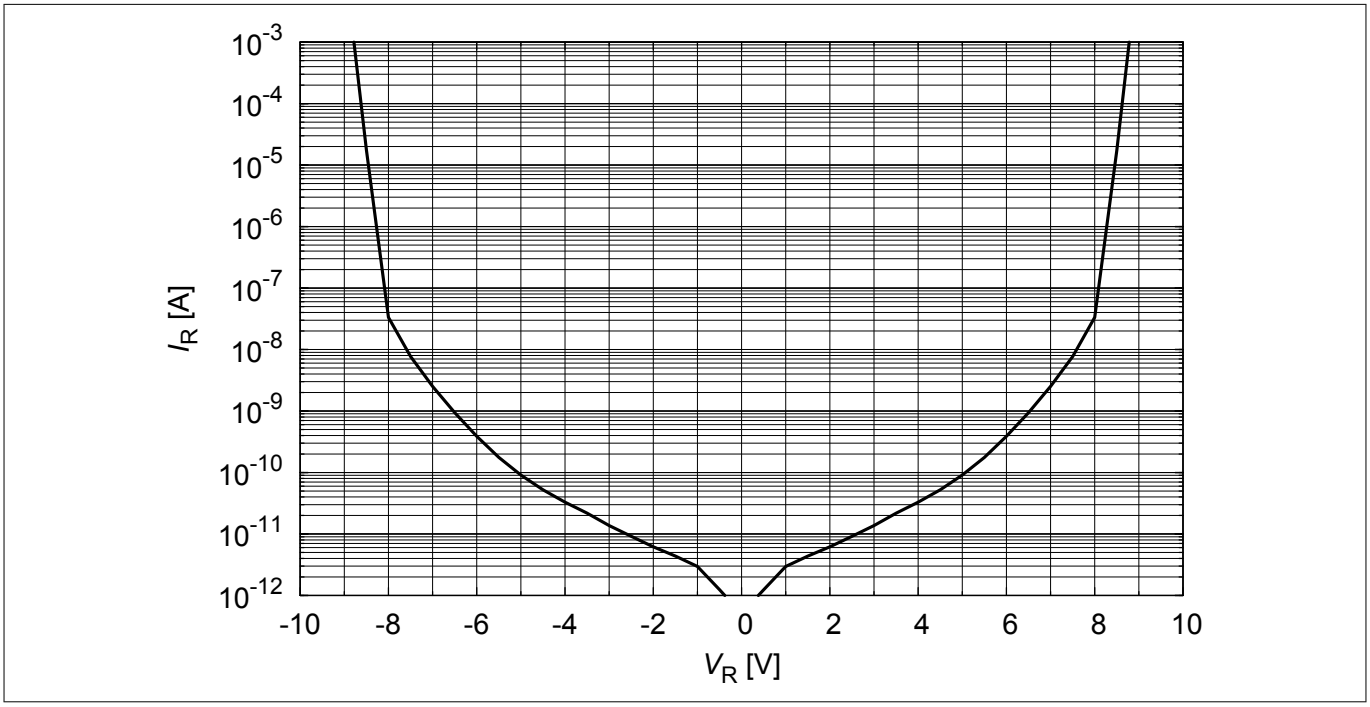

Figure 3 Reverse leakage current: $I_R = f(V_R)$

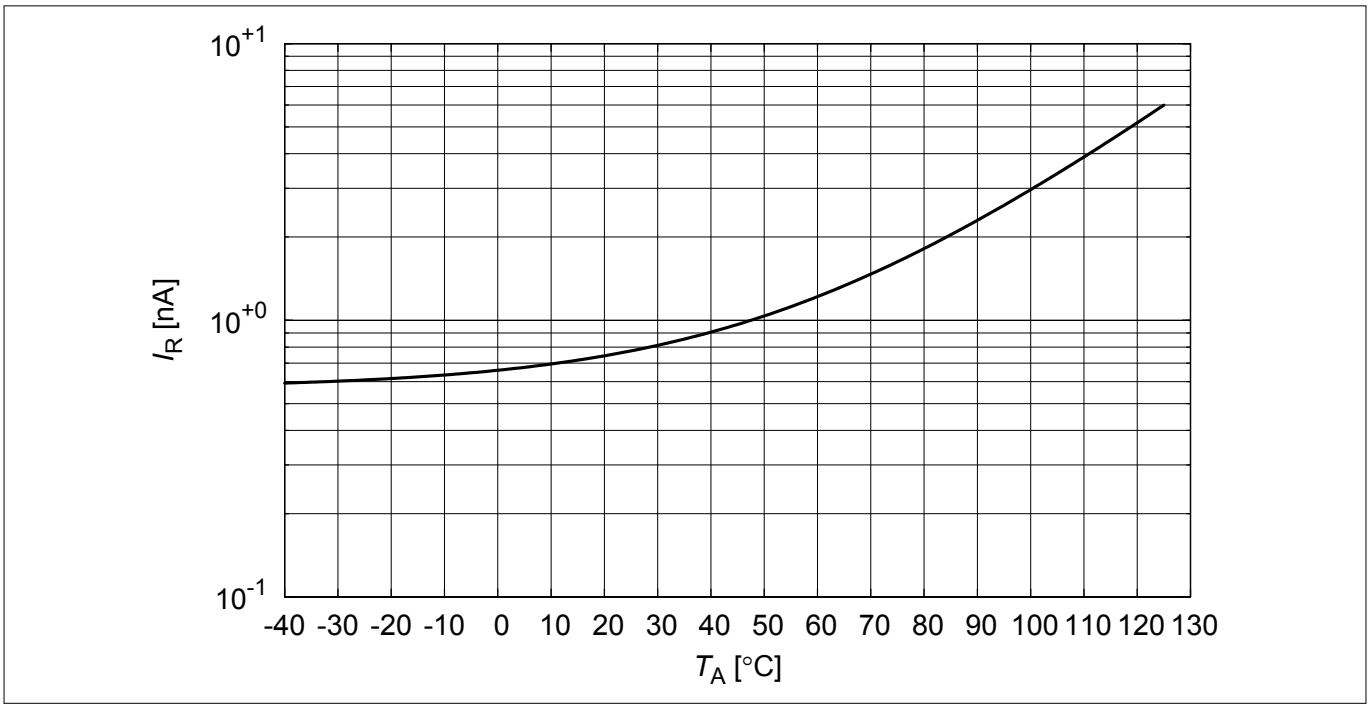

Figure 4 Reverse current $I_R = f(T_A)$, $V_R = 5.5$ V

Typical characteristic diagrams

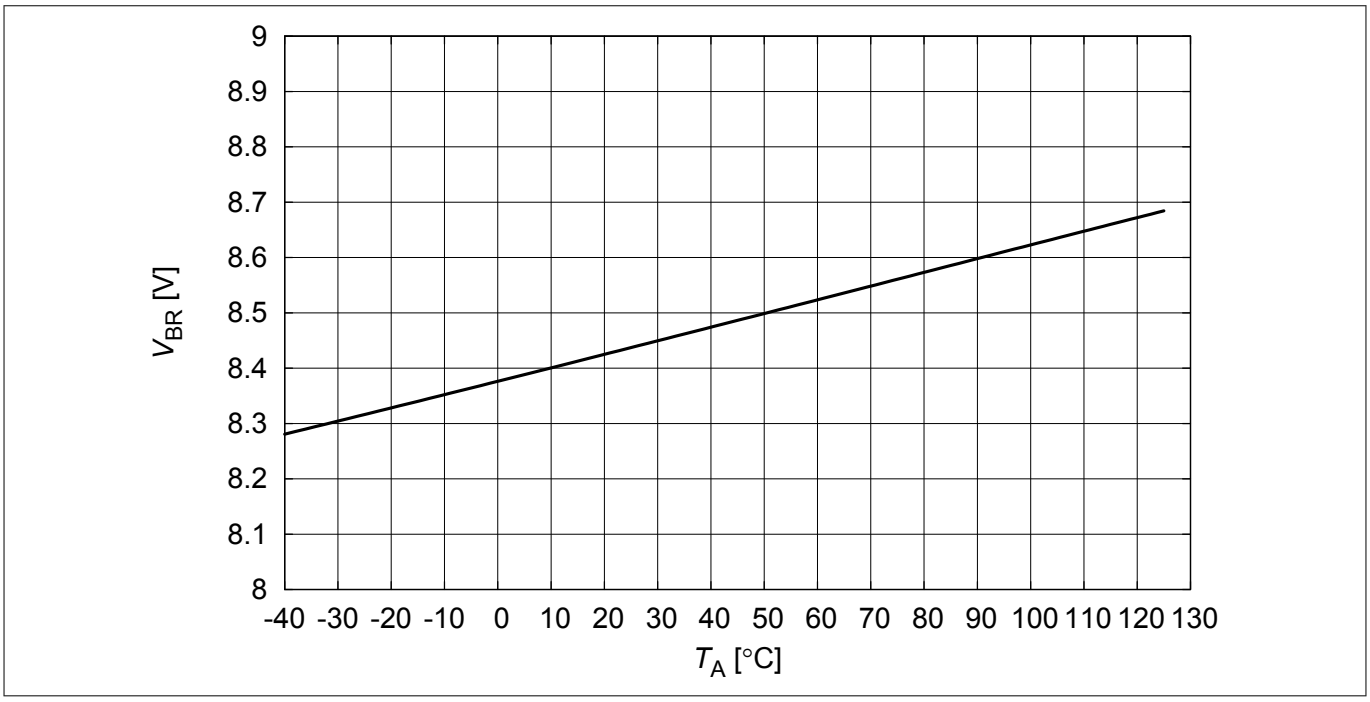

Figure 5 Reverse voltage V_{BR} = f(T_A), I_{BR} = 1 mA

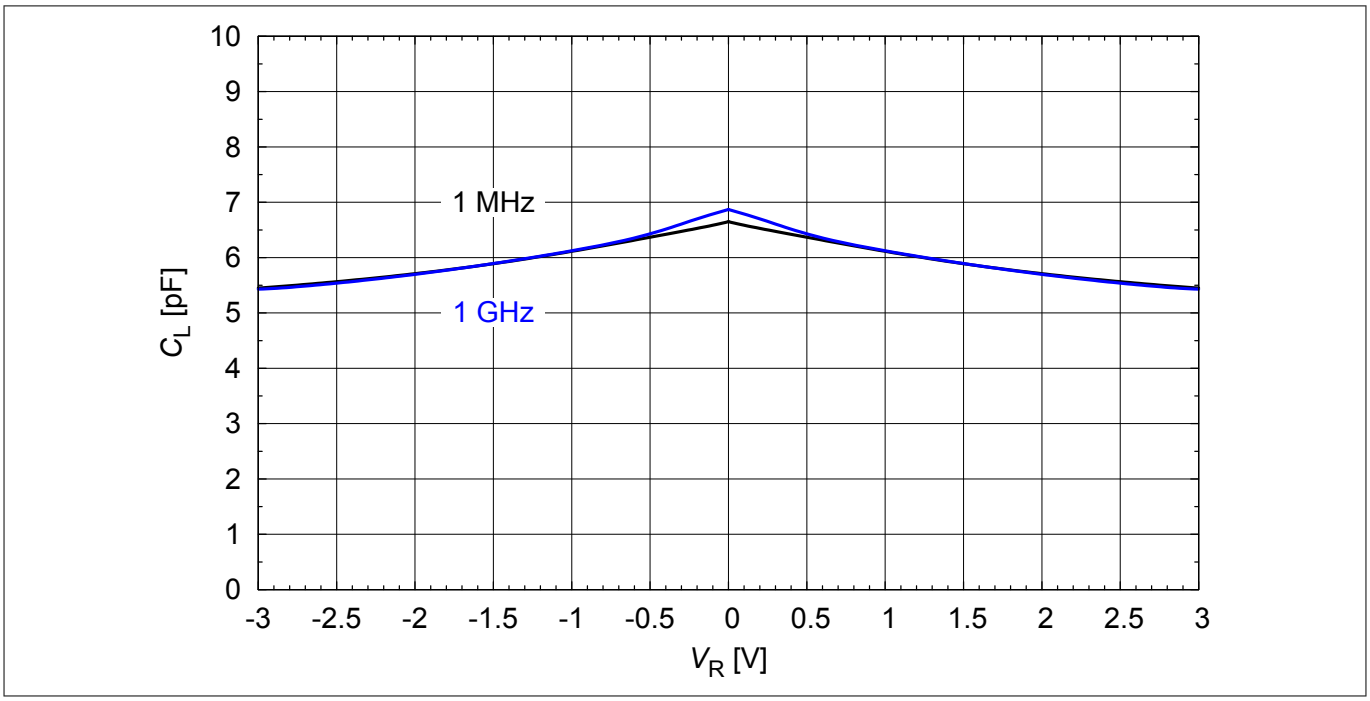

Figure 6 Line capacitance: C_L = f(V_R), f = 1 MHz, 1 GHz

Typical characteristic diagrams

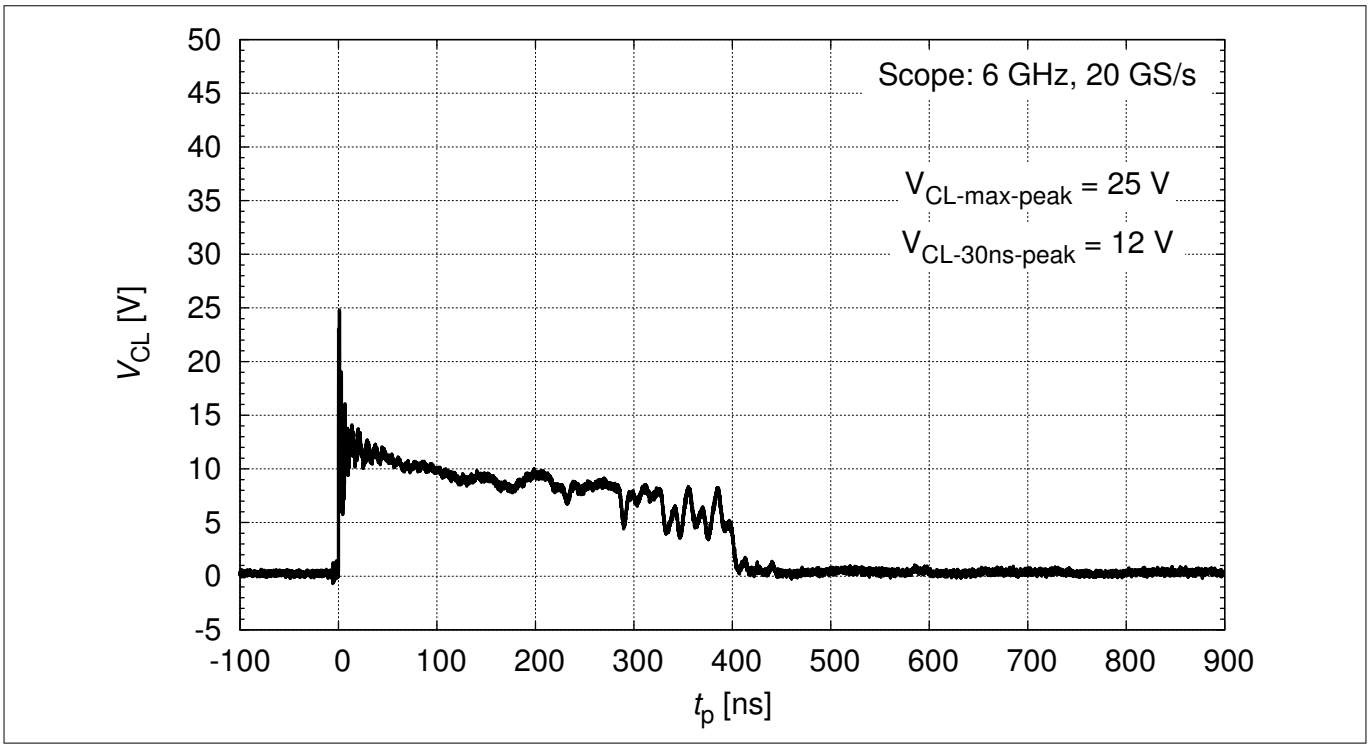

Figure 7 Clamping voltage (ESD): V_{CL} = f(t), 8 kV positive pulse according to IEC61000-4-2

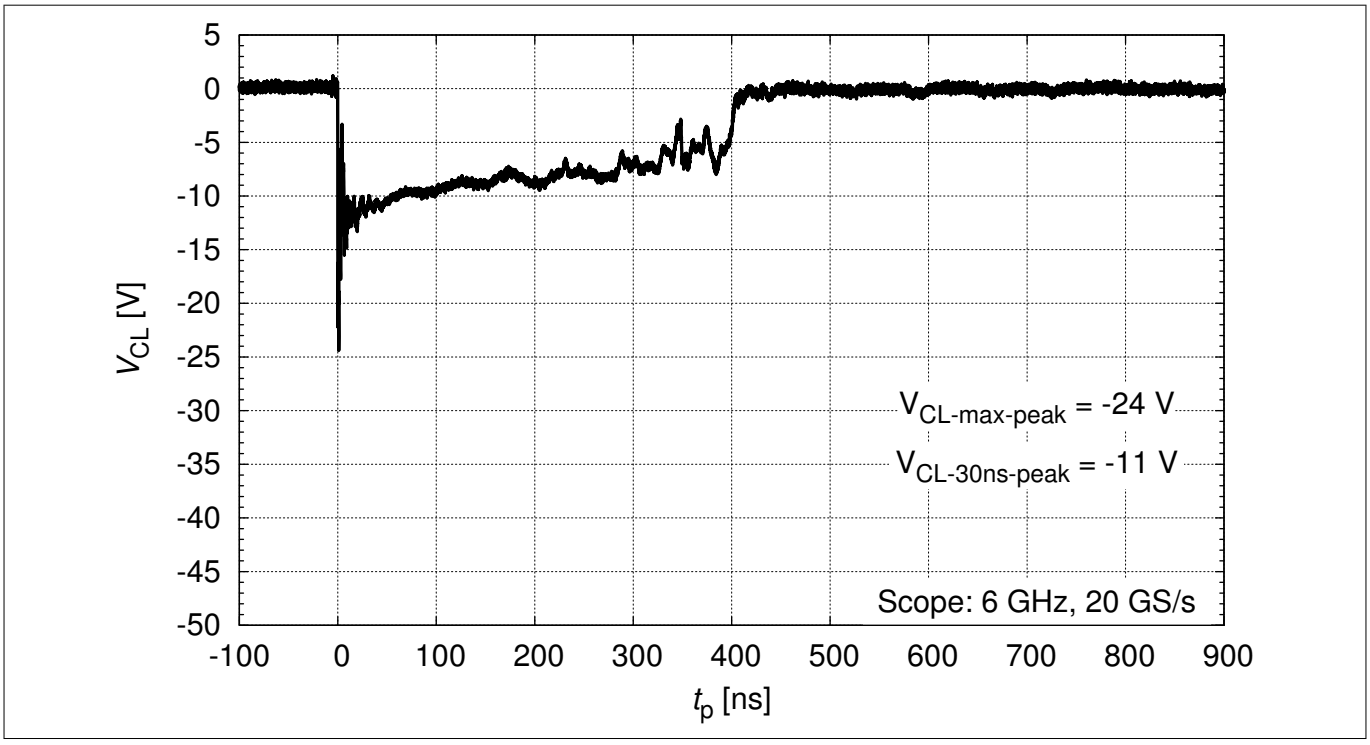

Figure 8 Clamping voltage (ESD): V_{CL} = f(t), 8 kV negative pulse according to IEC61000-4-2

Typical characteristic diagrams

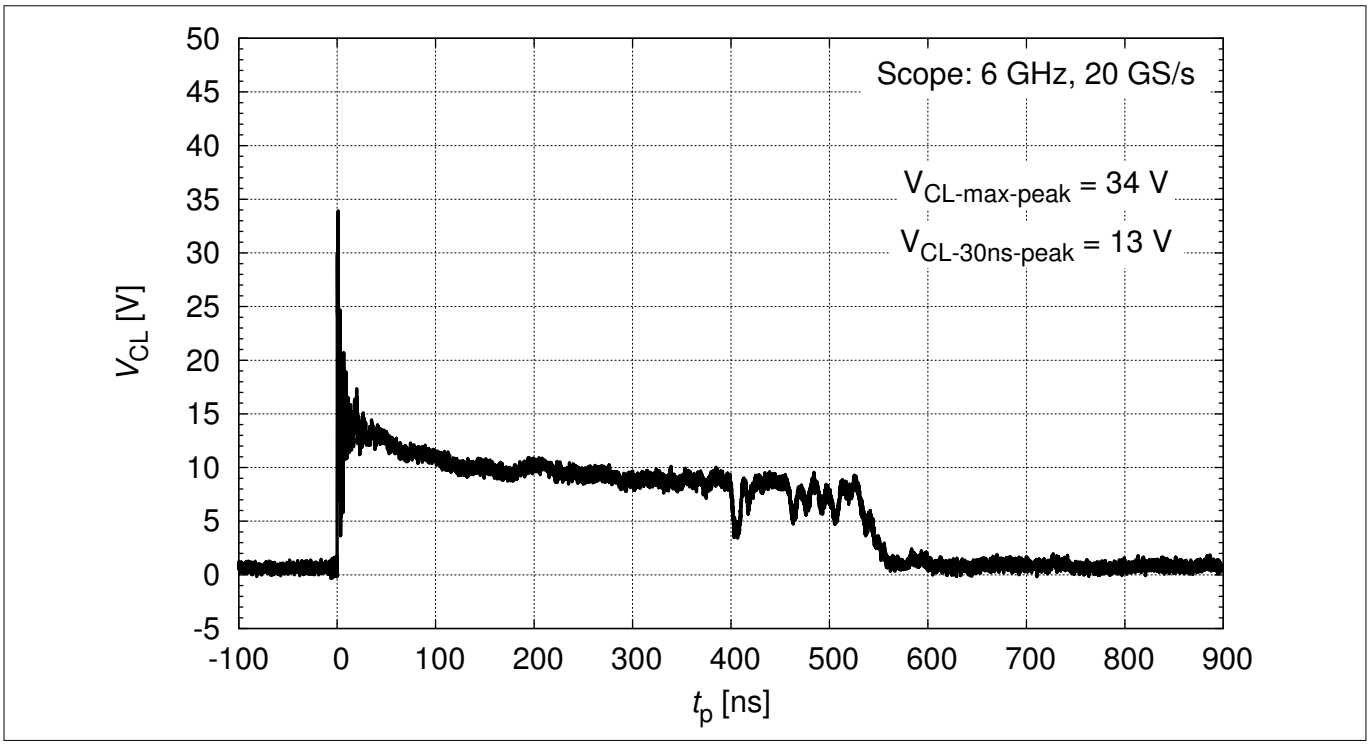

Figure 9 Clamping voltage (ESD): V_{CL} = f(t), 15 kV positive pulse according to IEC61000-4-2

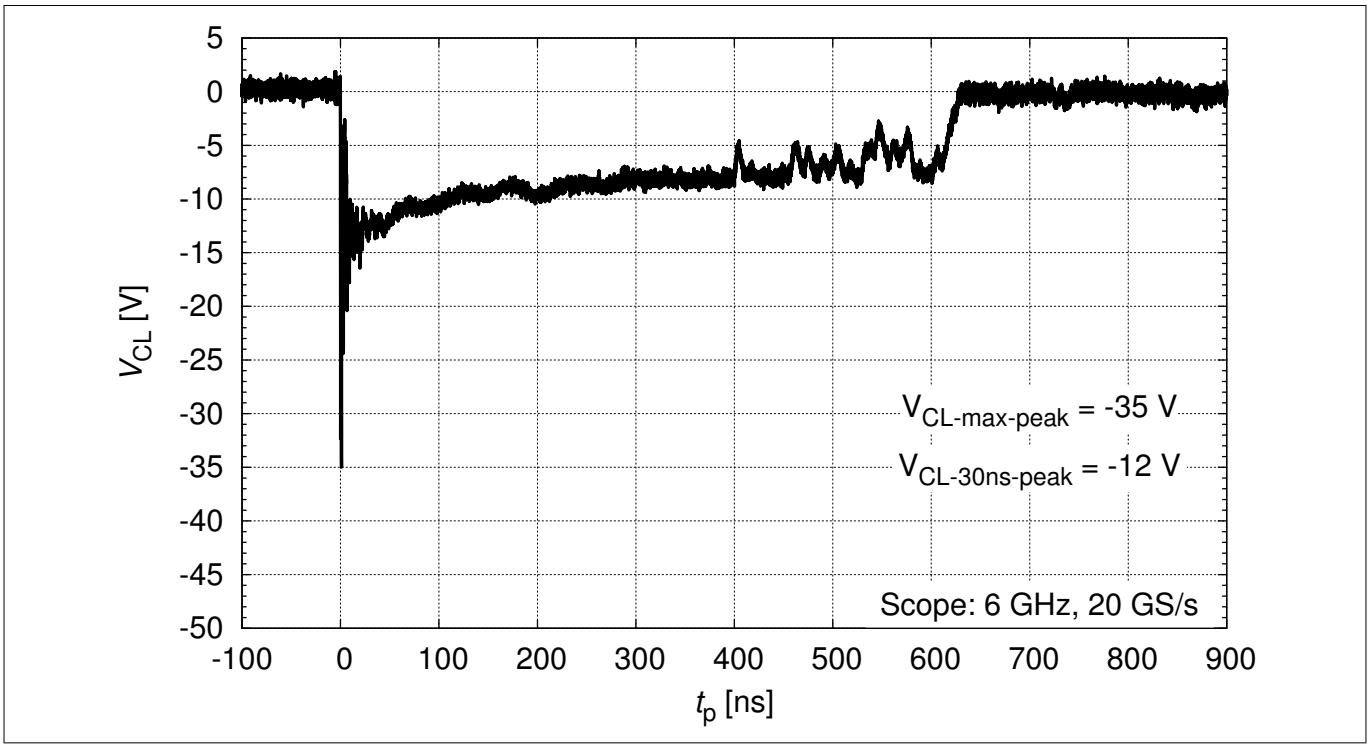

Figure 10 Clamping voltage (ESD): V_{CL} = f(t), 15 kV negative pulse according to IEC61000-4-2

Typical characteristic diagrams

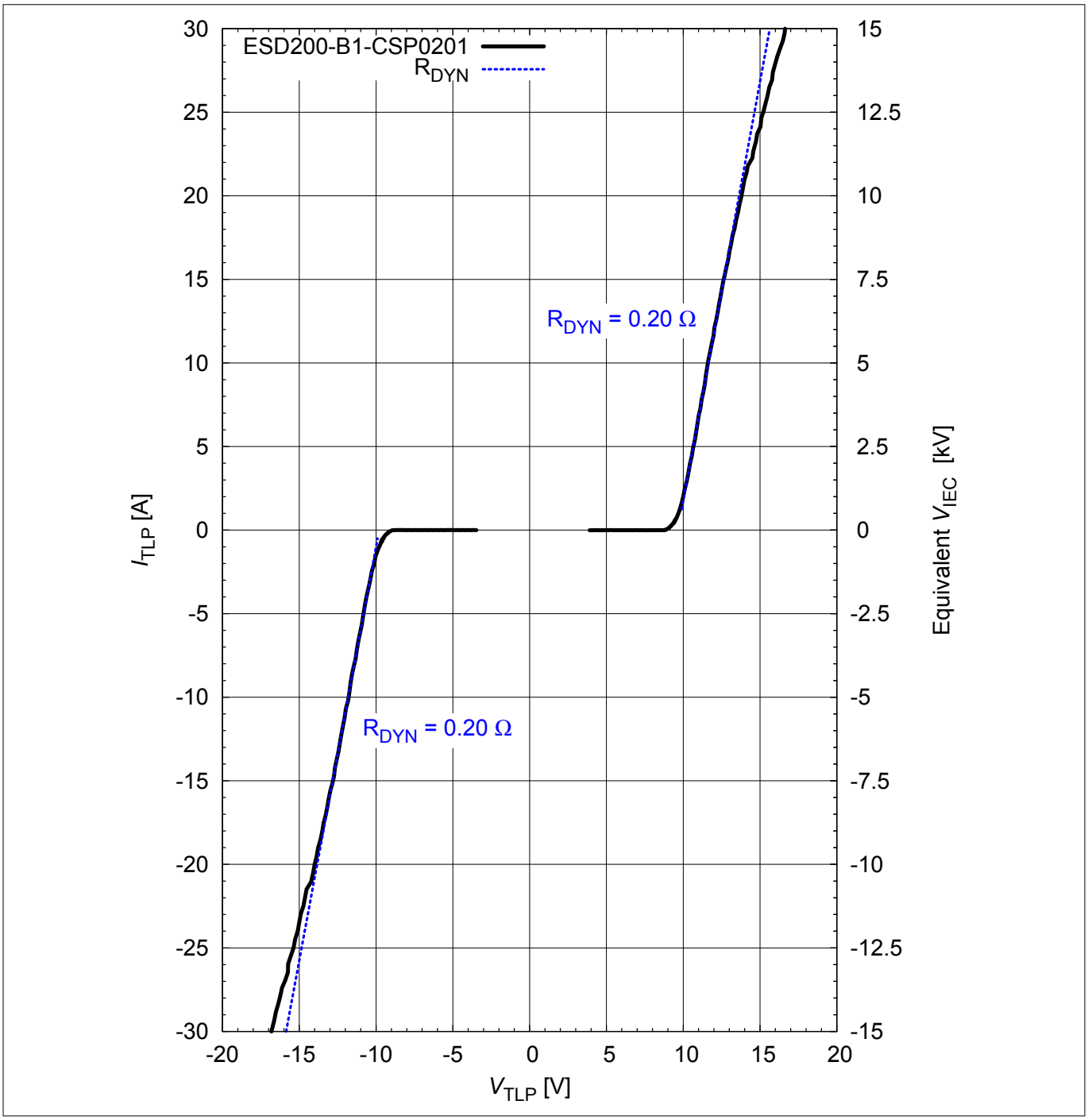

Figure 11 Clamping voltage (TLP): I_{TLP} = f(V_{TLP}) *[1]*

Typical characteristic diagrams

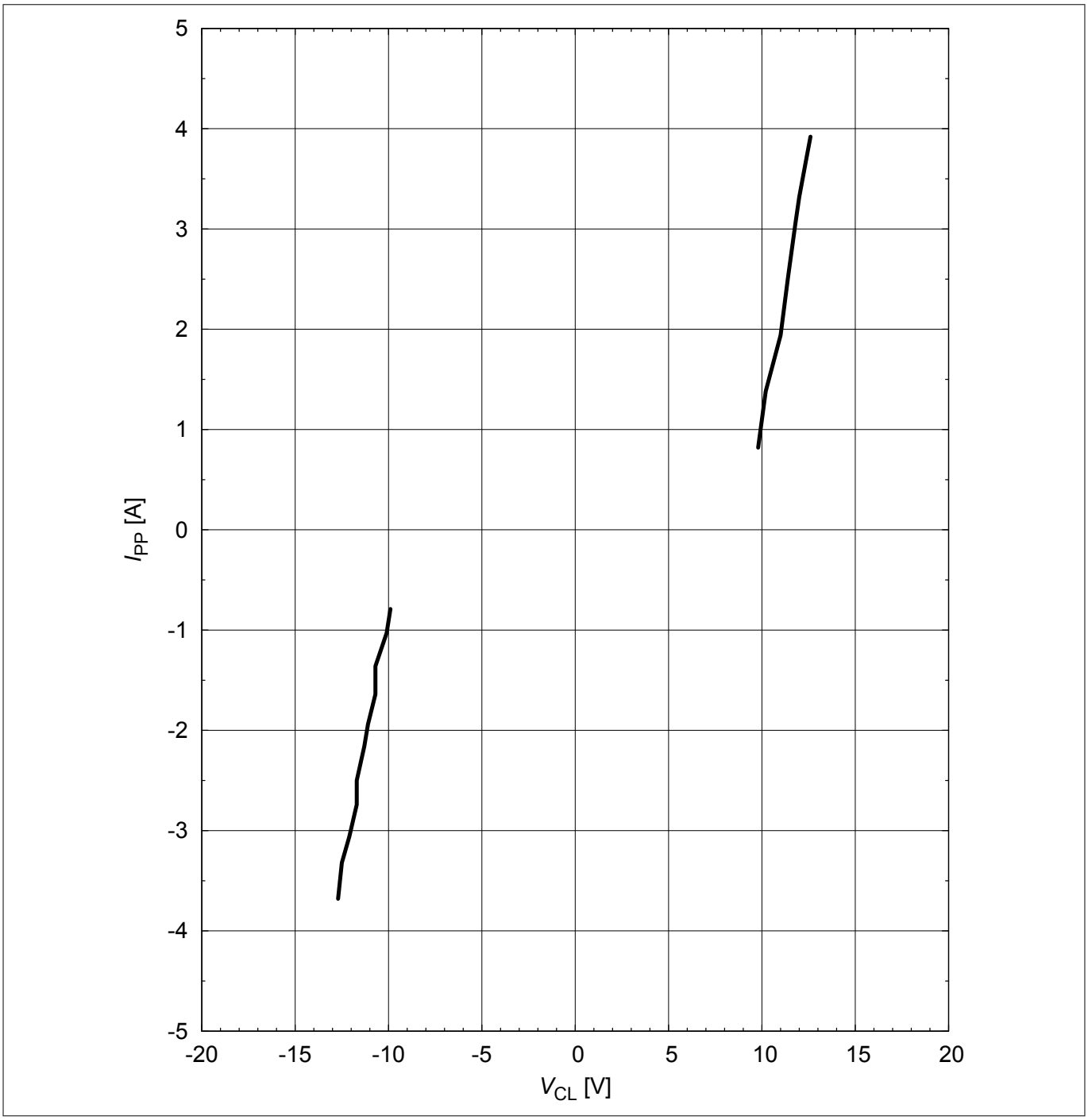

Figure 12 Clamping voltage (Surge): I_{PP} = f(V_{CL}) according to IEC61000-4-5 *[1]*

Typical characteristic diagrams

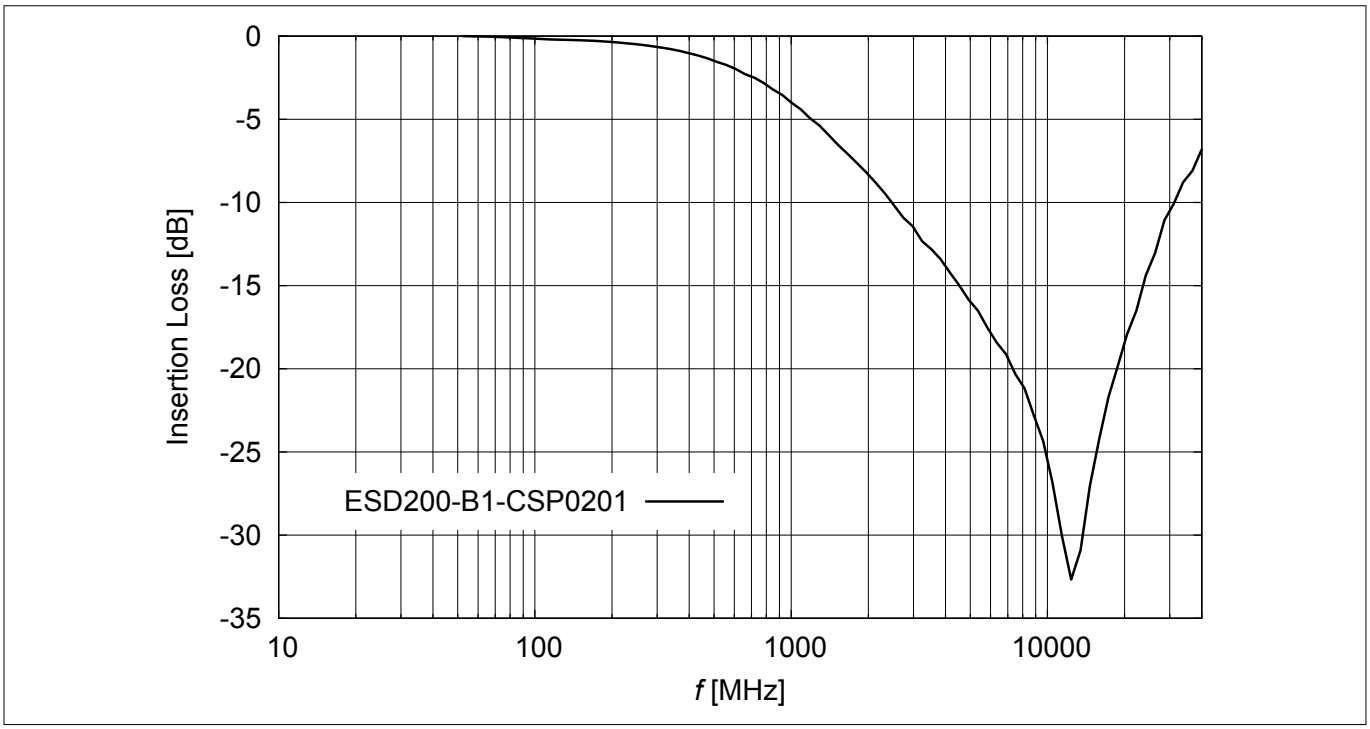

Figure 13 Insertion loss versus frequency in a 50 Ω system

4 Package information

4.1 WLL-2-1 package

Note: *Dimensions in mm*

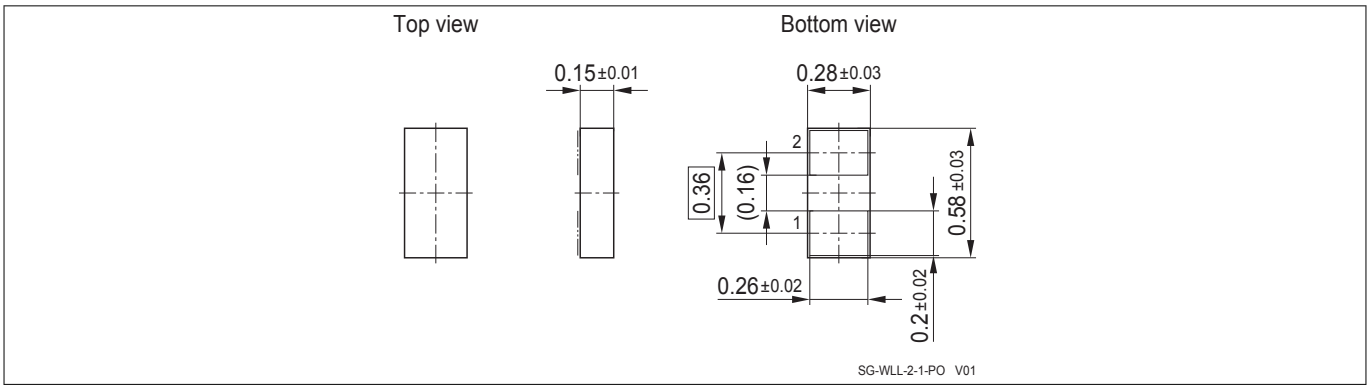

Figure 14 WLL-2-1 package outline

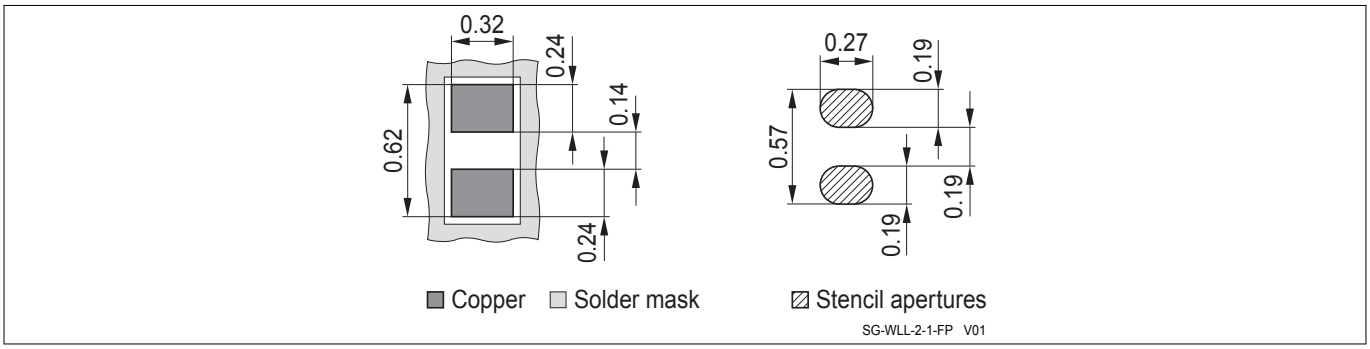

Figure 15 WLL-2-1 footprint

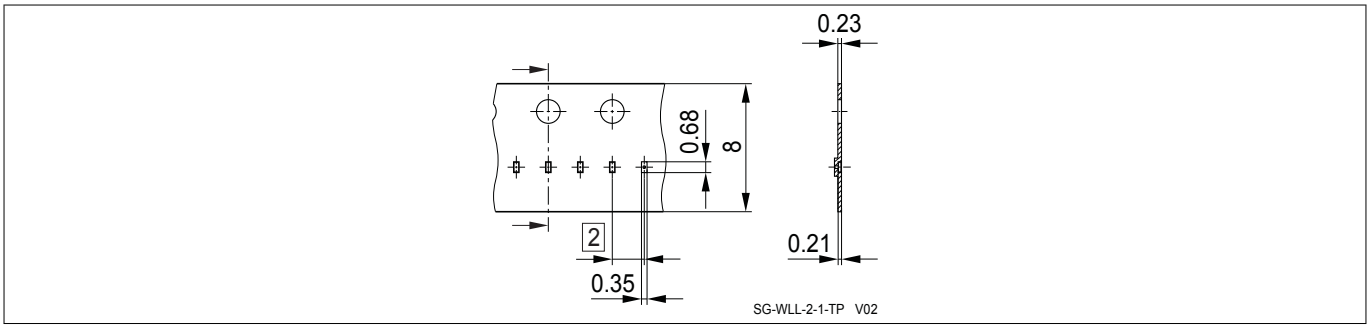

Figure 16 WLL-2-1 packing

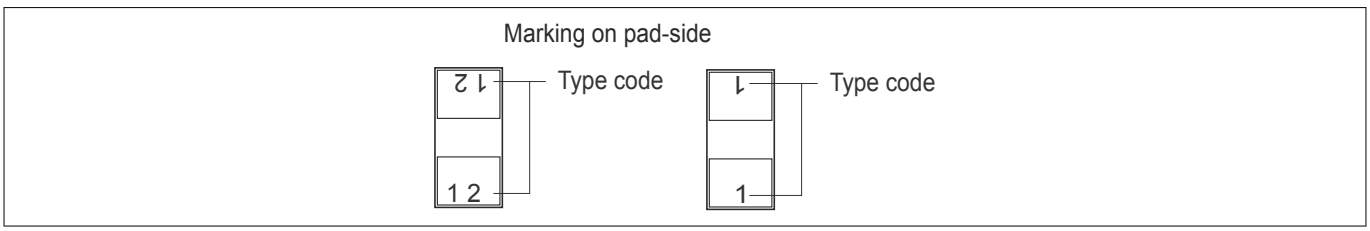

Figure 17 WLL-2-1 marking example (marking code see *Device information*)

5 References

[1] Infineon AG - **Application note AN210**: Effective ESD protection design at system level using VF-TLP characterization methodology

[2] Infineon AG - Recommendations for Printed Circuit Board Assembly of Infineon WLL Packages
http://www.infineon.com/Packageinformation_WLL

[3] Infineon AG - **Application note AN392**: TVS diodes in ChipScalePackage reduce size and save cost

Revision history

Revision history: Rev. 1.2. 2016-05-13	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.3, 2018-02-19	
All	Data sheet layout changed
	References updated, editorial changes

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