THE DATASHEET OF

PI4IOE5V96224ZLEX

24-bit I²C-bus I/O Expander

Features

- Operation power supply voltage from 2.3V to 5.5V
- 24-bit remote I/O pins that default to inputs at power-up
- 1MHz I²C-bus interface
- Compliant with the I²C-bus Fast and Standard modes
- 5.0V tolerant I/Os
- SDA with 30 mA sink capability for 4000 pF buses
- Latched outputs with 25 mA sink capability for directly driving LEDs
- Total package sink capability of 600 mA
- Active LOW open-drain interrupt output
- Low standby current
- 64 programmable slave addresses using 3 address pins
- ESD protection (4KV HBM and 1KV CDM)
- Latch-up tested (exceeds 100mA)
- Offered in TQFN-32 3mm x 6mm (ZL32) package

Description

The PI4IOE5V96224 provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C-bus) and is a part of the Fast-mode Plus family.

The PI4IOE5V96224 supports high I²C-bus drive (25 mA) so that many more devices can be on the bus without the need for bus buffers, high total package sink capacity (600 mA) that supports having all 25 mA LEDs on at the same time and more device addresses (64) are available to allow many more devices on the bus without address conflicts.

The device consists of a 24-bit quasi-bidirectional port and an I²C-bus interface. The PI4IOE5V96224 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs.

It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. The internal Power-On Reset (POR) or software reset sequence initializes the I/Os as inputs.

Pin Configuration

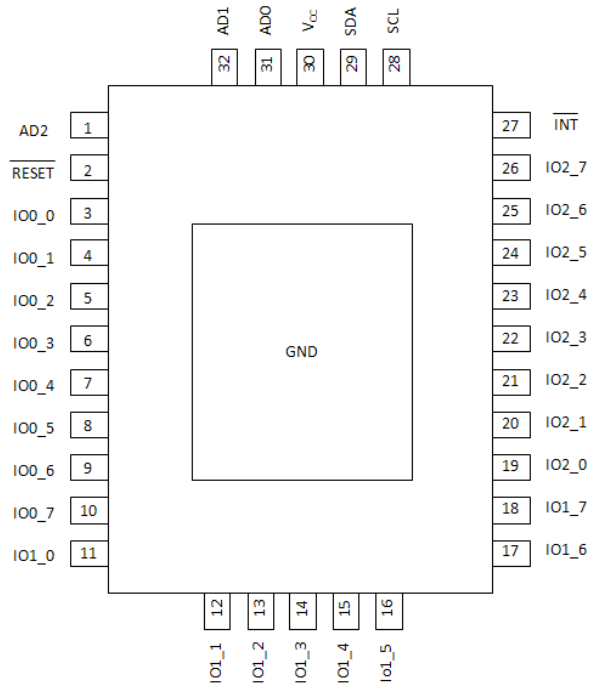


Fig 1 Pin Assignment

Pin Description

Table 1: Pin Description

Pin	Name	Type	Description
1	AD2	I	Address input 2
2	$\overline{\text{RESET}}$	I	RESET
3 - 10	IO0_0 – IO0_7	I/O	Port 0 input/output 0 - 7
11 – 18	IO1_0 – IO1_7	I/O	Port 1 input/output 0 - 7
19 - 26	IO2_0 – IO2_7	I/O	Port 2 input/output 0 - 7
27	$\overline{\text{INT}}$	O	Interrupt output (open-drain)
28	SCL	I	Serial clock line input
29	SDA	I	Serial data line open-drain
30	VCC	P	Supply voltage
31	AD0	I	Address input 0
32	AD1	I	Address input 1
Thermal Pad	GND	G	Ground

* I = Input; O = Output; P = Power; G = Ground

Maximum Ratings

Power supply	-0.5V to +6.0V
Voltage on an I/O pin	GND-0.5V to +6.0V
Input current	±20mA
Output current on an I/O pin	±50mA
Supply current	±160mA
Ground supply current	800mA
Total power dissipation	600mW
Operation temperature	-40~85℃
Storage temperature	-65~150℃
Maximum Junction temperature ,T j(max)	125℃

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static characteristics

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb= -40 °C to +85 °C; unless otherwise specified.
Table 2: Static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
VCC	Supply voltage		2.3	-	5.5	V
I_{CC}	Supply current	Operating mode; VCC= 5.5 V; no load; f_{SCL}= 1MHz	-	250	500	µA
I_{stb}	Standby current	Standby mode; VCC= 5.5 V; no load; V_I = VCC;;f_{SCL}= 0 kHz; I/O = inputs	-	0.25	1	uA
V_{POR}	Power-on reset voltage[1]		-	1.16	1.41	V
Input SCL, input/output SDA						
V_{IL}	Low level input voltage		-0.5	-	+0.3VCC	V
V_{IH}	High level input voltage		0.7VCC	-	5.5	V
I_{OL}	Low level output current	V_{OL}=0.4	20	-	-	mA
I_L	Leakage current	V_I=VCC=GND	-1	-	1	µA
C_i	Input capacitance	V_I =GND	-	5	10	pF
I/Os						
I_{OL}	Low level output current	VCC = 2.3 V; V_{OL} = 0.5 V[2]	12	28		mA
		VCC=3.0V; V_{OL} = 0.5 V[2]	17	35		mA
		VCC=4.5V; V_{OL} = 0.5 V[2]	25	42		mA
I_{OL}(tot)	total LOW-level output current	VOL=0.5V;VCC=4.5V			600	mA
I_{OH}	HIGH-level output current	VOH = GND	-30	-359	-480	uA
Itrt(pu)	transient boosted pull-up current	VOH= GND	-0.5	-1.0		mA
C_i	Off-state Input capacitance	[3]	-	9	10	pF
C_o	Off-state Output capacitance	[3]	-	9	10	pF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Interrupt $\overline{INT}$						
I_{OL}	Low level output current	V_{OL}=0.4V	6	-	-	mA
C_o	Output capacitance			2.1	10	pF
Select inputs AD2,AD1,AD0 and $\overline{RESET}$						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_L	Input leakage current		-1		1	µA
Ci	input capacitance			2.4	10	pF

Note:
[1]:VCC must be lowered to 0.2 V for at least 20us in order to reset part.
[2]:Each I/O must be externally limited to a maximum of 25 mA and the total package limited to 600 mA due to internal busing limits.
[3]: The value is not tested, but verified on sampling basis.

Dynamic Characteristics

Table 3: Dynamic characteristics

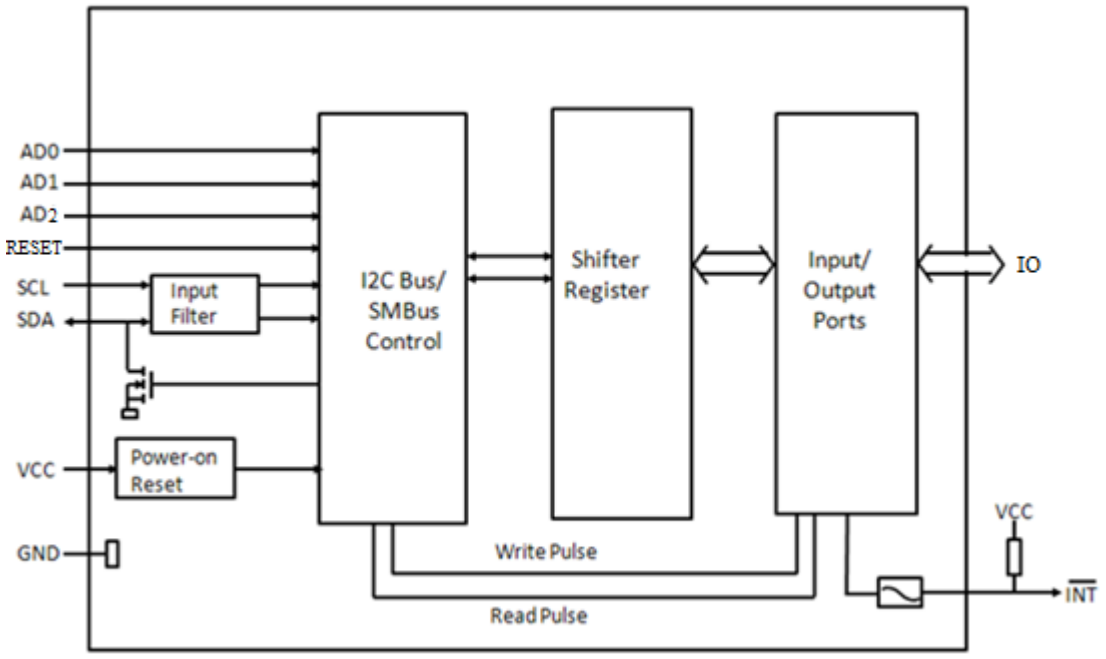
Symbol	Parameter	Standard mode I^2C		Fast mode I^2C		Fast mode Plus I^2C		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition	4.7	-	1.3	-	0.5		µs
$t_{HD;STA}$	hold time (repeated) START condition	4.0	-	0.6	-	0.26		µs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	-	0.6	-	0.26		µs
$t_{SU;STO}$	set-up time for STOP condition	4.0	-	0.6	-	0.26		µs
$t_{VD;ACK}$[1]	data valid acknowledge time	-	3.45	-	0.9	-	0.45	µs
$t_{HD;DAT}$[2]	data hold time	0	-	0	-	0		ns
$t_{VD;DAT}$	data valid time	-	3.45	-	0.9	-	0.45	ns
$t_{SU;DAT}$	data set-up time	250	-	100	-	50		ns
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	0.26		µs
t_f	fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
t_r	rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	-	50	-	50	-	50	ns
Port timing C_L≤100pF								
$t_{v(Q)}$	Data output valid time[3]		200		200		200	ns

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C		Fast mode Plus I^2C		Unit
		Min	Max	Min	Max	Min	Max	
$t_{su(D)}$	Data input set-up time	0		0		0		ns
$t_{h(D)}$	Data input hold time	4		4		4		µs
Interrupt timing C_L≤100pF								
$t_{v(D)}$	Valid time on pin $\overline{INT}$	-	4	-	4	-	4	µs
td(rst)	Reset time on pin $\overline{INT}$	-	4	-	4	-	4	µs
Reset timing								
$t_{w(rst)}$	Reset pulse width	-	25	-	25	-	25	ns
$t_{vrec(rst)}$	Reset recovery time[4]	-	0	-	0	-	0	ns
t_{rst}	Reset time	-	1	-	1	-	1	µs

Note:
[1]: $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
[2]: $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[3]: $t_{v(Q)}$measured from 0.7VCC on SCL to 50% I/O output.

Block Diagram

Fig 2: Block diagram



Note: All I/Os are set to inputs at reset.

Details Description

a. Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PI4IOE5V96224 is shown in below. Slave address pins AD2, AD1, and AD0 choose 1 of 64 slave addresses. To conserve power, no internal pull-up resistors are incorporated on AD2, AD1, and AD0. Address values depending on AD2, AD1, and AD0 can be found in Table 4 "PI4IOE5V96224 address map".

PI4IOE5V96224 Address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	A6	A5	A4	A3	A2	A1	A0	R/W

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

Table 4 PI4IOE5V96224 Address Maps

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address (Write)	Address (Read)
GND	SCL	GND	0	0	1	0	0	0	0	20h	21h
GND	SCL	VDD	0	0	1	0	0	0	1	22h	23h
GND	SDA	GND	0	0	1	0	0	1	0	24h	25h
GND	SDA	VDD	0	0	1	0	0	1	1	26h	27h
VDD	SCL	GND	0	0	1	0	1	0	0	28h	29h
VDD	SCL	VDD	0	0	1	0	1	0	1	2Ah	2Bh
VDD	SDA	GND	0	0	1	0	1	1	0	2Ch	2Dh
VDD	SDA	VDD	0	0	1	0	1	1	1	2Eh	2Fh
GND	SCL	SCL	0	0	1	1	0	0	0	30h	31h
GND	SCL	SDA	0	0	1	1	0	0	1	32h	33h
GND	SDA	SCL	0	0	1	1	0	1	0	34h	35h
GND	SDA	SDA	0	0	1	1	0	1	1	36h	37h
VDD	SCL	SCL	0	0	1	1	1	0	0	38h	39h
VDD	SCL	SDA	0	0	1	1	1	0	1	3Ah	3Bh
VDD	SDA	SCL	0	0	1	1	1	1	0	3Ch	3Dh
VDD	SDA	SDA	0	0	1	1	1	1	1	3Eh	3Fh
GND	GND	GND	0	1	0	0	0	0	0	40h	41h
GND	GND	VDD	0	1	0	0	0	0	1	42h	43h
GND	VDD	GND	0	1	0	0	0	1	0	44h	45h
GND	VDD	VDD	0	1	0	0	0	1	1	46h	47h
VDD	GND	GND	0	1	0	0	1	0	0	48h	49h
VDD	GND	VDD	0	1	0	0	1	0	1	4Ah	4Bh
VDD	VDD	GND	0	1	0	0	1	1	0	4Ch	4Dh
VDD	VDD	VDD	0	1	0	0	1	1	1	4Eh	4Fh
GND	GND	SCL	0	1	0	1	0	0	0	50h	51h

GND	GND	SDA	0	1	0	1	0	0	1	52h	53h
GND	VDD	SCL	0	1	0	1	0	1	0	54h	55h
GND	VDD	SDA	0	1	0	1	0	1	1	56h	57h
VDD	GND	SCL	0	1	0	1	1	0	0	58h	59h
VDD	GND	SDA	0	1	0	1	1	0	1	5Ah	5Bh
VDD	VDD	SCL	0	1	0	1	1	1	0	5Ch	5Dh
VDD	VDD	SDA	0	1	0	1	1	1	1	5Eh	5Fh
SCL	SCL	GND	1	0	1	0	0	0	0	A0h	A1h
SCL	SCL	VDD	1	0	1	0	0	0	1	A2h	A3h
SCL	SDA	GND	1	0	1	0	0	1	0	A4h	A5h
SCL	SDA	VDD	1	0	1	0	0	1	1	A6h	A7h
SDA	SCL	GND	1	0	1	0	1	0	0	A8h	A9h
SDA	SCL	VDD	1	0	1	0	1	0	1	AAh	ABh
SDA	SDA	GND	1	0	1	0	1	1	0	ACh	ADh
SDA	SDA	VDD	1	0	1	0	1	1	1	AEh	AFh
SCL	SCL	SCL	1	0	1	1	0	0	0	B0h	B1h
SCL	SCL	SDA	1	0	1	1	0	0	1	B2h	B3h
SCL	SDA	SCL	1	0	1	1	0	1	0	B4h	B5h
SCL	SDA	SDA	1	0	1	1	0	1	1	B6h	B7h
SDA	SCL	SCL	1	0	1	1	1	0	0	B8h	B9h
SDA	SCL	SDA	1	0	1	1	1	0	1	BAh	BBh
SDA	SDA	SCL	1	0	1	1	1	1	0	BCh	BDh
SDA	SDA	SDA	1	0	1	1	1	1	1	BEh	BFh
SCL	GND	GND	1	1	0	0	0	0	0	C0h	C1h
SCL	GND	VDD	1	1	0	0	0	0	1	C2h	C3h
SCL	VDD	GND	1	1	0	0	0	1	0	C4h	C5h
SCL	VDD	VDD	1	1	0	0	0	1	1	C6h	C7h
SDA	GND	GND	1	1	0	0	1	0	0	C8h	C9h
SDA	GND	VDD	1	1	0	0	1	0	1	CAh	CBh
SDA	VDD	GND	1	1	0	0	1	1	0	CCh	CDh
SDA	VDD	VDD	1	1	0	0	1	1	1	CEh	CFh
SCL	GND	SCL	1	1	1	0	0	0	0	E0h	E1h
SCL	GND	SDA	1	1	1	0	0	0	1	E2h	E3h
SCL	VDD	SCL	1	1	1	0	0	1	0	E4h	E5h
SCL	VDD	SDA	1	1	1	0	0	1	1	E6h	E7h
SDA	GND	SCL	1	1	1	0	1	0	0	E8h	E9h
SDA	GND	SDA	1	1	1	0	1	0	1	EAh	EBh
SDA	VDD	SCL	1	1	1	0	1	1	0	ECh	Edh
SDA	VDD	SDA	1	1	1	0	1	1	1	EEh	EFh

Quasi-bidirectional I/O Architecture

The PI4IOE5V96224's 24 ports (see Figure 3) are entirely independent and can be used either as input or output ports. Input data is transferred from the ports to the microcontroller in the Read mode. Output data is transmitted to the ports in the Write mode. Every data transmission from the PI4IOE5V96224 must consist of a multiple of three bytes, the first byte will be referred to as IO1_7 to IO1_0, and the second byte as IO2_7 to IO2_0. The third will be referred to as P2_7 to IO_0.

This quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data directions. At power-on the I/Os are HIGH. In this mode only a current source (I_{OH}) to VCC is active. An additional strong pull-up to VCC (Itrt(pu)) allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs. After power-on, as all the I/Os are set HIGH, all of them can be used as inputs. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode.

Remark: If a HIGH is applied to an I/O which has been written earlier to LOW, a large current (I_{OL}) will flow to GND.

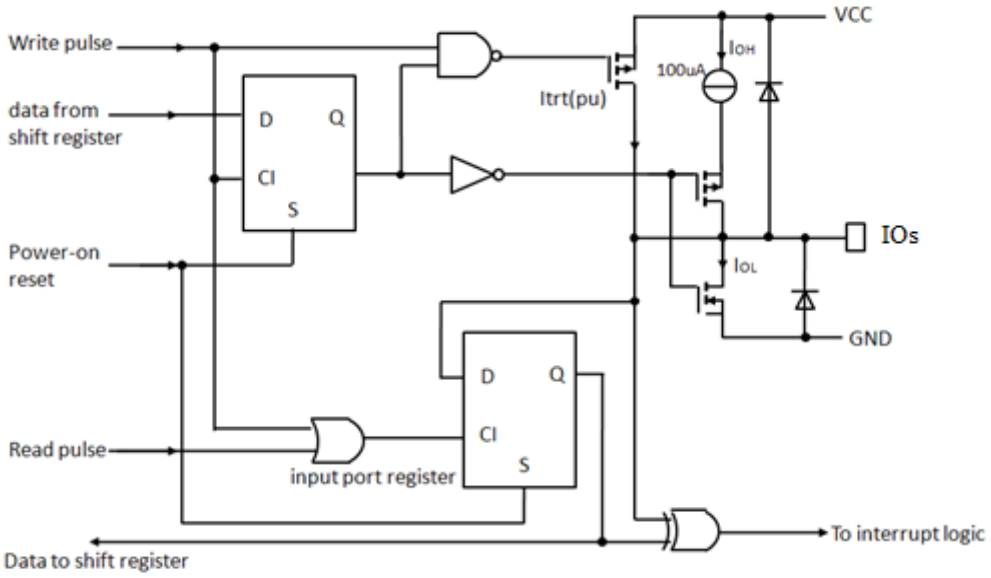


Fig 3.Simplified schematic diagram of IOX_0 to IOX_7

Writing to the Port (Output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the Write mode is entered. The PI4IOE5V96224 acknowledges and the master sends the first data byte for IO0_7 to IO0_0. After the first data byte is acknowledged by the PI4IOE5V96224, the second data byte IO1_7 to IO1_0 is sent by the master. After the second data byte is acknowledged by the PI4IOE5V96224, the three data byte IO2_7 to IO2_0 is sent by the master. Once again, the PI4IOE5V96224 acknowledges the receipt of the data. Each 8-bit data is presented on the port lines after it has been acknowledged by the PI4IOE5V96224.

The number of data bytes that can be sent successively is not limited. After every three bytes, the previous data is overwritten.

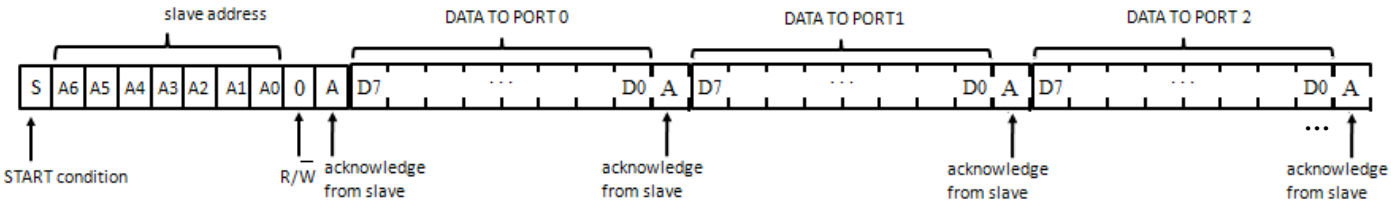


Fig 4. Write Mode

Reading from a Port (Input Mode)

All ports programmed as input should be set to logic 1. To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the Read mode is entered.
The data bytes that follow on the SDA are the values on the ports.
If the data on the input port changes faster than the master can read, this data may be lost. Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid.

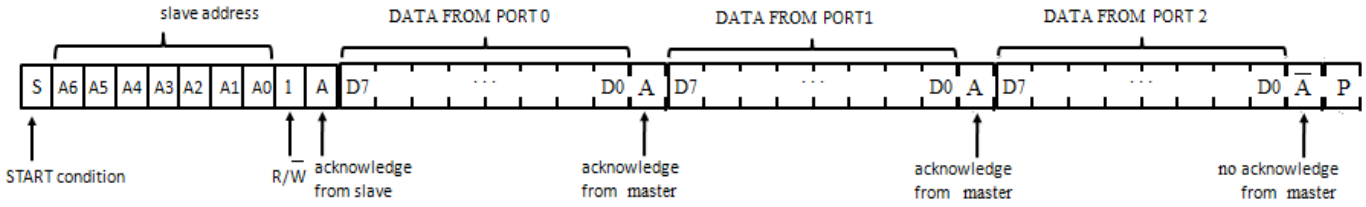


Fig 5.Read input port register

Power-On Reset

When power is applied to VCC, an internal Power-On Reset (POR) holds the PI4IOE5V96224 in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and the PI4IOE5V96224 registers and I^2C-bus state machine will initialize to their default states. Thereafter VCC must be lowered below 0.2 V to reset the device.

Interrupt Output (INT)

The PI4IOE5V96224 provides an open-drain interrupt (INT) which can be fed to a corresponding input of the microcontroller. This gives these chips a kind of master function which can initiate an action elsewhere in the system.
An interrupt is generated by any rising or falling edge of the port inputs. After time $t_{(V)D}$ the signal INT is valid.
The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt.
In the write mode, the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH).
The interrupt is reset in the read mode on the rising edge of the read from port pulse.
During the resetting of the interrupt itself, any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an INT.

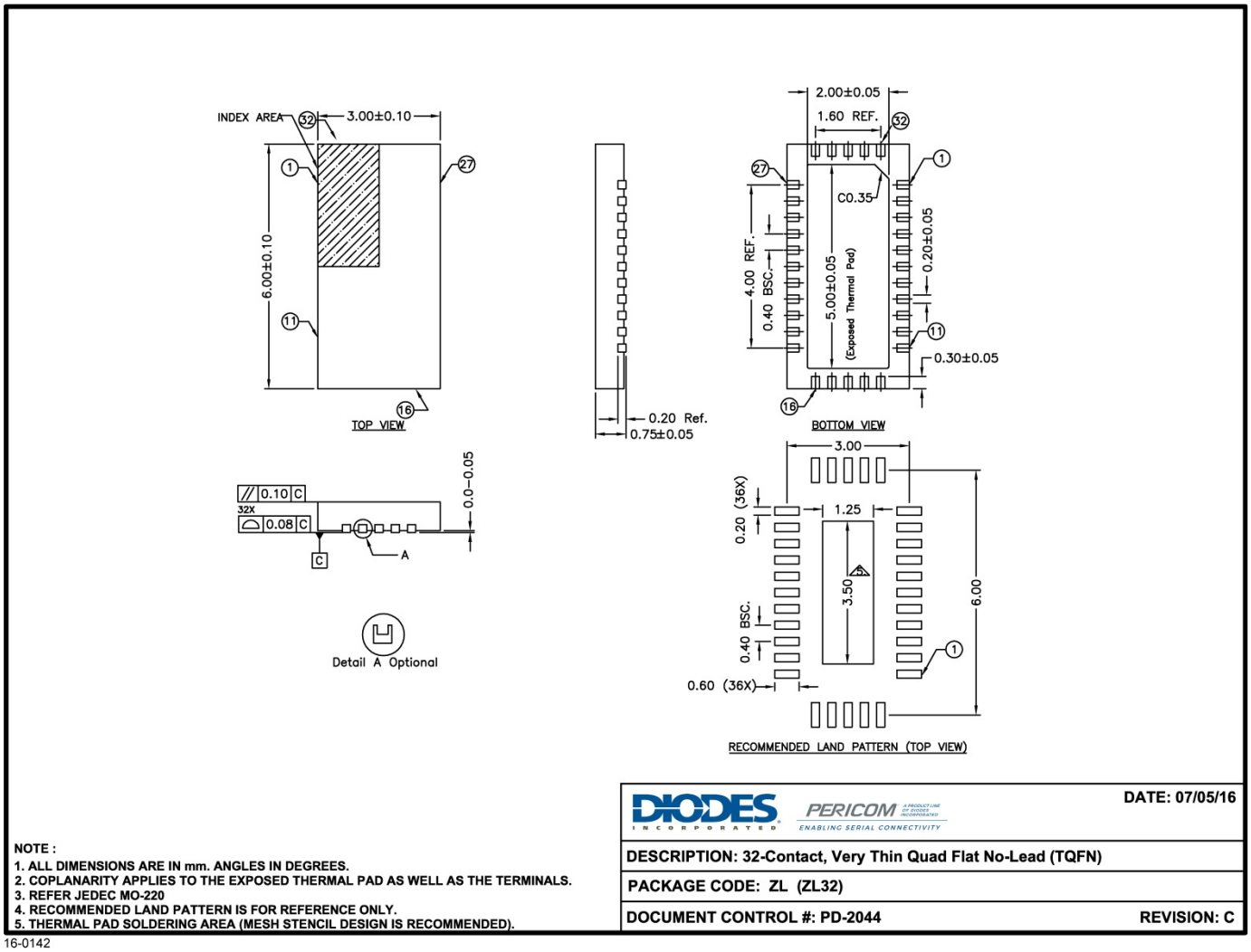
$\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PI4IOE5V96224 registers and I^2C-bus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH.

Part Marking

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical



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Ordering Information

Part Number	Package Code	Package
PI4IOE5V96224ZLEX	ZL	32-contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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