Low-Voltage Translating 34-bit I2C-bus I/O Expander

Features

- Operating power supply voltage range of 0.8V to 3.6V on the I²C-bus side
- Allows bidirectional voltage-level translation and GPIO expansion between:
  - 0.8V to 3.6V SCL/SDA and 1.8/2.5/3.3/5.5V Port
- Low standby current consumption:
  - 2 µA typical at 3.3 V $V_{DD(P)}$
- 5.5 V tolerant I/O ports and 3.6 V tolerant I²C-bus pins
- 1 MHz Fast-mode Plus I²C-bus interface
- Compliant with the I²C-bus Fast-mode plus, Fast-mode and Standard mode
- I/O Features
  - Output port configurations: bank selectable or pin selectable push-pull or open-drain output stages
  - Interrupt status: read-only register identifies the source of an interrupt
  - I/O programming features:
    - Output drive strength: four programmable drive strengths to reduce rise and fall times in low-capacitance applications
    - Input latch: Input Port register values changes are kept until the Input Port register is read
    - Pull-up/pull-down enable: floating input or pull-up/pull-down resistor enable
    - Pull-up/pull-down selection: 100k-ohm pull-up/pull-down resistor selection
    - Interrupt mask: mask prevents the generation of the interrupt when input changes state to prevent spurious interrupts
    - Interrupt edge specification on a bit-by-bit basis
    - Interrupt individual clear without disturbing other events
    - Read all interrupt events without clear
    - Switch debounce hardware
    - General call software reset
    - I²C software Device ID function
- Power-on reset
- Active LOW open-drain interrupt output ($\overline{INT}$)
- Active LOW reset input ($\overline{RESET}$)
- Latch-up tested (exceeds 100mA)
- Latched Outputs for Directly Driving LEDs
- AEC-Q100 (Grade 2)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The PI4IOE5V6534Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 46-Pin, Wettable TQFN 4.5x6.5mm (ZLW)

Description

The PI4IOE5V6534Q is a 34-bit general-purpose I/O expander that provides remote I/O expansion for most microcontroller families via the I²C-bus interface.

The device provides a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc.

The expander IC can operate from 1.65 V to 5.5 V on the GPIO-port side and 0.8 V to 3.6 V on the SDA/SCL side. This allows the PI4IOE5V6534Q to interface with next generation microprocessors and microcontrollers on the SDA/SCL side, where supply levels are dropping down to conserve power.

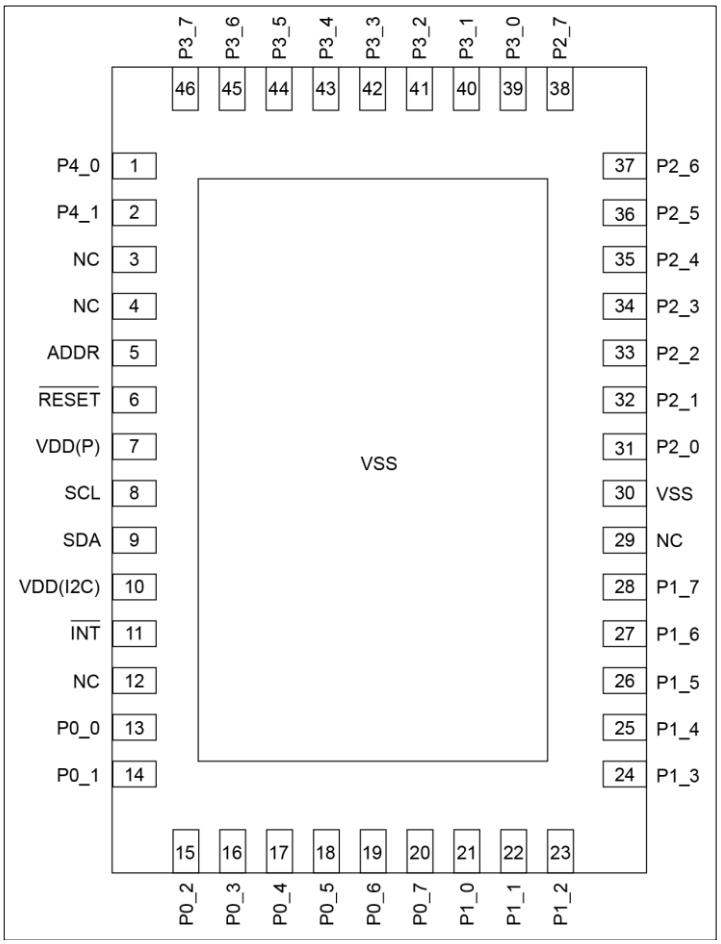
The $V_{DD\ (I2C\text{-}bus)}$ pin in PI4IOE5V6534Q provides bidirectional voltage-level translation, and the pin should be connected to the V_{DD} of the external SCL/SDA lines. The voltage level on the GPIO-port of the PI4IOE5V6534Q is determined by $V_{DD(P)}$.

At power-on, the I/Os are configured as inputs; however, the system master can enable the I/Os as either inputs or outputs by writing to the I/O direction bits. The data for each input or output is kept in the corresponding Input or Output register. All registers can be read by the system master.

PI4IOE5V6534Q has open-drain interrupt **($\overline{INT}$)** output pin that goes LOW when the input state of a GPIO-port changes from the input-state default register value. The device also has an interrupt masking feature, which the user can use to mask the interrupt from an individual GPIO-port.

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Transparent Top View

Pin Description

Pin Name	Pin#	Description
P4_0	1	Port 4 input/output 0.
P4_1	2	Port 4 input/output 1.
NC	3, 4, 12, 29	No Connected
ADDR	5	Address input. Connect directly to VDD (I2C-bus), ground, SCL or SDA.
$\overline{\text{RESET}}$	6	Active LOW reset input. Connect to $V_{DD\ (I2C\text{-}bus)}$ through a pull-up resistor if no active connection is used.
$V_{DD\ (P)}$	7	Supply voltage of PI4IOE5V6534Q for Port P.
SCL	8	Serial clock bus. Connect to $V_{DD\ (I2C\text{-}bus)}$ through a pull-up resistor.
SDA	9	Serial data bus. Connect to $V_{DD\ (I2C\text{-}bus)}$ through a pull-up resistor.
$V_{DD\ (I2C)}$	10	Supply voltage of I^2C-bus. Connect directly to the VDD of the external I^2C master. Provides voltage-level translation.
$\overline{\text{INT}}$	11	Interrupt output. Connect to $V_{DD\ (I2C\text{-}bus)}$ or $V_{DD\ (P)}$ through a pull-up resistor.
P0_0	13	Port 0 input/output 0.
P0_1	14	Port 0 input/output 1.

Pin Name	Pin#	Description
P0_2	15	Port 0 input/output 2.
P0_3	16	Port 0 input/output 3.
P0_4	17	Port 0 input/output 4.
P0_5	18	Port 0 input/output 5.
P0_6	19	Port 0 input/output 6.
P0_7	20	Port 0 input/output 7.
P1_0	21	Port 1 input/output 0.
P1_1	22	Port 1 input/output 1.
P1_2	23	Port 1 input/output 2.
P1_3	24	Port 1 input/output 3.
P1_4	25	Port 1 input/output 4.
P1_5	26	Port 1 input/output 5.
P1_6	27	Port 1 input/output 6.
P1_7	28	Port 1 input/output 7.
V_{SS}	30, Center Pad	Ground
P2_0	31	Port 2 input/output 0.
P2_1	32	Port 2 input/output 1.
P2_2	33	Port 2 input/output 2.
P2_3	34	Port 2 input/output 3.
P2_4	35	Port 2 input/output 4.
P2_5	36	Port 2 input/output 5.
P2_6	37	Port 2 input/output 6.
P2_7	38	Port 2 input/output 7.
P3_0	39	Port 3 input/output 0.
P3_1	40	Port 3 input/output 1.
P3_2	41	Port 3 input/output 2.
P3_3	42	Port 3 input/output 3.
P3_4	43	Port 3 input/output 4.
P3_5	44	Port 3 input/output 5.
P3_6	45	Port 3 input/output 6.
P3_7	46	Port 3 input/output 7.

Maximum Ratings

I^2C-bus power supply	-0.5V to +4.0V
Port P power supply	-0.5V to +6.0V
Input / Output voltage on all ports	-0.5V to +6.0V
Input voltage on $\overline{RESET}$, SCL, SDA, ADDR pins	-0.5V to +4.0V
Output voltage on $\overline{INT}$, SCL, SDA, pins	-0.5V to +4.0V
Input clamping current on $\overline{RESET}$, SCL, ADDR pins ($V_I < 0$ V)	±20mA
Output clamping current $\overline{INT}$ pin ($V_O < 0$ V)	±20mA
Input / Output clamping current on all ports ($V_O < 0$ V or $V_O > V_{DD(P)}$)	±20mA
Input / Output clamping current on SDA pin ($V_O < 0$ V or $V_O > V_{DD(I2C\text{-}bus)}$)	±20mA
LOW – level output current on all ports	50mA
HIGH– level output current on all ports	25mA
LOW – level output current on $\overline{INT}$, SDA	25mA
Supply current through $V_{DD(I2C\text{-}bus)}$	10mA
Supply current through $V_{DD(P)}$	400mA
Ground supply current	500mA
Storage temperature	-65~150℃
Maximum junction temperature ,T j(max)	125℃
ESD (HBM)	2kV
ESD (CDM)	1kV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{DD(I2C\text{-}bus)}$	I^2C-bus power supply		0.8	3.6	V
$V_{DD(P)}$	GPIO port power supply		1.65	5.5	V
V_{IH}	HIGH-level input voltage	$\overline{RESET}$, SCL, SDA, ADDR			
		$V_{DD\ (I2C\text{-}bus)} \leq 1.1$ V	0.8 x $V_{DD(I2C\text{-}bus)}$	3.6	V
		$V_{DD\ (I2C\text{-}bus)} > 1.1$ V	0.7 x $V_{DD(I2C\text{-}bus)}$	3.6	V
		P4_1 to P0_0	0.7 x $V_{DD(P)}$	5.5	V
V_{IL}	LOW-level input voltage	$\overline{RESET}$, SCL, SDA, ADDR			
		$V_{DD\ (I2C\text{-}bus)} \leq 1.1$ V	-0.5	0.2 x $V_{DD(I2C\text{-}bus)}$	V
		$V_{DD\ (I2C\text{-}bus)} > 1.1$ V	-0.5	0.3 x $V_{DD(I2C\text{-}bus)}$	V
		P4_1 to P0_0	-0.5	0.3 x $V_{DD(P)}$	V
I_{OH}	HIGH-Level Output Current	P4_1 to P0_0 CCX.X=11b	-	10	mA
I_{OL}	LOW-Level Output Current	P4_1 to P0_0 CCX.X=11b	-	25	mA
T_{amb}	Ambient temperature		-40	105	℃

Static Characteristics

$V_{DD(I2C\_bus)}$ = 0.8 V to 3.6 V; Temp = -40℃ to +105℃; unless otherwise specified. Typical values are at Temp = 25℃.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Power supply							
I_{DD}	Supply current	Clocked mode; $I_{DD(I2C-bus)}$ + $I_{DD(P)}$; P port, ADDR, $\overline{RESET}$, SDA; V_I on ADDR, $\overline{RESET}$ and SDA = $V_{DD(I2C-bus)}$ or V_{SS}; V_I on P port= $V_{DD(P)}$; IO = 0 mA; I/O = inputs;					
		f_{SCL} = 0 kHz	$V_{DD(P)}$=3.6-5.5V	-	3	11.5	µA
			$V_{DD(P)}$=2.3-3.6V	-	2	6.8	µA
			$V_{DD(P)}$=1.65-2.3V	-	1.5	5.25	µA
		f_{SCL} = 400 kHz	$V_{DD(P)}$=3.6-5.5V	-	27	51	µA
			$V_{DD(P)}$=2.3-3.6V	-	15	30	µA
			$V_{DD(P)}$=1.65-2.3V	-	9.5	19	µA
		f_{SCL} = 1 MHz	$V_{DD(P)}$ = 3.6-5.5V	-	72	110	µA
			$V_{DD(P)}$ = 2.3-3.6V	-	36	60	µA
			$V_{DD(P)}$ = 1.65-2.3V	-	22	40	µA
		Active mode; $I_{DD(I2C-bus)}$ + $I_{DD(P)}$; P port, ADDR, $\overline{RESET}$; V_I on ADDR, $\overline{RESET}$ = $V_{DD(I2C-bus)}$; V_I on P port= $V_{DD(P)}$; IO = 0 mA; I/O = inputs; Continuous register read					
		f_{SCL} = 400 kHz	$V_{DD(P)}$ = 3.6-5.5V	-	150	250	µA
			$V_{DD(P)}$ = 2.3-3.6V	-	120	200	µA
			$V_{DD(P)}$ = 1.65-2.3V	-	75	150	µA
		f_{SCL} = 1 MHz	$V_{DD(P)}$ = 3.6-5.5V	-	450	625	µA
			$V_{DD(P)}$ = 2.3-3.6V	-	270	500	µA
			$V_{DD(P)}$ = 1.65-2.3V	-	160	210	µA
V_{IK}	Input clamping voltage	I_I = - 18 mA		-1.2	-	-	V
V_{POR}	Power-on reset voltage	Rising		-	1.1	1.4	V
		Falling		0.5	-	-	
$T_{d(rst)}$	Reset time	Time of $V_{DD(P)}$ drop to $V_{POR(min)}$ − 50 mV for successful Power-on reset		22	-	-	µs
Input SCL, input/output SDA							
I_{OL}	SDA LOW-level output current	V_{OL}= 0.4 V; $V_{DD(I2C-bus)} \leq$ 2 V		15	-	-	mA
		V_{OL}= 0.4 V; $V_{DD(I2C-bus)}$ > 2 V		20	-	-	mA
I_I	Input current	V_I = $V_{DD(I2C-bus)}$ or V_{SS} ; $V_{DD(P)}$ = 1.65 V to 5.5 V		-1	-	1	µA
C_{io}	Input / Output capacitance	V_I = $V_{DD(I2C-bus)}$ or V_{SS} ; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	7	-	pF
Interrupt $\overline{INT}$							
I_{OL}	LOW-level output current	V_{OL}=0.4V; $V_{DD(P)}$ = 1.65 V to 5.5 V		3	-	-	mA
C_o	Output capacitance	V_I = $V_{DD(I2C-bus)}$ or V_{SS} ; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	7.5	-	pF
Select inputs ADDR and $\overline{RESET}$							
I_I	Input current	V_I = $V_{DD(I2C-bus)}$ or V_{SS} ; $V_{DD(P)}$ = 1.65 V to 5.5 V		-1	-	1	µA

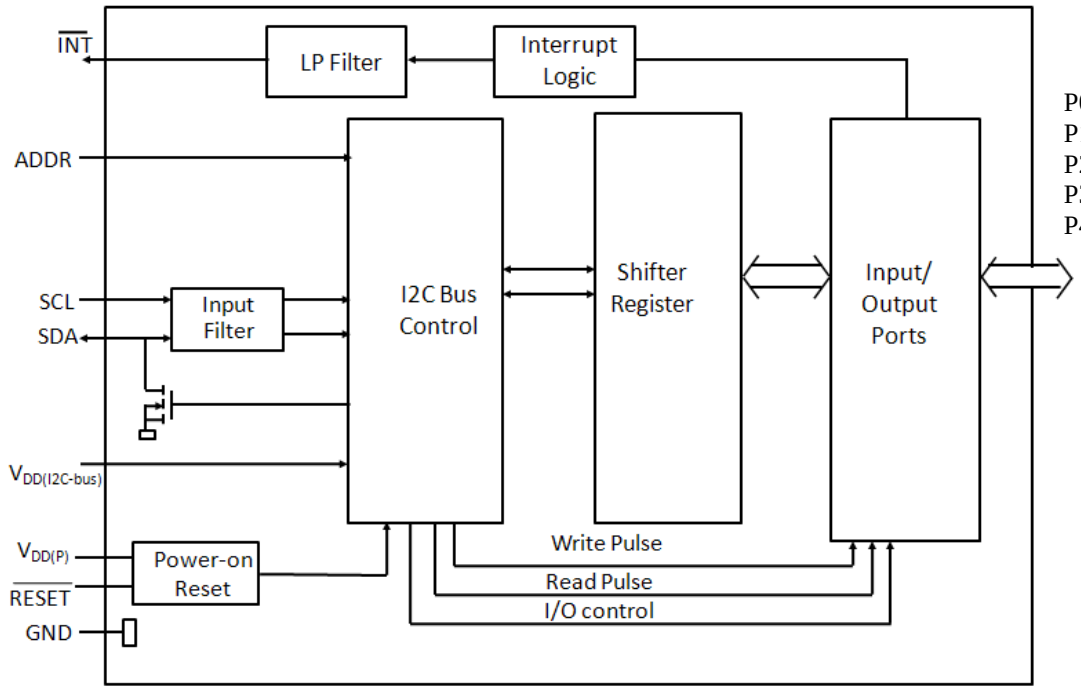
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ci	Input capacitance	$V_I = V_{DD(I2C-bus)}$ or V_{SS} ; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	6	-	pF
I/Os						
V_{OH}	HIGH-level output voltage	I_{OH} = -2.5mA; CCX.X=00b I_{OH} = -5mA; CCX.X=01b I_{OH} = -7.5mA; CCX.X=10b I_{OH} = -10mA; CCX.X=11b				
		$V_{DD(P)}$ = 1.65 V	1.1	-	-	V
		$V_{DD(P)}$ = 2.3 V	1.7	-	-	V
		$V_{DD(P)}$ = 3 V	2.5	-	-	V
		$V_{DD(P)}$ = 4.5 V	4.0	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 2.5mA; CCX.X=00b I_{OL} = 5mA; CCX.X=01b I_{OL} = 7.5mA; CCX.X=10b I_{OL} = 10mA; CCX.X=11b				
		$V_{DD(P)}$ = 1.65 V	-	-	0.5	V
		$V_{DD(P)}$ = 2.3 V	-	-	0.3	V
		$V_{DD(P)}$ = 3 V	-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V	-	-	0.2	V
I_{IH}	HIGH-level input current	P port; $V_I = V_{DD(P)}$	-	-	1	µA
I_{IL}	LOW-level input current	P port; $V_I = V_{SS}$	-	-	1	µA
C_{io}	Input / Output Capacitance	$V_{I/O} = V_{DD(P)}$ or V_{SS}		7.5	-	pF
$R_{pu(int)}$	Internal pull-up resistance	Input/Output	50	100	150	kΩ
$R_{pd(int)}$	Internal pull-down resistance	Input/Output	50	100	150	kΩ

Note:
1. The sum of source current by all I/Os must be limited to 160 mA.
2. Each I/O current must be externally limited to 25 mA. Each octal (P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7) must be limited to a maximum current of 100 mA and P4_1 to P4_0 must be limited to a maximum current of 50 mA for a device of total 500 mA.

Dynamic Characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C		Fast mode Plus I^2C		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45	-	0.9	-	0.45	µs
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	ns
$t_{VD;DAT}$	Data valid time	-	3.45	-	0.9	-	0.45	ns
$t_{SU;DAT}$	Data set-up time	250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	0.26	-	µs
t_f	Fall time of both SDA and SCL signals	-	300	20 x (VDD/ 3.6V)	300	-	120	ns
t_r	Rise time of both SDA and SCL signals	-	1000	20	300	-	120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	0	50	0	50	ns
Interrupt Timing								
$t_{V(INT)}$	Valid time on pin $\overline{INT}$ (from P port to $\overline{INT}$)	-	1	-	1	-	1	µs
$t_{RST(INT)}$	Reset time on pin $\overline{INT}$ (from SCL port to $\overline{INT}$)	-	1	-	1	-	1	µs
Reset Timing								
$t_{w(rst)}$	Reset pulse width	150	-	150	-	150	-	ns
t_{rst_rec}	Reset recovery time	500	-	500	-	500	-	ns
t_{rst}	Reset time	600	-	600	-	600	-	ns
P Port Timing								
$t_{V(Q)}$	Data output valid time (from SCL to P Port)	-	400	-	400	-	400	ns
$t_{SU(D)}$	Data input setup time (from P Port to SCL)	0	-	0	-	0	-	ns
$t_{h(D)}$	Data input hold time (from P Port to SCL)	300	-	300	-	300	-	ns

Block Diagram



Note: All I/Os are set to inputs at reset.

Functional Description

A. I²C Read/ Write Procedures

i. WRITE Commands

Data is transmitted to the PI4IOE5V6534Q by sending the device address with the Least Significant Bit (LSB) set to a logic 0. The command byte is sent after the address and determines which register receives the data that follows the command byte.

Many of the registers within the PI4IOE5V6534Q are configured to operate as register quinary. The 5-register groups are input ports, output ports, polarity inversion and configuration registers, as well as input latch, pull-up/pull-down enable and selection registers, Interrupt mask and interrupt status, interrupt clear, and input port (status) without interrupt clear registers, individual pin output port configuration registers. After sending data to one register, the next data byte is sent to the next register in the group. For example, if the first byte is sent to Output Port 1 (register 06h), the next byte is stored in Output Port 2 (register 07h). The next byte sent is stored in Output Port 3 (register 08h) and the next byte will Output Port 4 (register 09h). Since every new write access after a STOP condition requires a Command byte, which sets the Pointer register, the next new write access will be to an arbitrary register.

There is no limit on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register group independently of the other registers or the host can simply update a single register.

There is one 3-register group: switch debounce (6Dh to 6Fh) registers and two 9-register groups: Output drive strength (30h to 38h) and interrupt edge (54h to 5Ch) registers which can be programmed continuously in this group.

There is one register that is not part of a register group: Output port configuration (53h). When this register is accessed multiple times, the register address remains fixed on the same address.

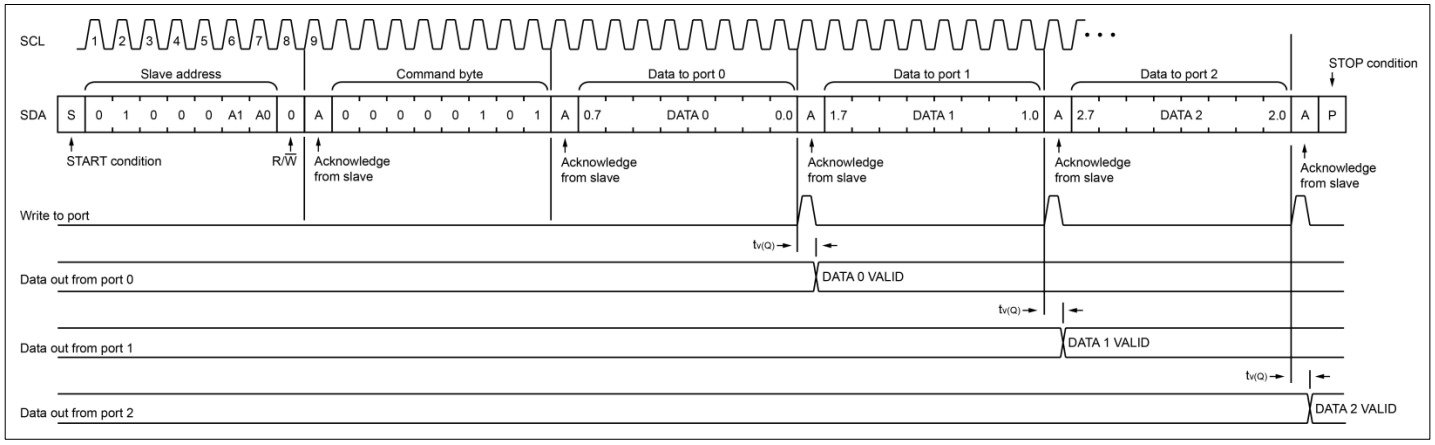


Figure 1. Write to Output Port Register

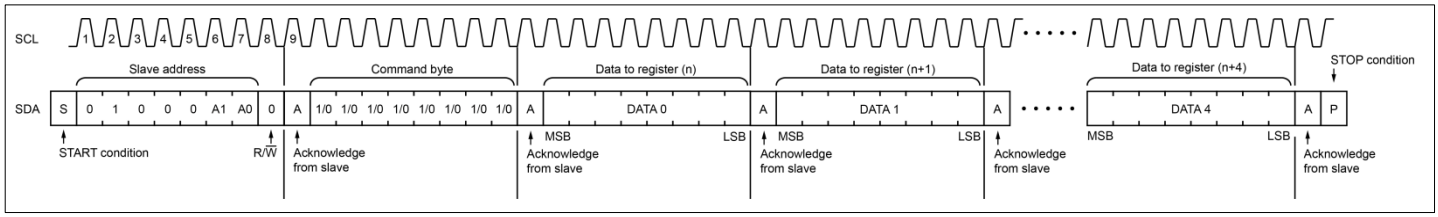


Figure 2. Write to Device Register

ii. READ Commands

To read data from the PI4IOE5V6534Q, the bus master must first send the PI4IOE5V6534Q address with the least significant bit set to a logic 0. The command byte is sent after the address and determines which register is to be accessed.

After a restart or a STOP followed by a START condition, the device address is sent again, but this time the least significant bit is set to a logic 1 to read data. Data from the register defined by the command byte is sent by the PI4IOE5V6534Q. Additional bytes may be read after the first byte read is complete and will reflect the next register in the group. For example, if Input Port 1 is read,

the next byte read is Input Port 2. There is no limit on the number of data bytes received in one read transmission, but one the final byte received the bus master must not acknowledge the data.
After a subsequent restart or a STOP followed by a START condition, the command byte contains the value of the next register to be read in the group. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 2.

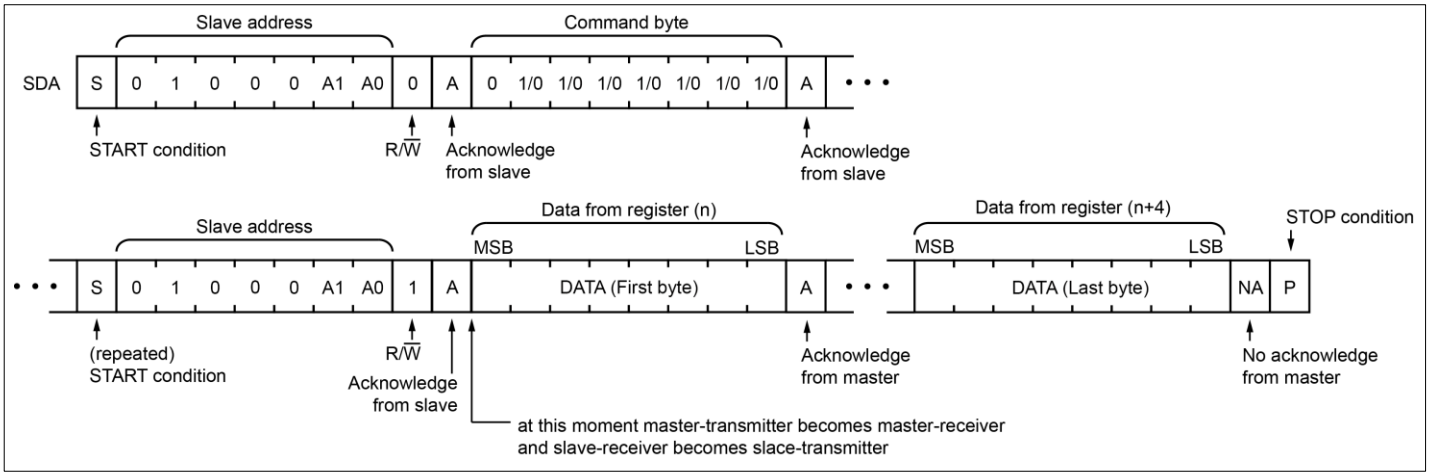
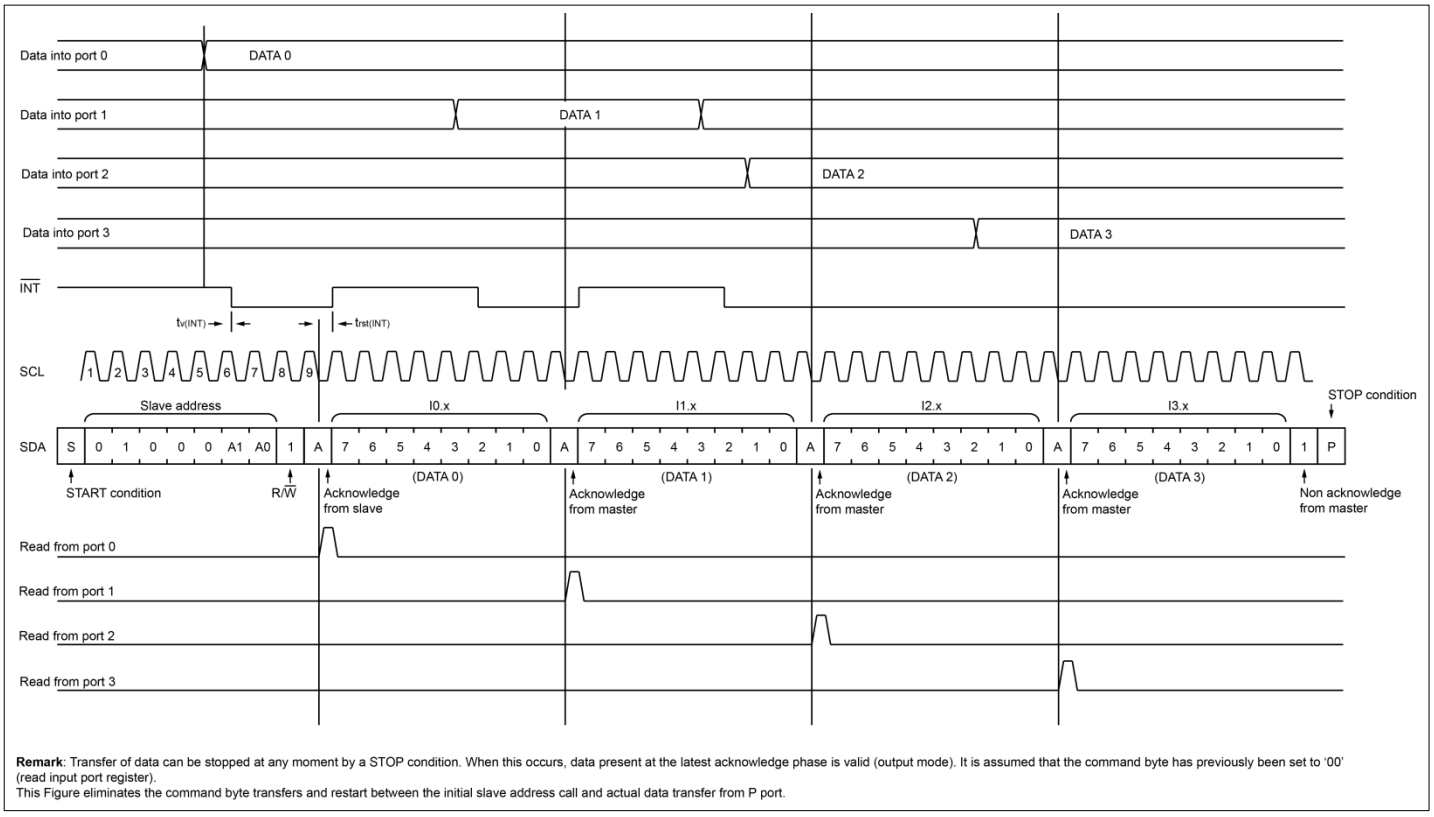
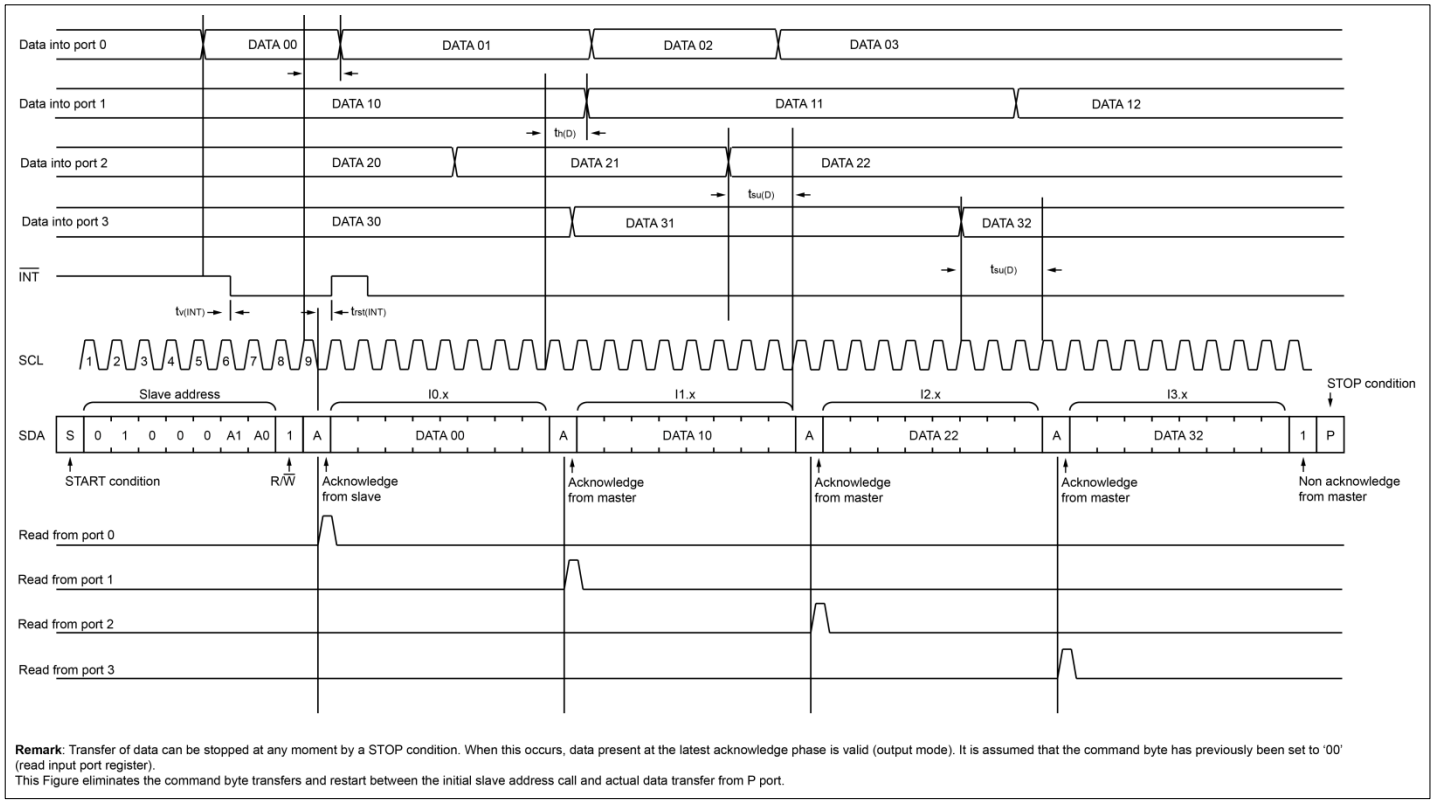


Figure 3. Read from Device Register



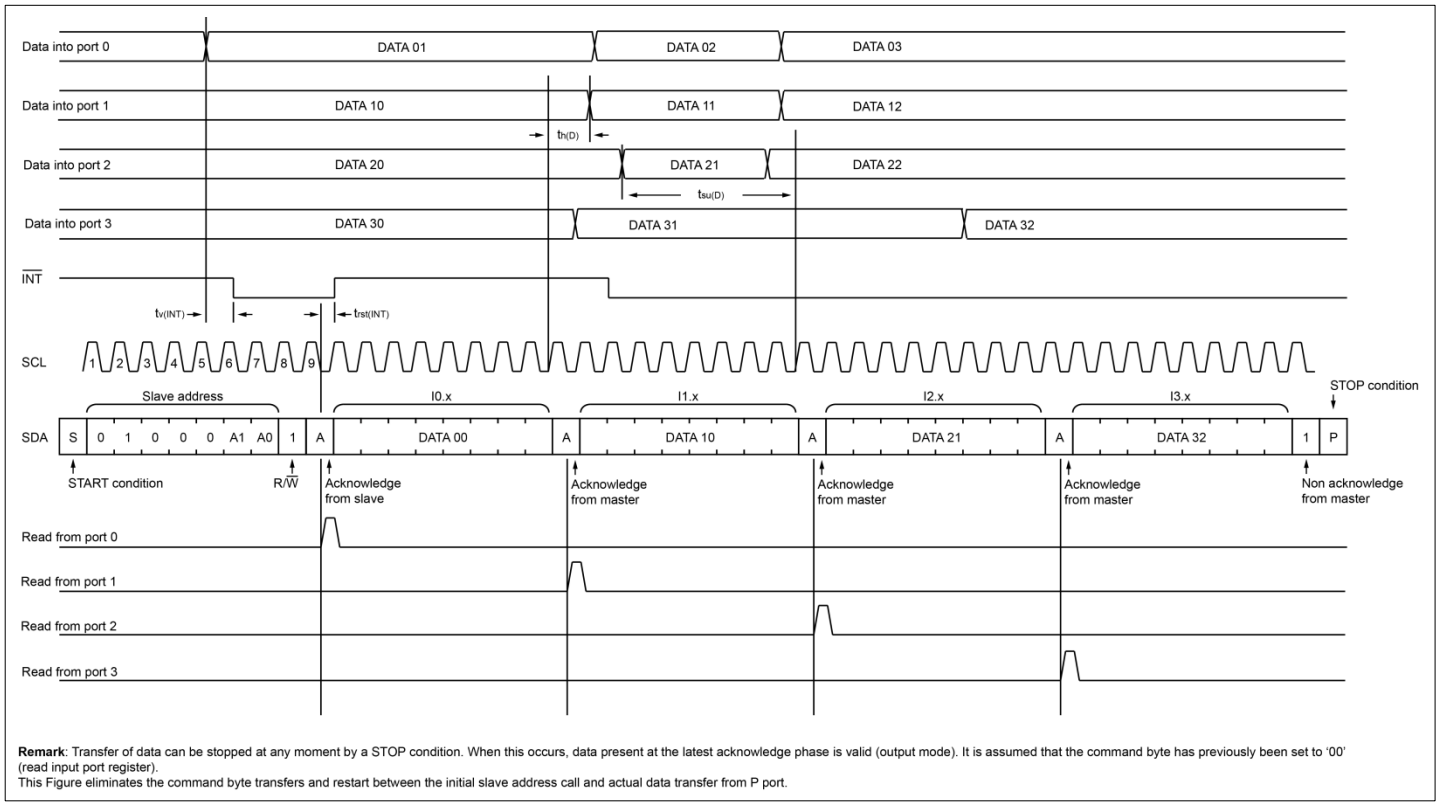
Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).
This Figure eliminates the command byte transfers and restart between the initial slave address call and actual data transfer from P port.

Figure 4. Read Input Port Register (non-latched), Scenario 1



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).
This Figure eliminates the command byte transfers and restart between the initial slave address call and actual data transfer from P port.

Figure 5. Read Input Port Register (non-latched), Scenario 2



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).
This Figure eliminates the command byte transfers and restart between the initial slave address call and actual data transfer from P port.

Figure 6. Read Input Port Register (non-latched), Scenario 3

B. Slave Address

ADDR is the hardware address package pin and is held to SCL, SDA, VSS or VDD to assign one of the 4 possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

Table 1 shows all four slave addresses by connecting the ADDR pin to SCL, SDA, VSS, or VDD

Table 1: PI4IOE5V6534Q Address Map

ADDR	High-Order Address Bits					Variable Portion of Address		Address
	A6	A5	A4	A3	A2	A1	A0	
SCL	0	1	0	0	0	0	0	40h
SDA						0	1	42h
V_{SS}						1	0	44h
V_{DD}						1	1	46h

C. Interface Definition

Table 2: Interface Definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I2C-bus Slave Address	0	1	0	0	0	A1	A0	R/$\overline{W}$
I/O Data Bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
	P3.7	P2.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
							P4.1	P4.0

D. Software Reset

The Software Reset Call allows all the devices in the I^2C-bus to be reset to the power-up state value through a specific formatted I^2C-bus command. To be performed correctly, it implies that the I^2C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I2C-bus master.
2. The reserved General Call I2C-bus address '0000 000' with the R/$\overline{W}$ bit set to 0 (write) is sent by the I2C-bus master.
3. The device acknowledges after seeing the General Call address '0000 0000' (00h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I2C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
   - The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.

If more than 1 byte of data is sent, the device does not acknowledge any more.

5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I^2C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

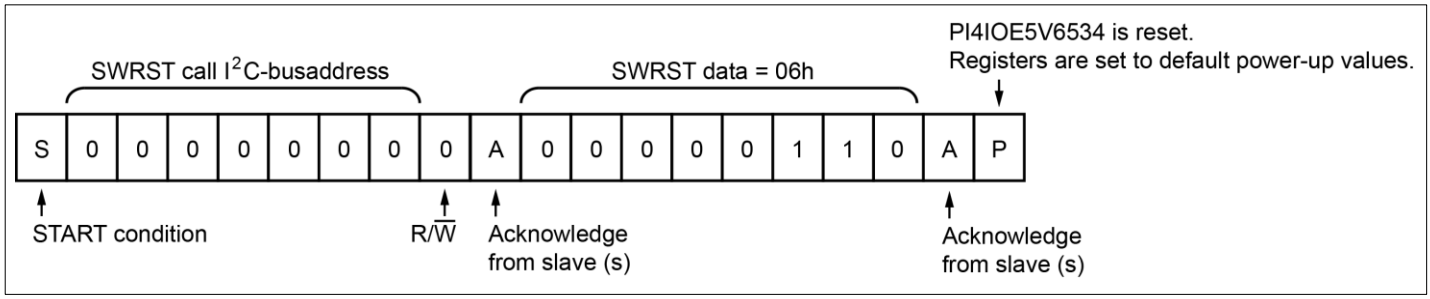


Figure 7. Software Reset Sequence

E. Device ID

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer.
- 9 bits with the part identification, assigned by manufacturer.
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I2C-bus address followed by the R/W bit set to 0 (write): '1111 1000'.
3. The master sends the I2C-bus slave address of the slave device it needs to identify. The LSB is a 'Don't care' value. Only one device must acknowledge this byte (the one that has the I^2C-bus slave address).
4. The master sends a Re-START command.

Remark: A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID Read cannot be performed.

5. The master sends the Reserved Device ID I^2C-bus address followed by the R/$\overline{W}$ bit set to 1 (read): '1111 1001'.
6. The Device ID Read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte), and then the 3 die revision bits (3 LSBs of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

Remark: The reading of the Device ID can be stopped anytime by sending a NACK command.
If the master continues to ACK the bytes after the third byte, the slave rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

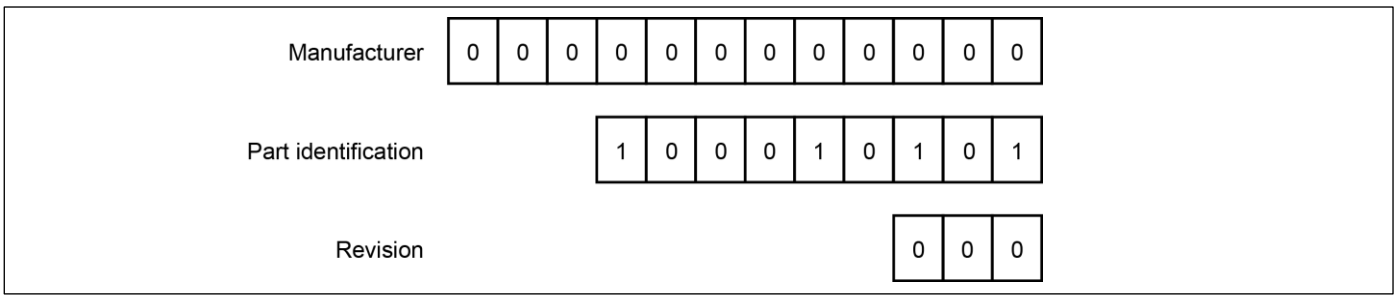


Figure 8. PI4IOE5V6534Q Device ID Field

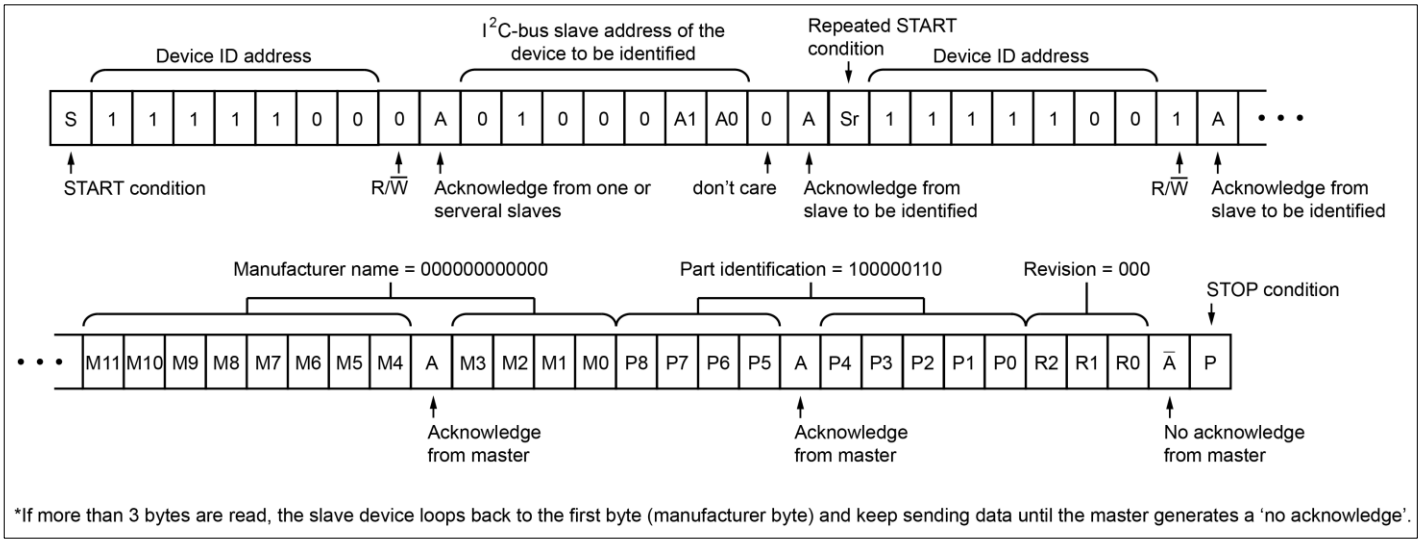


Figure 9. Device ID Field Reading

F. Register Address

Following the successful acknowledgement of the address byte, the bus master sends a register address, which is stored in the Pointer register in the PI4IOE5V6534Q. The lowest 7 bits (B[6:0] in Table 3) are used as a pointer to determine which register is accessed and the highest bit is used as Auto-Increment (AI) as shown in Figure 10. At power- up, hardware or software reset, the pointer register defaults to 00h, with the AI bit set to '0' and the lowest seven bits set to '000 0000'.

When the Auto-Increment bit is set (AI = 1), the seven low -order bits of the pointer register are automatically incremented after a read or write until a STOP condition is encountered. This allows the user to program the registers sequentially without modifying the pointer register. The contents of these bits will roll over to '000 0000' after the last register (address = 6Fh) is accessed. Unimplemented register addresses (reserved registers) are skipped. If more than 82 bytes are written, the address will loop back to the register which is indicated by the seven low-order bits in the pointer register, and previously-written data will be overwritten. A STOP condition will keep the pointer register value in the last read or write location.

When the Auto-Increment bit is cleared (AI = 0), the content of pointer register bits are automatically incremented after a read or write for 5-register group which allows the user to program each of the 5-register group sequentially. If more than 5 bytes of data are read or written when AI is 0, previous data in the selected registers will be overwritten. For example: if input port 3 is read first, the next 2nd byte will be input port 4, and next 3nd byte will be input port 0, there is no limit on the number of data bytes for this read operation. There are two special 9-register groups: output drive strength (30h~38h) and interrupt edge (54h~5Ch) registers will allow user to program each of the 9-register group sequentially. Only Output port configuration register location (53h) remains in the same location after a successive read or write.

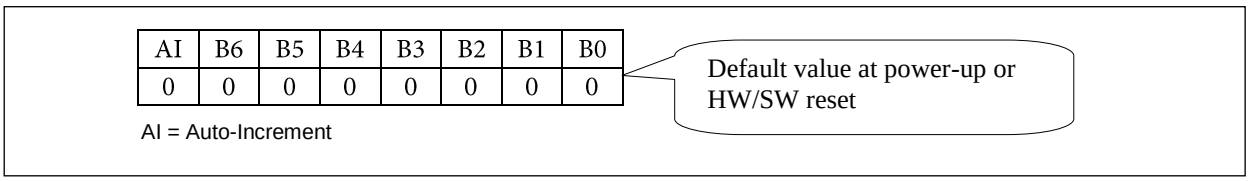


Figure 10. Pointer Register Bits

The data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, Configuration, or the extended features of the device). This register is WRITE only.

Table 3. Register Address

Register Address Bits								Register	Protocol	Power-up default
B6	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**Hex**			
0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx
0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx
0	0	0	0	0	1	0	02h	Input port 2	read byte	xxxx xxxx
0	0	0	0	0	1	1	03h	Input port 3	read byte	xxxx xxxx
0	0	0	0	1	0	0	04h	Input port 4	read byte	0000 00xx
0	0	0	0	1	0	1	05h	Output port 0	read/write byte	1111 1111
0	0	0	0	1	1	0	06h	Output port 1	read/write byte	1111 1111
0	0	0	0	1	1	1	07h	Output port 2	read/write byte	1111 1111
0	0	0	1	0	0	0	08h	Output port 3	read/write byte	1111 1111
0	0	0	1	0	0	1	09h	Output port 4	read/write byte	0000 0011
0	0	0	1	0	1	0	0Ah	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	1	0	1	1	0Bh	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	1	1	0	0	0Ch	Polarity Inversion port 2	read/write byte	0000 0000
0	0	0	1	1	0	1	0Dh	Polarity Inversion port 3	read/write byte	0000 0000
0	0	0	1	1	1	0	0Eh	Polarity Inversion port 4	read/write byte	0000 0000
0	0	0	1	1	1	1	0Fh	Configuration port 0	read/write byte	1111 1111
0	0	1	0	0	0	0	10h	Configuration port 1	read/write byte	1111 1111
0	0	1	0	0	0	1	11h	Configuration port 2	read/write byte	1111 1111
0	0	1	0	0	1	0	12h	Configuration port 3	read/write byte	1111 1111
0	0	1	0	0	1	1	13h	Configuration port 4	read/write byte	0000 0011
-	-	-	-	-	-	-	14h to 2Fh	Reserved	Reserved	Reserved
0	1	1	0	0	0	0	30h	Output drive strength register port 0A	read/write byte	1111 1111
0	1	1	0	0	0	1	31h	Output drive strength register port 0B	read/write byte	1111 1111
0	1	1	0	0	1	0	32h	Output drive strength register port 1A	read/write byte	1111 1111
0	1	1	0	0	1	1	33h	Output drive strength register port 1B	read/write byte	1111 1111
0	1	1	0	1	0	0	34h	Output drive strength register port 2A	read/write byte	1111 1111
0	1	1	0	1	0	1	35h	Output drive strength register port 2B	read/write byte	1111 1111
0	1	1	0	1	1	0	36h	Output drive strength register port 3A	read/write byte	1111 1111
0	1	1	0	1	1	1	37h	Output drive strength register port 3B	read/write byte	1111 1111
0	1	1	1	0	0	0	38h	Output drive strength register port 4A	read/write byte	0000 1111
0	1	1	1	0	0	1	39h	Reserved	Reserved	Reserved
0	1	1	1	0	1	0	3Ah	Input latch register Port 0	read/write byte	0000 0000
0	1	1	1	0	1	1	3Bh	Input latch register Port 1	read/write byte	0000 0000
0	1	1	1	1	0	0	3Ch	Input latch register Port 2	read/write byte	0000 0000
0	1	1	1	1	0	1	3Dh	Input latch register Port 3	read/write byte	0000 0000
0	1	1	1	1	1	0	3Eh	Input latch register Port 4	read/write byte	0000 0000
0	1	1	1	1	1	1	3Fh	Pull-up/pull-down enable register Port 0	read/write byte	0000 0000
1	0	0	0	0	0	0	40h	Pull-up/pull-down enable register Port 1	read/write byte	0000 0000
1	0	0	0	0	0	1	41h	Pull-up/pull-down enable register Port 2	read/write byte	0000 0000
1	0	0	0	0	1	0	42h	Pull-up/pull-down enable register Port 3	read/write byte	0000 0000
1	0	0	0	0	1	1	43h	Pull-up/pull-down enable register Port 4	read/write byte	0000 0000

Register Address Bits								Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0	Hex			
1	0	0	0	1	0	0	44h	Pull-up/pull-down selection register Port 0	read/write byte	1111 1111
1	0	0	0	1	0	1	45h	Pull-up/pull-down selection register Port 1	read/write byte	1111 1111
1	0	0	0	1	1	0	46h	Pull-up/pull-down selection register Port 2	read/write byte	1111 1111
1	0	0	0	1	1	1	47h	Pull-up/pull-down selection register Port 3	read/write byte	1111 1111
1	0	0	1	0	0	0	48h	Pull-up/pull-down selection register Port 4	read/write byte	0000 0011
1	0	0	1	0	0	1	49h	Interrupt mask register port 0	read/write byte	1111 1111
1	0	0	1	0	1	0	4Ah	Interrupt mask register port 1	read/write byte	1111 1111
1	0	0	1	0	1	1	4Bh	Interrupt mask register port 2	read/write byte	1111 1111
1	0	0	1	1	0	0	4Ch	Interrupt mask register port 3	read/write byte	1111 1111
1	0	0	1	1	0	1	4Dh	Interrupt mask register port 4	read/write byte	0000 0011
1	0	0	1	1	1	0	4Eh	Interrupt status register port 0	read byte	0000 0000
1	0	0	1	1	1	1	4Fh	Interrupt status register port 1	read byte	0000 0000
1	0	1	0	0	0	0	50h	Interrupt status register port 2	read byte	0000 0000
1	0	1	0	0	0	1	51h	Interrupt status register port 3	read byte	0000 0000
1	0	1	0	0	1	0	52h	Interrupt status register port 4	read byte	0000 0000
1	0	1	0	0	1	1	53h	Output port configuration register	read/write byte	0000 0000
1	0	1	0	1	0	0	54h	Interrupt edge register port 0A	read/write byte	0000 0000
1	0	1	0	1	0	1	55h	Interrupt edge register port 0B	read/write byte	0000 0000
1	0	1	0	1	1	0	56h	Interrupt edge register port 1A	read/write byte	0000 0000
1	0	1	0	1	1	1	57h	Interrupt edge register port 1B	read/write byte	0000 0000
1	0	1	1	0	0	0	58h	Interrupt edge register port 2A	read/write byte	0000 0000
1	0	1	1	0	0	1	59h	Interrupt edge register port 2B	read/write byte	0000 0000
1	0	1	1	0	1	0	5Ah	Interrupt edge register port 3A	read/write byte	0000 0000
1	0	1	1	0	1	1	5Bh	Interrupt edge register port 3B	read/write byte	0000 0000
1	0	1	1	1	0	0	5Ch	Interrupt edge register port 4A	read/write byte	0000 0000
1	0	1	1	1	0	1	5Dh	Reserved	Reserved	Reserved
1	0	1	1	1	1	0	5Eh	Interrupt clear register port 0	write byte	0000 0000
1	0	1	1	1	1	1	5Fh	Interrupt clear register port 1	write byte	0000 0000
1	1	0	0	0	0	0	60h	Interrupt clear register port 2	write byte	0000 0000
1	1	0	0	0	0	1	61h	Interrupt clear register port 3	write byte	0000 0000
1	1	0	0	0	1	0	62h	Interrupt clear register port 4	write byte	0000 0000
1	1	0	0	0	1	1	63h	Input Status register port 0	read byte	xxxx xxxx
1	1	0	0	1	0	0	64h	Input Status register port 1	read byte	xxxx xxxx
1	1	0	0	1	0	1	65h	Input Status register port 2	read byte	xxxx xxxx
1	1	0	0	1	1	0	66h	Input Status register port 3	read byte	xxxx xxxx
1	1	0	0	1	1	1	67h	Input Status register port 4	read byte	0000 00xx
1	1	0	1	0	0	0	68h	Individual pin output port 0 configuration register	read/write byte	0000 0000
1	1	0	1	0	0	1	69h	Individual pin output port 1 configuration register	read/write byte	0000 0000
1	1	0	1	0	1	0	6Ah	Individual pin output port 2 configuration register	read/write byte	0000 0000

Register Address Bits								Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0	Hex			
1	1	0	1	0	1	1	6Bh	Individual pin output port 3 configuration register	read/write byte	0000 0000
1	1	0	1	1	0	0	6Ch	Individual pin output port 4 configuration register	read/write byte	0000 0000
1	1	0	1	1	0	1	6Dh	Switch debounce enable 0	read/write byte	0000 0000
1	1	0	1	1	1	0	6Eh	Switch debounce enable 1	read/write byte	0000 0000
1	1	0	1	1	1	1	6Fh	Switch debounce count	read/write byte	0000 0000
-	-	-	-	-	-	-	70h to 7Fh	Reserved	Reserved	Reserved

G. Register Description

i. Input Port Register Pair (00h, 01h, 02h, 03h, 04h)

The Input port registers reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level. If a pin is configured as an output (registers 05h, 06h, 07h, 08h, 09h), the port value is equal to the actual voltage level on that pin. If the output is configured as open-drain (register 53h and registers 68h, 69h, 6Ah, 6Bh, 6Ch), the input port value is forced to 0. After reading input port registers, all interrupts will be cleared.

Table 4: Input Port Register Pair

Port 0 (address 00h)								
Bit	7	6	5	4	3	2	1	0
Name	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Port 1 (address 01h)								
Bit	7	6	5	4	3	2	1	0
Name	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

Port 2 (address 02h)								
Bit	7	6	5	4	3	2	1	0
Name	I2.7	I2.6	I2.5	I2.4	I2.3	I2.2	I2.1	I2.0
Default	X	X	X	X	X	X	X	X

Port 3 (address 03h)								
Bit	7	6	5	4	3	2	1	0
Name	I3.7	I3.6	I3.5	I3.4	I3.3	I3.2	I3.1	I3.0
Default	X	X	X	X	X	X	X	X

Port 4 (address 04h)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	I4.1	I4.0
Default	X	X	X	X	X	X	X	X

ii. Output Port Register Pair (05h, 06h, 07h, 08h, 09h)

The Output port registers shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, not the actual pin value.

Table 5: Output Port Register Pair

Port 0 (address 05h)								
Bit	7	6	5	4	3	2	1	0
Name	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Port 1 (address 06h)								
Bit	7	6	5	4	3	2	1	0
Name	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

Port 2 (address 07h)								
Bit	7	6	5	4	3	2	1	0
Name	O2.7	O2.6	O2.5	O2.4	O2.3	O2.2	O2.1	O2.0
Default	1	1	1	1	1	1	1	1

Port 3 (address 08h)								
Bit	7	6	5	4	3	2	1	0
Name	O3.7	O3.6	O3.5	O3.4	O3.3	O3.2	O3.1	O3.0
Default	1	1	1	1	1	1	1	1

Port 4 (address 09h)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	O4.1	O4.0
Default	X	X	X	X	X	X	1	1

iii. Polarity Inversion Register Pair (0Ah, 0Bh, 0Ch, 0Dh, 0Eh)

The Polarity inversion registers allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained

Table 6: Polarity Inversion Port Register Pair

Port 0 (address 0Ah)								
Bit	7	6	5	4	3	2	1	0
Name	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Port 1 (address 0Bh)								
Bit	7	6	5	4	3	2	1	0
Name	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

Port 2 (address 0Ch)								
Bit	7	6	5	4	3	2	1	0
Name	N2.7	N2.6	N2.5	N2.4	N2.3	N2.2	N2.1	N2.0
Default	0	0	0	0	0	0	0	0

Port 3 (address 0Dh)								
Bit	7	6	5	4	3	2	1	0
Name	N3.7	N3.6	N3.5	N3.4	N3.3	N3.2	N3.1	N3.0
Default	0	0	0	0	0	0	0	0

Port 4 (address 0Eh)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	N4.1	N4.0
Default	X	X	X	X	X	X	0	0

iv. Configuration Register Pair (0Fh, 10h, 11h, 12h and 13h)

The Configuration registers configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output.

Table 7: Configuration Port Register Pair

Port 0 (address 0Fh)								
Bit	7	6	5	4	3	2	1	0
Name	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Port 1 (address 10h)								
Bit	7	6	5	4	3	2	1	0
Name	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Port 2 (address 11h)								
Bit	7	6	5	4	3	2	1	0
Name	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
Default	1	1	1	1	1	1	1	1

Port 3 (address 12h)								
Bit	7	6	5	4	3	2	1	0
Name	C3.7	C3.6	C3.5	C.4	C3.3	C3.2	C3.1	C3.0
Default	1	1	1	1	1	1	1	1

Port 4 (address 13h)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	C4.1	C4.0
Default	X	X	X	X	X	X	1	1

v. Output Drive Strength Register Pairs (30h, 31h, 32h, 33h, 34h, 35h, 36h, 37h and 38h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example Port 0.7 is controlled by register 31h CC0.7 (bits [7:6]), Port

0.6 is controlled by register 31h CC0.6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25x, 01b = 0.5x, 10b = 0.75x or 11b = 1x of the drive capability of the I/O.

Table 8: Current Control Port Register Pair

Port 0A (address 30h)								
Bit	7	6	5	4	3	2	1	0
Name	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Port 0B (address 31h)								
Bit	7	6	5	4	3	2	1	0
Name	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Port 1A (address 32h)								
Bit	7	6	5	4	3	2	1	0
Name	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Port 1B (address 33h)								
Bit	7	6	5	4	3	2	1	0
Name	CC1.7		CC1.6		CC1.5		CC1.4	

Port 2A (address 34h)								
Bit	7	6	5	4	3	2	1	0
Name	CC2.3		CC2.2		CC2.1		CC2.0	
Default	1	1	1	1	1	1	1	1

Port 2B (address 35h)								
Bit	7	6	5	4	3	2	1	0
Name	CC2.7		CC2.6		CC2.5		CC2.4	
Default	1	1	1	1	1	1	1	1

Port 3A (address 36h)								
Bit	7	6	5	4	3	2	1	0
Name	CC3.3		CC3.2		CC3.1		CC3.0	
Default	1	1	1	1	1	1	1	1

Port 3B (address 37h)								
Bit	7	6	5	4	3	2	1	0
Name	CC3.7		CC3.6		CC3.5		CC3.4	
Default	1	1	1	1	1	1	1	1

Port 4A (address 38h)								
Bit	7	6	5	4	3	2	1	0
Name	x		x		CC4.1		CC4.0	
Default	x	x	x	x	1	1	1	1

vi. Input Latch Register Pair (3Ah, 3Bh, 3Ch, 3Dh, 3Eh)

The input latch registers enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0, 1, 2, 3 and 4). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt.

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read '1'. The next read of the input port register bit 4 register should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is not cleared if the input latches register changes from latched to non-latched configuration and I/O pin is difference from its original state.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level.

Table 9: Input Latch Port Register Pair

Port 0 (address 3Ah)								
Bit	7	6	5	4	3	2	1	0
Name	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Port 1 (address 3Bh)								
Bit	7	6	5	4	3	2	1	0
Name	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

Port 2 (address 3Ch)								
Bit	7	6	5	4	3	2	1	0
Name	L2.7	L2.6	L2.5	L2.4	L2.3	L2.2	L2.1	L2.0
Default	0	0	0	0	0	0	0	0

Port 3 (address 3Dh)								
Bit	7	6	5	4	3	2	1	0
Name	L3.7	L3.6	L3.5	L3.4	L3.3	L3.2	L3.1	L3.0
Default	0	0	0	0	0	0	0	0

Port 4 (address 3Eh)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	L4.1	L4.0
Default	X	X	X	X	X	X	0	0

vii. Pull-up/Pull-down Enable Register Pair (3Fh, 40h, 41h, 42h, 43h)

These registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs. Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor.

Table 10: Pull-up/Pull-down Enable Port Register Pair

Port 0 (address 3Fh)								
Bit	7	6	5	4	3	2	1	0
Name	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

Port 1 (address 40h)								
Bit	7	6	5	4	3	2	1	0
Name	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	0	0	0	0	0	0	0	0

Port 2 (address 41h)								
Bit	7	6	5	4	3	2	1	0
Name	PE2.7	PE2.6	PE2.5	PE2.4	PE2.3	PE2.2	PE2.1	PE2.0
Default	0	0	0	0	0	0	0	0

Port 3 (address 42h)								
Bit	7	6	5	4	3	2	1	0
Name	PE3.7	PE3.6	PE3.5	PE3.4	PE3.3	PE3.2	PE3.1	PE3.0
Default	0	0	0	0	0	0	0	0

Port 4 (address 43h)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	PE4.1	PE4.0
Default	X	X	X	X	X	X	0	0

viii. Pull-up/pull-down Selection Register Pair (44h, 45h, 46h, 47h, 48h)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 k pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 k pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 k with minimum of 50 k and maximum of 150 k.

Table 11: Pull-up/Pull-down Selection Register Pair

Port 0 (address 44h)								
Bit	7	6	5	4	3	2	1	0
Name	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

Port 1 (address 45h)								
Bit	7	6	5	4	3	2	1	0
Name	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

Port 2 (address 46h)								
Bit	7	6	5	4	3	2	1	0
Name	PUD2.7	PUD2.6	PUD2.5	PUD2.4	PUD2.3	PUD2.2	PUD2.1	PUD2.0
Default	1	1	1	1	1	1	1	1

Port 3 (address 47h)								
Bit	7	6	5	4	3	2	1	0
Name	PUD3.7	PUD3.6	PUD3.5	PUD3.4	PUD3.3	PUD3.2	PUD3.1	PUD3.0
Default	1	1	1	1	1	1	1	1

Port 4 (address 48h)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	PUD4.1	PUD4.0
Default	X	X	X	X	X	X	1	1

ix. Interrupt Mask Register Pair (49h, 4Ah, 4Bh, 4Ch, 4Dh)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0. If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted. When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted.

Table 12: Interrupt Mask Port Register Bit Description

Port 0 (address 49h)								
Bit	7	6	5	4	3	2	1	0
Name	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Port 1 (address 4Ah)								
Bit	7	6	5	4	3	2	1	0
Name	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

Port 2 (address 4Bh)								
Bit	7	6	5	4	3	2	1	0
Name	M2.7	M2.6	M2.5	M2.4	M2.3	M2.2	M2.1	M2.0
Default	1	1	1	1	1	1	1	1

Port 3 (address 4Ch)								
Bit	7	6	5	4	3	2	1	0
Name	M3.7	M3.6	M3.5	M3.4	M3.3	M3.2	M3.1	M3.0
Default	1	1	1	1	1	1	1	1

Port 4 (address 4Dh)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	M4.1	M4.0
Default	X	X	X	X	X	X	1	1

x. Interrupt Status Register Pair (4Eh, 4Fh, 50h, 51h, 52h)

These read-only registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt. When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0.

Table 13: Interrupt Status Port Register Bit Description

Port 0 (address 4Eh)								
Bit	7	6	5	4	3	2	1	0
Name	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

Port 1 (address 4Fh)								
Bit	7	6	5	4	3	2	1	0
Name	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

Port 2 (address 50h)								
Bit	7	6	5	4	3	2	1	0
Name	S2.7	S2.6	S2.5	S2.4	S2.3	S2.2	S2.1	S2.0
Default	0	0	0	0	0	0	0	0

Port 3 (address 51h)								
Bit	7	6	5	4	3	2	1	0
Name	S3.7	S3.6	S3.5	S3.4	S3.3	S3.2	S3.1	S3.0
Default	0	0	0	0	0	0	0	0

Port 4 (address 52h)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	S4.1	S4.0
Default	X	X	X	X	X	X	0	0

xi. Output Port Configuration Register (53h)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull. A logic 1 configures the I/O as open-drain and the recommended command sequence is to program this register (53h) before the configuration register (0Fh, 10h, 11h, 12h, 13h) sets the port pins as outputs.
ODEN0 configures Port 0_x and ODEN1 configures Port 1_x, ODEN2 configures Port 2_x,
ODEN3 configures Port 3_x, and ODEN4 configures Port 4_x.
Individual pins may be programmed as open-drain or push-pull by programming Individual Pin Output Configuration registers (68h, 69h, 6Ah, 6Bh, 6Ch).
A register group read or write operation is not allowed on this register. Successive read or write accesses will remain at this register address.

Table 14: Output Port Configuration Register (address 53h)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	ODEN4	ODEN3	ODEN2	ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

xii. Interrupt Edge Registers (54h, 55h, 56h, 57h, 58h, 59h, 5Ah, 5Bh, 5Ch)

The interrupt edge registers determine what action on an input pin will cause an interrupt along with the Interrupt Mask registers. If the Interrupt is enabled (set '0' in the Mask register) and the action at the corresponding pin matches the required activity, the $\overline{\text{INT}}$ output will become active. The default value for each pin is 00b or level triggered, meaning a level change on the pin will cause an interrupt event. A level triggered action means a change in logic state (HIGH -to-LOW or LOW-to -HIGH), since the last read of the Input port (00h, 01, 02h, 03h , 04h) which can be latched with a corresponding '1' set in the Input Latch register (3Ah, 3Ah, 3Ch, 3Dh, 3Eh). If the Interrupt edge register entry is set to 11b, any edge, positive- or negative-going, causes an interrupt event. If an entry is 01b, only a positive-going edge will cause an interrupt event, while a 10b will require a negative-going edge to cause an interrupt event. These edge interrupt events are latched, regardless of the status of the Input Latch register (3Ah, 3Ah, 3Ch, 3Dh, 3Eh h). These edged interrupts can be cleared in a number of ways: Reading input port registers (00h, 01, 02h, 03h , 04h); setting the Interrupt Mask register (49h, 4Ah, 4Bh, 4Ch, 4Dh) to 1 (masked); setting the Interrupt Clear register (5Eh, 5Fh, 60h, 61h, 62h) to 1 (this is a write-only register); resetting the Interrupt Edge register (54h to 5Ch) back to 0.

Table 15: Interrupt Edge Port Register

Port 0A (address 54h)								
Bit	7	6	5	4	3	2	1	0
Name	IE0.3		IE0.2		IE0.1		IE0.0	
Default	0	0	0	0	0	0	0	0

Port 0B (address 55h)								
Bit	7	6	5	4	3	2	1	0
Name	IE0.7		IE0.6		IE0.5		IE0.4	
Default	0	0	0	0	0	0	0	0

Port 1A (address 56h)								
Bit	7	6	5	4	3	2	1	0
Name	IE1.3		IE1.2		IE1.1		IE1.0	
Default	0	0	0	0	0	0	0	0

Port 1B (address 57h)								
Bit	7	6	5	4	3	2	1	0
Name	IE1.7		IE1.6		IE1.5		IE1.4	
Default	0	0	0	0	0	0	0	0

Port 2A (address 58h)								
Bit	7	6	5	4	3	2	1	0
Name	IE2.3		IE2.2		IE2.1		IE2.0	
Default	0	0	0	0	0	0	0	0

Port 2B (address 59h)								
Bit	7	6	5	4	3	2	1	0
Name	IE2.7		IE2.6		IE2.5		IE2.4	
Default	0	0	0	0	0	0	0	0

Port 3A (address 5Ah)								
Bit	7	6	5	4	3	2	1	0
Name	IE3.3		IE3.2		IE3.1		IE3.0	
Default	0	0	0	0	0	0	0	0

Port 3B (address 5Bh)								
Bit	7	6	5	4	3	2	1	0
Name	IE3.7		IE3.6		IE3.5		IE3.4	
Default	0	0	0	0	0	0	0	0

Port 4A (address 5Ch)								
Bit	7	6	5	4	3	2	1	0
Name	x		x		IE4.1		IE4.0	
Default	0	0	0	0	0	0	0	0

Table 16 Interrupt Edge Bits (IEX.X)

Bit 1	Bit 0	Description
0	0	level-triggered interrupt
0	1	positive-going (rising) edge triggered interrupt
1	0	negative-going (falling) edge triggered interrupt
1	1	any edge (positive or negative-going) triggered interrupt

xiii. Interrupt Clear Registers (5Eh, 5Fh, 60h, 61h, 62h)

The write-only interrupt clear registers clear individual interrupt sources (status bit). Setting an individual bit or any combination of bits to logic 1 will reset the corresponding interrupt source, so if that source was the only event causing an interrupt, the $\overline{INT}$ will be cleared. After writing a logic 1 the bit returns to logic 0.

Table 17: Interrupt Clear Port Register Bit Description

Port 0 (address 5Eh)								
Bit	7	6	5	4	3	2	1	0
Name	IC0.7	IC0.6	IC0.5	IC0.4	IC0.3	IC0.2	IC0.1	IC0.0
Default	0	0	0	0	0	0	0	0

Port 1 (address 5Fh)								
Bit	7	6	5	4	3	2	1	0
Name	IC1.7	IC1.6	IC1.5	IC1.4	IC1.3	IC1.2	IC1.1	IC1.0
Default	0	0	0	0	0	0	0	0

Port 2 (address 60h)								
Bit	7	6	5	4	3	2	1	0
Name	IC2.7	IC2.6	IC2.5	IC2.4	IC2.3	IC2.2	IC2.1	IC2.0
Default	0	0	0	0	0	0	0	0

Port 3 (address 61h)								
Bit	7	6	5	4	3	2	1	0
Name	IC 3.7	IC 3.6	IC 3.5	IC 3.4	IC 3.3	IC 3.2	IC 3.1	IC3.0
Default	0	0	0	0	0	0	0	0

Port 4 (address 62h)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	IC 4.1	IC 4.0
Default	X	X	X	X	X	X	0	0

xiv. Input Status Registers (63h, 64h, 65h, 66h, 67h)

The read-only input status registers function exactly like Input Port 0, 1, 2, 3 and 4 (00h, 01h, 02h, 03h, 04h) without resetting the interrupt logic. This allows inspection of the actual state of the input pins without upsetting internal logic. If the pin is configured as an input, the port read is unaffected by input latch logic or other features, the state of the register is simply a reflection of the current state of the input pins. If a pin is configured as an output by the Configuration register (0Fh, 10h, 11h, 12h, 13h), and is also configured as open-drain (register 53h and 68h, 69h, 6Ah, 6Bh, 6Ch), the read for that pin will always return 0, otherwise that state of that pin is returned.

Table 18: Input Status Port Register Bit Description

Port 0 (address 63h)								
Bit	7	6	5	4	3	2	1	0
Name	II0.7	II0.6	II0.5	II0.4	II0.3	II0.2	II0.1	II0.0
Default	X	X	X	X	X	X	X	X

Port 1 (address 64h)								
Bit	7	6	5	4	3	2	1	0
Name	II1.7	II1.6	II1.5	II1.4	II1.3	II1.2	II1.1	II1.0
Default	X	X	X	X	X	X	X	X

Port 2 (address 65h)								
Bit	7	6	5	4	3	2	1	0
Name	II2.7	II2.6	II2.5	II2.4	II2.3	II2.2	II2.1	II2.0
Default	X	X	X	X	X	X	X	X

Port 3 (address 66h)								
Bit	7	6	5	4	3	2	1	0
Name	II 3.7	II 3.6	II 3.5	II 3.4	II 3.3	II 3.2	II 3.1	II3.0
Default	X	X	X	X	X	X	X	X

Port 4 (address 67h)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	II 4.1	II 4.0
Default	X	X	X	X	X	X	X	X

xv. Individual Pin Output Configuration Registers (68h, 69h 6Ah, 6Bh, 6Ch)

The individual pin output configuration registers modify output configuration (push-pull or open-drain) set by the Output Port Configuration register (53h).
If the ODENx bit is set at logic 0 (push-pull), any bit set to logic 1 in the IOCRx register will reverse the output state of that pin only to open-drain. When ODENx bit is set at logic 1 (open-drain), a logic 1 in IOCRx will set that pin to push-pull.
The recommended command sequence to program the output pin is to program ODENx (53h), the IOCRx, and finally the Configuration register (0Fh, 10h, 11h, 12h, 13h) to set the pins as outputs.

Table 19: Individual Pin Output Configuration Register Bit Description

Port 0 (address 68h)								
Bit	7	6	5	4	3	2	1	0
Name	IOCR0.7	IOCR0.6	IOCR0.5	IOCR0.4	IOCR0.3	IOCR0.2	IOCR0.1	IOCR0.0
Default	0	0	0	0	0	0	0	0

Port 1 (address 69h)								
Bit	7	6	5	4	3	2	1	0
Name	IOCR1.7	IOCR1.6	IOCR1.5	IOCR1.4	IOCR1.3	IOCR1.2	IOCR1.1	IOCR1.0
Default	0	0	0	0	0	0	0	0

Port 2 (address 6Ah)								
Bit	7	6	5	4	3	2	1	0
Name	IOCR2.7	IOCR2.6	IOCR2.5	IOCR2.4	IOCR2.3	IOCR2.2	IOCR2.1	IOCR2.0
Default	0	0	0	0	0	0	0	0

Port 3 (address 6Bh)								
Bit	7	6	5	4	3	2	1	0
Name	IOCR 3.7	IOCR 3.6	IOCR 3.5	IOCR 3.4	IOCR 3.3	IOCR 3.2	IOCR 3.1	IOCR3.0
Default	0	0	0	0	0	0	0	0

Port 4 (address 6Ch)								
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	IOCR 4.1	IOCR 4.0
Default	X	X	X	X	X	X	0	0

xvi. Switch Debounce Enable Registers (6Dh, 6Eh)

The switch debounce enable registers enable the switch debounce function for Port 0 and Port 1 pins. If a pin on Port 0 or Port 1 is designated as an input, a logic 1 in the Switch debounce enable register will connect debounce logic to that pin. If a pin is assigned as an output (via Configuration Port 0 or Port 1 register) the debounce logic is not connected to that pin and it will function as a normal output. The switch debounce logic requires an oscillator time base input and if this function is used, P2_0 is designated as the oscillator input. If P2_0 is not configured as input, then switch debounce logic is not connected to any pin. See "L. Switch debounce circuitry" for additional information about Switch debounce logic functionality.

Table 20: Switch Debounce Enable Port 0 Register (address 6Dh) Bit Description

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	SD0.7	SD0.6	SD0.5	SD0.4	SD0.3	SD0.2	SD0.1	SD0.0
Default	0	0	0	0	0	0	0	0

Table 21: Switch Debounce Enable Port 1 Register (address 6Eh) Bit Description

Bit	7	6	5	4	3	2	1	0
Name	SD1.7	SD1.6	SD1.5	SD1.4	SD1.3	SD1.2	SD1.1	SD1.0
Default	0	0	0	0	0	0	0	0

xvii. Switch Debounce Count Registers (6Fh)

The switch debounce count register is used to count the debounce time that the switch debounce logic uses to determine if a switch connected to one of the Port 0 or Port 1 pins finally stays open (logic 1) or closed (logic 0). This number, together with the oscillator frequency supplied to P2_0, determines the debounce time (for example, the debounce time will be 10 us if this register is set to 0Ah and external oscillator frequency is 1 MHz). See "L. Switch debounce circuitry" for further information.

Table 22: Switch Debounce Count Register (address 6Fh) Bit Description

Bit	7	6	5	4	3	2	1	0
Name	SDC1.7	SDC1.6	SDC1.5	SDC1.4	SDC1.3	SDC1.2	SDC1.1	SDC1.0
Default	0	0	0	0	0	0	0	0

H. I/O Port

When an I/O is configured as an input, the pull-up FET and pull-down FET are off, which creates a high-impedance input. If the I/O is configured as an output, there are low impedance paths between the I/O pin and either $V_{DD(P)}$ or V_{SS} depending on the state of the Output Port Register. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation. Pull-up/down FETs series with resistors are enabled accordingly to the Pull-up or Pull-down Select Register and the Pull-up or Pull-down Enable Register. When the GPIO-port is set as an output, the input buffers are disabled such that the bus is allowed to float.

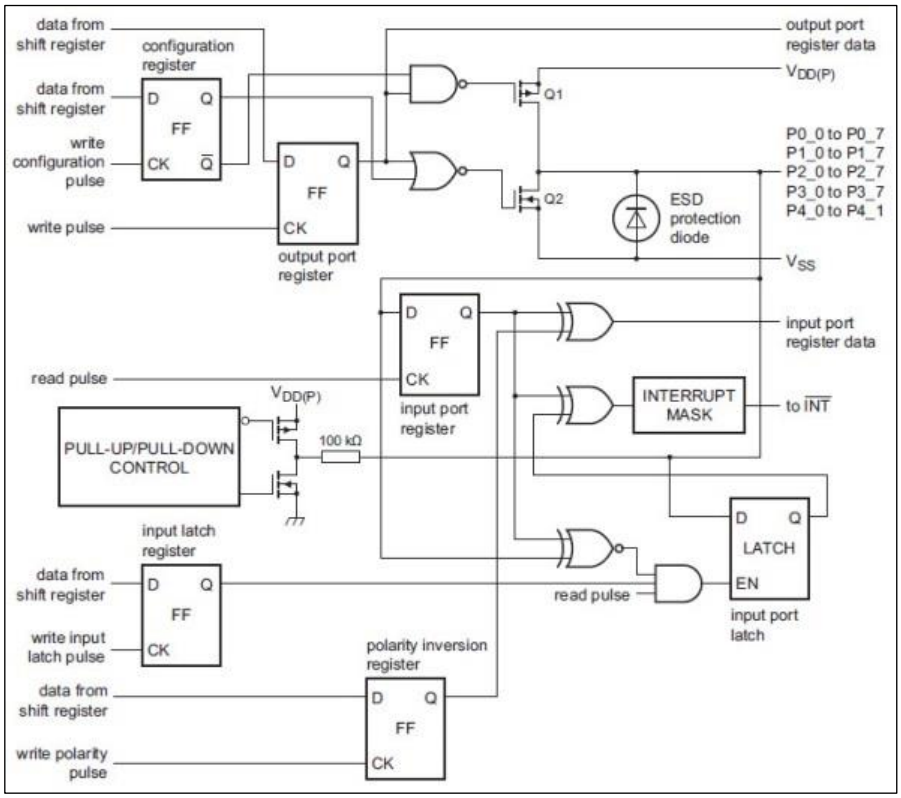


Figure 11: Block Diagram

I. Power-on Reset

When power is applied to $V_{DD(P)}$, an internal power-on reset holds the PI4IOE5V6534Q in a reset condition until $V_{DD(P)}$ has reached V_{POR}. At that point, the reset condition is released and the PI4IOE5V6534Q registers will initialize to their default states.

J. Reset Input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping $V_{DD(P)}$ at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of $t_{W(RST)}$. The PI4IOE5V6534Q registers are changed to their default state once $\overline{\text{RESET}}$ is low (0). Only when $\overline{\text{RESET}}$ is high (1), GPIO registers can be accessed by the I^2C pin. This input requires a pull-up resistor to $V_{DD(I2C\_bus)}$, if no active connection is used.

K. Interrupt Output ($\overline{\text{INT}}$)

The $\overline{\text{INT}}$ pin is a LOW-asserted open-drain output and requires an external pull-up resistor to $V_{DD(P)}$ or $V_{DD(I2C\_bus)}$ depending on the application. The PI4IOE5V6534Q signals an interrupt to the processor when any current input port state differs from its corresponding input port register state, the interrupt output pin is asserted (logic 0) to indicate the system master (MCU) that one of input port states has changed.

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt. A pin configured as an

output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the inputs after resetting is detected and is transmitted as $\overline{INT}$.

L. Switch Debounce Circuitry

Mechanical switches do not make clean make-or-break connections and the contacts can 'bounce' for a significant period of time before settling into a steady-state condition. This can confuse fast processors and make the physical interface difficult to design and the software interface difficult to make reliable.

The PI4IOE5V6534Q implements hardware to ease the hardware interface by debouncing switch closures with dedicated circuitry. P0_0 to P0_7, P1_0 to P1_7 can connect to this debounce hardware on a pin-by-pin basis. These switch debouncers remove bounce when a switch opens or closes by requiring that sequentially clocked inputs remain in the same state for a number of sampling periods. The output does not change until the input is stable for a programmable duration. The block diagram (Figure 12) shows the functional blocks consisting of an external oscillator, counter, edge detector, and D flip-flop. When the switch input state changes, the edge detector will reset the counter. When the switch input state is stable for the full qualification period, the counter clocks the flip-flop, updating the output.

To use the debounce circuitry, set the port pins (P0_0 to P0_7, and P1_0 to P1_7) with switches attached in the Switch Debounce Enable 0 and 1 registers (6Dh, 6Eh). Connect an external oscillator signal on P2_0, which serves as a time base to the debounce timer. Finally, set a delay time in the Switch Debounce Count register (6Fh). The combination of time base of the external oscillator and the debounce count sets the qualification debounce period or tDP. Note that all debounce counters will use the same time base and count, but they all function independently.

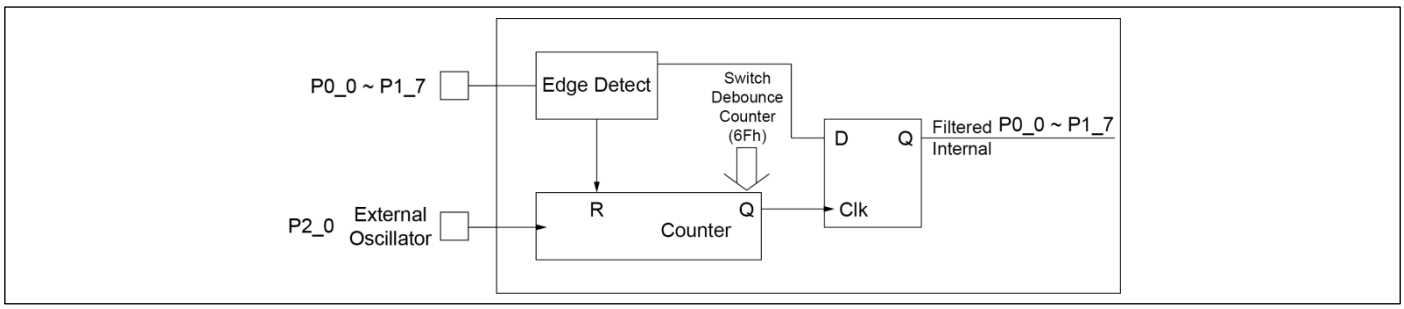


Figure 12. Debouncer Block Diagram

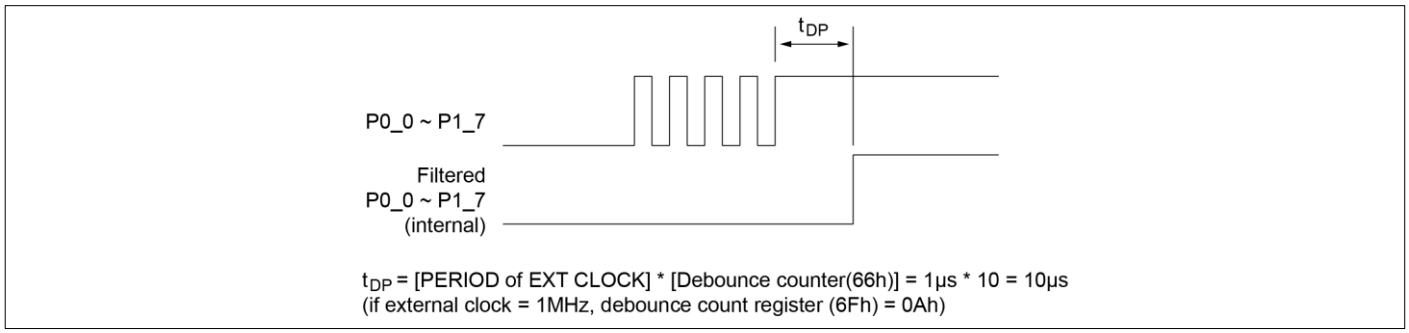


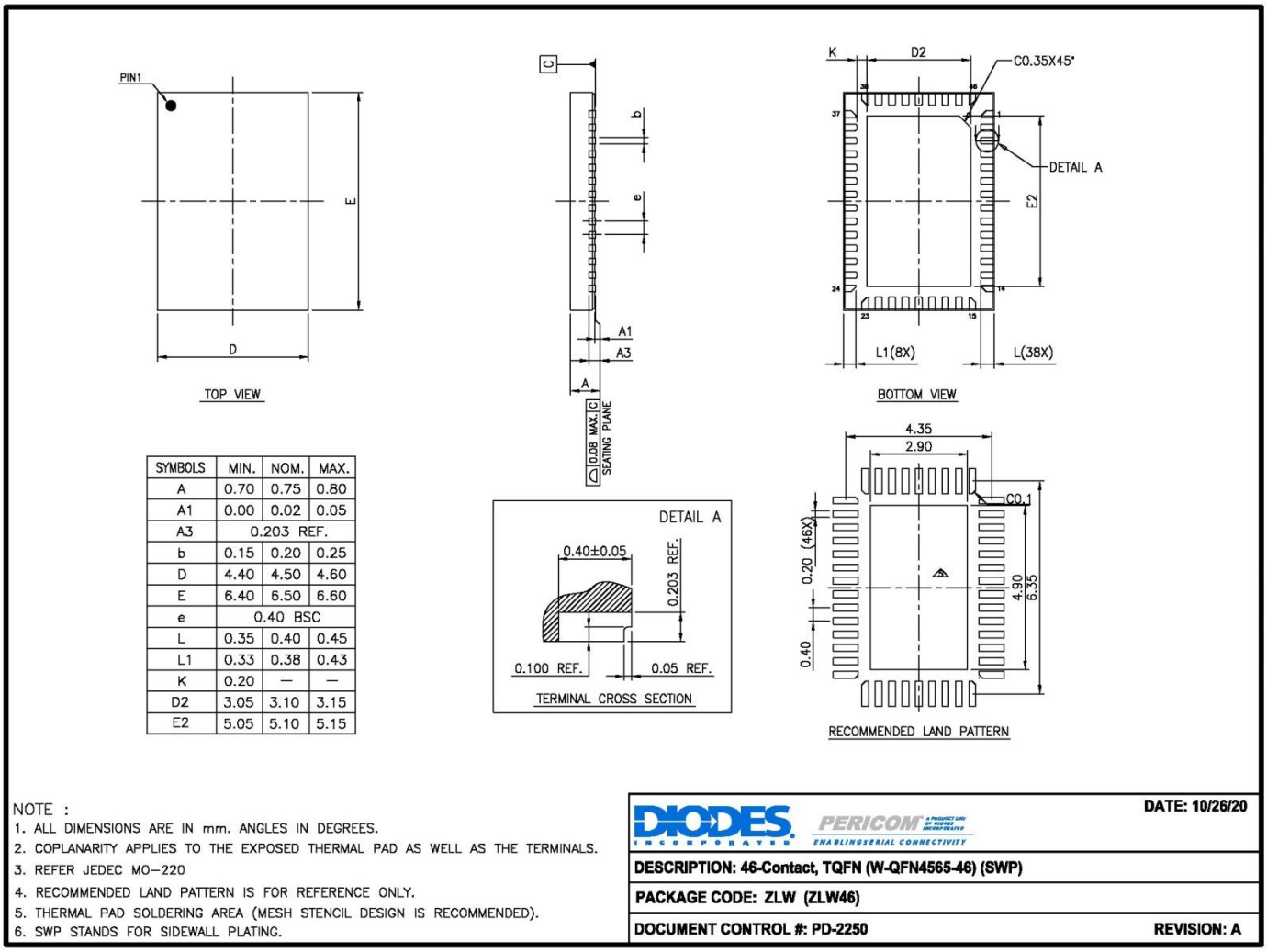
Figure 13. Switch Debounce Timing

Part Marking

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code
Date Code per MA-1251
Bar above fab code means Cu wire

Packaging Mechanical

46-TQFN (ZLW)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	4.40	4.50	4.60
E	6.40	6.50	6.60
e		0.40 BSC	
L	0.35	0.40	0.45
L1	0.33	0.38	0.43
K	0.20	—	—
D2	3.05	3.10	3.15
E2	5.05	5.10	5.15

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).
6. SWP STANDS FOR SIDEWALL PLATING.

DATE: 10/26/20

DESCRIPTION: 46-Contact, TQFN (W-QFN4565-46) (SWP)

PACKAGE CODE: ZLW (ZLW46)

DOCUMENT CONTROL #: PD-2250 REVISION: A

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Ordering Information

Part Number	Package Code	Package Description
PI4IOE5V6534Q2ZLWEX	ZLW	46-Contact, W-QFN4565-46 (TQFN) (SWP)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
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5. 2 = AEC-Q 100 Grade Level
6. E = Pb-free and Green
7. X suffix = Tape/Reel

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