

16-Kbit I²C Serial EEPROM High Temp Data Sheet

Device Selection Table

Part Number	V _{CC} Range	Max. Clock Frequency	Temp. Ranges	Packages
24LC16B	2.5V-5.5V	400 kHz	H	SN, OT

Features

- Single Supply with Operation Down to 2.5V
- Low-Power CMOS Technology:
 - Active current: 1 mA, typical
 - Standby current: 1 μ A, typical
- Two-Wire Serial Interface, I²C Compatible
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Clock Compatibility
- Page Write Time: 5 ms, Maximum
- Self-Timed Erase/Write Cycle
- 16-Byte Page Write Buffer
- Hardware Write-Protect
- ESD Protection > 4,000V
- More Than 1 Million Erase/Write Cycles
- Data Retention > 200 Years
- Factory Programming Available
- RoHS Compliant
- Temperature Ranges:
 - High (H): -40°C to +150°C
- Automotive AEC-Q100 Qualified

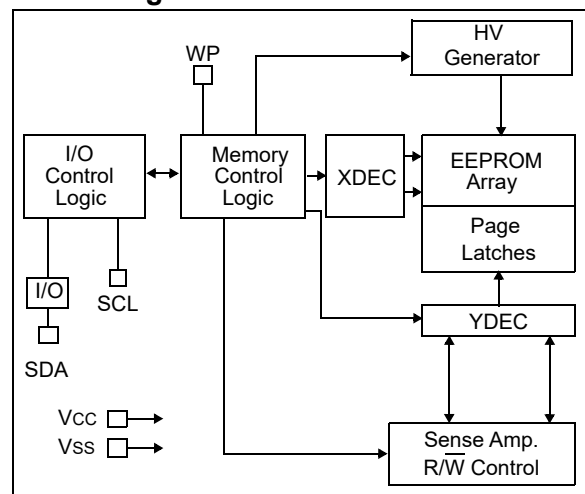
Packages

- 8-Lead SOIC and 5-Lead SOT-23

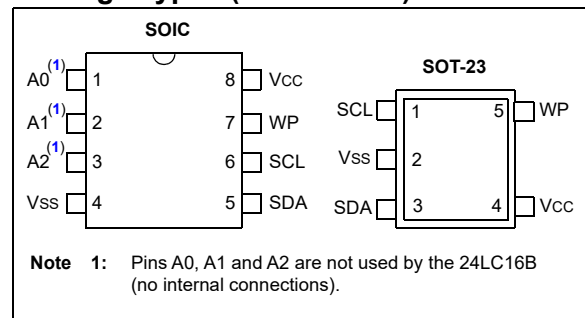
Description

The Microchip Technology Inc. 24LC16B is a 16-Kbit Electrically Erasable PROM (EEPROM). The device is organized as eight blocks of 256 x 8-bit memory with a two-wire serial interface. Its low-voltage design permits operation down to 2.5V with standby and active currents of only 1 μ A and 1 mA, respectively. The 24LC16B also has a page write capability for up to 16 bytes of data.

Block Diagram



Package Types (not to scale)



24LC16B

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V _{CC}	6.5V
All inputs and outputs w.r.t. V _{SS}	-0.3V to V _{CC} +1.0V
Storage temperature	-65°C to +155°C
Ambient temperature with power applied	-40°C to +150°C ⁽¹⁾
ESD protection on all pins	≥ 4 kV

Note 1: AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: High (H): T _A = -40°C to +150°C, V _{CC} = +2.5V to +5.5V			
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
D1	V _{IH}	High-Level Input Voltage	0.7 V _{CC}	—	V	
D2	V _{IL}	Low-Level Input Voltage	—	0.3 V _{CC}	V	
D3	V _{HYS}	Hysteresis of Schmitt Trigger Inputs	0.05 V _{CC}	—	V	Note 1
D4	V _{OL}	Low-Level Output Voltage	—	0.40	V	I _{OL} = 3.0 mA, V _{CC} = 2.5V
D5	I _{LI}	Input Leakage Current	—	±1	µA	V _{IN} = V _{SS} or V _{CC}
D6	I _{LO}	Output Leakage Current	—	±1	µA	V _{OUT} = V _{SS} or V _{CC}
D7	C _{IN} , C _{OUT}	Pin Capacitance (all inputs/outputs)	—	10	pF	V _{CC} = 5.0V (Note 1) T _A = +25°C, F _{CLK} = 1 MHz
D8	I _{CC} Write	Operating Current	—	3	mA	V _{CC} = 5.5V, SCL = 400 kHz
D9	I _{CC} Read		—	1	mA	
D10	I _{CCS}	Standby Current	—	1	µA	SDA = SCL = V _{CC} , WP = V _{SS} , I-Temp.
			—	5	µA	SDA = SCL = V _{CC} , WP = V _{SS} , H-Temp.

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: High (H): TA = -40°C to +150°C, VCC = +2.5V to +5.5V			
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
1	FCLK	Clock Frequency	—	400	kHz	
2	THIGH	Clock High Time	600	—	ns	
3	TLOW	Clock Low Time	1300	—	ns	
4	TR	SDA and SCL Rise Time	—	300	ns	Note 1
5	TF	SDA and SCL Fall Time	—	300	ns	Note 1
6	THD:STA	Start Condition Hold Time	600	—	ns	
7	TSU:STA	Start Condition Setup Time	600	—	ns	
8	THD:DAT	Data Input Hold Time	0	—	ns	Note 2
9	TSU:DAT	Data Input Setup Time	100	—	ns	
10	TSU:STO	Stop Condition Setup Time	600	—	ns	
11	TAA	Output Valid from Clock	—	900	ns	Note 2
12	TBUF	Bus free time: The time the bus must be free before a new transmission can start	1300	—	ns	
13	TOF	Output Fall Time from VIH minimum to VIL Maximum	20+0.1CB	250	ns	Note 1
14	TSP	Input Filter Spike Suppression (SDA and SCL pins)	—	50	ns	Note 1 and Note 3
15	TWC	Write Cycle Time (byte or page)	—	5	ms	
16		Endurance	1,000,000	—	cycles	+25°C, 5.5V, Page Mode (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

- 2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
- 3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a Ti specification for standard operation.
- 4:** This parameter is not tested but ensured by characterization.

24LC16B

FIGURE 1-1: BUS TIMING DATA

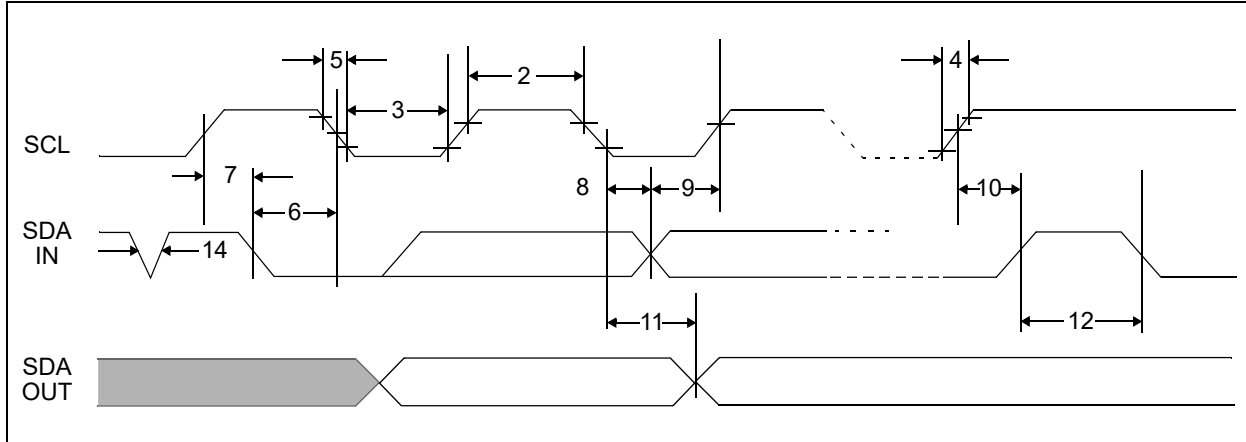
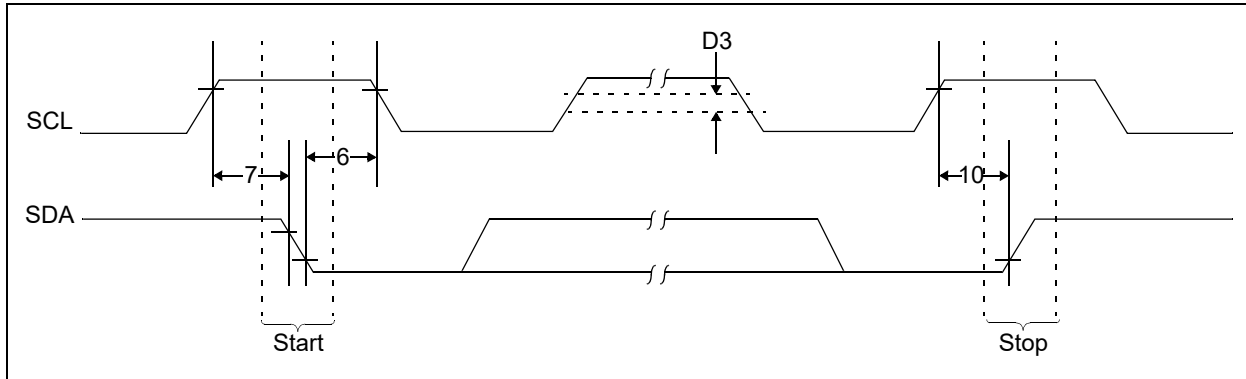


FIGURE 1-2: BUS TIMING START/STOP



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Name	SOIC	SOT-23	Description
A0	1	—	Not Connected
A1	2	—	Not Connected
A2	3	—	Not Connected
Vss	4	2	Ground
SDA	5	3	Serial Address/Data I/O
SCL	6	1	Serial Clock
WP	7	5	Write-Protect Input
Vcc	8	4	Power Supply

2.1 A0, A1, A2

The A0, A1 and A2 pins are not used by the 24LC16B. They may be left floating or tied to either Vss or Vcc.

2.2 Serial Address/Data Input/Output (SDA)

The SDA is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to Vcc (typical 10 kΩ for 100 kHz and 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating Start and Stop conditions.

2.3 Serial Clock (SCL)

The SCL input is used to synchronize the data transfer to and from the device.

2.4 Write-Protect (WP)

The WP pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to Vcc, write operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

24LC16B

3.0 FUNCTIONAL DESCRIPTION

The 24LC16B supports a bidirectional, two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a host device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24LC16B works as client. Both host and client can operate as transmitter or receiver, but the host device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is determined by the host device and is, theoretically, unlimited (although only the last 16 bytes will be stored when doing a write operation). When an overwrite does occur, it will replace data in a First-In First-Out (FIFO) principle.

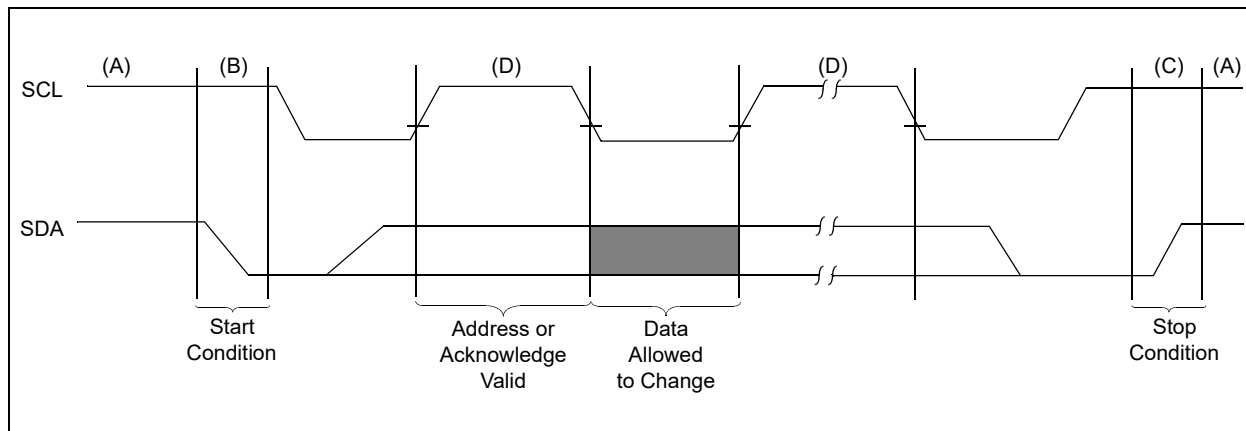
4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. The host device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note: The 24LC16B does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. During reads, a host must signal an end of data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24LC16B) will leave the data line high to enable the host to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the host device. The control byte consists of a four-bit control code. For the 24LC16B, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the block-select bits (B2, B1, B0). They are used by the host device to select which of the eight 256 word-blocks of memory are to be accessed. These bits are in effect the three Most Significant bits (MSb) of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore, the protocol can support only one 24LC16B per system. The combination of the 4-bit control code and the next three bits are called the client address.

The last bit of the control byte is the Read/Write ($\overline{R/W}$) bit and it defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. Following the Start condition, the 24LC16B monitors the SDA bus, checking the device type identifier being transmitted and, upon receiving a valid client address and the $\overline{R/W}$ bit, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the $\overline{R/W}$ bit, the 24LC16B will select a read or write operation.

The next byte received defines the address of the first data byte within the selected block (Figure 5-2). The word address byte uses all eight bits.

Operation	Control Code	Block Select	$\overline{R/W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 5-1: CONTROL BYTE ALLOCATION

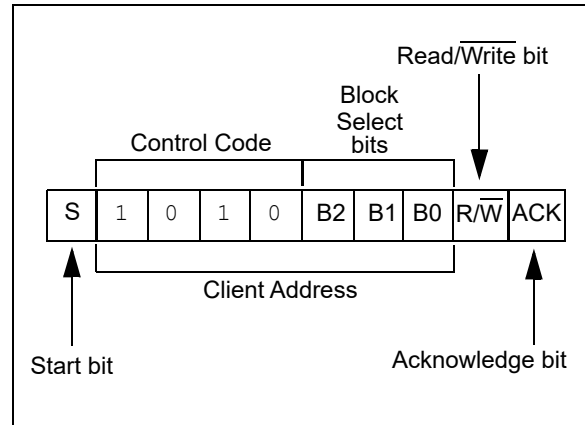
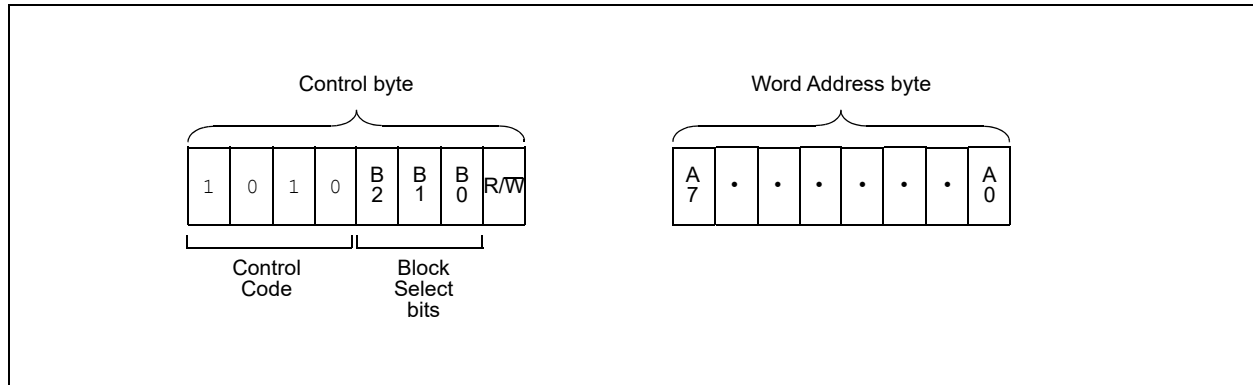


FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



24LC16B

6.0 WRITE OPERATION

6.1 Byte Write

Following the Start condition from the host, the device code (4 bits), the block address (3 bits) and the R/W bit, which is a logic-low, are placed onto the bus by the host transmitter. This indicates to the addressed client receiver that a byte with a word address will follow once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the word address and will be written into the Address Pointer of the 24LC16B. After receiving another Acknowledge signal from the 24LC16B, the host device will transmit the data word to be written into the addressed memory location. The 24LC16B acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and, during this time, the 24LC16B will not generate Acknowledge signals (Figure 6-1).

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC16B in the same way as in a byte write. However, instead of generating a Stop condition, the host transmits up to 16 data bytes to the 24LC16B, which are temporarily stored in the on-chip page buffer and will be written into memory once the host has transmitted a Stop condition. Upon receipt of each word, the four lower-order Address Pointer bits, which form the byte counter, are internally incremented by one.

The higher-order 7 bits of the word address remain constant. If the host should transmit more than 16 bytes prior to generating the Stop condition, the Address Pointer will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received an internal write cycle will begin (Figure 6-2).

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page-size') and end at addresses that are integer multiples of page size - 1. If a page write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

6.3 Write Protection

The WP pin allows the user to write-protect the entire array (000-7FF) when the pin is tied to VCC. If tied to VSS the write protection is disabled.

FIGURE 6-1: BYTE WRITE

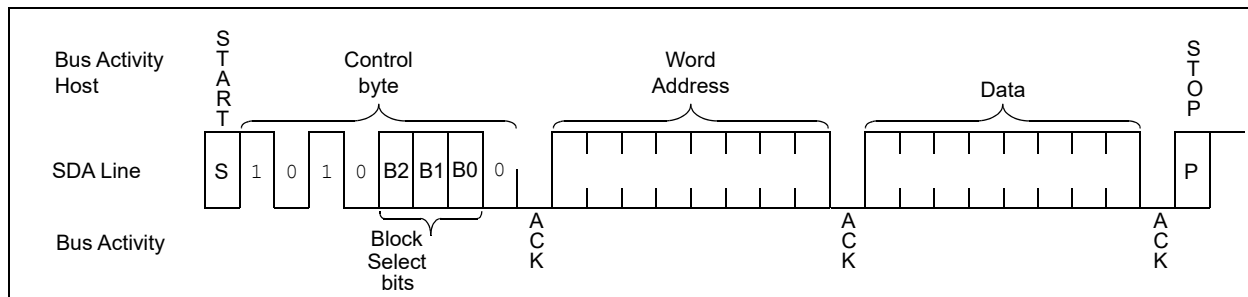
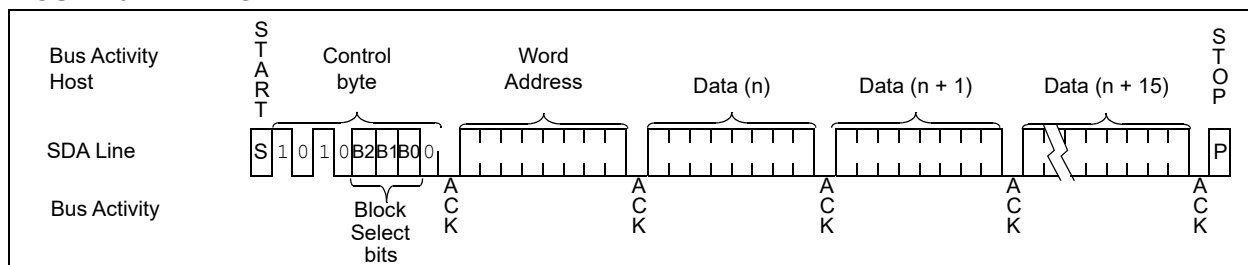


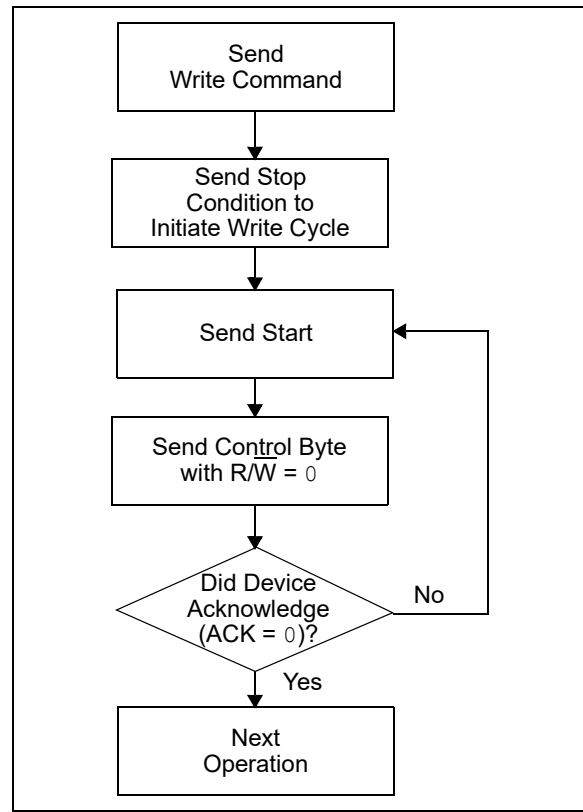
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the host, the device initiates the internally-timed write cycle and ACK polling can then be initiated immediately. This involves the host sending a Start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, no ACK will be returned. If the cycle is complete, the device will return the ACK and the host can then proceed with the next read or write operation. See [Figure 7-1](#) for a flow diagram of this operation.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



24LC16B

8.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/W bit of the client address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24LC16B contains an Address Pointer that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address 'n', the next current address read operation would access data from address $n + 1$. Upon receipt of the client address with R/W bit set to '1', the 24LC16B issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24LC16B discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24LC16B as part of a write operation. Once the word address is sent, the host generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again, but with the R/W bit set to a '1'. The 24LC16B will then issue an Acknowledge and transmit the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24LC16B will discontinue transmission (Figure 8-2). After a random Read command, the internal Address Pointer will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read, except that once the 24LC16B transmits the first data byte, the host issues an Acknowledge as opposed to a Stop condition in a random read. This directs the 24LC16B to transmit the next sequentially-addressed 8-bit word (Figure 8-3).

To provide sequential reads, the 24LC16B contains an internal Address Pointer that is incremented by one upon completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation, even on a noisy bus.

FIGURE 8-1: CURRENT ADDRESS READ

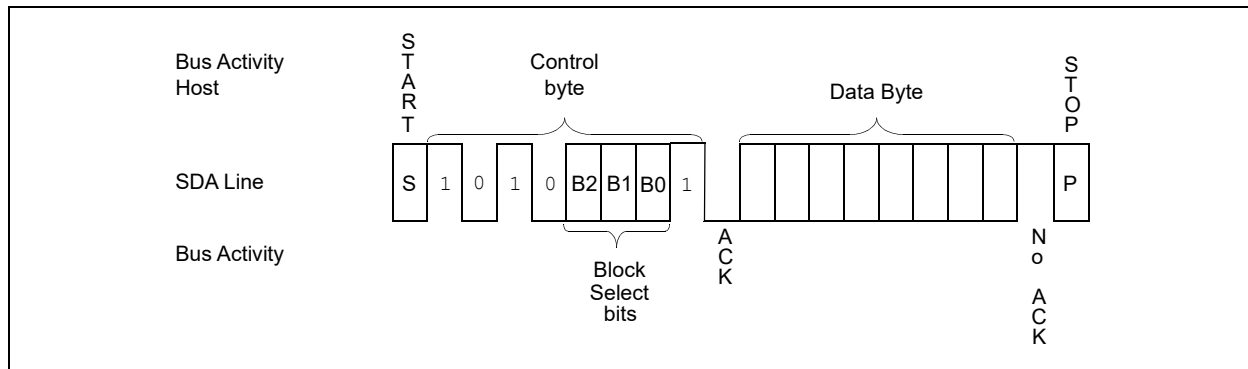


FIGURE 8-2: RANDOM READ

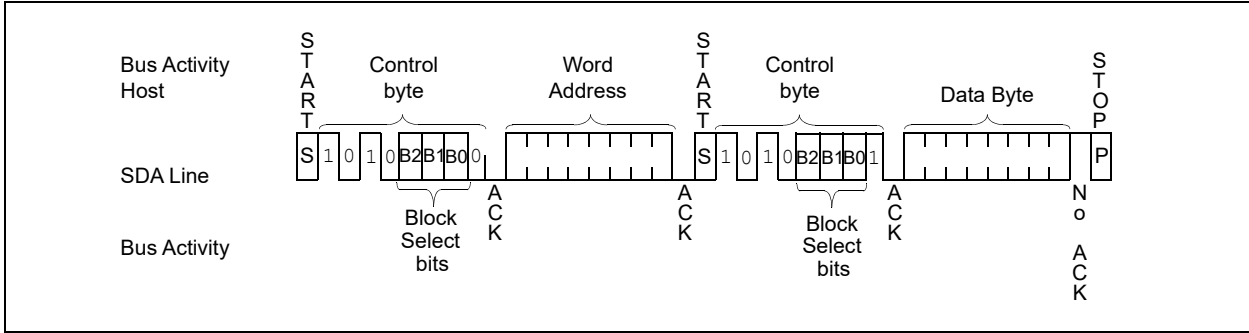
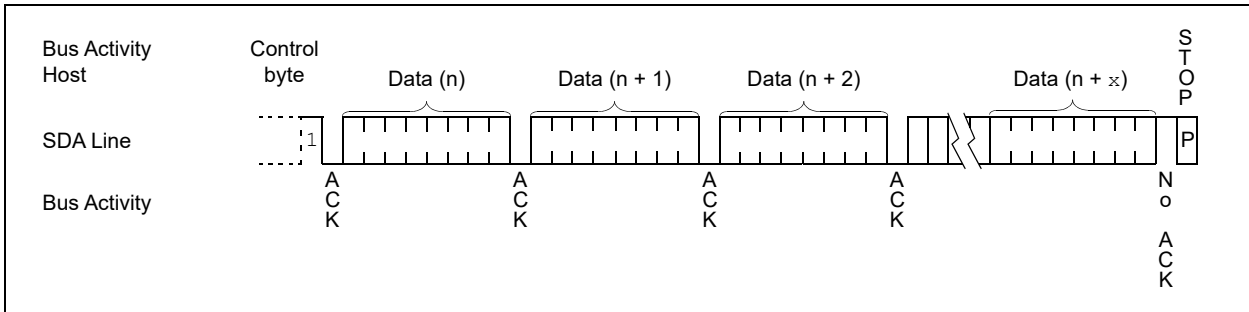


FIGURE 8-3: SEQUENTIAL READ

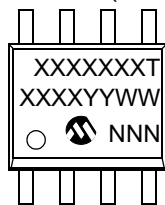


24LC16B

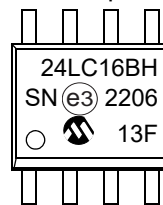
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

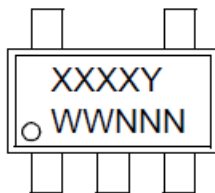
8-Lead SOIC (3.90 mm)



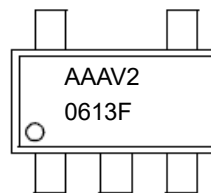
Example



5-Lead SOT-23



Example



Part Number	1 st Line Marking Codes	
	SOIC	SOT-23
24LC16B	24LC16BT ⁽¹⁾	AAAV

Note 1: T = Temperature grade (H)

Legend:	XX...X	Part number or part number code
	T	Temperature (H)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	JEDEC [®] designator for Matte Tin (Sn)

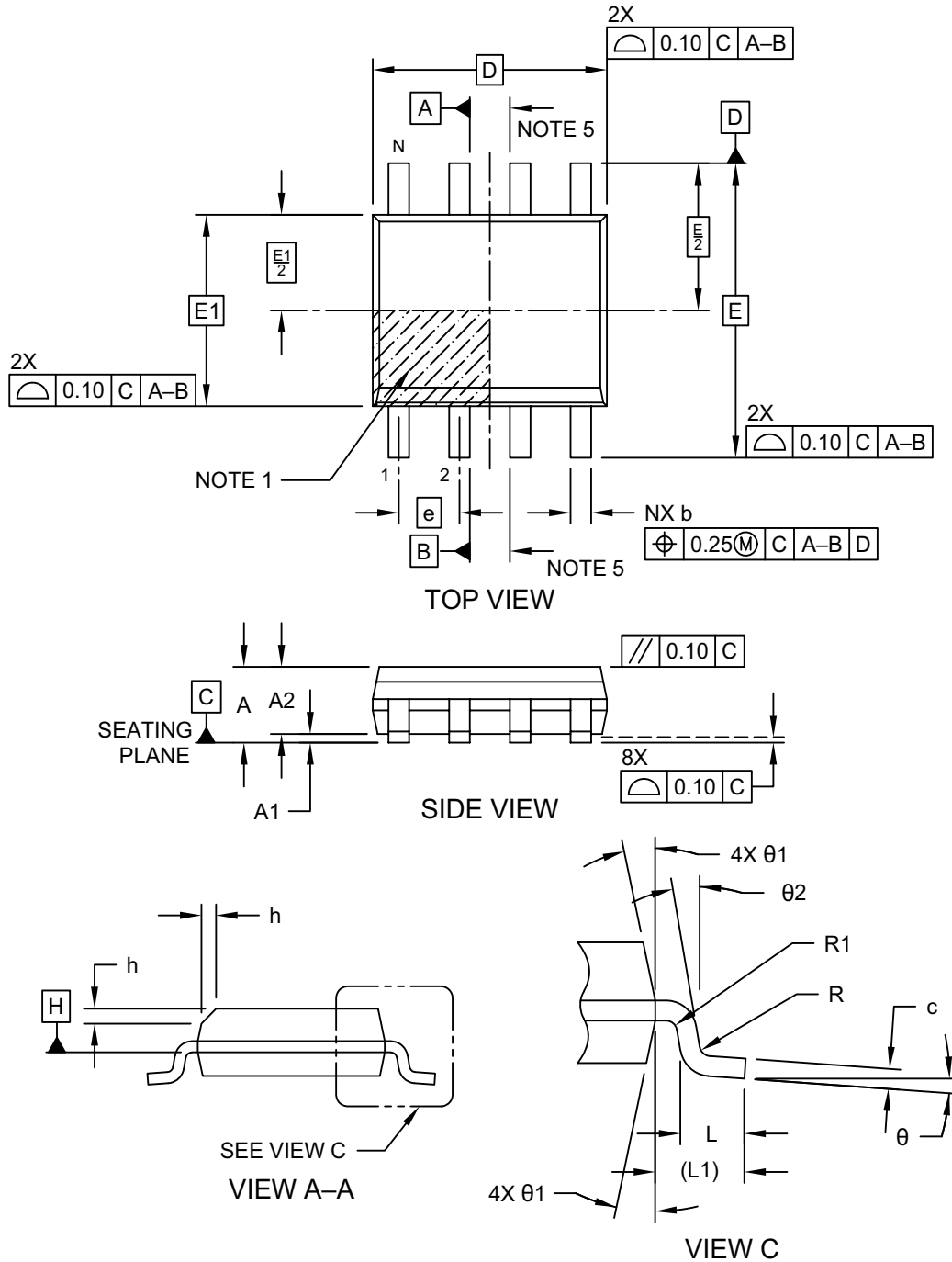
* Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

Note: For very small packages with no room for the JEDEC[®] designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

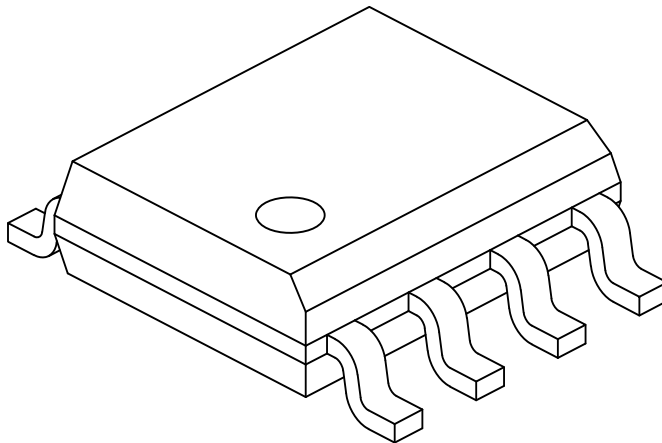


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24LC16B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		8		
Pitch	e		1.27 BSC		
Overall Height	A		–	–	1.75
Molded Package Thickness	A2		1.25	–	–
Standoff §	A1		0.10	–	0.25
Overall Width	E		6.00 BSC		
Molded Package Width	E1		3.90 BSC		
Overall Length	D		4.90 BSC		
Chamfer (Optional)	h		0.25	–	0.50
Foot Length	L		0.40	–	1.27
Footprint	L1		1.04 REF		
Lead Thickness	c		0.17	–	0.25
Lead Width	b		0.31	–	0.51
Lead Bend Radius	R		0.07	–	–
Lead Bend Radius	R1		0.07	–	–
Foot Angle	θ		0°	–	8°
Mold Draft Angle	θ1		5°	–	15°
Lead Angle	θ2		0°	–	8°

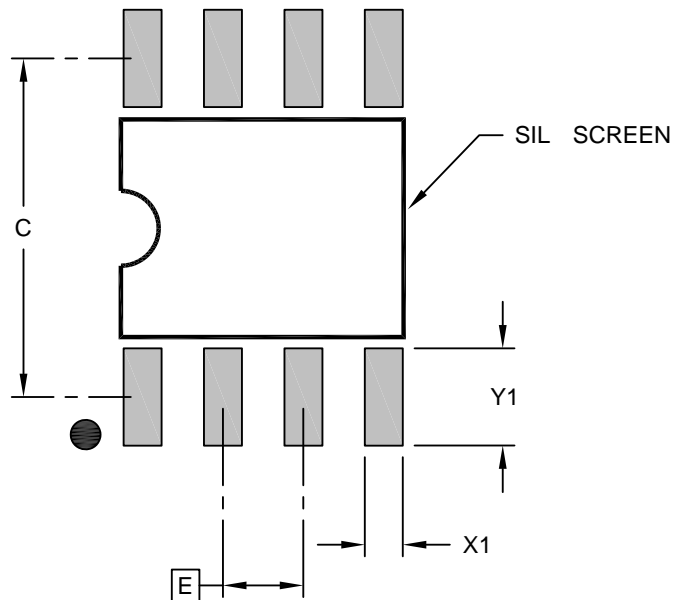
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev G Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

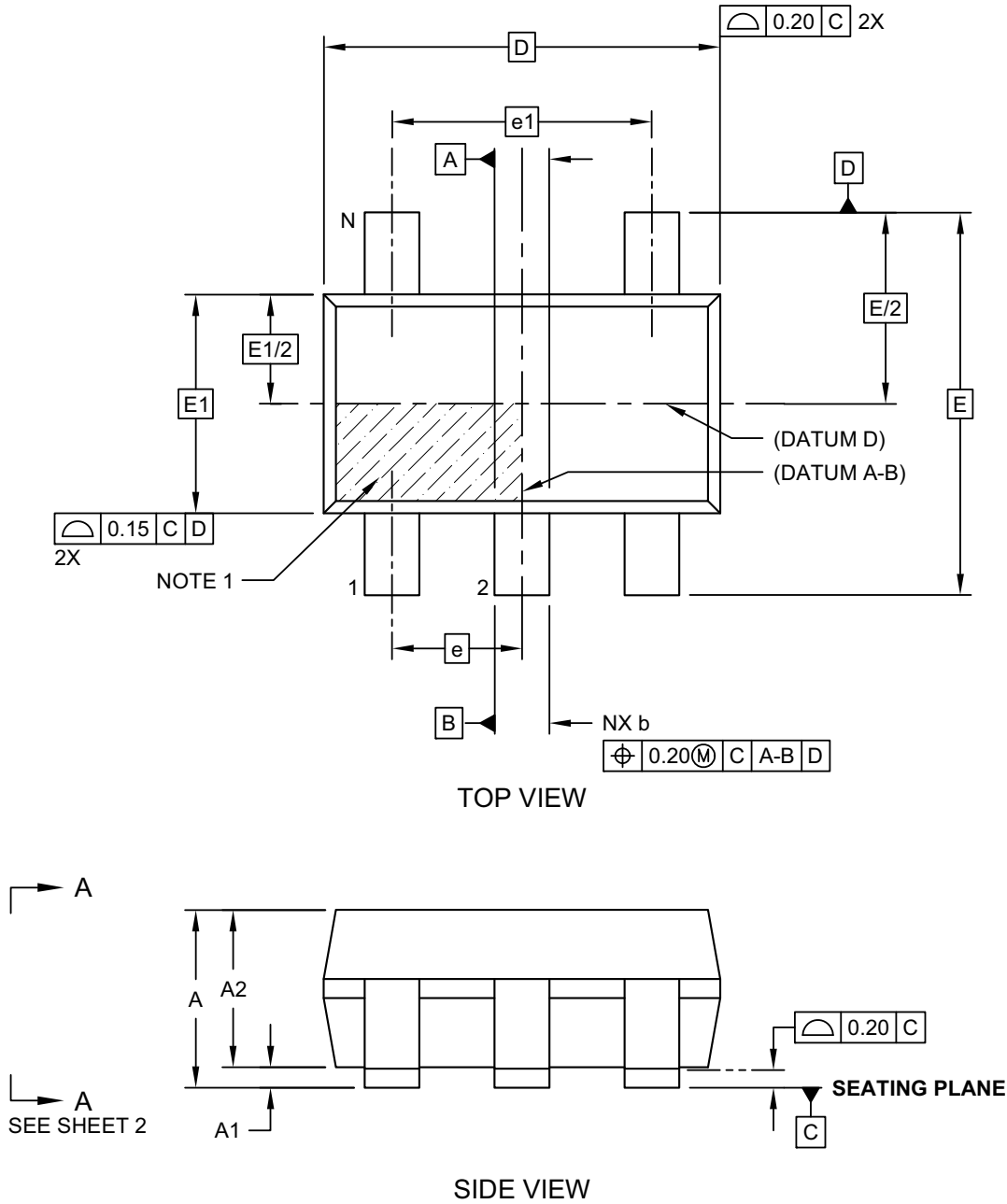
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev G

24LC16B

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

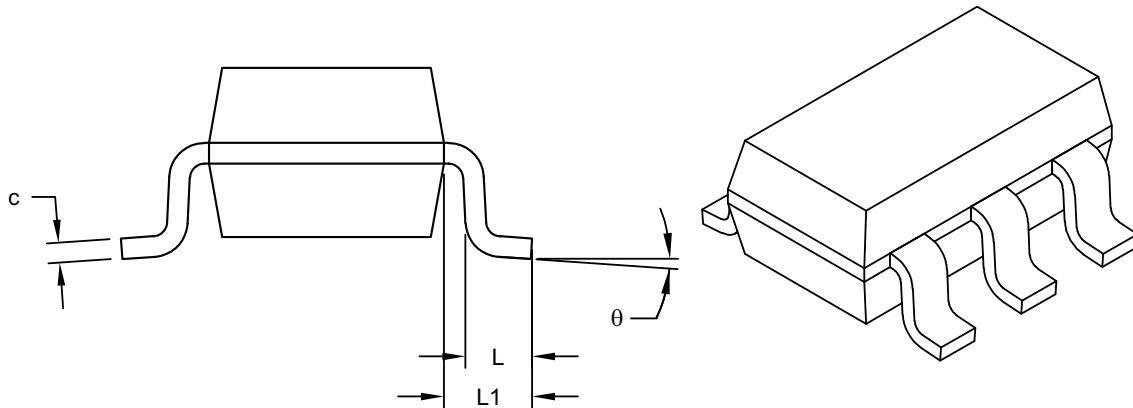
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-091-OT Rev G Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



VIEW A-A
SHEET 1

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	-	0.60
Footprint	L1	0.60 REF		
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

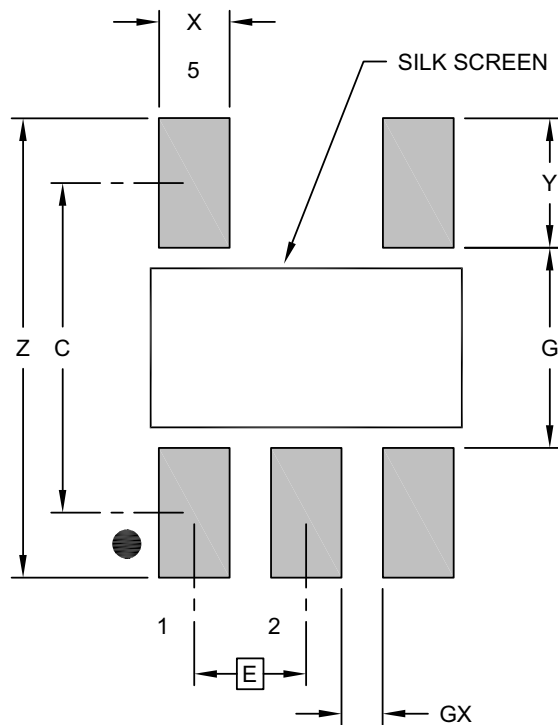
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev G Sheet 2 of 2

24LC16B

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev G

APPENDIX A: REVISION HISTORY

Revision B (April 2022)

Added Product Identification System section for Automotive; Updated SOIC and SOT-23 package drawings; Replaced terminology “Master” and “Slave” with “Host” and “Client”, respectively; Reformatted some sections for better readability.

Revision A (August 2018)

Initial release of this document.

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PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	$\bar{X}^{(1)}$	$-X$	ΔXX	
Device	Tape and Reel Option	Temperature Range	Package	Examples
Device: 24LC16B = 2.5V, 16-Kbit I ² C Serial EEPROM				a) 24LC16B-H/SN: 16-Kbit I ² C Serial EEPROM, High temp., SOIC package. b) 24LC16BT-H/SN: 16-Kbit I ² C Serial EEPROM, Tape and Reel, High temp., SOIC package. c) 24LC16BT-H/OT: 16-Kbit, I ² C Serial EEPROM, Tape and Reel, High temp., SOT-23 package.
Tape and Reel Option: Blank = Standard packaging (tube) T = Tape and Reel ⁽¹⁾				
Temperature Range: H = -40°C to +150°C (High)				
Package: SN = Plastic Small Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC) OT = Plastic Small Outline Transistor – 5-Lead (SOT-23) (Tape and Reel only)				
				Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

24LC16B

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u> ⁽¹⁾	<u>-X</u>	<u>/XX</u>	<u>XXX</u> ^(2,3)	Examples
Device	Tape and Reel Option	Temperature Range	Package	Variant	
Device:	24LC16B	=	2.5V, 16-Kbit I ² C Serial EEPROM		
Tape and Reel Option:	Blank T	=	Standard packaging (tube) Tape and Reel ⁽¹⁾		
Temperature Range:	H	=	-40°C to +150°C (AEC-Q100 Grade 0)		
Package:	SN OT	=	Plastic Small Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC) Plastic Small Outline Transistor – 5-Lead (SOT-23) (Tape and Reel only)		
Variant:^(2,3)	16KVAO 16KVXX	=	Standard Automotive, 16K Process Customer-Specific Automotive, 16K Process		
					<p>a) 24LC16BT-H/SN16KVAO: 16-Kbit I²C Serial EEPROM, Tape and Reel, Automotive Grade 0, SOIC package.</p> <p>b) 24LC16BT-H/OT16KVAO: 16-Kbit I²C Serial EEPROM, Tape and Reel, Automotive Grade 0, SOT-23 package.</p> <p>Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.</p> <p>2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.</p> <p>3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.</p>

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