



PIC18(L)F2X/45K50

PIC18(L)F2X/45K50 USB Flash MCU Product Brief

Universal Serial Bus Features:

- USB V2.0 Compliant
- Crystal-less Full Speed (12 Mb/s) and Low-Speed Operation (1.5 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 Bidirectional)
- 1 Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver

Flexible Oscillator Structure:

- 3x and 4x PLL Clock Multipliers
- Two External Clock modes, Up to 48 MHz (12 MIPS)
- Internal 31 kHz Oscillator
- Internal Oscillator, 31 kHz to 16 MHz
 - Factory calibrated to $\pm 1\%$
 - Self-tune to $\pm 0.20\%$ max. from USB or secondary oscillator
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- Up to 33 I/O Pins plus 3 Input-Only Pins:
 - High-current Sink/Source 25 mA/25 mA
 - Three programmable external interrupts
 - 11 programmable Interrupt-on-Change
 - 9 programmable weak pull-ups
 - Programmable slew rate
- SR Latch
- Enhanced Capture/Compare/PWM (ECCP) module:
 - One, two or four PWM outputs
 - Selectable polarity
 - Programmable dead time
 - Auto-shutdown and auto-restart
 - Pulse steering control
- Capture/Compare/PWM (CCP) module
- Master Synchronous Serial Port (MSSP) module Supporting 3-Wire SPI (all 4 modes) and I²C™ Master and Slave modes
- Two Analog Comparators with Input Multiplexing
- 10-Bit Analog-to-Digital (A/D) Converter module:
 - Up to 25 input channels
 - Auto-acquisition capability
 - Conversion available during Sleep
- Digital-to-Analog Converter (DAC) module:
 - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
 - 5-bit rail-to-rail resistive DAC with positive and negative reference selection

- High/Low-Voltage Detect module
- Charge Time Measurement Unit (CTMU):
 - Supports capacitive touch sensing for touch screens and capacitive switches
- Enhanced USART module:
 - Supports RS-485, RS-232 and LIN/J2602
 - Auto-wake-up on Start bit
 - Auto-Baud Detect

Extreme Low-Power Management with XLP:

- Sleep mode: 20 nA, typical
- Watchdog Timer: 300 nA, typical
- Timer1 Oscillator: 800 nA @ 32 kHz
- Peripheral Module Disable

Special Microcontroller Features:

- Low-Power, High-Speed CMOS Flash Technology
- C Compiler Optimized Architecture for Re-Entrant Code
- Power Management Features:
 - Run: CPU on, peripherals on, SRAM on
 - Idle: CPU off, peripherals on, SRAM on
 - Sleep: CPU off, peripherals off, SRAM on
- Priority Levels for Interrupts
- Self-Programmable under Software Control
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
 - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Optional dedicated ICD/ICSP Port (44-Pin TQFP Package Only)
- Wide Operating Voltage Range:
 - F devices: 2.3V to 5.5V
 - LF devices: 1.8V to 3.6V
- Flash Program Memory of 10,000 Erase/Write Cycles Minimum and 20-year Data Retention

PIC18(L)F2X/45K50

PIC18(L)F2X/45K50 Family Types

Device	Program Memory		Data Memory		Pins	I/O	10-bit A/D channels	Comparators	CCP/ ECCP	BOR/LVD	CTMU	MSSP	EUSART	Timers 8-bit/16-bit	USB 2.0
	Flash (bytes)	Single Word Instructions	SRAM (bytes)	Data EEPROM (bytes)											
PIC18(L)F45K50	32K	16384	2048	256	40/44	36	25-ch	2	1/1	Yes	Yes	1	1	2/2	Yes
PIC18(L)F25K50	32K	16384	2048	256	28	25	14-ch	2	1/1	Yes	Yes	1	1	2/2	Yes
PIC18(L)F24K50	16K	8192	2048	256	28	25	14-ch	2	1/1	Yes	Yes	1	1	2/2	Yes

FIGURE 1: 28-PIN PDIP, SOIC, SSOP DIAGRAM FOR PIC18(L)F2XK50

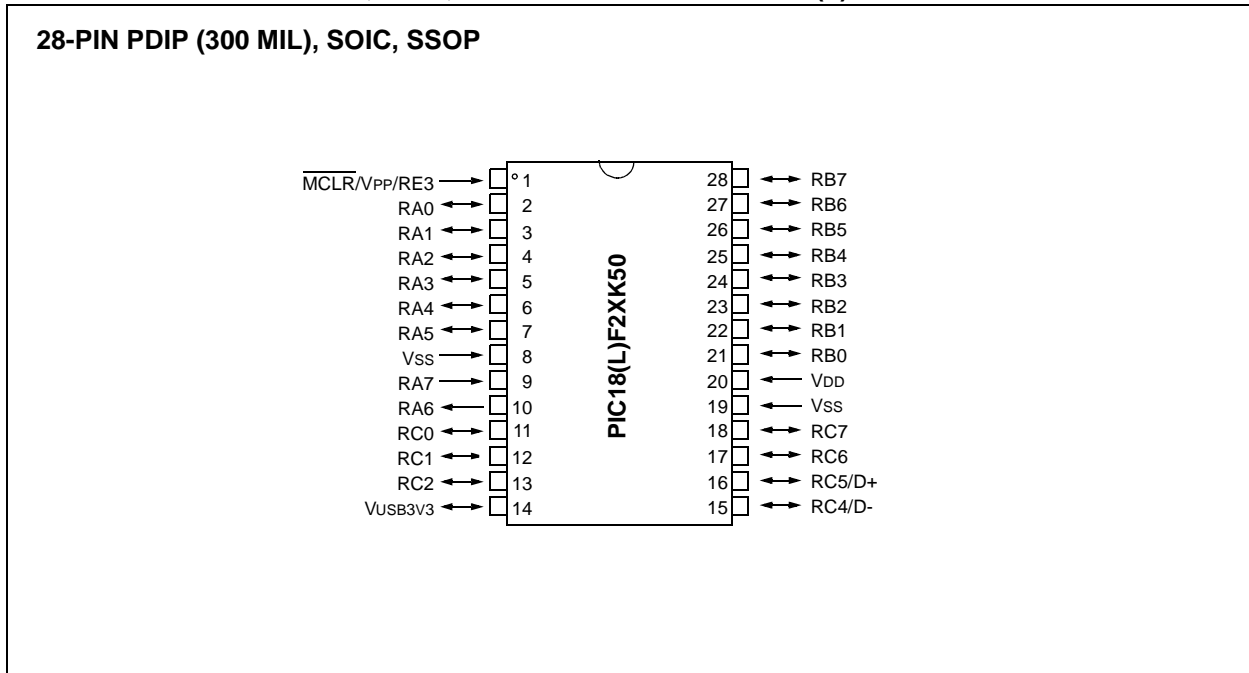
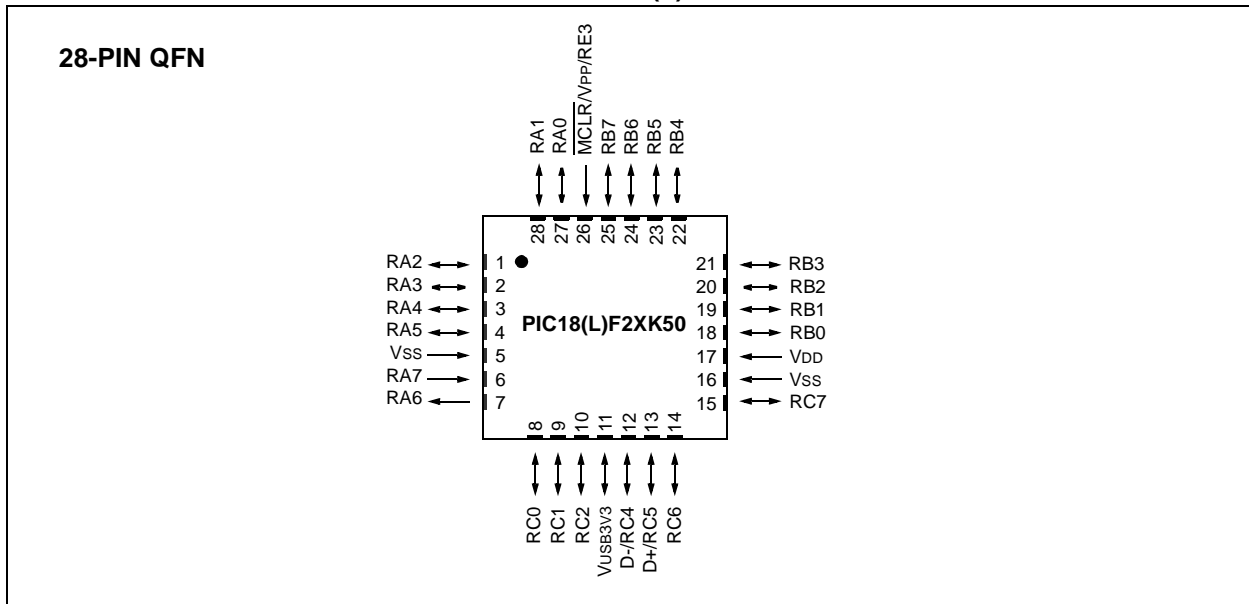


FIGURE 2: 28-PIN QFN DIAGRAM FOR PIC18(L)F2XK50



PIC18(L)F2X/45K50

FIGURE 3: 40-PIN PDIP DIAGRAM FOR PIC18(L)F45K50

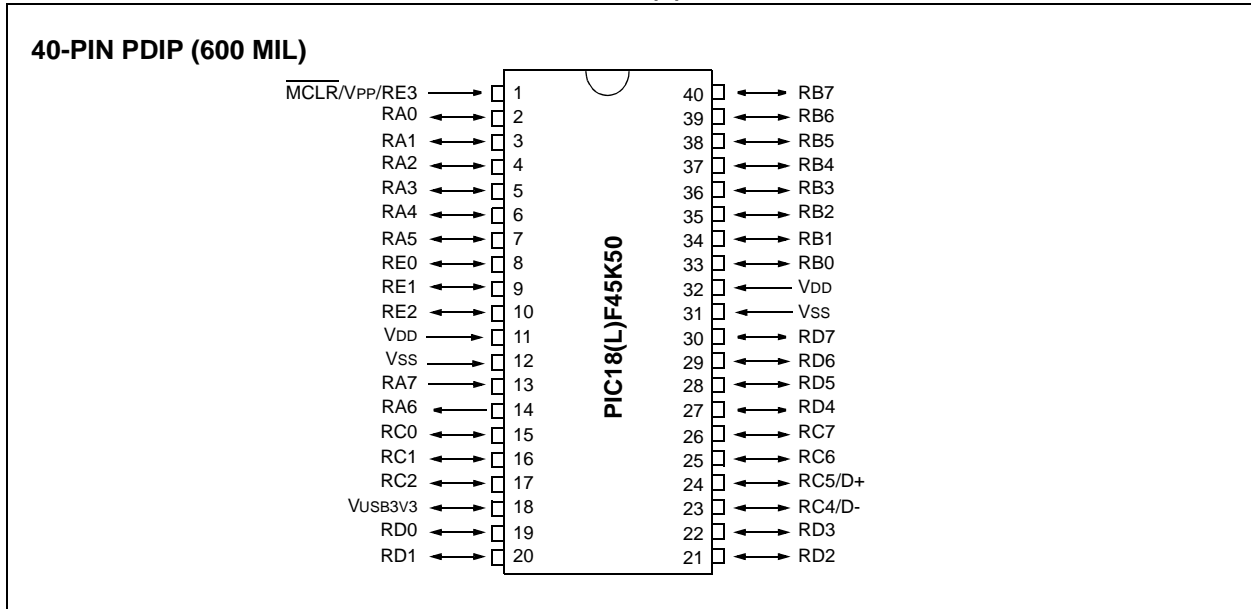
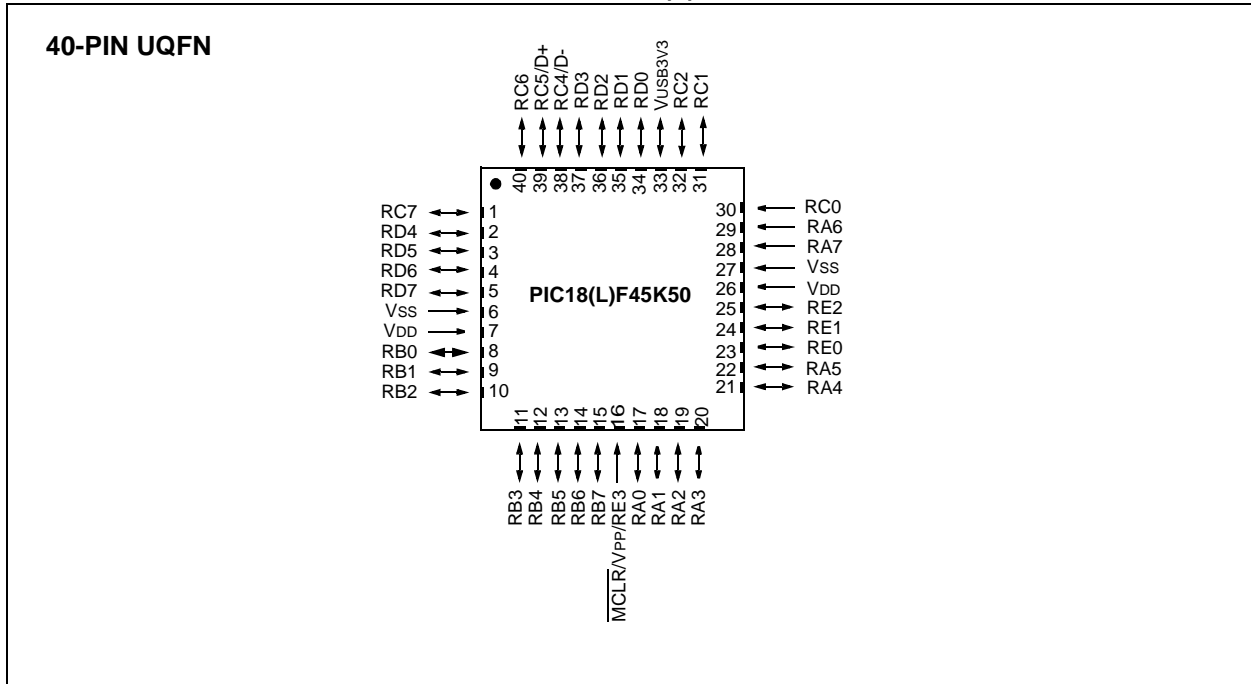


FIGURE 4: 40-PIN UQFN DIAGRAM FOR PIC18(L)F45K50



PIC18(L)F2X/45K50

FIGURE 5: 44-PIN TQFP DIAGRAM FOR PIC18(L)F45K50

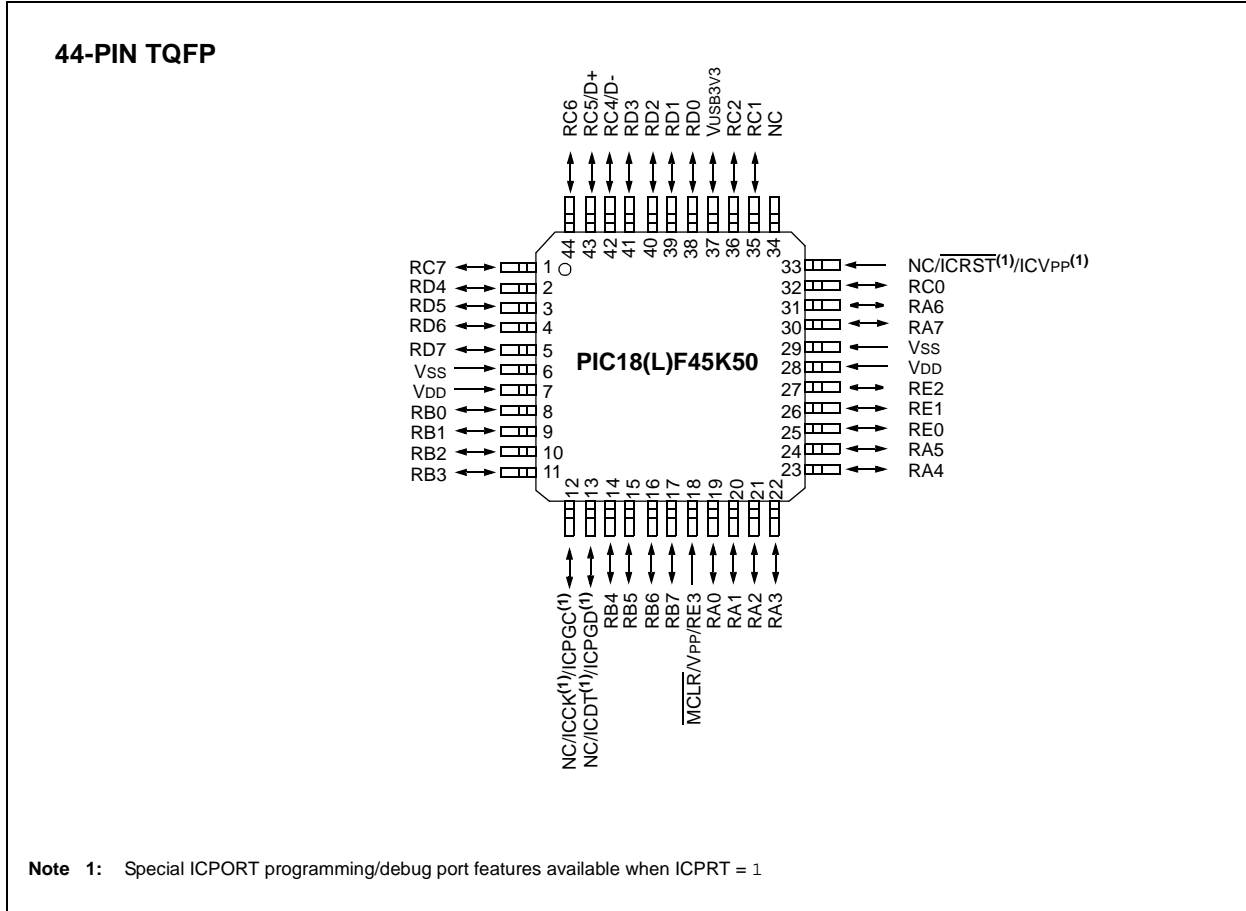


TABLE 1: PIC18(L)F2X/45K50 PIN SUMMARY

I/O	28-Pin PDIP/SOIC/SSOP	28-Pin PDIP	40-Pin QFN	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	Analog	Comparator	CTMU	SR Latch	Reference	USB	(E)CCP	EUSART	MSSP	Timers	Interrupts	
RA0	2	27	2	2	17	19	AN0	C12IN0-										
RA1	3	28	3	3	18	20	AN1	C12IN1-	CTCMP									
RA2	4	1	4	4	19	21	AN2	C2IN+			VREF- DACOUT							
RA3	5	2	5	5	20	22	AN3	C1IN+			VREF+							
RA4	6	3	6	6	21	23		C1OUT		SRQ						T0CKI		
RA5	7	4	7	7	22	24	AN4	C2OUT		SRNQ	LVDIN				SS			
RA6	10	7	14	14	29	31												
RA7	9	6	13	13	28	30												
RB0	21	18	33	33	8	8	AN12			SRI			FLT0		SDI SDA		INT0	
RB1	22	19	34	34	9	9	AN10	C12IN3-					P1C(5)		SCK SCL		INT1	
RB2	23	20	35	35	10	10	AN8		CTED1				P1B(5)				INT2	
RB3	24	21	36	36	11	11	AN9	C12IN2-	CTED2				CCP2(1)		SDO			
RB4	25	22	37	37	12	14	AN11						P1D(5)					
RB5	26	23	38	38	13	15	AN13											
RB6	27	24	39	39	14	16												
RB7	28	25	40	40	15	17												

Note 1: Alternate CCP2 pin location based on Configuration bit.

2: Alternate T3CKI pin location based on Configuration bits.

3: Pins are enabled when ICPRT = 1, otherwise, they are disabled.

4: Location on 40/44-Pin parts (PIC18(L)F45K50). Function not on this pin on 28-Pin parts (PIC18(L)F2XK50).

5: Location on 28-Pin parts (PIC18(L)F2XK50). Function not on this pin on 40/44-Pin parts (PIC18(L)F45K50).

6: Alternate SDO pin location based on Configuration bits.

7: RE3, RC4 and RC5 can be used for digital input only (no output functionality).

TABLE 1: PIC18(L)F2X/45K50 PIN SUMMARY

I/O	28-Pin PDIP/SOIC/SSOP	28-Pin QFN	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	Analog	Comparator	CTMU	SR Latch	Reference	USB	(E)CCP	EUSART	MSSP	Timers	Interrupts
RC0	11	8	15	30	32										SOSCO T1CKI T3CKI T3G	IOCC0
RC1	12	9	16	31	35							CCP2			SOSCI	IOCC1
RC2	13	10	17	32	36	AN14		CTPLS				CCP1 P1A				IOCC2
—	14	11	18	33	37	—				VUSB3V3						
RC4 ⁽⁷⁾	15	12	23	38	42	—				D-						IOCC4
RC5 ⁽⁷⁾	16	13	24	39	43	—				D+						IOCC5
RC6	17	14	25	40	44	AN18							TX CK			IOCC6
RC7	18	15	26	1	1	AN19							RX DT	SDO ⁽⁶⁾		IOCC7
RD0	—	—	19	34	38	AN20										
RD1	—	—	20	35	39	AN21										
RD2	—	—	21	36	40	AN22										
RD3	—	—	22	37	41	AN23										
RD4	—	—	27	2	2	AN24										
RD5	—	—	28	3	3	AN25						P1B ⁽⁴⁾				
RD6	—	—	29	4	4	AN26						P1C ⁽⁴⁾				
RD7	—	—	30	5	5	AN27						P1D ⁽⁴⁾				
RE0	—	—	8	23	25	AN5										

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RE1	—	—	9	24	26	AN6										
RE2	—	—	10	25	27	AN7										
RE3 ⁽⁷⁾	1	26	1	16	18	—										
	20	17	11, 32	7, 26	7, 28											
	8, 19	5, 16	12, 31	6, 27	6, 29											
			—	—	12 ⁽³⁾											
			—	—	13 ⁽³⁾											
			—	—	33 ⁽³⁾											

Note 1: Alternate CCP2 pin location based on Configuration bit.

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NOTES:

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