THE DATASHEET OF

NXH450N65L4Q2F2PG

3-Level NPC Inverter Module

NXH450N65L4Q2F2

The NXH450N65L4Q2F2 is a power module containing a I− type neutral point clamped three−level inverter. The integrated field stop trench IGBTs and FRDs provide lower conduction losses and switching losses, enabling designers to achieve high efficiency and superior reliability.

Features

- Neutral Point Clamped Three−Level Inverter Module
- 650 V Field Stop 4 IGBTs
- Low Inductive Layout
- Solderable Pins
- Thermistor

Typical Applications

- Solar Inverters
- Uninterruptable Power Supplies Systems

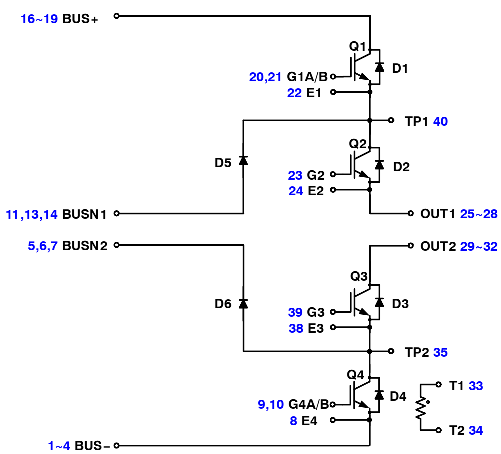
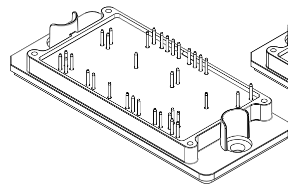
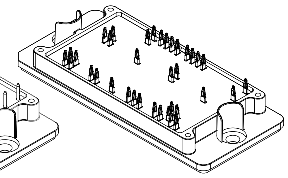


Figure 1. Schematic Diagram

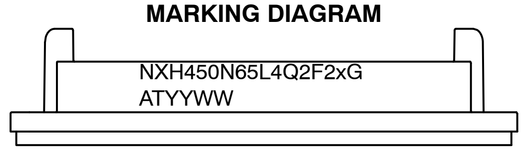




PIM40, Q2PACK CASE 180BE

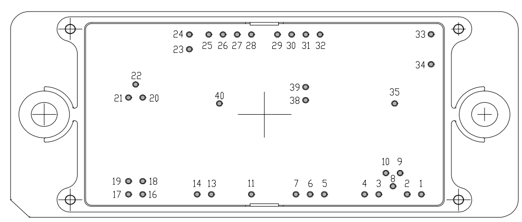
PIM36, Q2PACK CASE 180CD

MARKING DIAGRAM



NXH450N65L4Q2F2x = Specific Device Code
G = Pb−Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

PIN ASSIGNMENTS



ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 5 of this data sheet.

Table 1. MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
OUTER IGBT (Q1−1, Q1−2, Q4−1, Q4−2)			
Collector−Emitter Voltage	V_{CES}	650	V
Gate−Emitter Voltage Positive Transient Gate−Emitter Voltage (t_{pulse} = 5 μs, D < 0.10)	V_{GE}	±20 30	V
Continuous Collector Current @ T_c = 80°C (T_J = 175°C)	I_C	167	A
Pulsed Collector Current (T_J = 175°C)	I_{Cpulse}	501	A
Maximum Power Dissipation (T_J = 175°C)	P_{tot}	365	W
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
INNER IGBT (Q2, Q3)			
Collector−Emitter Voltage	V_{CES}	650	V
Gate−Emitter Voltage Positive Transient Gate−Emitter Voltage (t_{pulse} = 5 μs, D < 0.10)	V_{GE}	±20 30	V
Continuous Collector Current @ T_c = 80°C (T_J = 175°C)	I_C	280	A
Pulsed Collector Current (T_J = 175°C)	I_{Cpulse}	840	A
Maximum Power Dissipation (T_J = 175°C)	P_{tot}	633	W
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
NEUTRAL POINT DIODE (D5, D6)			
Peak Repetitive Reverse Voltage	V_{RRM}	650	V
Continuous Forward Current @ T_c = 80°C (T_J = 175°C)	I_F	271	A
Repetitive Peak Forward Current (T_J = 175°C)	I_{FRM}	813	A
Maximum Power Dissipation (T_J = 175°C)	P_{tot}	559	W
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
INVERSE DIODES (D1, D2, D3, D4)			
Peak Repetitive Reverse Voltage	V_{RRM}	650	V
Continuous Forward Current @ T_c = 80°C (T_J = 175°C)	I_F	131	A
Repetitive Peak Forward Current (t_p = 1 ms)	I_{FRM}	450	A
Maximum Power Dissipation (T_J = 175°C)	P_{tot}	288	W
Maximum Operating Junction Temperature	T_{JMAX}	150	°C
THERMAL PROPERTIES			
Storage Temperature Range	T_{stg}	−40 to 150	°C
INSULATION PROPERTIES			
Isolation Test Voltage, t = 1 s, 50 Hz	V_{is}	4000	V_{RMS}
Creepage Distance		12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

Table 2. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	−40	T_{JMAX}	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
OUTER IGBT (Q1−1, Q1−2, Q4−1, Q4−2)						
Collector−Emitter Cutoff Current	V_{GE} = 0 V, V_{CE} = 650 V	I_{CES}	–	–	300	μA
Collector−Emitter Saturation Voltage	V_{GE} = 15 V, I_C = 225 A, T_J = 25°C	$V_{CE(sat)}$	–	1.49	2.2	V
	V_{GE} = 15 V, I_C = 225 A, T_J = 150°C		–	1.70	–	
Gate−Emitter Threshold Voltage	V_{GE} = V_{CE}, I_C = 2.25 mA	$V_{GE(TH)}$	3.1	4.0	5.2	V
Gate Leakage Current	V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	–	600	nA
Turn−on Delay Time	T_J = 25°C V_{CE} = 400 V, I_C = 100 A V_{GE} = −5 V to +15 V, $R_{G(on)}$ = 15 Ω, $R_{G(off)}$ = 15 Ω	$t_{d(on)}$	–	163	–	ns
Rise Time		t_r	–	45	–	
Turn−off Delay Time		$t_{d(off)}$	–	831	–	
Fall Time		t_f	–	61	–	
Turn−on Switching Loss per Pulse		E_{on}	–	2.344	–	mJ
Turn off Switching Loss per Pulse		E_{off}	–	3.125	–	
Turn−on Delay Time	T_J = 125°C V_{CE} = 400 V, I_C = 100 A V_{GE} = −5 V to +15 V, $R_{G(on)}$ = 15 Ω, $R_{G(off)}$ = 15 Ω	$t_{d(on)}$	–	141	–	ns
Rise Time		t_r	–	51	–	
Turn−off Delay Time		$t_{d(off)}$	–	898	–	
Fall Time		t_f	–	80	–	
Turn−on Switching Loss per Pulse		E_{on}	–	3.75	–	mJ
Turn off Switching Loss per Pulse		E_{off}	–	2.97	–	
Input Capacitance	V_{CE} = 20 V, V_{GE} = 0 V, f = 10 kHz	C_{ies}	–	14630	–	pF
Output Capacitance		C_{oes}	–	230	–	
Reverse Transfer Capacitance		C_{res}	–	64	–	
Total Gate Charge	V_{CE} = 480 V, I_C = 225 A, V_{GE} = 0~+15 V	Q_g	–	452	–	nC
Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, λ = 2.8 W/mK	R_{thJH}	–	0.45	–	°C/W
Thermal Resistance − Chip−to−Case		R_{thJC}	–	0.26	–	°C/W
NEUTRAL POINT DIODE (D5, D6)						
Diode Forward Voltage	I_F = 375 A, T_J = 25°C	V_F	–	1.80	2.3	V
	I_F = 375 A, T_J = 150°C		–	1.77	–	
Reverse Recovery Time	T_J = 25°C V_{CE} = 400 V, I_C = 100 A V_{GE} = −5 V to +15 V, R_G = 15 Ω	t_{rr}	–	46	–	ns
Reverse Recovery Charge		Q_{rr}	–	1.5	–	μC
Peak Reverse Recovery Current		I_{RRM}	–	53	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	2541	–	A/μs
Reverse Recovery Energy		E_{rr}	–	0.3	–	mJ
Reverse Recovery Time	T_J = 125°C V_{CE} = 400 V, I_C = 100 A V_{GE} = −5 V to +15 V, R_G = 15 Ω	t_{rr}	–	75	–	ns
Reverse Recovery Charge		Q_{rr}	–	4	–	μC
Peak Reverse Recovery Current		I_{RRM}	–	96	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	2500	–	A/μs
Reverse Recovery Energy		E_{rr}	–	0.83	–	mJ
Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, λ = 2.8 W/mK	R_{thJH}	–	0.37	–	°C/W
Thermal Resistance − Chip−to−Case		R_{thJC}	–	0.17	–	°C/W

Table 3. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INNER IGBT (Q2, Q3)						
Collector−Emitter Cutoff Current	V_{GE} = 0 V, V_{CE} = 650 V	I_{CES}	–	–	300	µA
Collector−Emitter Saturation Voltage	V_{GE} = 15 V, I_C = 375 A, T_J = 25°C	$V_{CE(sat)}$	–	1.49	2.2	V
	V_{GE} = 15 V, I_C = 375 A, T_J = 150°C		–	1.72	–	
Gate−Emitter Threshold Voltage	V_{GE} = V_{CE}, I_C = 3.75 mA	$V_{GE(TH)}$	3.1	4.1	5.2	V
Gate Leakage Current	V_{GE} = 20 V, V_{CE} = 0 V	I_{GES}	–	–	1000	nA
Turn−on Delay Time	T_J = 25°C V_{CE} = 400 V, I_C = 100 A V_{GE} = −5 V to +15 V, $R_{G(on)}$ = 15 Ω, $R_{G(off)}$ = 15 Ω	$t_{d(on)}$	–	134	–	ns
Rise Time		t_r	–	47	–	
Turn−off Delay Time		$t_{d(off)}$	–	709	–	
Fall Time		t_f	–	32	–	
Turn−on Switching Loss per Pulse		E_{on}	–	1.72	–	mJ
Turn off Switching Loss per Pulse		E_{off}	–	2.65	–	
Turn−on Delay Time	T_J = 125°C V_{CE} = 400 V, I_C = 100 A V_{GE} = −5 V to +15 V, $R_{G(on)}$ = 15 Ω, $R_{G(off)}$ = 15 Ω	$t_{d(on)}$	–	118	–	ns
Rise Time		t_r	–	52	–	
Turn−off Delay Time		$t_{d(off)}$	–	765	–	
Fall Time		t_f	–	29	–	
Turn−on Switching Loss per Pulse		E_{on}	–	2.34	–	mJ
Turn off Switching Loss per Pulse		E_{off}	–	2.89	–	
Input Capacitance	V_{CE} = 20 V, V_{GE} = 0 V, f = 10 kHz	C_{ies}	–	24383	–	pF
Output Capacitance		C_{oes}	–	383	–	
Reverse Transfer Capacitance		C_{res}	–	105	–	
Total Gate Charge	V_{CE} = 480 V, I_C = 375 A, V_{GE} = 0~+15 V	Q_g	–	753	–	nC
Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, λ = 2.8 W/mK	R_{thJH}	–	0.31	–	°C/W
Thermal Resistance − Chip−to−Case		R_{thJC}	–	0.15	–	°C/W
INVERSE DIODES (D1, D2, D3, D4)						
Diode Forward Voltage	I_F = 150 A, T_J = 25°C	V_F	–	1.78	2.3	V
	I_F = 150 A, T_J = 150°C		–	1.77	–	
Reverse Recovery Time	T_J = 25°C V_{CE} = 400 V, I_C = 100 A V_{GE} = −5 V to +15 V, R_G = 15 Ω	t_{rr}	–	43	–	ns
Reverse Recovery Charge		Q_{rr}	–	1.14	–	µC
Peak Reverse Recovery Current		I_{RRM}	–	46	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	2473	–	A/µs
Reverse Recovery Energy		E_{rr}	–	0.313	–	mJ
Reverse Recovery Time	T_J = 125°C V_{CE} = 400 V, I_C = 100 A V_{GE} = −5 V to +15 V, R_G = 15 Ω	t_{rr}	–	67	–	ns
Reverse Recovery Charge		Q_{rr}	–	2.5	–	µC
Peak Reverse Recovery Current		I_{RRM}	–	66	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	2317	–	A/µs
Reverse Recovery Energy		E_{rr}	–	0.625	–	mJ
Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, λ = 2.8 W/mK	R_{thJH}	–	0.58	–	°C/W
Thermal Resistance − Chip−to−Case		R_{thJC}	–	0.33	–	°C/W

Table 3. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
THERMISTOR CHARACTERISTICS						
Nominal Resistance	T = 25°C	R_{25}	–	22	–	kΩ
Nominal Resistance	T = 100°C	R_{100}	–	1486	–	Ω
Deviation of R25		ΔR/R	−5	–	5	%
Power Dissipation		P_D	–	200	–	mW
Power Dissipation Constant			–	2	–	mW/K
B−value	B(25/50), tolerance ±3%		–	3950	–	K
B−value	B(25/100), tolerance ±3%		–	3998	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH450N65L4Q2F2SG	NXH450N65L4Q2F2SG	PIM40, Q2PACK (Pb−Free and Halide−Free)	12 Units / Blister Tray
NXH450N65L4Q2F2PG	NXH450N65L4Q2F2PG	PIM436 Q2PACK (Pb−Free and Halide−Free)	12 Units / Blister Tray

TYPICAL CHARACTERISTICS – IGBT Q1–1, Q1–2, Q4–1, Q4–2 AND DIODE D1, D4

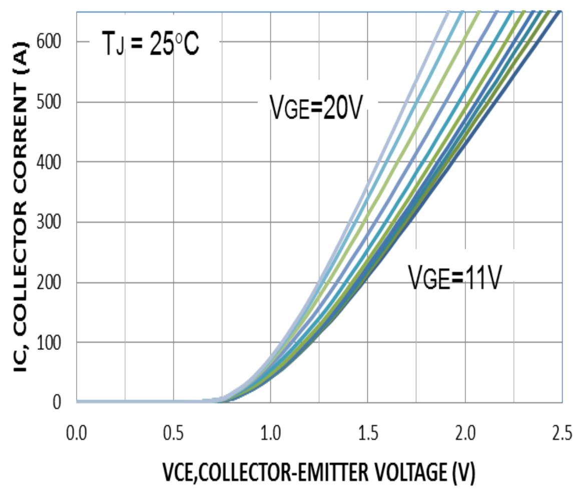


Figure 2. Typical Output Characteristics

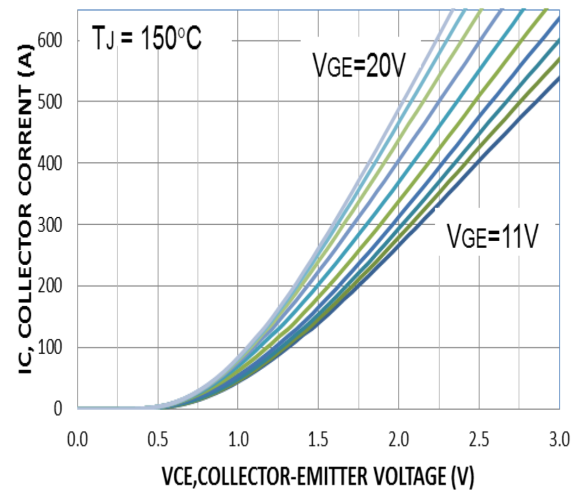


Figure 3. Typical Output Characteristics

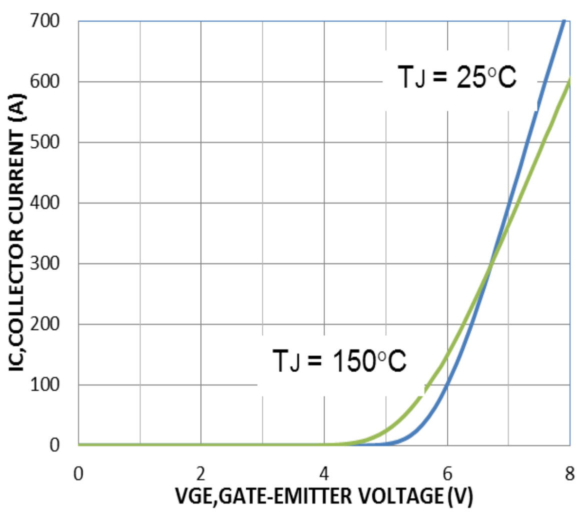


Figure 4. Typical Transfer Characteristics

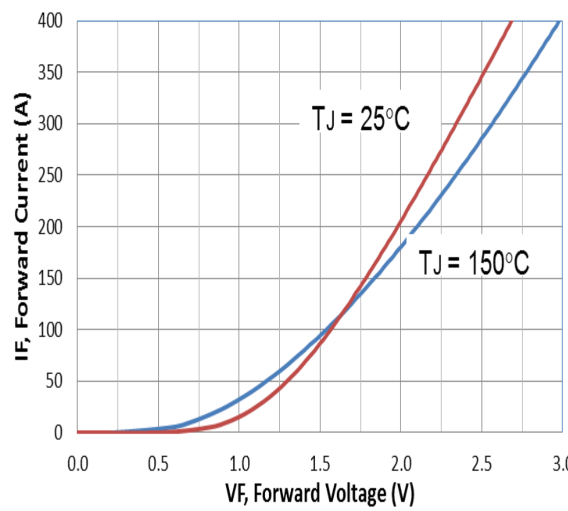


Figure 5. Typical Transfer Characteristics

TYPICAL CHARACTERISTICS − IGBT Q1−1, Q1−2, Q4−1, Q4−2 AND DIODE D1, D4

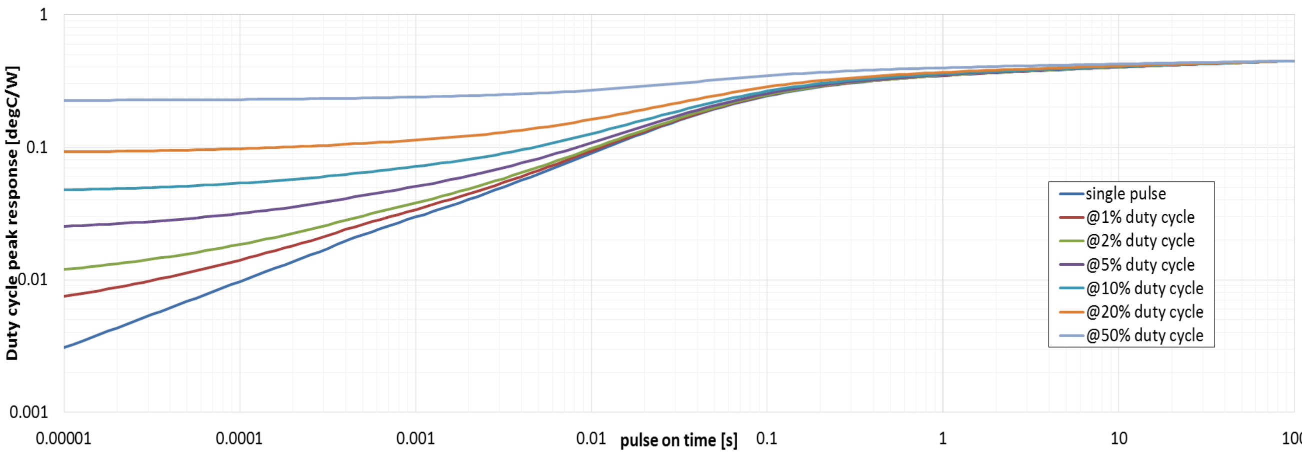


Figure 6. Transient Thermal Impedance (Q1−1, Q1−2, Q4−1, Q4−2)

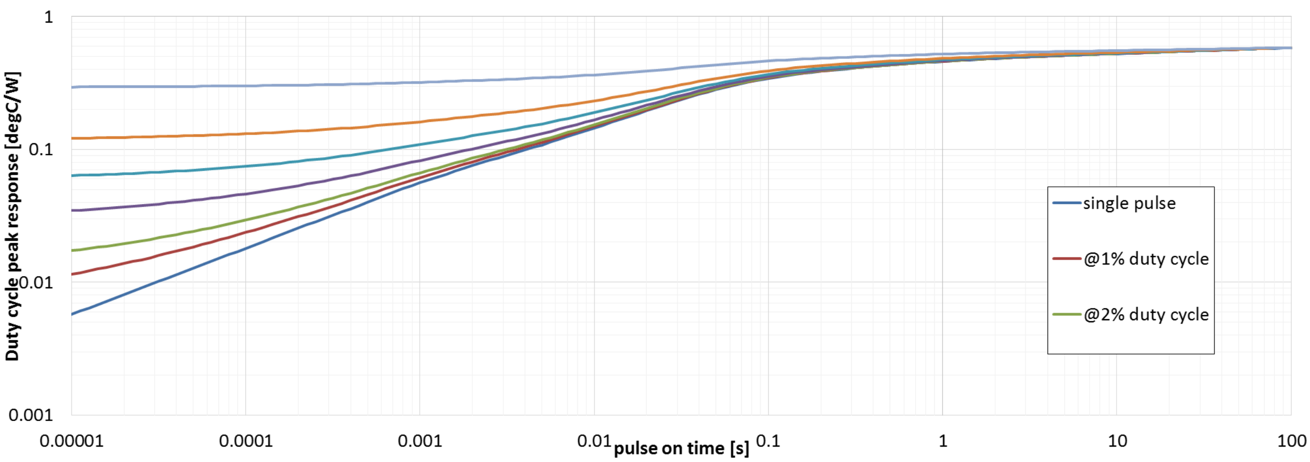


Figure 7. Transient Thermal Impedance (D1, D4)

TYPICAL CHARACTERISTICS – IGBT Q1–1, Q1–2, Q4–1, Q4–2 AND DIODE D1, D4

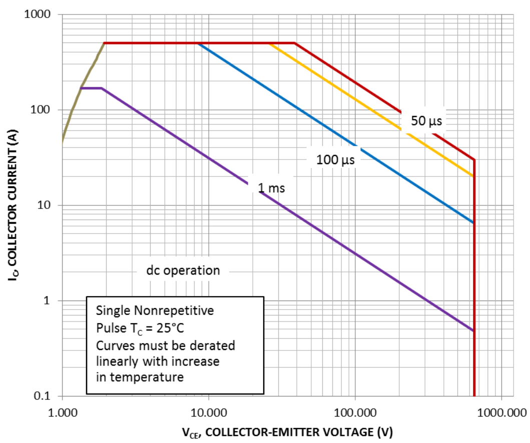


Figure 8. FBSOA (Q1–1, Q1–2, Q4–1, Q4–2)

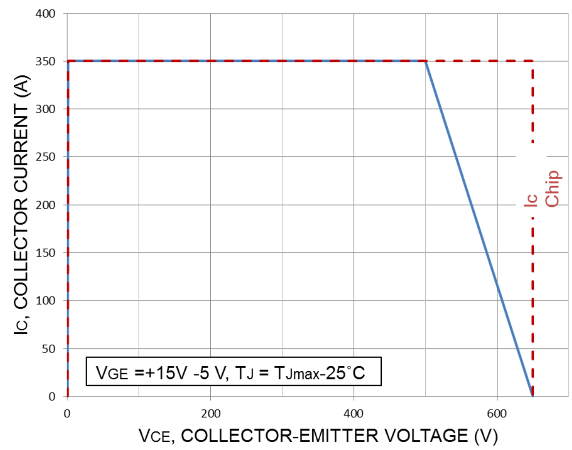


Figure 9. RBSOA (Q1–1, Q1–2, Q4–1, Q4–2)

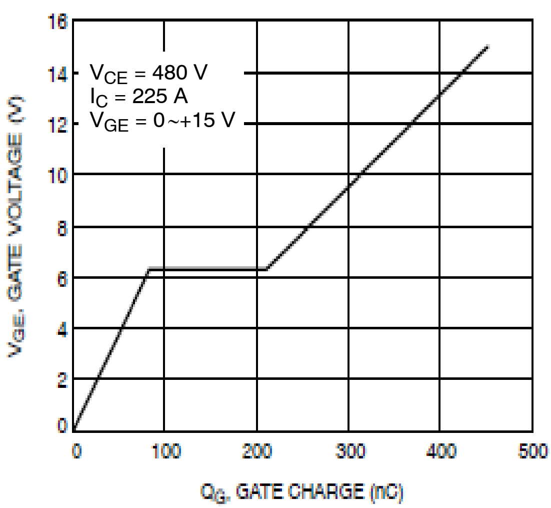


Figure 10. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – IGBT Q2, Q3 AND DIODE D2, D3

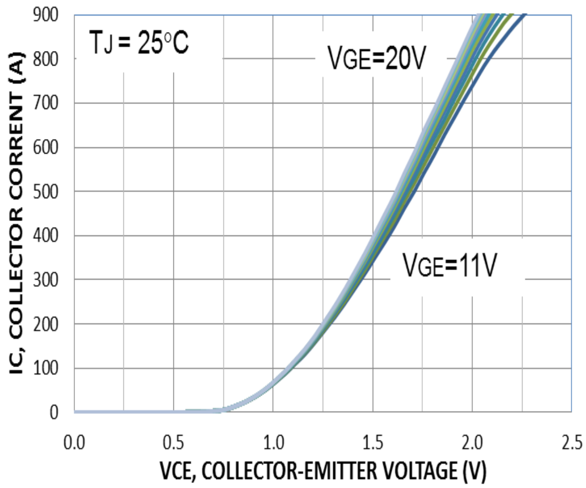


Figure 11. Typical Output Characteristics

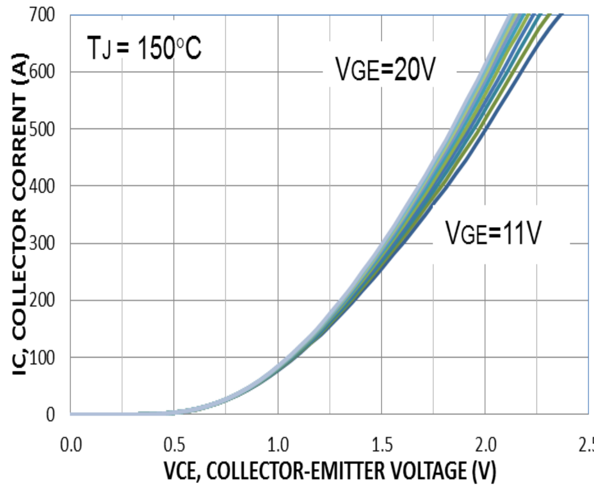


Figure 12. Typical Output Characteristics

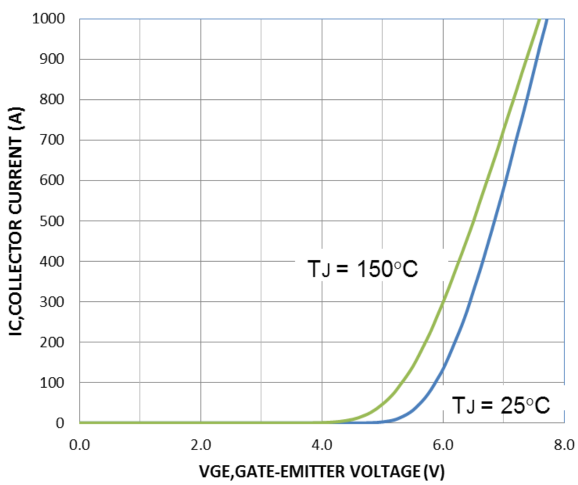


Figure 13. Typical Transfer Characteristics

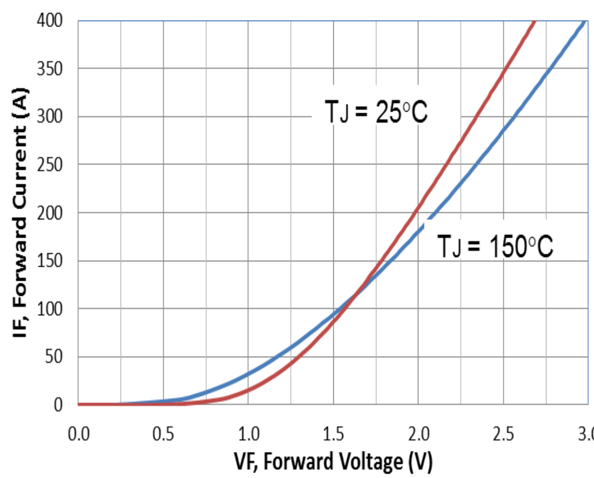


Figure 14. Typical Transfer Characteristics

TYPICAL CHARACTERISTICS – IGBT Q2, Q3 AND DIODE D2, D3

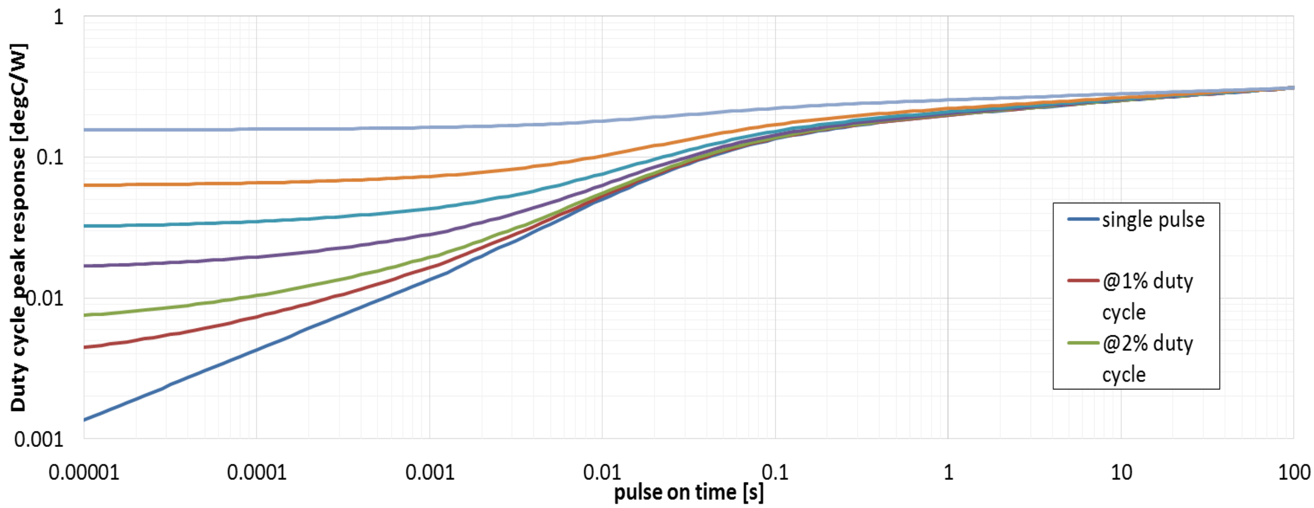


Figure 15. Transient Thermal Impedance (Q2, Q3)

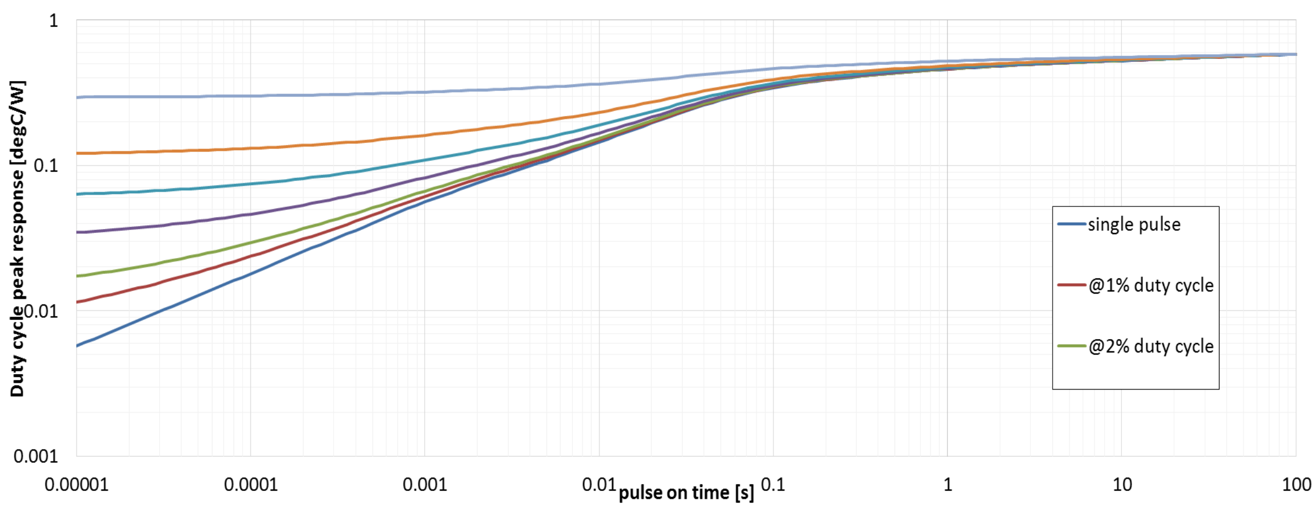


Figure 16. Transient Thermal Impedance (D2, D3)

TYPICAL CHARACTERISTICS – IGBT Q2, Q3 AND DIODE D2, D3

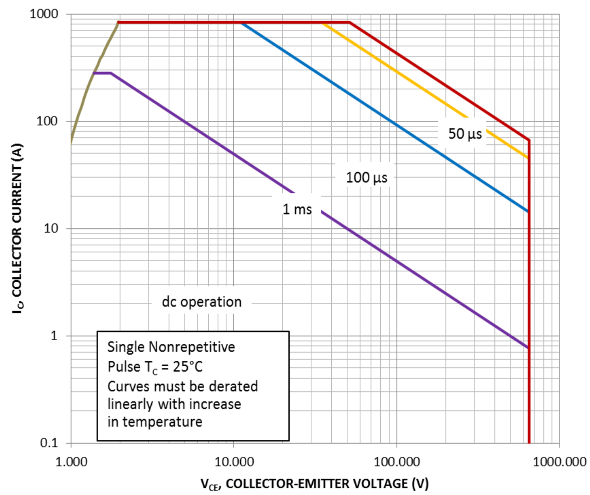


Figure 17. FBSOA (Q2, Q3)

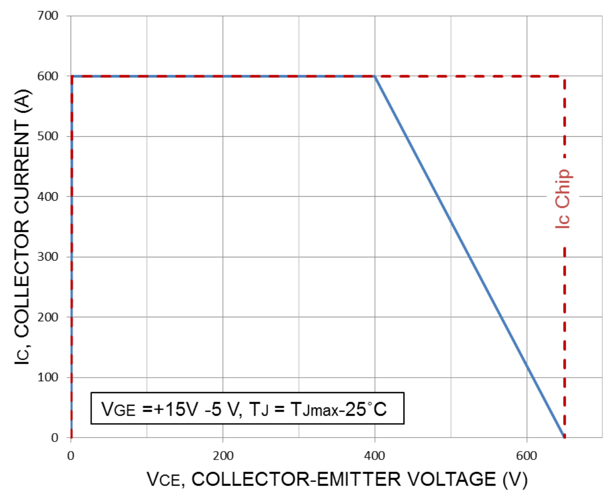


Figure 18. RBSOA (Q2, Q3)

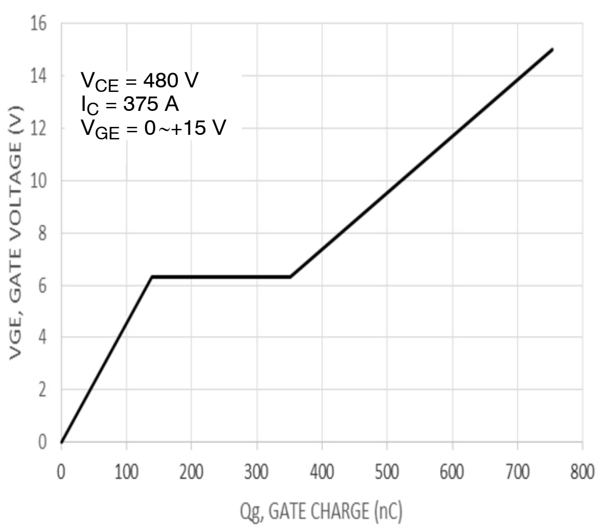


Figure 19. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – DIODE D5, D6

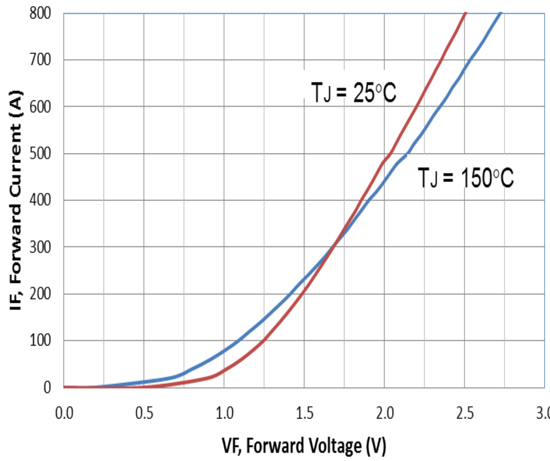


Figure 20. Diode Forward Characteristics

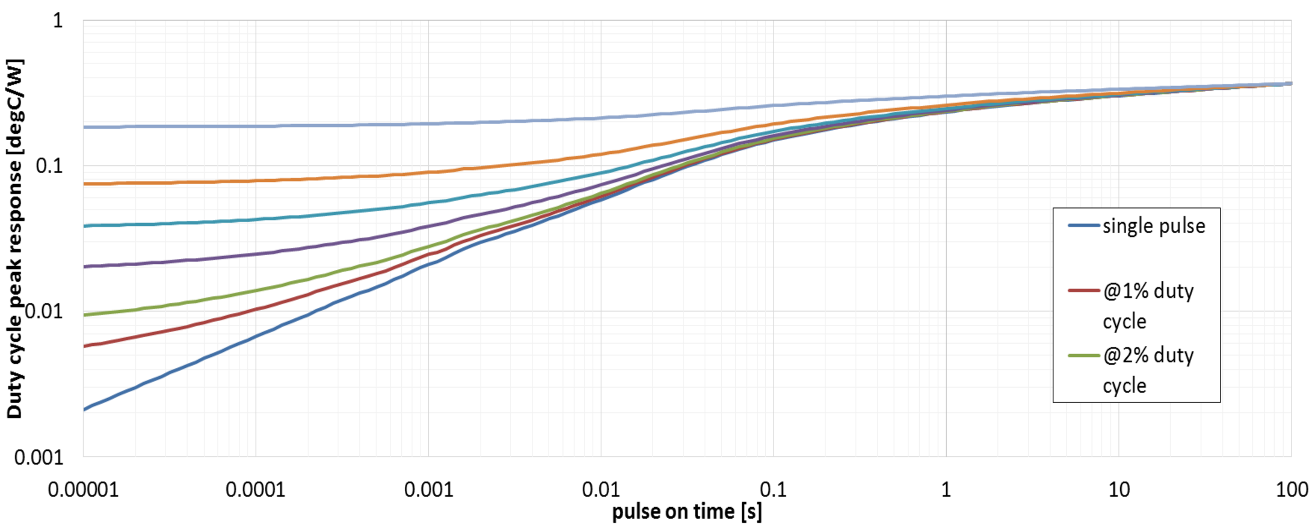


Figure 21. Transient Thermal Impedance (D5, D6)

TYPICAL CHARACTERISTICS – Q1/Q4 IGBT COMUTATES D5/D6 DIODE

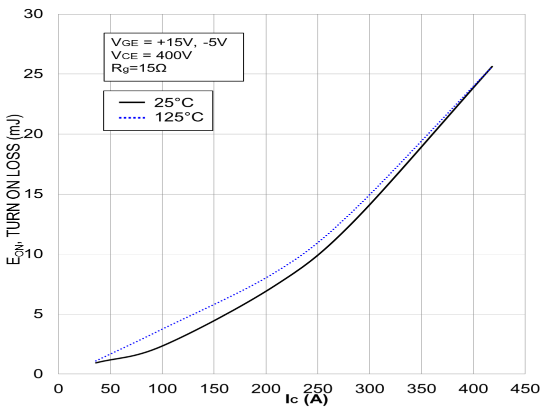


Figure 22. Typical Switching Loss Eon vs. IC

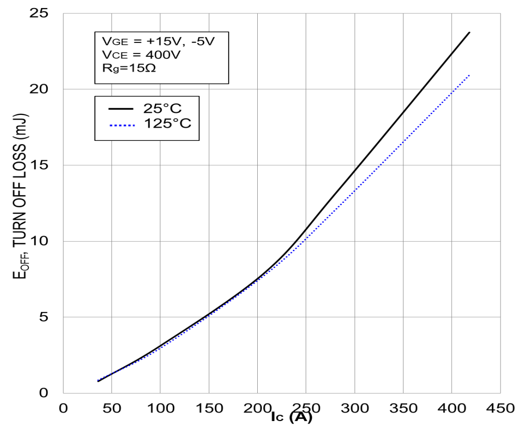


Figure 23. Typical Switching Loss Eoff vs. IC

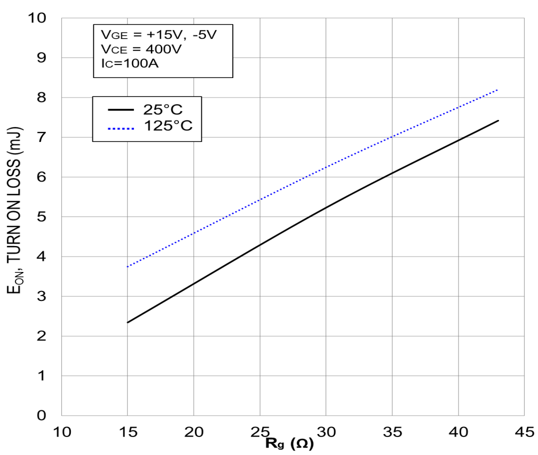


Figure 24. Typical Switching Loss Eon vs. R_G

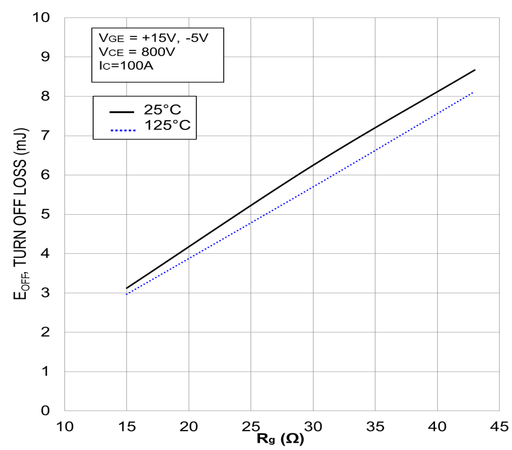


Figure 25. Typical Switching Loss Eoff vs. R_G

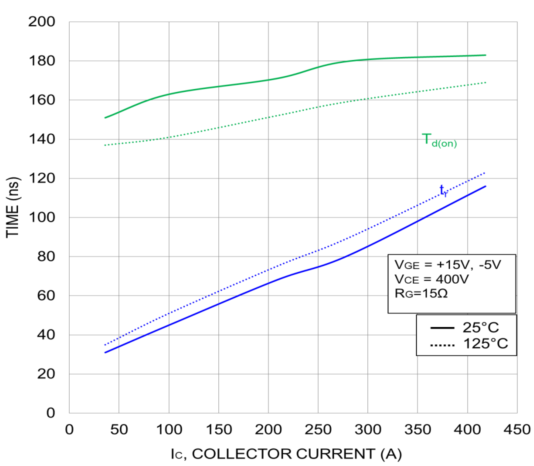


Figure 26. Typical Switching Time Tdon vs. IC

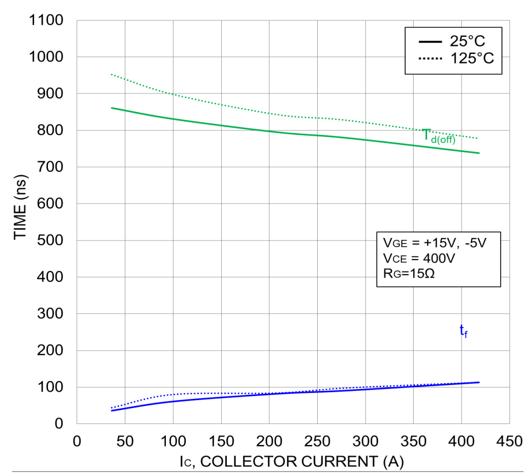


Figure 27. Typical Switching Time Tdoff vs. IC

TYPICAL CHARACTERISTICS – Q1/Q4 IGBT COMUTATES D5/D6 DIODE

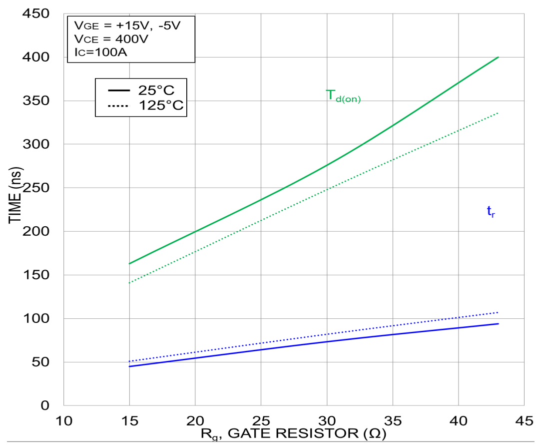


Figure 28. Typical Switching Time Tdon vs. R_G

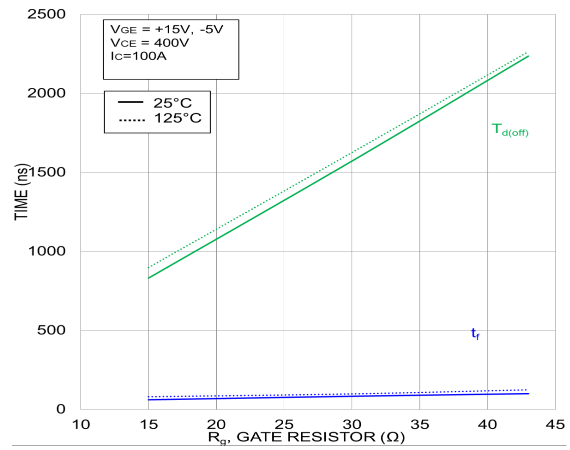


Figure 29. Typical Switching Time Tdoff vs. R_G

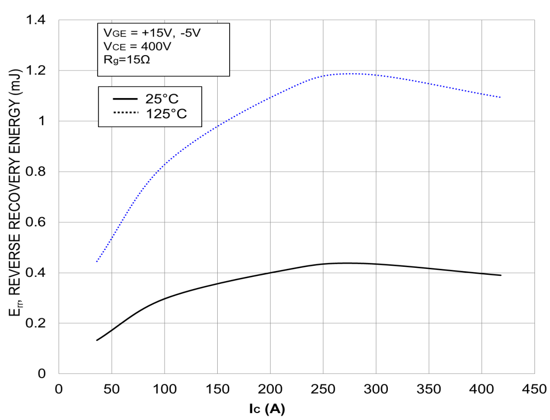


Figure 30. Typical Reverse Recovery Energy vs. IC

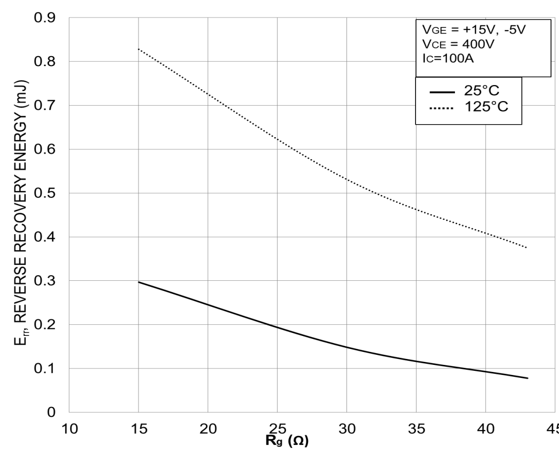


Figure 31. Typical Reverse Recovery Energy vs. R_G

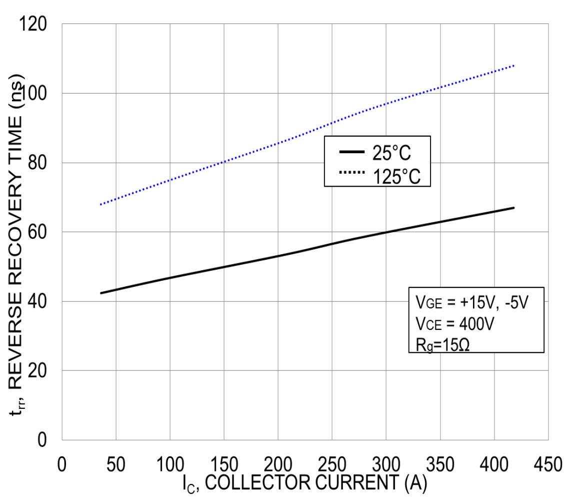


Figure 32. Typical Reverse Recovery Time vs. IC

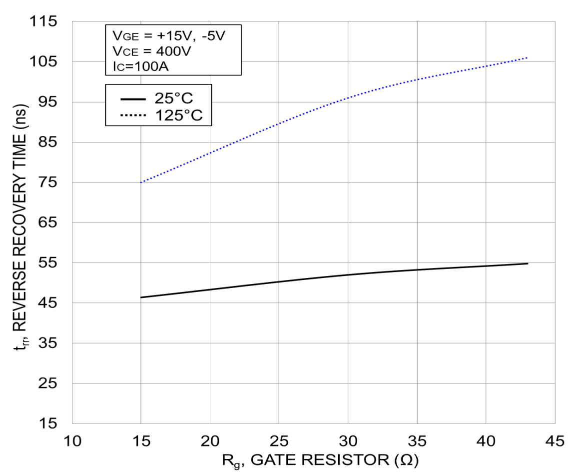


Figure 33. Typical Reverse Recovery Time vs. R_G

TYPICAL CHARACTERISTICS – Q1/Q4 IGBT COMUTATES D5/D6 DIODE

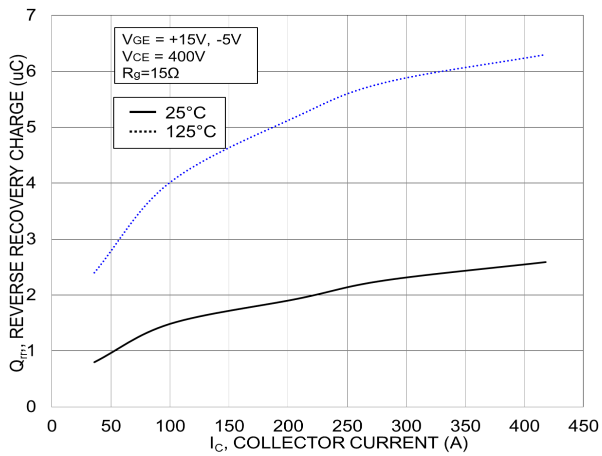


Figure 34. Typical Reverse Recovery Charge vs. IC

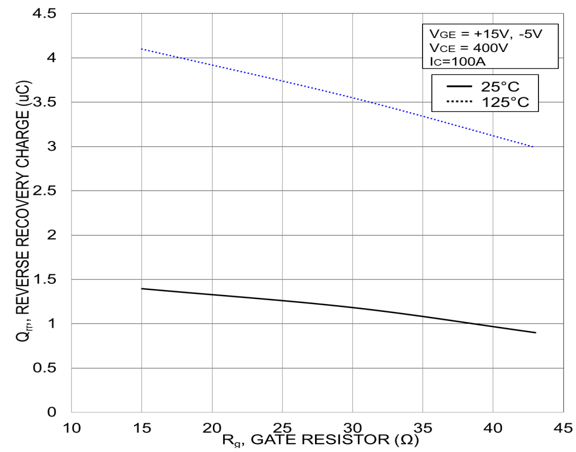


Figure 35. Typical Reverse Recovery Charge vs. R_G

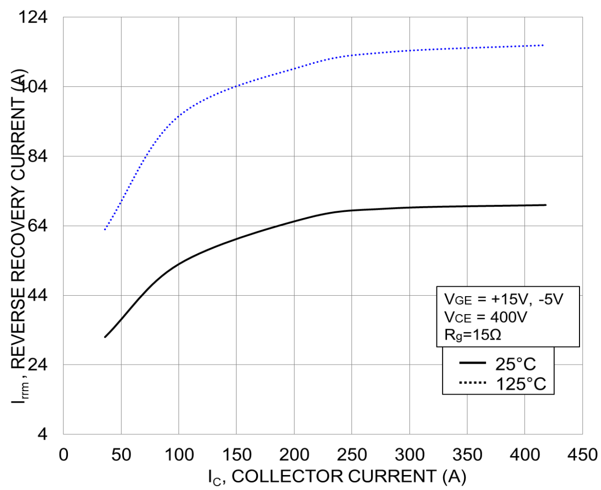


Figure 36. Typical Reverse Recovery Current vs. IC

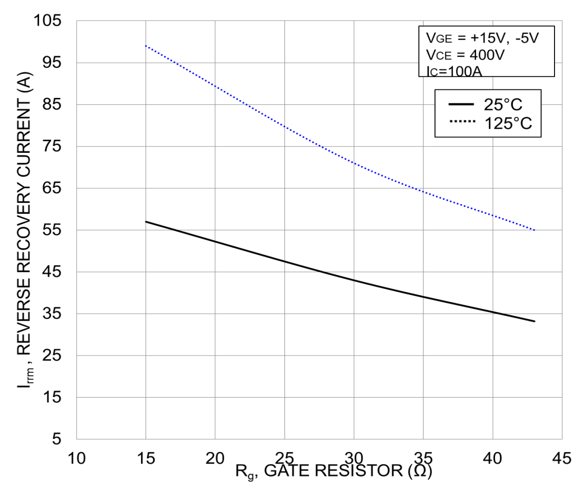


Figure 37. Typical Reverse Recovery Current vs. R_G

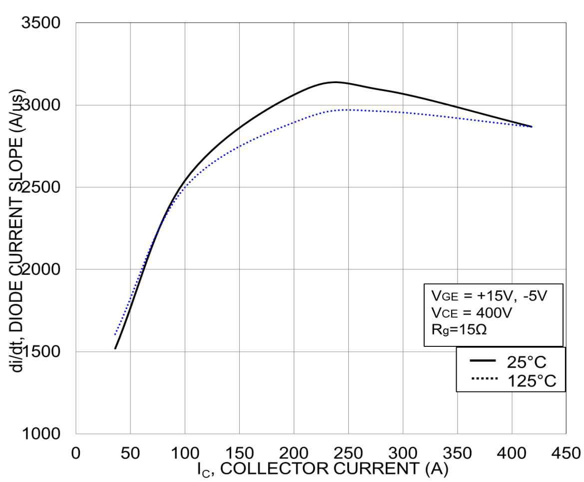


Figure 38. Typical di/dt vs. IC

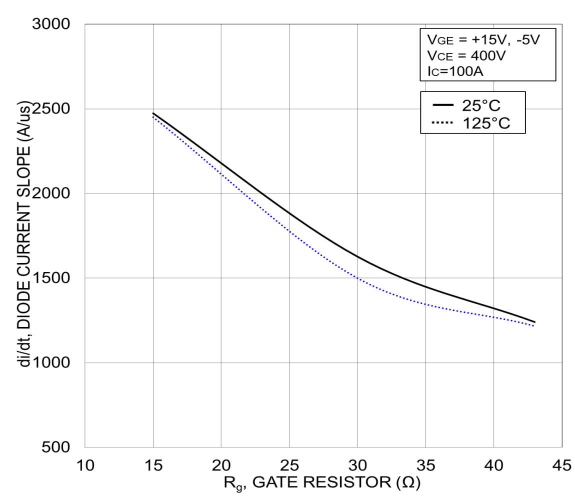


Figure 39. Typical di/dt vs. R_G

TYPICAL CHARACTERISTICS – Q2/Q3 IGBT COMUTATES D1/D4 DIODE

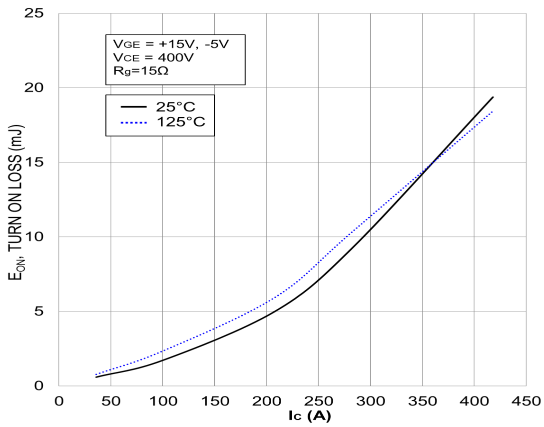


Figure 40. Typical Switching Loss Eon vs. IC

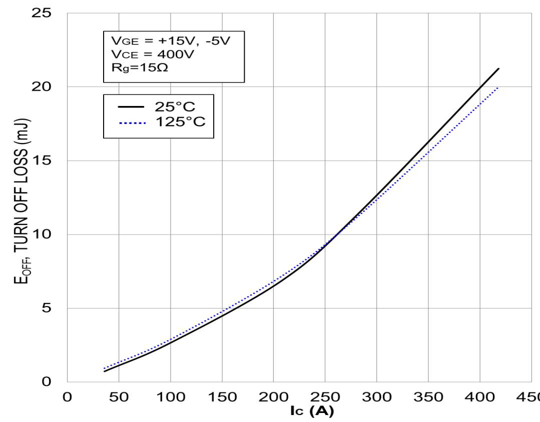


Figure 41. Typical Switching Loss Eoff vs. IC

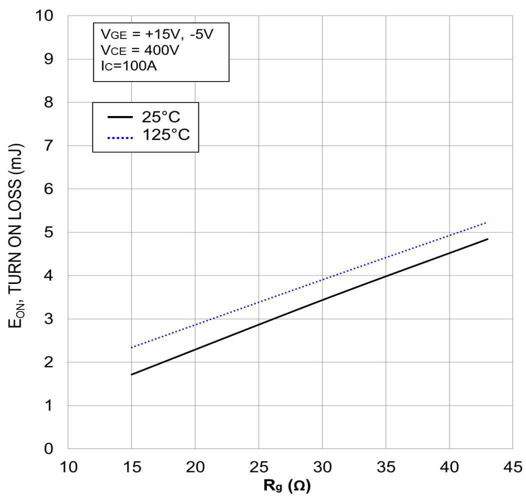


Figure 42. Typical Switching Loss Eon vs. R_G

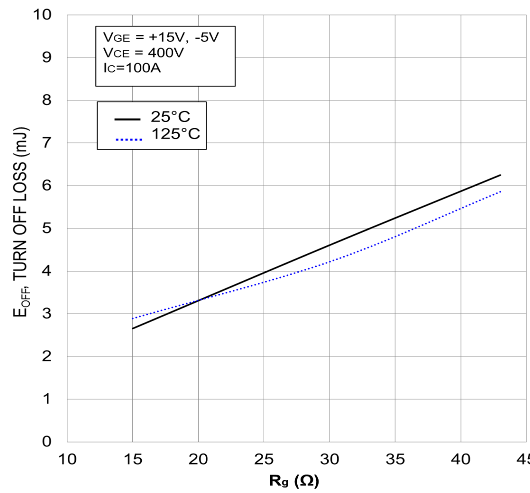


Figure 43. Typical Switching Loss Eoff vs. R_G

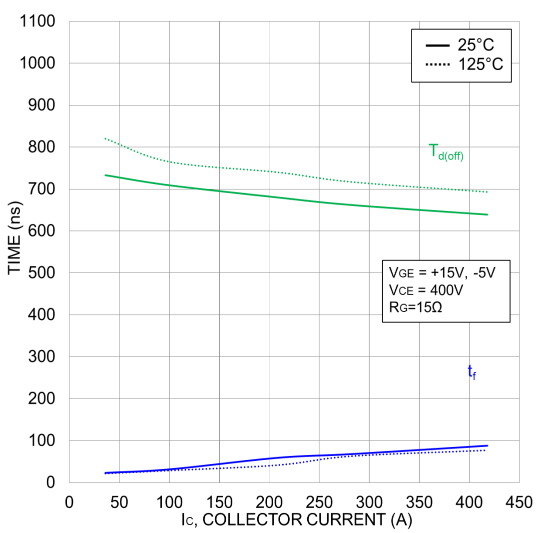


Figure 44. Typical Turn−On Switching Time vs. IC

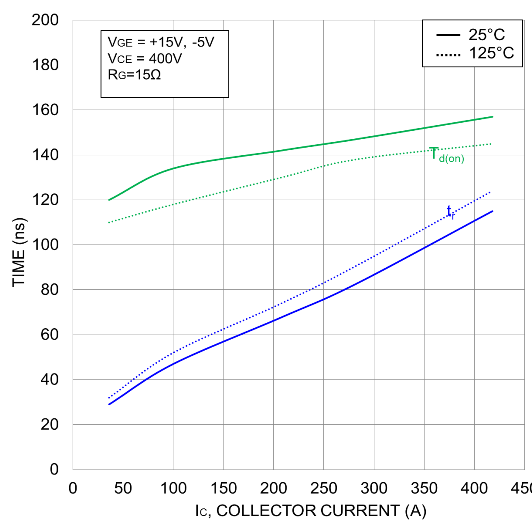


Figure 45. Typical Turn−Off Switching Time vs. IC

TYPICAL CHARACTERISTICS – Q2/Q3 IGBT COMUTATES D1/D4 DIODE

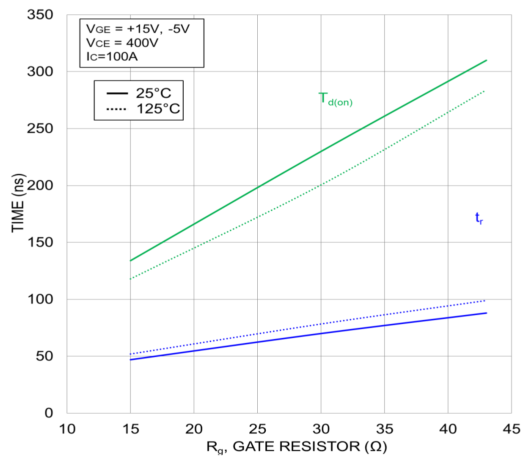


Figure 46. Typical Turn−On Switching Time vs. R_G

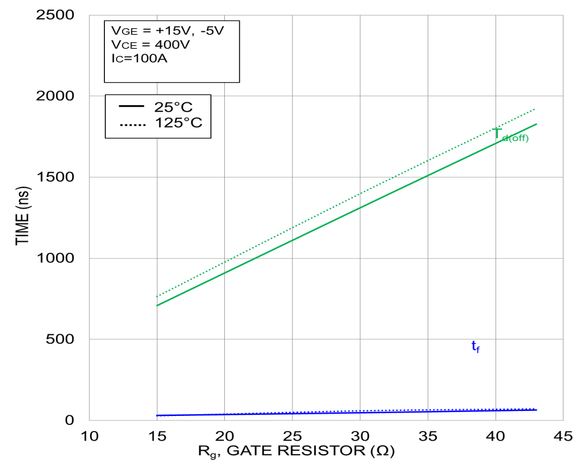


Figure 47. Typical Turn−Off Switching Time vs. R_G

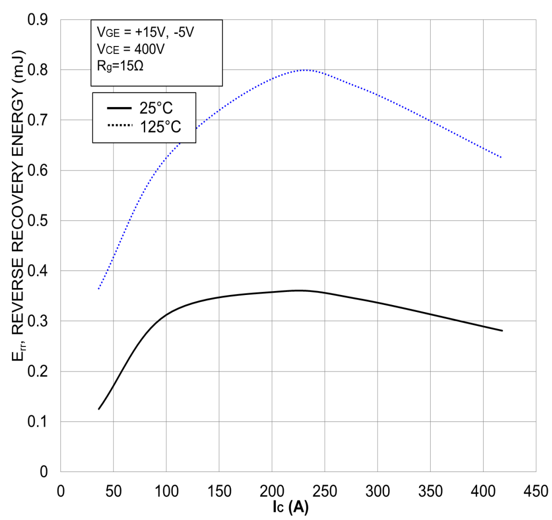


Figure 48. Typical Reverse Recovery Energy Loss vs. IC

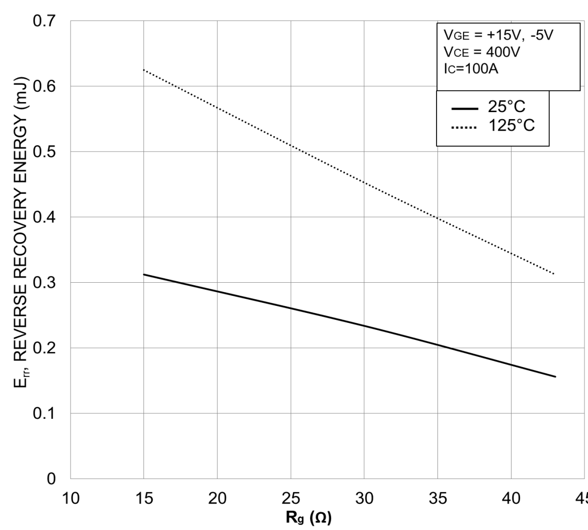


Figure 49. Typical Reverse Recovery Energy Loss vs. R_G

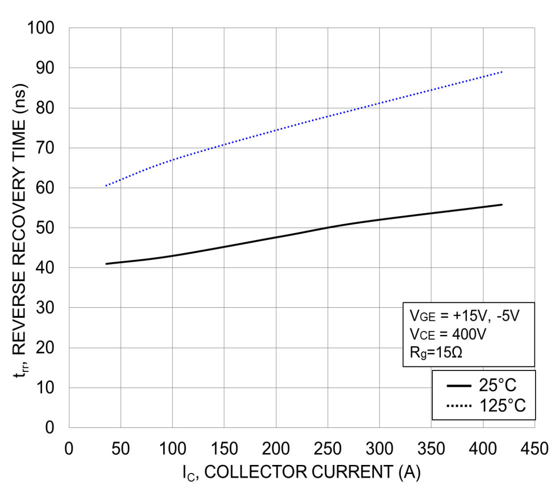


Figure 50. Typical Reverse Recovery Time vs. IC

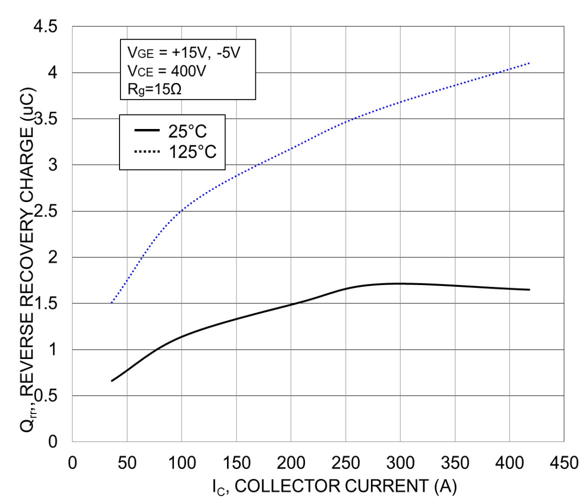


Figure 51. Typical Reverse Recovery Charge vs. IC

TYPICAL CHARACTERISTICS – Q2/Q3 IGBT COMUTATES D1/D4 DIODE

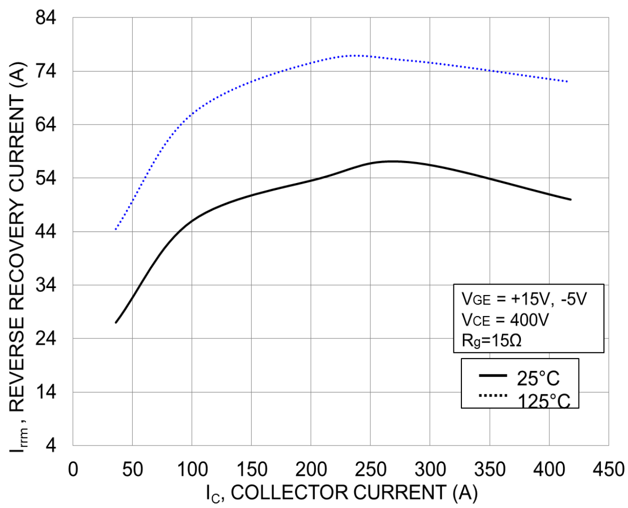


Figure 52. Typical Reverse Recovery Current vs. IC

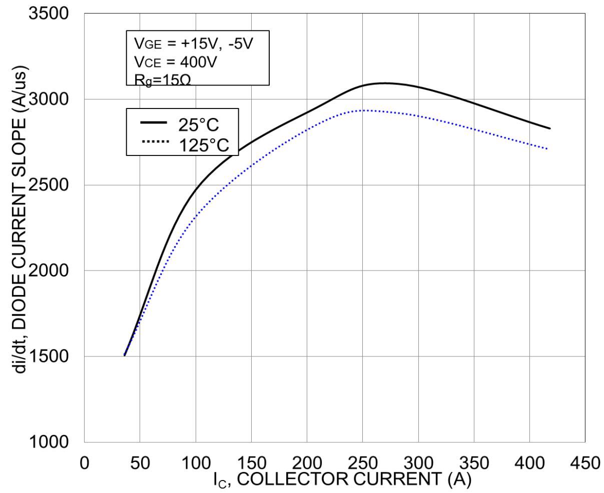


Figure 53. Typical di/dt Current Slope vs. IC

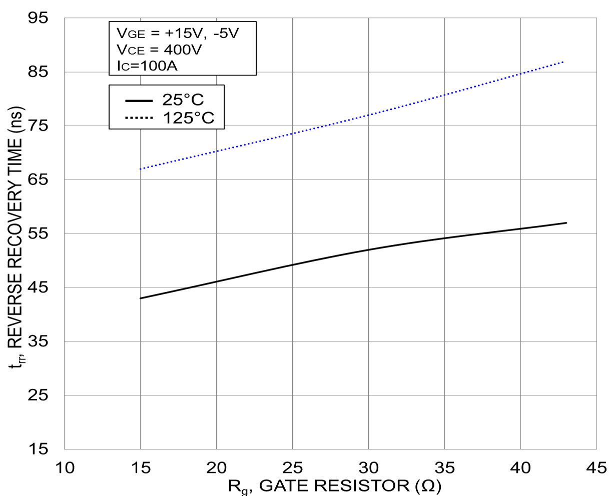


Figure 54. Typical Reverse Recovery Time vs. R_G

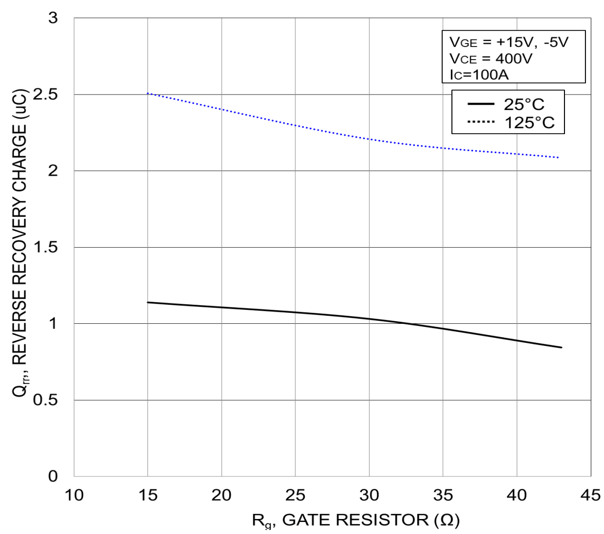


Figure 55. Typical Reverse Recovery Charge vs. R_G

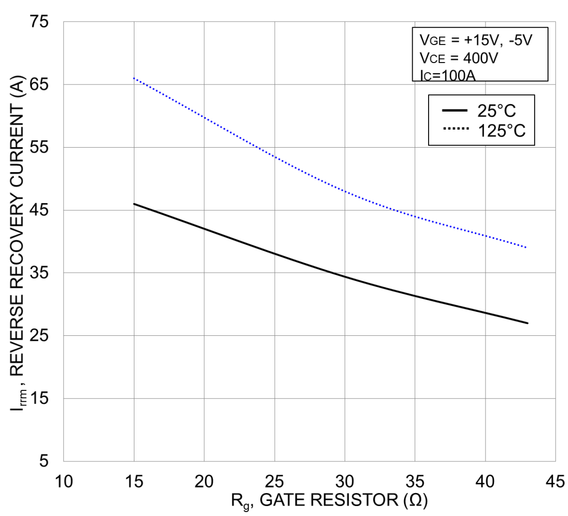


Figure 56. Typical Reverse Recovery Peak Current vs. R_G

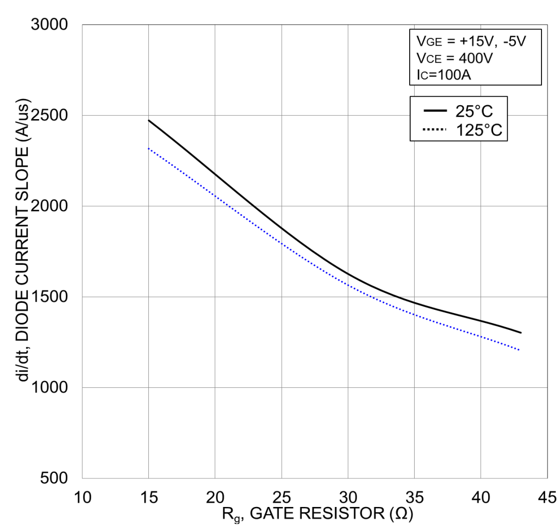
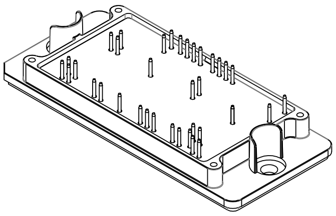


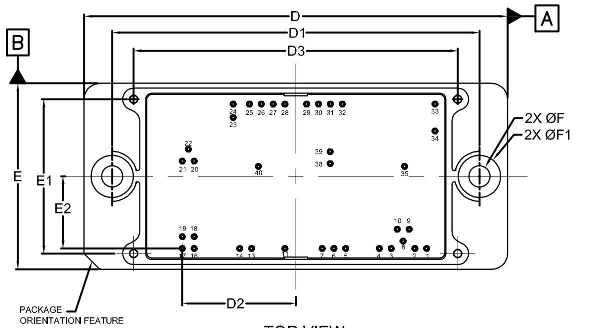
Figure 57. Typical di/dt vs. R_G



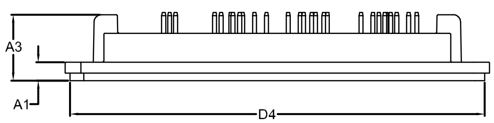
PIM40, 107.2x47
CASE 180BE
ISSUE C

DATE 27 JUL 2022

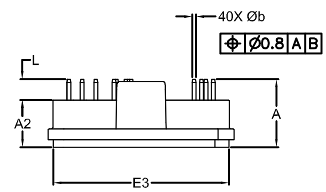
DIM	MILLIMETERS MIN.	NOM.	MAX.
A	16.63	17.23	17.83
A1	4.50	4.70	4.90
A2	11.60	12.00	12.40
A3	16.40	16.70	17.00
b	0.95	1.00	1.05
D	106.80	107.20	107.60
D1	92.90	93.00	93.10
D2	28.40	28.70	29.00
D3	81.80	82.00	82.20
D4	104.35	104.75	105.15
E	46.60	47.00	47.40
E1	38.80	39.00	39.20
E2	17.95	18.25	18.55
E3	44.30	44.40	44.50
F	5.40	5.50	5.60
F1		10.70 REF	
L	5.03	5.23	5.43



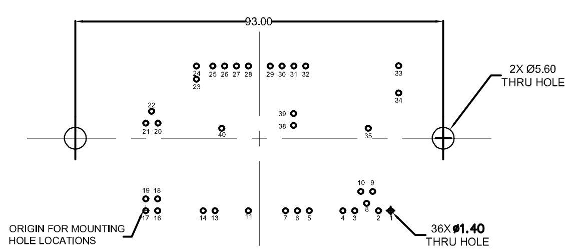
TOP VIEW



SIDE VIEW



END VIEW



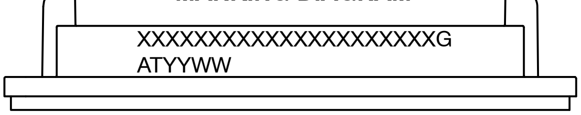
RECOMMENDED MOUNTING PATTERN*

For additional information on our Pb-Free strategy and soldering details, please download the On Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTE 4

PIN	PIN POSITION X	Y	PIN	PIN POSITION X	Y
1	61.85	0.0	21	0.0	22.1
2	58.85	0.0	22	1.5	25.1
3	52.85	0.0	23	12.85	33.15
4	49.85	0.0	24	12.85	36.5
5	41.35	0.0	25	16.95	36.5
6	38.35	0.0	26	19.95	36.5
7	35.35	0.0	27	22.95	36.5
8	55.85	1.85	28	25.95	36.5
9	57.35	4.85	29	31.45	36.5
10	54.35	4.85	30	34.45	36.5
11	25.95	0.0	31	37.45	36.5
13	17.5	0.0	32	40.45	36.5
14	14.5	0.0	33	63.9	36.55
16	3.0	0.0	34	63.9	29.7
17	0.0	0.0	35	56.2	20.75
18	3.0	3.0	38	37.4	21.5
19	0.0	3.0	39	37.4	24.5
20	3.0	22.1	40	19.2	20.75

GENERIC MARKING DIAGRAM*



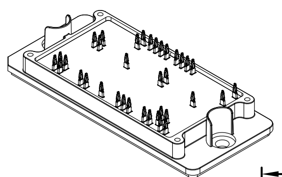
XXXXX = Specific Device Code
G = Pb−Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

NOTES:

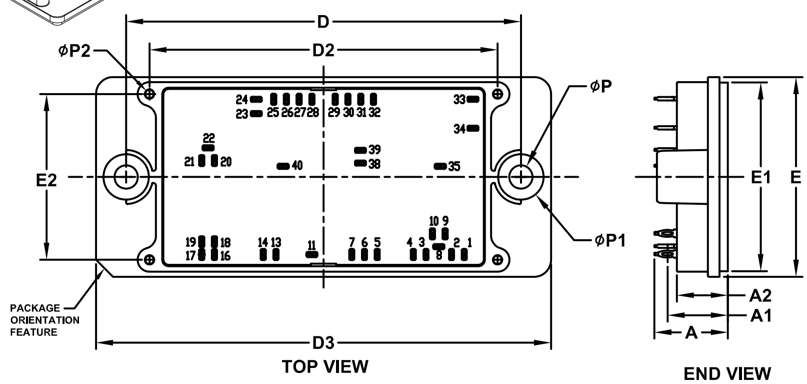
1. DIMENSIONING AND TOLERANCING PER ASME 7 14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b APPLY TO THE PLATED TERMINALS AND ARE MEASURED WHERE THE PIN EXITS THE PACKAGE BODY.
4. POSITION OF THE CENTER OF THE TERMINALS IS DETERMINED FROM PIN 17. POSITIONAL TOLERANCE, AS NOTED IN THE DRAWING, APPLIES TO EACH TERMINAL.

DOCUMENT NUMBER:	98AON06409H	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PIM40, 107.2x47	PAGE 1 OF 1

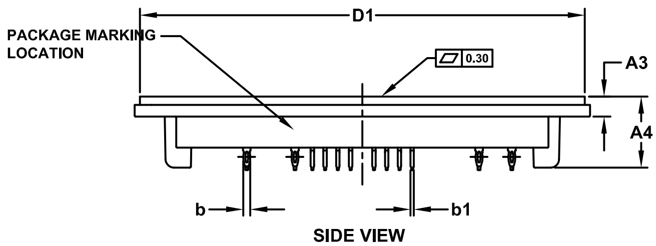


PIM36, 93x47 (PRESSFIT)
CASE 180CD
ISSUE O

DATE 24 APR 2020

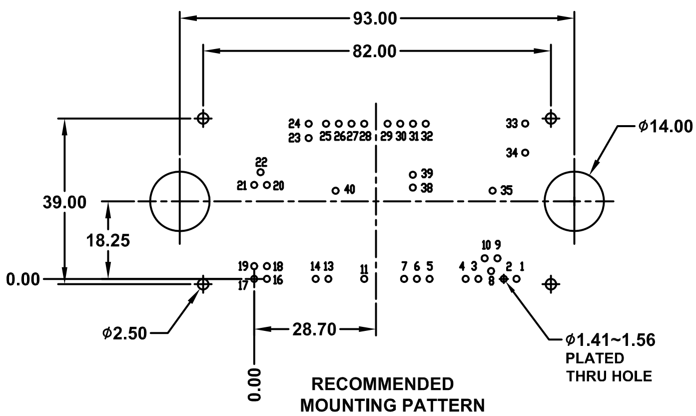


DIM	MILLIMETERS MIN.	NOM.	MAX.
A	16.90	17.30	17.70
A1	13.97	14.18	14.39
A2	11.70	12.00	12.30
A3	4.40	4.70	5.00
A4	16.40	16.70	17.00
b	1.61	1.66	1.71
b1	0.75	0.80	0.85
D	92.90	93.00	93.10
D1	104.45	104.75	105.05
D2	81.80	82.00	82.20
D3	106.90	107.20	107.50
E	46.70	47.00	47.30
E1	44.10	44.40	44.70
E2	38.80	39.00	39.20
P	5.40	5.50	5.60
P1	10.60	10.70	10.80
P2	1.80	2.00	2.20



NOTE 4

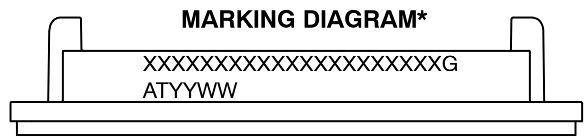
PIN	PIN POSITION X	Y	PIN	PIN POSITION X	Y
1	61.85	0.00	21	0.00	22.10
2	58.85	0.00	22	1.50	25.10
3	52.85	0.00	23	12.85	33.15
4	49.85	0.00	24	12.85	36.50
5	41.35	0.00	25	16.95	36.50
6	38.35	0.00	26	19.95	36.50
7	35.35	0.00	27	22.95	36.50
8	55.85	1.85	28	25.95	36.50
9	57.35	4.85	29	31.45	36.50
10	54.35	4.85	30	34.45	36.50
11	25.95	0.00	31	37.45	36.50
13	17.50	0.00	32	40.45	36.50
14	14.50	0.00	33	63.90	36.55
16	3.00	0.00	34	63.90	29.70
17	0.00	0.00	35	56.20	20.75
18	3.00	3.00	38	37.40	21.50
19	0.00	3.00	39	37.40	24.50
20	3.00	22.10	40	19.20	20.75



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009
2. CONTROLLING DIMENSION : MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A1
4. PIN POSITION TOLERANCE IS ± 0.4mm
5. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
G = Pb−Free Package
AT = Assembly & Test Site Code
YYWW= Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	PIM36 93X47 (PRESS FIT)	PAGE 1 OF 1

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