



THE DATASHEET OF EVAL-SDP-CS1Z



SDP-S Controller Board

FEATURES

USB-to-serial engine

Peripherals exposed

SPI

TWI/I²C

GPIO

USB 2.0 PC connectivity

PC software stack and base firmware provided

GENERAL DESCRIPTION

This user guide describes the EVAL-SDP-CS1Z system demonstration platform-serial (SDP-S) controller board from Analog Devices, Inc. The SDP-S controller board is part of the Analog Devices system demonstration platform (SDP). The SDP consists of a series of controller boards, interposer boards, and daughter boards. SDP controller boards provide a means of communicating with the system under evaluation from the PC. Interposer boards route signals between two connectors. Daughter boards are a collection of product evaluation boards and Circuits from the Lab™ reference circuit boards. The SDP-S is used as part of the evaluation system for many Analog Devices components and reference circuits. The primary audience for this user guide is the system engineer who seeks to understand

how to set up the SDP-S board and begin USB communications to the PC.

The SDP-S board is designed to be used in conjunction with various Analog Devices component evaluation boards and Circuits from the Lab reference circuits as part of a customer evaluation environment. The SDP-S provides USB connectivity through a USB 2.0 high speed connection to the computer, allowing users to evaluate components on this platform from a PC application. The SDP-S is based on a USB-to-serial engine, which has SPI, I²C, and GPIO lines available, with a 120-pin small footprint connector.

This user guide provides instructions for installing the SDP-S hardware (EVAL-SDP-CS1Z board) and software onto a computer. The necessary installation files are provided with the evaluation daughter board package. The Getting Started section provides software and hardware installation procedures, PC system requirements, and basic board information. The Evaluation Board Hardware section provides information on the EVAL-SDP-CS1Z components. The EVAL-SDP-CS1Z schematics are provided in the Evaluation Board Schematics section.

For more information about the SDP-S board, go to www.analog.com/sdp.



Figure 1. Picture of EVAL-SDP-CS1Z

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REVISION HISTORY

8/11—Rev. 0 to Rev. A

| | |
|--|---|
| Removed SDRAM Memory from Features Section..... | 1 |
| Removed SDRAM Memory from Product Overview Section ... | 3 |

7/11—Revision 0: Initial Version

PRODUCT OVERVIEW

The SDP-S board includes the following:

- USB-to-serial engine
- 1 × 120-pin small footprint connector
 - Hirose FX8-120P-SV1(91), 120-pin header
- Peripherals exposed
 - SPI
 - TWI/I²C
 - GPIO

PACKAGE CONTENTS

The EVAL-SDP-CS1Z board package contains the following:

- EVAL-SDP-CS1Z board
- 1 m USB Standard-A-to Mini-B-cable

Contact the vendor where the SDP-S board was purchased, or contact Analog Devices if anything is missing.

TECHNICAL OR CUSTOMER SUPPORT

Analog Devices customer support can be reached in the following ways:

- Visit the SDP homepage at www.analog.com/sdp
- Email processor questions to psa.support@analog.com
- Visit the Analog Devices Wiki page at www.wiki.analog.com/sdp
- Visit the EngineerZone for community technical support at ez.analog.com.
- Phone questions to 1-800-ANALOGD
- Contact your Analog Devices local sales office or authorized distributor.
- Send questions by mail to
Analog Devices, Inc.
Three Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
USA

ANALOG DEVICES WEB SITE

The Analog Devices website, www.analog.com, provides information about a broad range of products—analogue integrated circuits, amplifiers, converters, and digital signal processors.

Also, note that MyAnalog.com is a free feature of the Analog Devices website that allows customization of a web page to display only the latest information about products of interest to you. You can choose to receive weekly email notifications containing updates to the web pages that meet your interests, including documentation errata against all documents.

MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Visit MyAnalog.com to sign up. If you are a registered user, simply log on. Your user name is your email address.

GETTING STARTED

This section provides specific information to assist with using the SDP-S board as part of the user's evaluation system.

The following topics are covered:

- PC configuration
- USB installation
- Powering up/powering down the SDP-S

PC CONFIGURATION

For correct operation of the SDP board, the user's computer must have the following minimum configuration:

- Windows XP Service Pack 2 or Windows Vista®
- USB 2.0 port

When removing the SDP-S board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components.

USB INSTALLATION

Perform the following tasks to safely install the SDP-S board onto the computer. There are two stages in the software application installation procedure. The first stage installs the application software. The second stage installs the .NET Framework 3.5 and the necessary drivers.

Installing the Software

1. Run the application installation file provided. The first stage installs the application GUI and the necessary support files onto the computer.
2. Immediately following the application installation, the .NET Framework 3.5 and the driver package for the SDP board are installed. If the .NET Framework 3.5 is already preinstalled on the computer, this stage is skipped and Step 2 consists of a driver package installation only.

Connecting the SDP-S Board to the PC

Attach the SDP-S board to a USB 2.0 port on the computer via the Standard-A-to-Mini-B cable provided.

Verifying Driver Installation

Before using the SDP-S board, verify the driver software has installed properly.

Open the Windows Device Manager and verify the SDP-S board appears under **ADI Development Tools**, as shown in Figure 2.

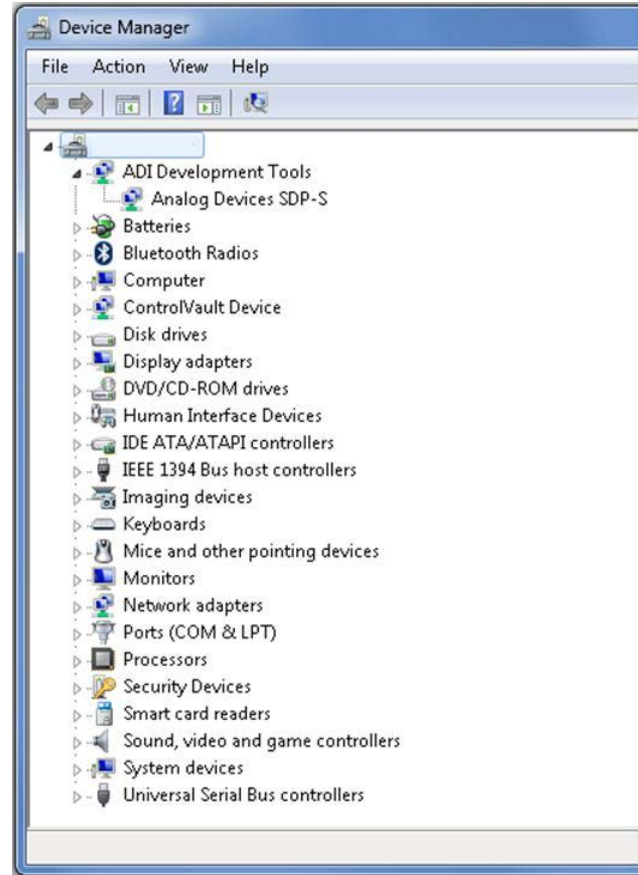


Figure 2. Device Manager

POWERING UP/POWERING DOWN THE SDP-S

The following sections describe how to safely power up and power down the SDP-S.

Powering Up the SDP-S Board

1. Connect the SDP-S board to the daughter evaluation board through the 120-pin mating connector.
2. Power up the daughter board.
3. Connect the USB port on the computer to the SDP-S board.

Powering Down the SDP-S Board

1. Disconnect the USB port on the computer from the SDP-S board.
2. Power down the daughter evaluation board.
3. Disconnect the SDP-S board from the daughter evaluation board.

EVALUATION BOARD HARDWARE

This section describes the hardware design of the EVAL-SDP-CS1Z board.

The following topics are covered:

- LEDs—This section describes the SDP-S on-board LEDs.
- Connector details—This section details the pin assignments on the 120-pin connector.
- Power—This section lists power requirements of the SDP-S and identifies connector power inputs and output pins.
- Daughter board design guidelines—This section provides guidelines on how to design daughter boards for use with the SDP-S.
- Mechanical specifications—This section provides dimensional information.

LEDS

There are two LEDs located on the SDP-S board (see Figure 3).

Power LED (PWR)

The green power LED indicates that the SDP-S board is powered. This is not an indication of USB connectivity between the SDP-S and the PC.

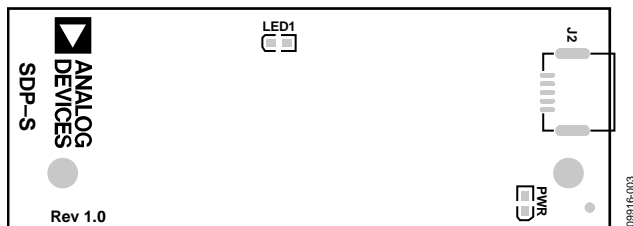


Figure 3. SDP-S Board LEDs

LED1

The orange LED is an LED used as a diagnostic tool for evaluation application developers.

CONNECTOR DETAILS

The SDP-S board contains one Hirose FX8-120P-SV1(91), 120-pin header connector. Through this connector, the peripheral communication interfaces of the USB-to-serial engine are exposed. The exposed peripherals are

- SPI
- I²C/TWI
- GPIO

Also included on the connector specification are input and output power pins, ground pins, and pins reserved for future use.

Connector Pin Assignments

Table 1 lists the connector pins and identifies the functionality assigned to each connector pin on the SDP-S board.

The pinout of this connector is consistent with other connectors across the SDP family.

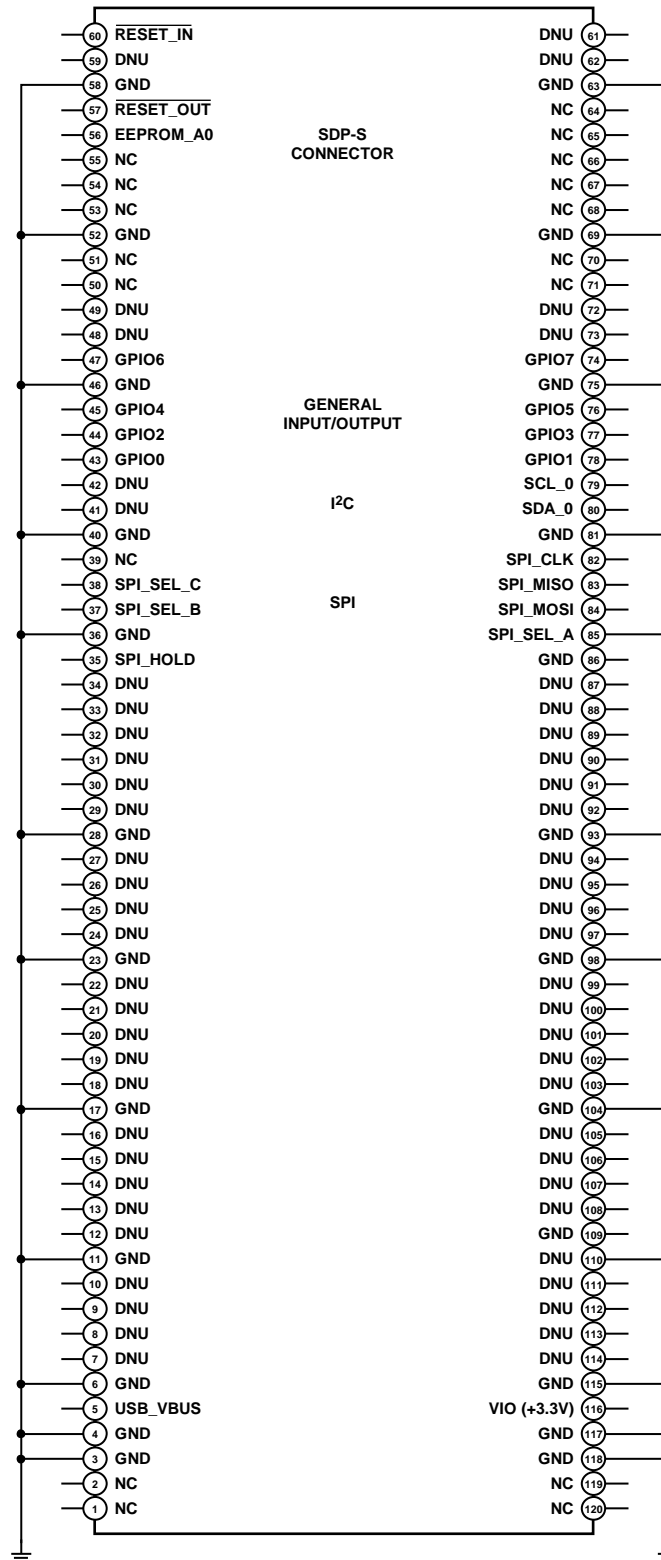
Table 1. 120-Pin Connector Pin Assignments

| Pin No. | Pin Name | Description |
|---------|-----------|--|
| 1 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 2 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 3 | GND | Connect to the ground plane of the daughter board. |
| 4 | GND | Connect to the ground plane of the daughter board. |
| 5 | USB_VBUS | Connected directly to the USB 5 V supply. |
| 6 | GND | Connect to the ground plane of the daughter board. |
| 7 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 8 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 9 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 10 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 11 | GND | Connect to the ground plane of the daughter board. |
| 12 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 13 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 14 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 15 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 16 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 17 | GND | Connect to the ground plane of the daughter board. |
| 18 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 19 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 20 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 21 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 22 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 23 | GND | Connect to the ground plane of the daughter board. |
| 24 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 25 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 26 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 27 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 28 | GND | Connect to the ground plane of the daughter board. |
| 29 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 30 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 31 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 32 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 33 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 34 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 35 | SPI_HOLD | Detects the ready state of the daughter board for SPI transfer. |
| 36 | GND | Connect to the ground plane of the daughter board. |
| 37 | SPI_SEL_B | SPI Chip Select B. Use this to control a second device on the SPI bus. |
| 38 | SPI_SEL_C | SPI Chip Select C. Use this to control a third device on the SPI bus. |
| 39 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 40 | GND | Connect to the ground plane of the daughter board. |
| 41 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 42 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 43 | GPIO0 | General-purpose input/output. |
| 44 | GPIO2 | General-purpose input/output. |
| 45 | GPIO4 | General-purpose input/output. |
| 46 | GND | Connect to the ground plane of the daughter board. |
| 47 | GPIO6 | General-purpose input/output. |
| 48 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 49 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 50 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 51 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 52 | GND | Connect to the ground plane of the daughter board. |

| Pin No. | Pin Name | Description |
|---------|-----------|--|
| 53 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 54 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 55 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 56 | EEPROM_A0 | EEPROM A0. Connect to the A0 address line of the EEPROM. |
| 57 | RESET_OUT | Active low pin for resetting the daughter board. Driven by SDP-S. |
| 58 | GND | Connect to the ground plane of the daughter board. |
| 59 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 60 | RESET_IN | Active low pin to reset EVAL-SDP-CS1Z board. |
| 61 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 62 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 63 | GND | Connect to the ground plane of the daughter board. |
| 64 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 65 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 66 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 67 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 68 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 69 | GND | Connect to the ground plane of the daughter board. |
| 70 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 71 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 72 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 73 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 74 | GPIO7 | General-purpose input/output. |
| 75 | GND | Connect to the ground plane of the daughter board. |
| 76 | GPIO5 | General-purpose input/output. |
| 77 | GPIO3 | General-purpose input/output. |
| 78 | GPIO1 | General-purpose input/output. |
| 79 | SCL_0 | I ² C Clock 0. The daughter board EEPROM must be connected to this bus. |
| 80 | SDA_0 | I ² C Data 0. The daughter board EEPROM must be connected to this bus. |
| 81 | GND | Connect to the ground plane of the daughter board. |
| 82 | SPI_CLK | SPI clock. |
| 83 | SPI_MISO | SPI master in, slave out data. |
| 84 | SPI_MOSI | SPI master out, slave in data. |
| 85 | SPI_SEL_A | SPI Chip Select A. |
| 86 | GND | Connect to the ground plane of the daughter board. |
| 87 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 88 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 89 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 90 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 91 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 92 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 93 | GND | Connect to the ground plane of the daughter board. |
| 94 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 95 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 96 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 97 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 98 | GND | Connect to the ground plane of the daughter board. |
| 99 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 100 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 101 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 102 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 103 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 104 | GND | Connect to the ground plane of the daughter board. |
| 105 | DNU | Do not use. Leave this pin unconnected. Do not ground. |

| Pin No. | Pin Name | Description |
|---------|-------------|---|
| 106 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 107 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 108 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 109 | GND | Connect to the ground plane of the daughter board. |
| 110 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 111 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 112 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 113 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 114 | DNU | Do not use. Leave this pin unconnected. Do not ground. |
| 115 | GND | Connect to the ground plane of the daughter board. |
| 116 | VIO (+3.3V) | 3.3 V output. 20 mA maximum current available to power the I/O voltage on the daughter board. |
| 117 | GND | Connect to the ground plane of the daughter board. |
| 118 | GND | Connect to the ground plane of the daughter board. |
| 119 | NC | No connect. Leave this pin unconnected. Do not ground. |
| 120 | NC | No connect. Leave this pin unconnected. Do not ground. |

Each interface provided by the SDP-S is available on unique pins of the SDP-S 120-pin connector. The connector pin numbering scheme is outlined in Figure 4.



- NOTES**
 1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
 2. DNU = DO NOT USE. DO NOT CONNECT TO THIS PIN.

Figure 4. 120-Pin Connector Outline

09P16-004

POWER

The SDP-S board is powered by the USB connector. It does not require power to be supplied by the daughter board. The SDP-S board provides 3.3 V at 20 mA on Pin 116 (VIO_3.3) to connected daughter boards as the VIO voltage for the daughterboard. Pin 5 (USB_VBUS) is connected to the 5 V line of the USB connector, providing 5 V \pm 10% as an output of the SDP board.

DAUGHTER BOARD DESIGN GUIDELINES

The daughter board design guidelines specify the layout, connector positioning, keep out areas, and dimensions of potential daughter boards. This guidance is to ensure that a daughter board can connect to any controller board from the SDP family. Following these guidelines ensures that the connector on the SDP-S or any other controller board in the SDP family can have any one of the available daughter boards physically attached.

Connector Location

The daughter board connector and securing screw holes are located in the top left hand corner. This arrangement for a daughter board is shown in Figure 5.

If a daughter board exceeds these dimensions, it may not be possible to connect it to the other controller or interposer boards in the SDP family. Every effort was made to extend the 5.9 mm dimension as large as possible to allow space for vias between the connector and the edge of the board. These are absolute maximum dimensions and must not be exceeded.

The full specification drawing for the connector location on the daughter board is shown in Figure 6.

The mating daughter board 120-pin connector is the Hirose FX8-120S-SV(21), 120-pin receptacle, FEC 132-4660, Digi-Key H1219-ND. Consult the connector data sheet for full details on the connector. Note that Pin 1 to Pin 60 are placed on the left side of the connector and Pin 61 to Pin 120 are placed on the right side of the connector.

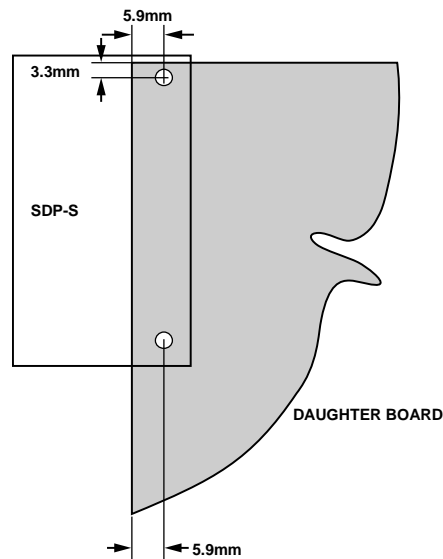


Figure 5. Maximum Board Dimensions for Connector Placement

09916-005

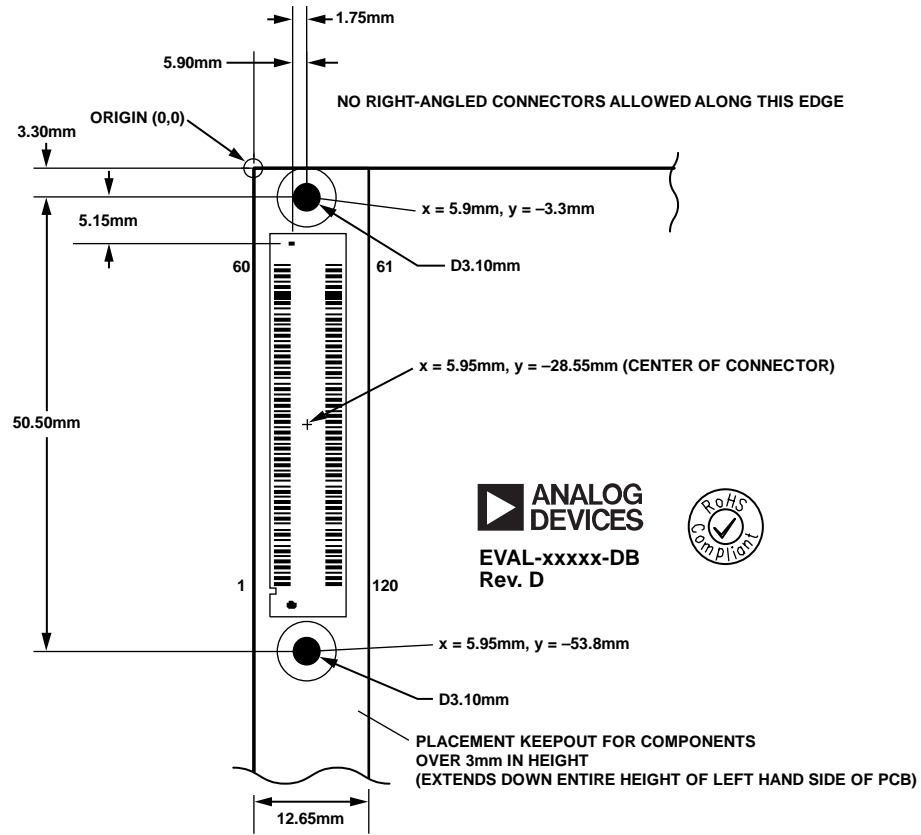


Figure 6. Connector Placement on Compatible Daughter Boards

Keep Out Area

To allow the greatest flexibility for future controller boards, a keep out area is established for components higher than 3 mm. The keep out area is 12.65 mm wide and extends down the entire left side of the daughter board.

Restriction on Right Angle Connectors

Due to the layout of other boards in the SDP family, and their daughter boards, right angle connectors are not allowed on the top and left edges of the daughter boards and (if required) should be placed on the right or bottom edges. A right angle

connector describes any connector that requires the connection to protrude over the edge of the board (for example, right angle SMB or screw terminal).

MECHANICAL SPECIFICATIONS

The mechanical specifications of the SDP-S board are 2.36 inch \times 0.87 inch (60 mm \times 22 mm). The tallest component on the top is approximately 0.17 inch (4.3 mm), and the tallest components on the bottoms are the 120-pin connectors at approximately 0.152 inch (3.86 mm). Refer to Figure 7.

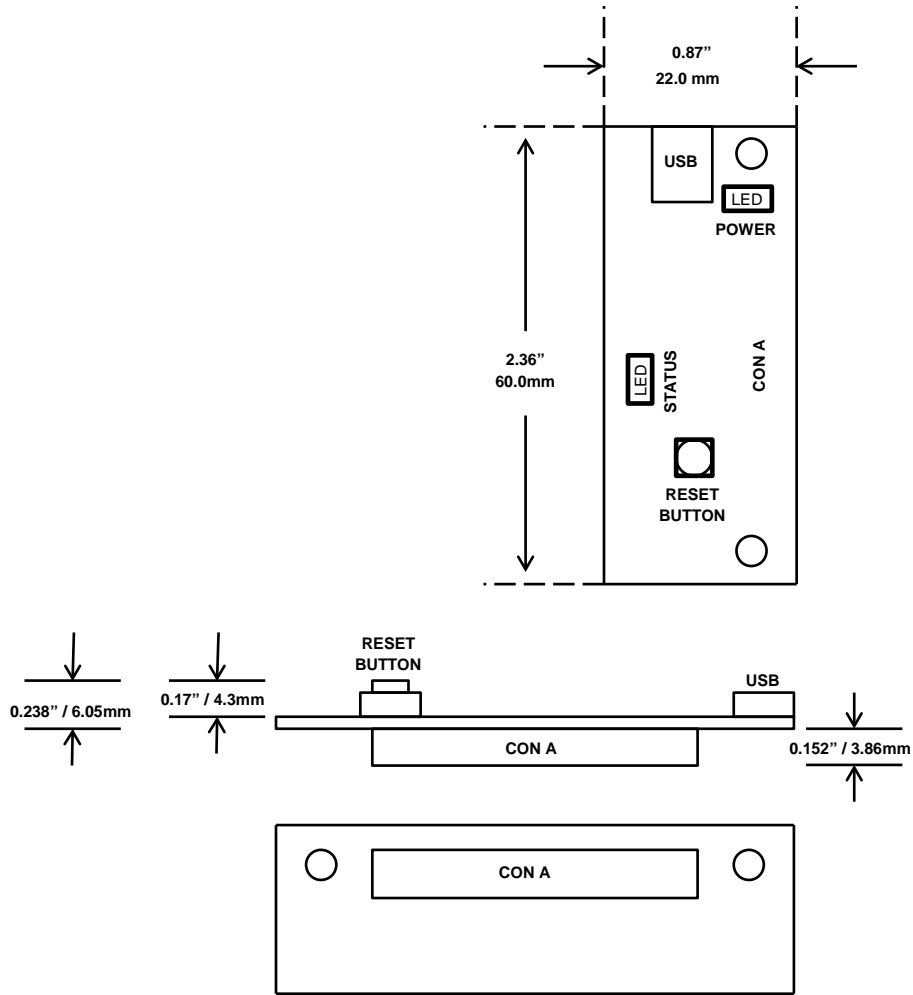


Figure 7. SDP-S Board Mechanical Specifications

EVALUATION BOARD SCHEMATICS

This section provides the schematic drawings for the EVAL-SDP-CB1Z board, which include

- SDP-S—USB-to-serial engine, USB, interface (see Figure 8)
- SDP-S—Connector (see Figure 9)

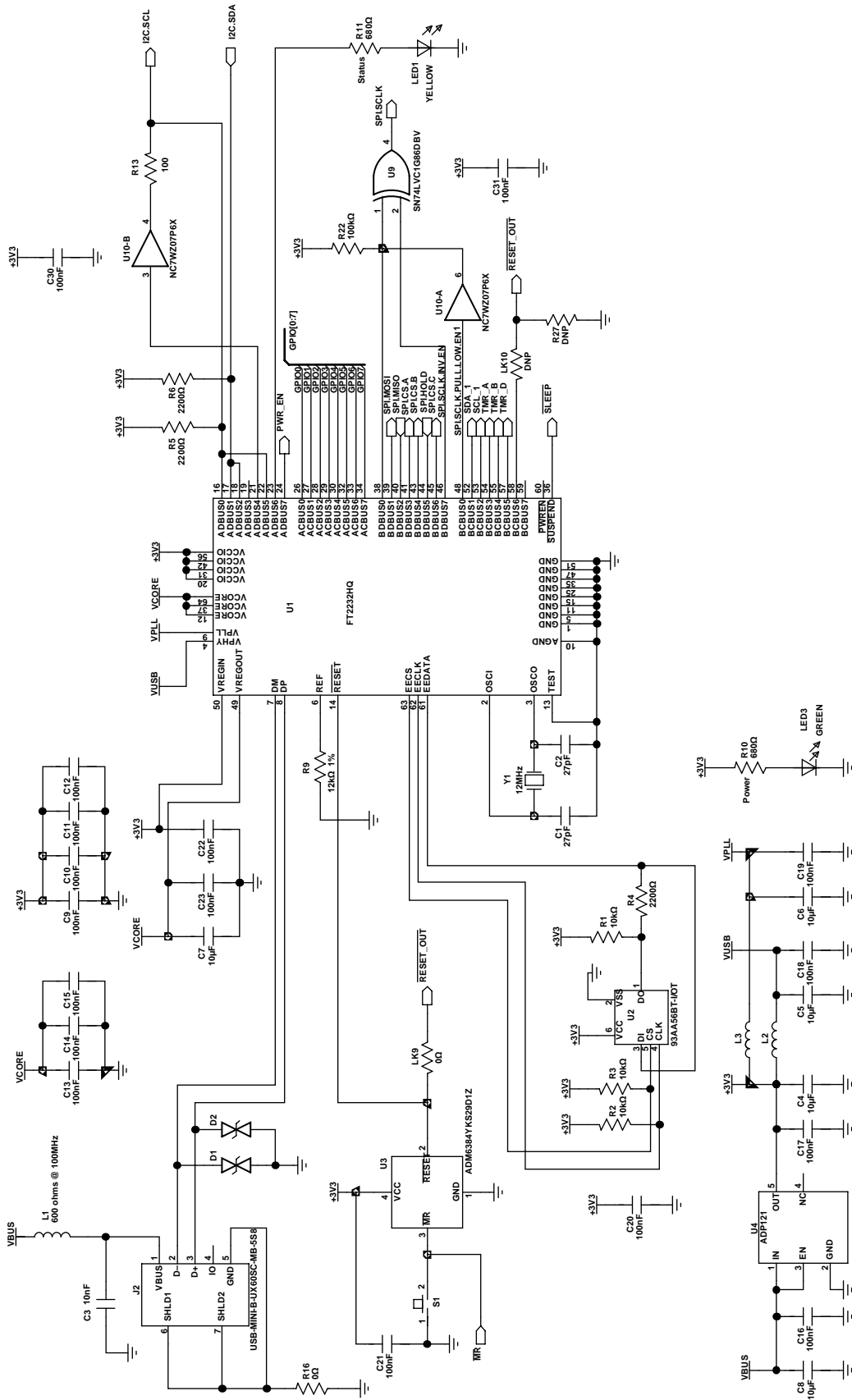


Figure 8. SDP-S—USB-to-Serial Engine, USB, Interface

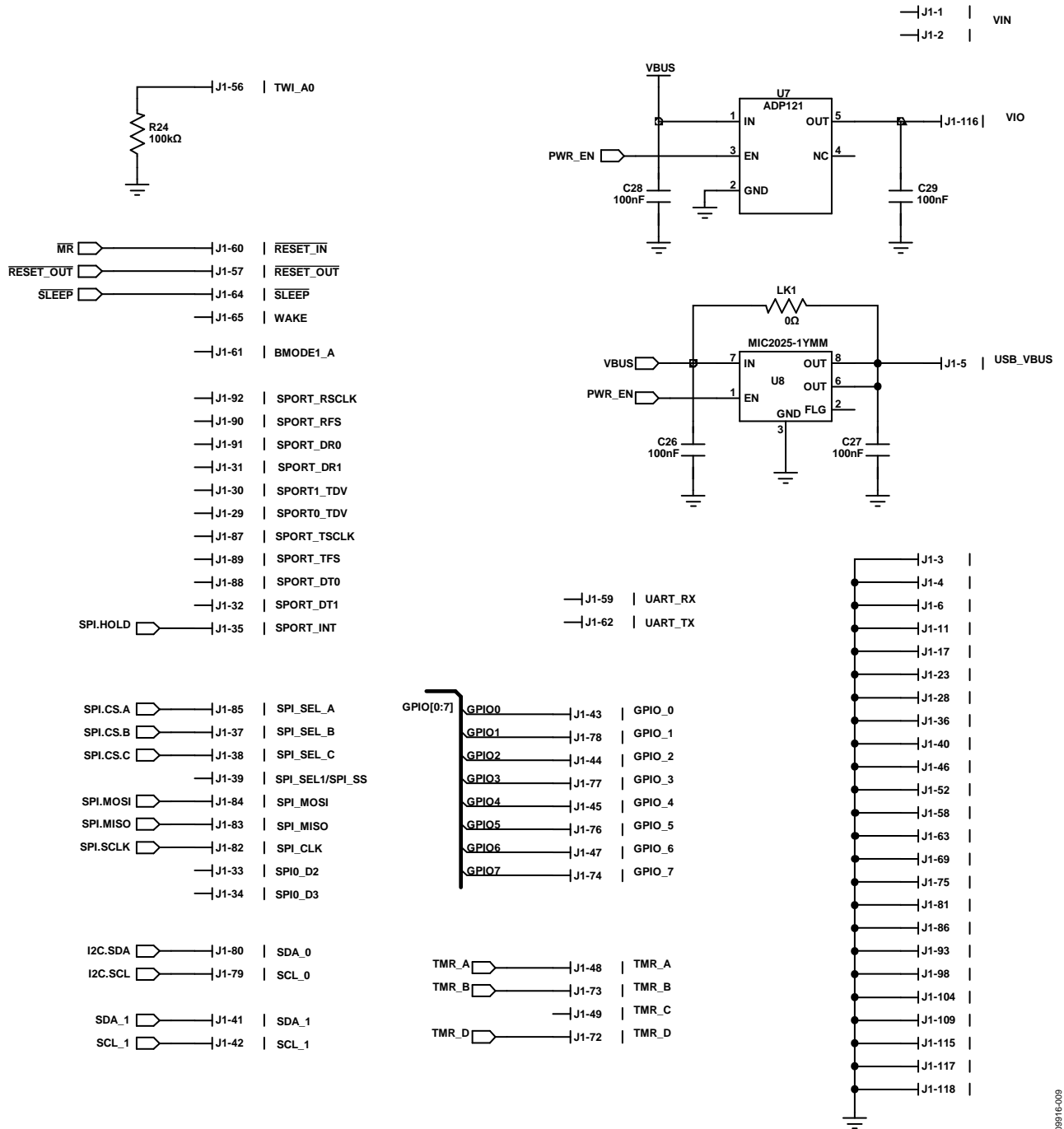


Figure 9. SDP-S—Connector

09915-009

NOTES

¹²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

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Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management