FEATURES

- ARM®720T Processor
  - — ARM7TDMI CPU operating at speeds of 74 and 90 MHz
  - — 8 KBytes of four-way set-associative cache
  - — MMU with 64-entry TLB
  - — Thumb code support enabled
- Ultra low power
  - — 90 mW at 74 MHz typical
  - — 108 mW at 90 MHz typical
  - — <.03 mW in the Standby State
- Advanced audio decoder/decompression capability
  - — Supports bit streams with adaptive bit rates
  - — Allows for support of multiple audio decompression algorithms (MP3, WMA, AAC, Audible, etc.)

Plays Windows Media™

(cont.)

High-Performance, Low-Power System on Chip with SDRAM and Enhanced Digital Audio Interface

OVERVIEW

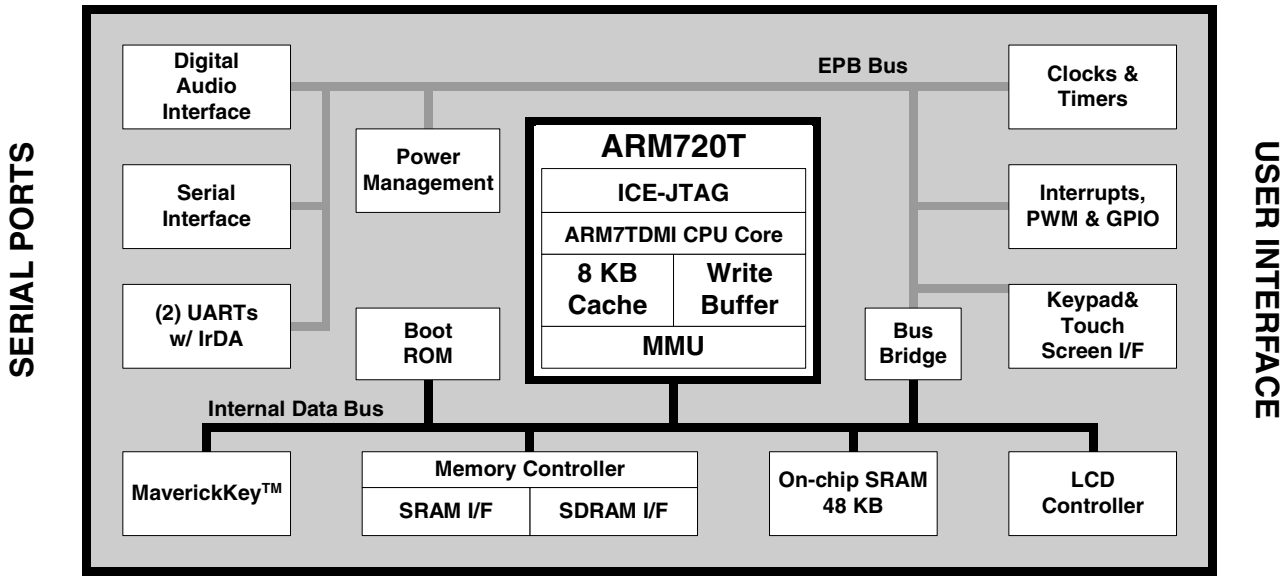
The Cirrus Logic™ EP7312 is designed for ultra-low-power portable and line-powered applications such as portable consumer entertainment devices, home and car audio juke box systems, and general purpose industrial control applications, or any device that features the added capability of digital audio compression & decompression. The core-logic functionality of the device is built around an ARM720T processor with 8 KBytes of four-way set-associative unified cache and a write buffer. Incorporated into the ARM720T is an enhanced memory management unit (MMU) which allows for support of sophisticated operating systems like Microsoft® Windows® CE and Linux®.

ORDERING INFORMATION:

See list of available parts with legend on page 63.

(cont.)

BLOCK DIAGRAM



MEMORY and STORAGE

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FEATURES *(cont)*

- 48 KBytes of on-chip SRAM
- MaverickKey™ IDs
  - — 32-bit unique ID can be used for DRM compliance 128-bit random ID
- Available in 74 and 90 MHz clock speeds
- LCD controller
  - — Interfaces directly to a single-scan panel monochrome STN LCD
  - — Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Full JTAG boundary scan and Embedded ICE® support
- Integrated Peripheral Interfaces
  - — 32-bit SDRAM Interface up to 2 external banks
  - — 8/32/16-bit SRAM/FLASH/ROM Interface
  - — Digital Audio Interface providing glueless interface to low-power DACs, ADCs and CODECs
  - — Two Synchronous Serial Interfaces (SSI1, SSI2)
  - — CODEC Sound Interface
  - — 8×8 Keypad Scanner
  - — 27 General Purpose Input/Output pins
  - — Dedicated LED flasher pin from the RTC
- Internal Peripherals
  - — Two 16550 compatible UARTs
  - — IrDA Interface
  - — Two PWM Interfaces
  - — Real-time Clock
  - — Two general purpose 16-bit timers
  - — Interrupt Controller
  - — Boot ROM
- Package
  - — 208-Pin LQFP
  - — 256-Ball PBGA
  - — 204-Ball TFBGA
- The fully static EP7312 is optimized for low power dissipation and is fabricated on a 0.25 micron CMOS process

OVERVIEW *(cont.)*

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states: operating, idle and standby.

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, high quality ADCs, DACs, or CODECs such as the Cirrus Logic CS53L32A, CS43L42, and CS42L50 are easily added to an EP73xx design via the DAI. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

Simply by adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

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Description of the EP7312's Components, Functionality, and Interfaces

The following sections describe the EP7312 in more detail.

Processor Core - ARM720T

The EP7312 incorporates an ARM 32-bit RISC micro controller that controls a wide range of on-chip peripherals. The processor utilizes a three-stage pipeline consisting of fetch, decode and execute stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) instruction sets
- Enhanced MMU for Microsoft Windows CE and other operating systems
- 8 KB of 4-way set-associative cache.
- Translation Look Aside Buffers with 64 Translated Entries

Power Management

The EP7312 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states:

- Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.
- Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.
- Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Table 1 shows the power management pin assignments.

Table 1. Power Management Pin Assignments

Pin Mnemonic	I/O	Pin Description
BATOK	I	Battery ok input
nEXTPWR	I	External power supply sense input
nPWRFL	I	Power fail sense input
nBATCHG	I	Battery changed sense input

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP7312 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP7312 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

Memory Interfaces

There are two main external memory interfaces. The first one is the ROM/SRAM/FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256 MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8-, 16-, or 32-bits wide. This allows the use of 8-bit-wide boot ROM options to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density. shows the Static Memory Interface pin assignments.

Table 2. Static Memory Interface Pin Assignments

Pin Mnemonic		I/O	Pin Description
nCS[5:0]		O	Chip select out
A[27:0]		O	Address output
D[31:0]		I/O	Data I/O
nMOE/nSDCAS	(Note)	O	ROM expansion OP enable
nMWE/nSDWE	(Note)	O	ROM expansion write enable
HALFWORD		O	Halfword access select output
WORD		O	Word access select output
WRITE/nSDRAS	(Note)	O	Transfer direction

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

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The second is the programmable 16- or 32-bit-wide SDRAM interface that allows direct connection of up to two banks of SDRAM, totaling 512 Mb. To assure the lowest possible power consumption, the EP7312 supports self-refresh SDRAMs, which are placed in a low-power state by the device when it enters the low-power Standby State. Table 3 shows the SDRAM Interface pin assignments.

Table 3. SDRAM Interface Pin Assignments

Pin Mnemonic		I/O	Pin Description
SDCLK		O	SDRAM clock output
SDCKE		O	SDRAM clock enable output
nSDCS[1:0]		O	SDRAM chip select out
WRITE/nSDRAS	(Note 2)	O	SDRAM RAS signal output
nMOE/nSDCAS	(Note 2)	O	SDRAM CAS control signal
nMWE/nSDWE	(Note 2)	O	SDRAM write enable control signal
A[27:15]/DRA[0:12]	(Note 1)	O	SDRAM address
A[14:13]/DRA[12:14]		O	SDRAM internal bank select
PD[7:6]/SDQM[1:0]	(Note 2)	I/O	SDRAM byte lane mask
SDQM[3:2]		O	SDRAM byte lane mask
D[31:0]		I/O	Data I/O

Note: 1. Pins A[27:13] map to DRA[0:14] respectively. (i.e. A[27}/DRA[0}, A[26}/DRA[1], etc.) This is to balance the load for large memory systems.
2. Pins are multiplexed. See Table 19 on page 11 for more information.

Digital Audio Capability

The EP7312 uses its powerful 32-bit RISC processing engine to implement audio decompression algorithms in software. The nature of the on-board RISC processor, and the availability of efficient C-compilers and other software development tools, ensures that a wide range of audio decompression algorithms can easily be ported to and run on the EP7312

Universal Asynchronous Receiver/Transmitters (UARTs)

The EP7312 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the RX/TX signals to/from UART 1 to enable these signals to drive an infrared communication interface directly. Table 4 shows the UART pin assignments.

Table 4. Universal Asynchronous Receiver/Transmitters Pin Assignments

Pin Mnemonic	I/O	Pin Description
TXD[1]	O	UART 1 transmit
RXD[1]	I	UART 1 receive
CTS	I	UART 1 clear to send
DCD	I	UART 1 data carrier detect
DSR	I	UART 1 data set ready
TXD[2]	O	UART 2 transmit
RXD[2]	I	UART 2 receive
LEDDRV	O	Infrared LED drive output
PHDIN	I	Photo diode input

Digital Audio Interface (DAI)

The EP7312 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, the DAI can directly interface with the Crystal CS43L41/42/43 low-power audio DACs and the Crystal CS53L32 low-power ADC. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions. Table 5 shows the DAI Interface pin assignments.

Table 5. DAI Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
SCLK	O	Serial bit clock
SDOUT	O	Serial data out
SDIN	I	Serial data in
LRCK	O	Sample clock
MCLKIN	I	Master clock input
MCLKOUT	O	Master clock output

Note: See Table 18 on page 11 for information on pin multiplexes.

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CODEC Interface

The EP7312 includes an interface to telephony-type CODECs for easy integration into voice-over-IP and other voice communications systems. The CODEC interface is multiplexed to the same pins as the DAI and SSI2. Table 6 shows the CODEC Interface Pin Assignments.

Table 6. CODEC Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
PCMCLK	O	Serial bit clock
PCMOUT	O	Serial data out
PCMIN	I	Serial data in
PCMSYNC	O	Frame sync

Note: See Table 18 on page 11 for information on pin multiplexes.

SSI2 Interface

An additional SPI/Microwire1-compatible interface is available for both master and slave mode communications. The SSI2 unit shares the same pins as the DAI and CODEC interfaces through a multiplexer. The SSI2 Interface has these features:

- Synchronous clock speeds of up to 512 kHz
- Separate 16 entry TX and RX half-word wide FIFOs
- Half empty/full interrupts for FIFOs
- Separate RX and TX frame sync signals for asymmetric traffic

Table 7 shows the SSI2 Interface pin assignments.

Table 7. SSI2 Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
SSICLK	I/O	Serial bit clock
SSITXDA	O	Serial data out
SSIRXDA	I	Serial data in
SSITXFR	I/O	Transmit frame sync
SSIRXFR	I/O	Receive frame sync

Note: See Table 18 on page 11 for information on pin multiplexes.

Synchronous Serial Interface

The EP7312 Synchronous Serial Interface has these features:

- ADC (SSI) Interface: Master mode only; SPI and Microwire1-compatible (128 kbps operation)
- Selectable serial clock polarity

Table 8 shows the Synchronous Serial Interface pin assignments.

Table 8. Serial Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
ADCLK	O	SSI1 ADC serial clock
ADCIN	I	SSI1 ADC serial input
ADCOUT	O	SSI1 ADC serial output
nADCCS	O	SSI1 ADC chip select
SMPCLK	O	SSI1 ADC sample clock

LCD Controller

A DMA address generator is provided that fetches video display data for the LCD controller from memory. The display frame buffer start address is programmable, allowing the LCD frame buffer to be in SDRAM, internal SRAM or external SRAM. The LCD controller has these features:

- Interfaces directly to a single-scan panel monochrome STN LCD
- Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Panel width size is programmable from 32 to 1024 pixels in 16-pixel increments
- Video frame buffer size programmable up to 128 KB
- Bits per pixel of 1, 2, or 4 bits

Table 9 shows the LCD Interface pin assignments.

Table 9. LCD Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
CL1	O	LCD line clock
CL2	O	LCD pixel clock out
DD[3:0]	O	LCD serial display data bus
FRM	O	LCD frame synchronization pulse
M	O	LCD AC bias drive

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64-Key Keypad Interface

Matrix keyboards and keypads can be easily read by the EP7312. A dedicated 8-bit column driver output generates strobes for each keyboard column signal. The pins of Port A, when configured as inputs, can be selectively OR'ed together to provide a keyboard interrupt that is capable of waking the system from a STANDBY or IDLE state. The Keypad Interface has these features:

- Column outputs can be individually set high with the remaining bits left at high-impedance
- Column outputs can be driven all-low, all-high, or all-high-impedance
- Keyboard interrupt driven by OR'ing together all Port A bits
- Keyboard interrupt can be used to wake up the system
- 8×8 keyboard matrix usable with no external logic, extra keys can be added with minimal glue logic

Table 10 shows the Keypad Interface Pin Assignments.

Table 10. Keypad Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
COL[7:0]	O	Keyboard scanner column drive

Interrupt Controller

When unexpected events arise during the execution of a program (i.e., interrupt or memory fault) an exception is usually generated. When these exceptions occur at the same time, a fixed priority system determines the order in which they are handled. The EP7312 interrupt controller has two interrupt types: interrupt request (IRQ) and fast interrupt request (FIQ). The interrupt controller has the ability to control interrupts from 22 different FIQ and IRQ sources. The Interrupt controller has these features:

- Supports 22 interrupts from a variety of sources (such as UARTs, SSI1, and key matrix.)
- Routes interrupt sources to the ARM720T's IRQ or FIQ (Fast IRQ) inputs
- Five dedicated off-chip interrupt lines operate as level sensitive interrupts

Table 11 shows the interrupt controller pin assignments.

Table 11. Interrupt Controller Pin Assignments

Pin Mnemonic	I/O	Pin Description
nEINT[2:1]	I	External interrupt
EINT[3]	I	External interrupt
nEXTFIQ	I	External Fast Interrupt input
nMEDCHG/nBROM (Note)	I	Media change interrupt input

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Real-Time Clock

The EP7312 contains a 32-bit Real Time Clock (RTC) that can be written to and read from in the same manner as the timer counters. It also contains a 32-bit output match register which can be programmed to generate an interrupt.

- Driven by an external 32.768 kHz crystal oscillator

Table 12 shows the Real-Time Clock pin assignments.

Table 12. Real-Time Clock Pin Assignments

Pin Mnemonic	Pin Description
RTCIN	Real-Time Clock Oscillator Input
RTCOUT	Real-Time Clock Oscillator Output
VDDRTC	Real-Time Clock Oscillator Power
VSSRTC	Real-Time Clock Oscillator Ground

PLL and Clocking

The EP7312 processor and peripheral clocks have these features:

- Processor and peripheral clocks operate from a single 3.6864 MHz crystal or external 13 MHz clock
- Programmable clock speeds allow the peripheral bus to run at 18 MHz when the processor is set to 18 MHz and at 36 MHz when the processor is set to 36, 49 or 74 MHz, and at 45 MHz when the processor is set to 90 MHz.

Table 13 shows the PLL and clocking pin assignments.

Table 13. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Description
MOSCIN	Main Oscillator Input
MOSCOUT	Main Oscillator Output
VDDOSC	Main Oscillator Power
VSSOSC	Main Oscillator Ground

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DC-to-DC Converter Interface (PWM)

- Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a positive or negative DC to DC converter

Table 14 shows the DC-to-DC Converter Interface pin assignments.

Table 14. DC-to-DC Converter Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
DRIVE[1:0]	I/O	PWM drive output
FB[1:0]	I	PWM feedback input

Timers

- Internal (RTC) timer
- Two internal 16-bit programmable hardware count-down timers

General Purpose Input/Output (GPIO)

- Three 8-bit and one 3-bit GPIO ports
- Supports scanning keyboard matrix

Table 15 shows the GPIO pin assignments.

Table 15. General Purpose Input/Output Pin Assignments

Pin Mnemonic	I/O	Pin Description
PA[7:0]	I	GPIO port A
PB[7:0]	I	GPIO port B
PD[0]/LEDFLSH (Note)	I/O	GPIO port D
PD[5:1]	I/O	GPIO port D
PD[7:6]/SDQM[1:0] (Note)	I/O	GPIO port D
PE[1:0]/BOOTSEL[1:0] (Note)	I	GPIO port E
PE[2]/CLKSEL (Note)	I	GPIO port E

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Hardware Debug Interface

- Full JTAG boundary scan and Embedded ICE® support

Table 16 shows the Hardware Debug Interface pin assignments.

Table 16. Hardware Debug Interface Pin Assignments

Pin Mnemonic	I/O	Pin Description
TCLK	I	JTAG clock
TDI	I	JTAG data input
TDO	O	JTAG data output
nTRST	I	JTAG async reset input
TMS	I	JTAG mode select

LED Flasher

A dedicated LED flasher module can be used to generate a low frequency signal on Port D pin 0 for the purpose of blinking an LED without CPU intervention. The LED flasher feature is ideal as a visual annunciator in battery powered applications, such as a voice mail indicator on a portable phone or an appointment reminder on a PDA. Table 17 shows the LED Flasher pin assignments.

- Software adjustable flash period and duty cycle
- Operates from 32 kHz RTC clock
- Will continue to flash in IDLE and STANDBY states
- 4 mA drive current

Table 17. LED Flasher Pin Assignments

Pin Mnemonic	I/O	Pin Description
PD[0]/LEDFLSH (Note)	O	LED flasher driver

Note: Pins are multiplexed. See Table 19 on page 11 for more information.

Internal Boot ROM

The internal 128-byte Boot ROM facilitates download of saved code to the on-board SRAM/FLASH.

Packaging

The EP7312 is available in a 208-pin LQFP package, 256-ball PBGA package, or a 204-ball TFBGA package.

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Pin Multiplexing

Table 18 shows the pin multiplexing of the DAI, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the DAI is controlled by the DAISEL bit in SYSCON3 (see the *EP7312 User's Manual* for more information).

Table 18. DAI/SSI2/CODEC Pin Multiplexing

Pin Mnemonic	I/O	DAI	SSI2	CODEC
SSICLK	I/O	SCLK	SSICLK	PCMCLK
SSITXDA	O	SDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SDIN	SSIRXDA	PCMIN
SSITXFR	I/O	LRCK	SSITXFR	PCMSYNC
SSIRXFR	I	MCLKIN	SSIRXFR	p/u
BUZ	O	MCLKOUT		

Table 19 shows the pins that have been multiplexed in the EP7312.

Table 19. Pin Multiplexing

Signal	Block	Signal	Block
nMOE	Static Memory	nSDCAS	SDRAM
nMWE	Static Memory	nSDWE	SDRAM
WRITE	Static Memory	nSDRAS	SDRAM
A[27:15]	Static Memory	DRA[0:12]	SDRAM
A[14:13]	Static Memory	DRA[13:14]	SDRAM
PD[7:6]	GPIO	SDQM[1:0]	SDRAM
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

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System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7312 completes a low-power system solution. All necessary interface logic is integrated on-chip.

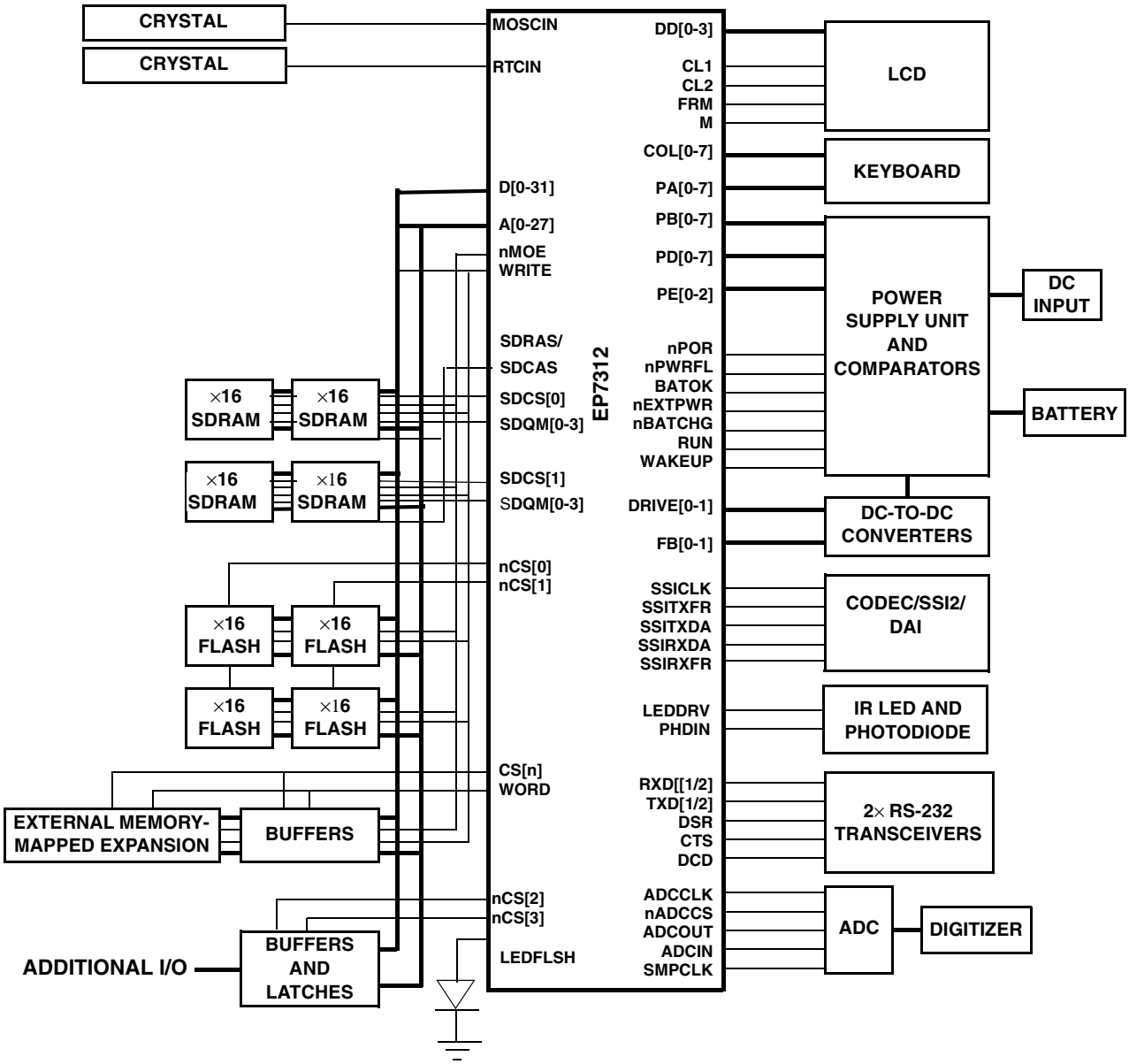

Figure 1. A Fully-Configured EP7312-Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or DAI.

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

DC Core, PLL, and RTC Supply Voltage	2.9 V
DC I/O Supply Voltage (Pad Ring)	3.6 V
DC Pad Input Current	±10 mA/pin; ±100 mA cumulative
Storage Temperature, No Power	–40°C to +125°C

Recommended Operating Conditions

DC core, PLL, and RTC Supply Voltage	2.5 V ± 0.2 V
DC I/O Supply Voltage (Pad Ring)	2.3 V - 3.5 V
DC Input / Output Voltage	O–I/O supply voltage
Operating Temperature	Extended -20°C to +70°C; Commercial 0°C to +70°C; Industrial -40°C to +85°C

DC Characteristics

All characteristics are specified at V_{DDCORE} = 2.5 V, V_{DDIO} = 3.3 V and V_{SS} = 0 V over an operating temperature of 0°C to +70°C for all frequencies of operation. The current consumption figures have test conditions specified per parameter."

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	CMOS input high voltage	$0.65 \times V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 2.5 V
VIL	CMOS input low voltage	V_{SS} – 0.3	-	$0.25 \times V_{DDIO}$	V	V_{DDIO} = 2.5 V
VT+	Schmitt trigger positive going threshold	-	-	2.1	V	
VT-	Schmitt trigger negative going threshold	0.8	-	-	V	
Vhst	Schmitt trigger hysteresis	0.1	-	0.4	V	VIL to VIH
VOH	CMOS output high voltage[a] Output drive 1[a] Output drive 2[a]	V_{DD} – 0.2 2.5 2.5	- - -	- - -	V V V	IOH = 0.1 mA IOH = 4 mA IOH = 12 mA
VOL	CMOS output low voltage[a] Output drive 1[a] Output drive 2[a]	- - -	- - -	0.3 0.5 0.5	V V V	IOL = –0.1 mA IOL = –4 mA IOL = –12 mA
IIN	Input leakage current	-	-	1.0	µA	VIN = V_{DD} or GND
IOZ	Bidirectional 3-state leakage current[b c]	25	-	100	µA	VOUT = V_{DD} or GND
CIN	Input capacitance	8	-	10.0	pF	

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Symbol	Parameter	Min	Typ	Max	Unit	Conditions
COUT	Output capacitance	8	-	10.0	pF	
CI/O	Transceiver capacitance	8	-	10.0	pF	
$IDD_{STANDBY}$ @ 25 C	Standby current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	77 41	- -	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 70 C	Standby current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	- -	570 111	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 85 C	Standby current consumption Core, Osc, RTC @2.5 V[1] I/O @ 3.3 V	- -	- -	1693 163	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{idle} at 74 MHz	Idle current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	6 10	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{IDLE} at 90 MHz	Idle current consumption Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	7 11	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$VDD_{STANDBY}$	Standby supply voltage	2.0	-	-	V	Minimum standby voltage for state retention, internal SRAM cache, and RTC operation only

a. Refer to the strength column in the pin assignment tables for all package types.

b. Assumes buffer has no pull-up or pull-down resistors.

c. The leakage value given assumes that the pin is configured as an input pin but is not currently being driven.

Note: 1) Total power consumption = IDD_{CORE} x 2.5 V + IDD_{IO} x 3.3 V

2) A typical design will provide 3.3 V to the I/O supply (i.e., V_{DDIO}), and 2.5 V to the remaining logic. This is to allow the I/O to be compatible with 3.3 V powered external logic (i.e., 3.3 V SDRAMs).

2) Pull-up current = 50 µA typical at V_{DD} = 3.3 V.

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Timings

Timing Diagram Conventions

This data sheet contains timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

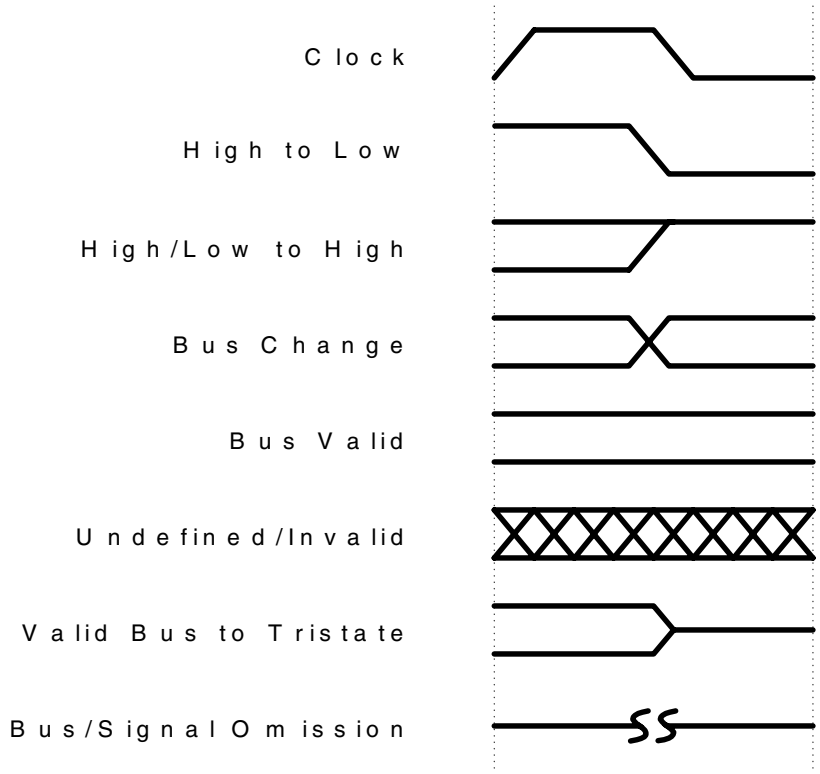

Figure 2. Legend for Timing Diagrams

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements. All characteristics are specified at V_{DDIO} = 3.1 - 3.5 V and V_{SS} = 0 V over an operating temperature of -40°C to +85°C. Pin loadings is 50 pF. The timing values are referenced to 1/2 V_{DD}.

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SDRAM Interface

Figure 3 through Figure 6 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK rising edge to SDCS assert delay time	t_{CSa}	0	2	4	ns
SDCLK rising edge to SDCS deassert delay time	t_{CSd}	– 3	2	10	ns
SDCLK rising edge to SDRAS assert delay time	t_{RAa}	1	3	7	ns
SDCLK rising edge to SDRAS deassert delay time	t_{RAd}	– 3	1	10	ns
SDCLK rising edge to SDRAS invalid delay time	t_{RAnv}	2	4	7	ns
SDCLK rising edge to SDCAS assert delay time	t_{CAa}	– 2	2	5	ns
SDCLK rising edge to SDCAS deassert delay time	t_{CAd}	– 5	0	3	ns
SDCLK rising edge to ADDR transition time	t_{ADv}	– 3	1	5	ns
SDCLK rising edge to ADDR invalid delay time	t_{ADx}	– 2	2	5	ns
SDCLK rising edge to SDMWE assert delay time	t_{MWa}	– 2	1	5	ns
SDCLK rising edge to SDMWE deassert delay time	t_{MWd}	– 4	0	4	ns
DATA transition to SDCLK rising edge time	t_{DAs}	-	-	2	ns
SDCLK rising edge to DATA transition hold time	t_{DAh}	-	-	1	ns
SDCLK rising edge to DATA transition delay time	t_{DAd}	0	-	15	ns

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SDRAM Load Mode Register Cycle

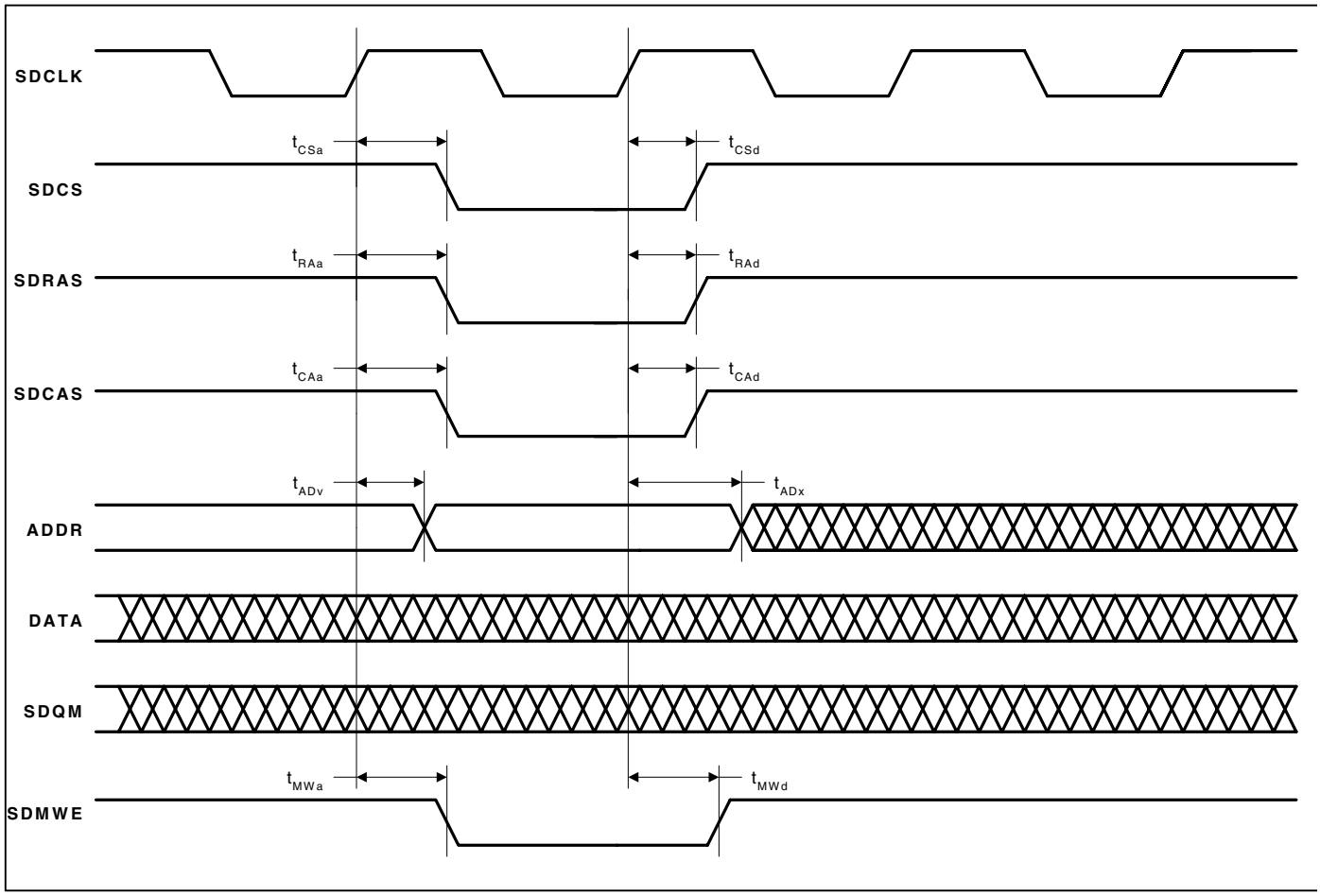

Figure 3. SDRAM Load Mode Register Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM control and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

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SDRAM Burst Read Cycle

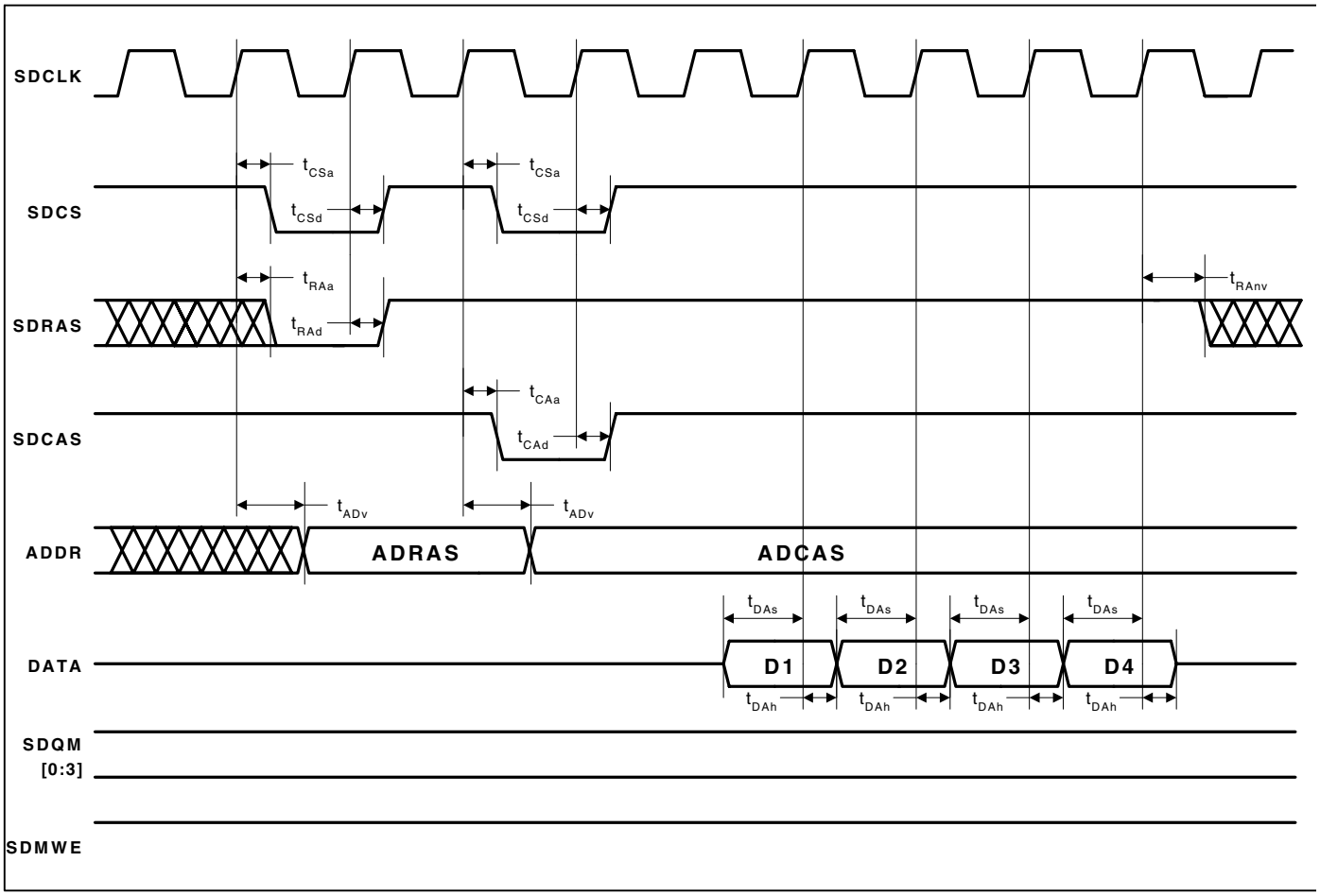

Figure 4. SDRAM Burst Read Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal.

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SDRAM Burst Write Cycle

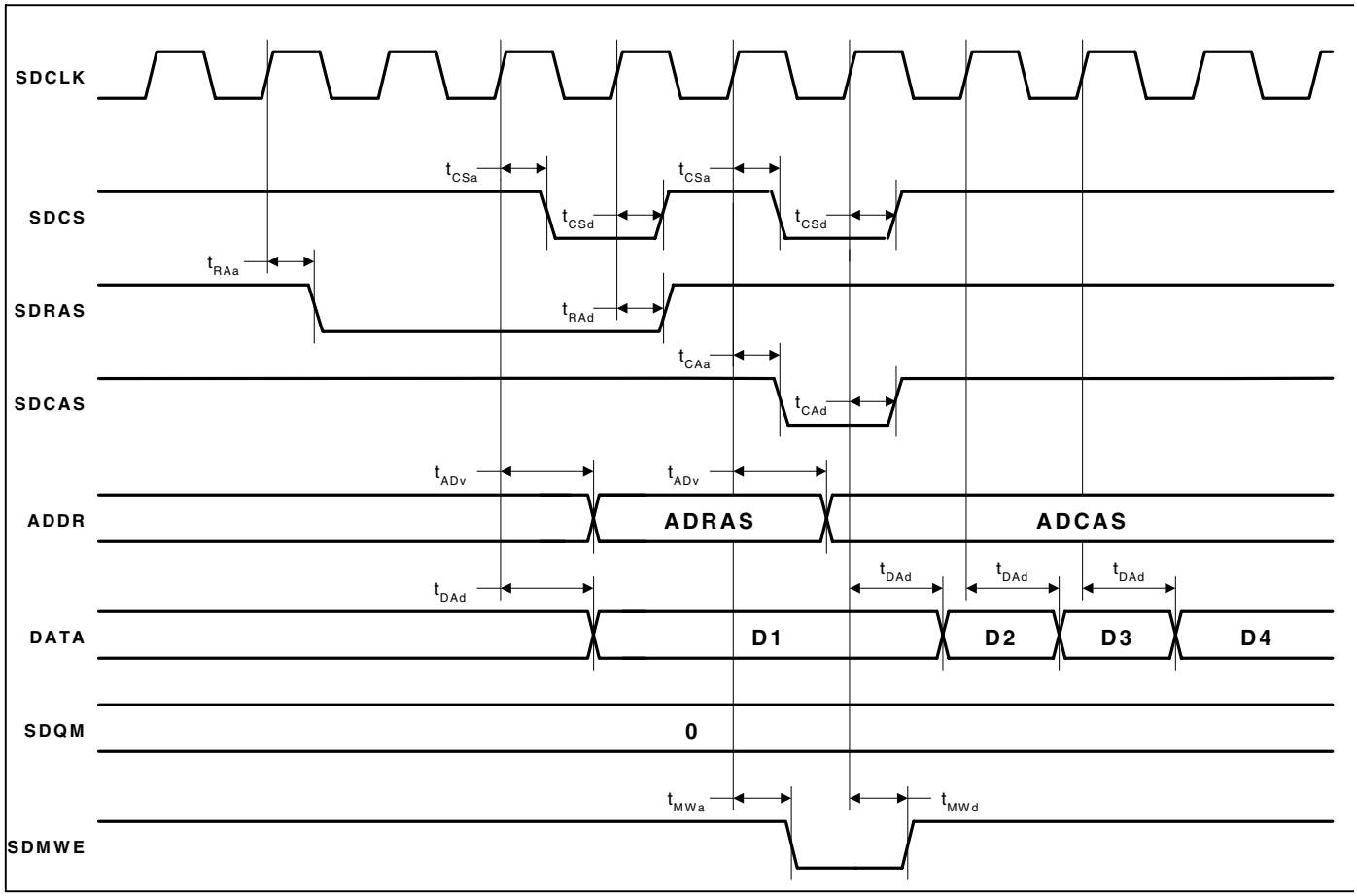

Figure 5. SDRAM Burst Write Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

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SDRAM Refresh Cycle

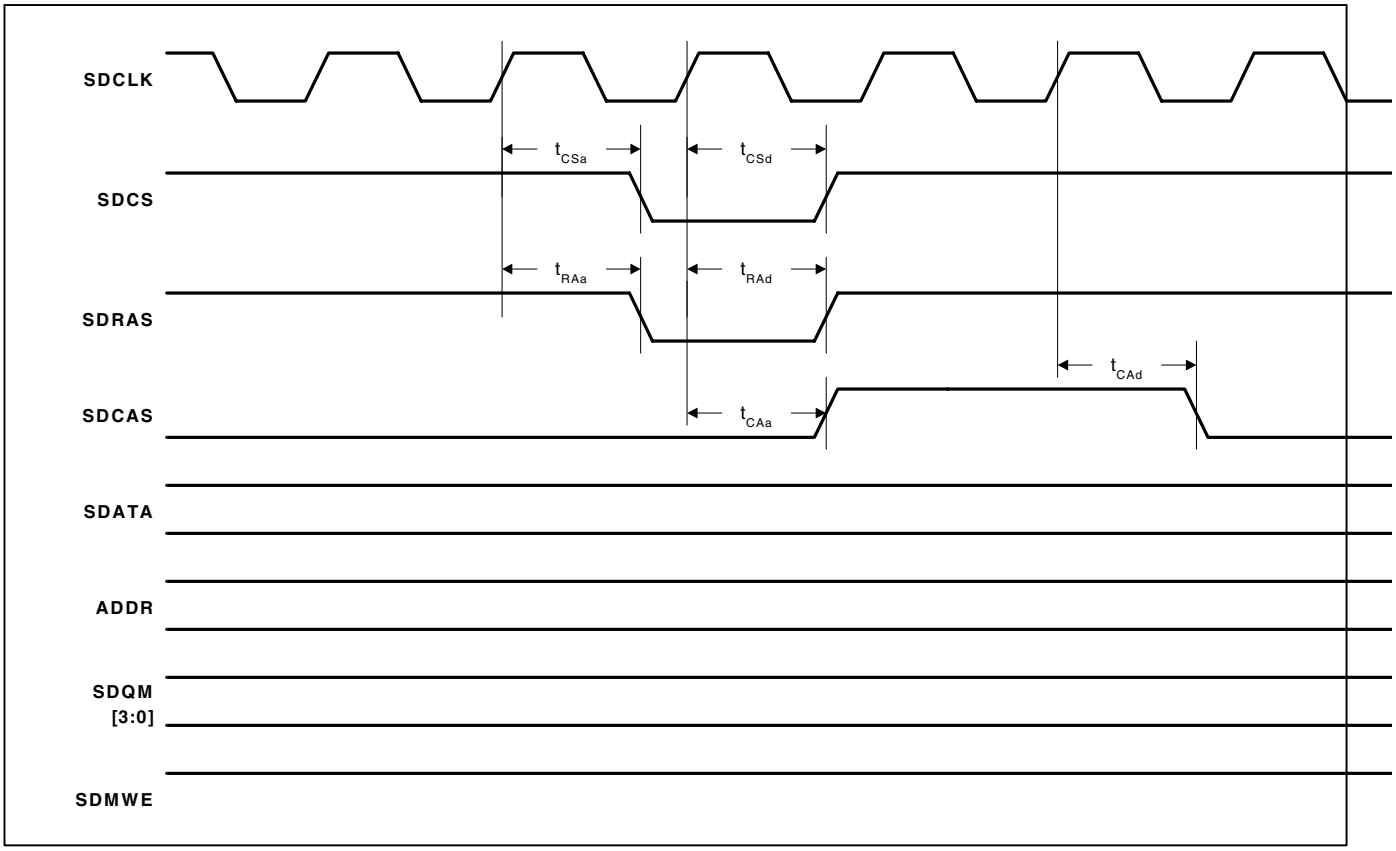

Figure 6. SDRAM Refresh Cycle Timing Measurement

Note: 1. Timings are shown with CAS latency = 2
2. The SDCLK signal may be phase shifted relative to the rest of the SDRAM central and data signals due to uneven loading. Designers should take care to ensure that delays between SDRAM controls and data signals are approximately equal

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Static Memory

Figure 7 through Figure 10 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

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Static Memory Single Read Cycle

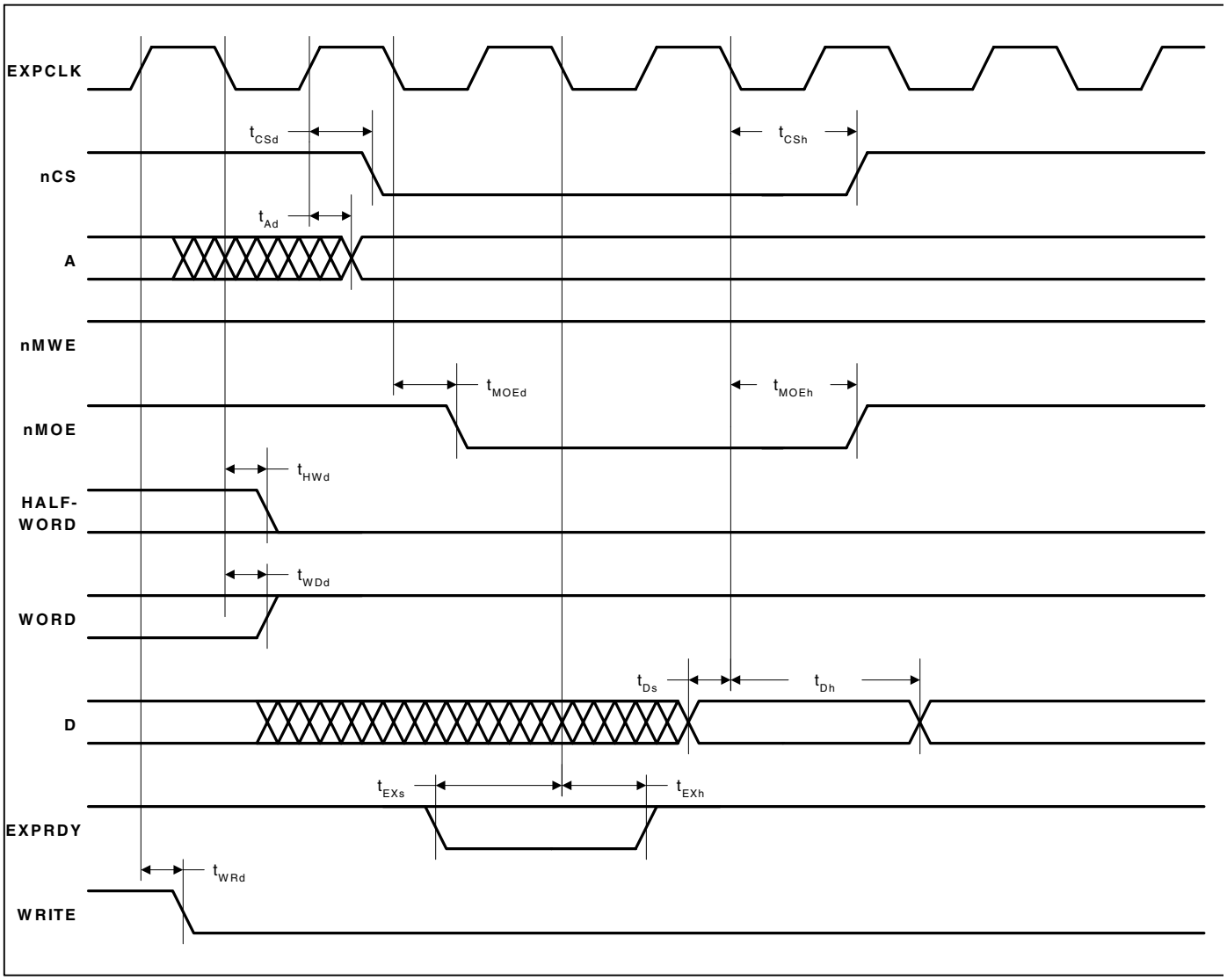

Figure 7. Static Memory Single Read Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
2. Address, Halfword, Word, and Write hold state until next cycle.

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Static Memory Single Write Cycle

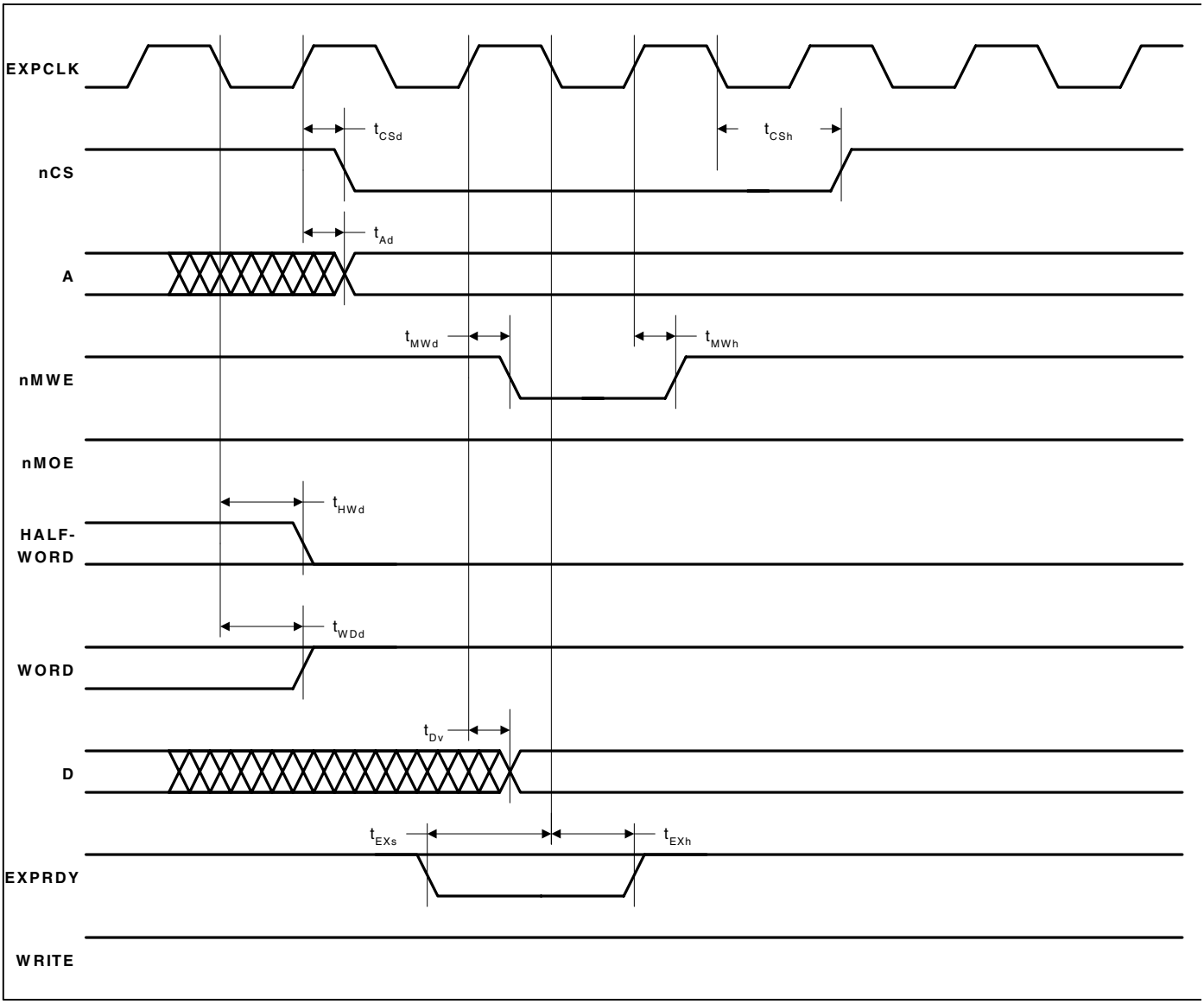

Figure 8. Static Memory Single Write Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

3. Address, Data, Halfword, Word, and Write hold state until next cycle.

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Static Memory Burst Read Cycle

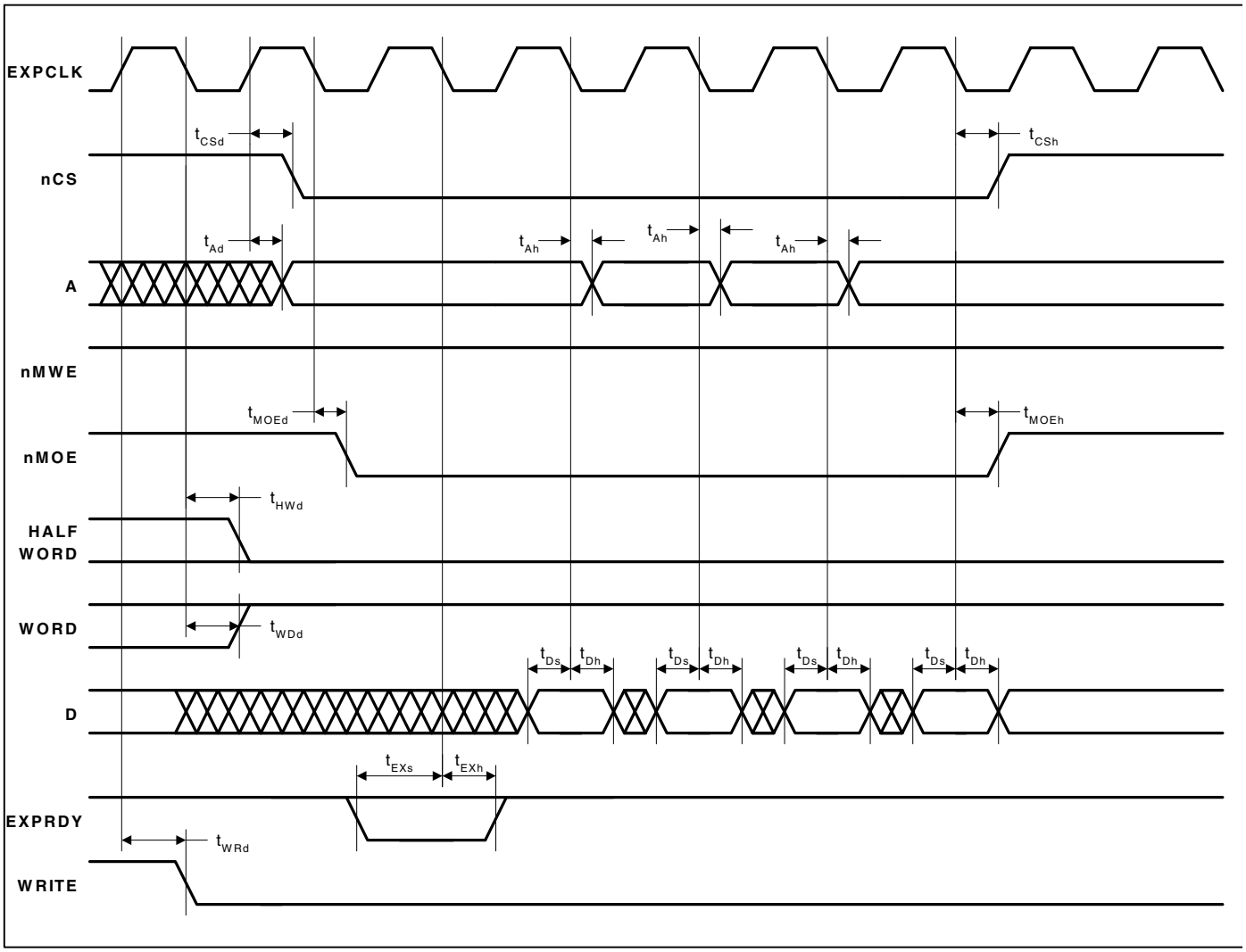

Figure 9. Static Memory Burst Read Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-0-0-0). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.
4. Address, Halfword, Word, and Write hold state until next cycle.

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Static Memory Burst Write Cycle

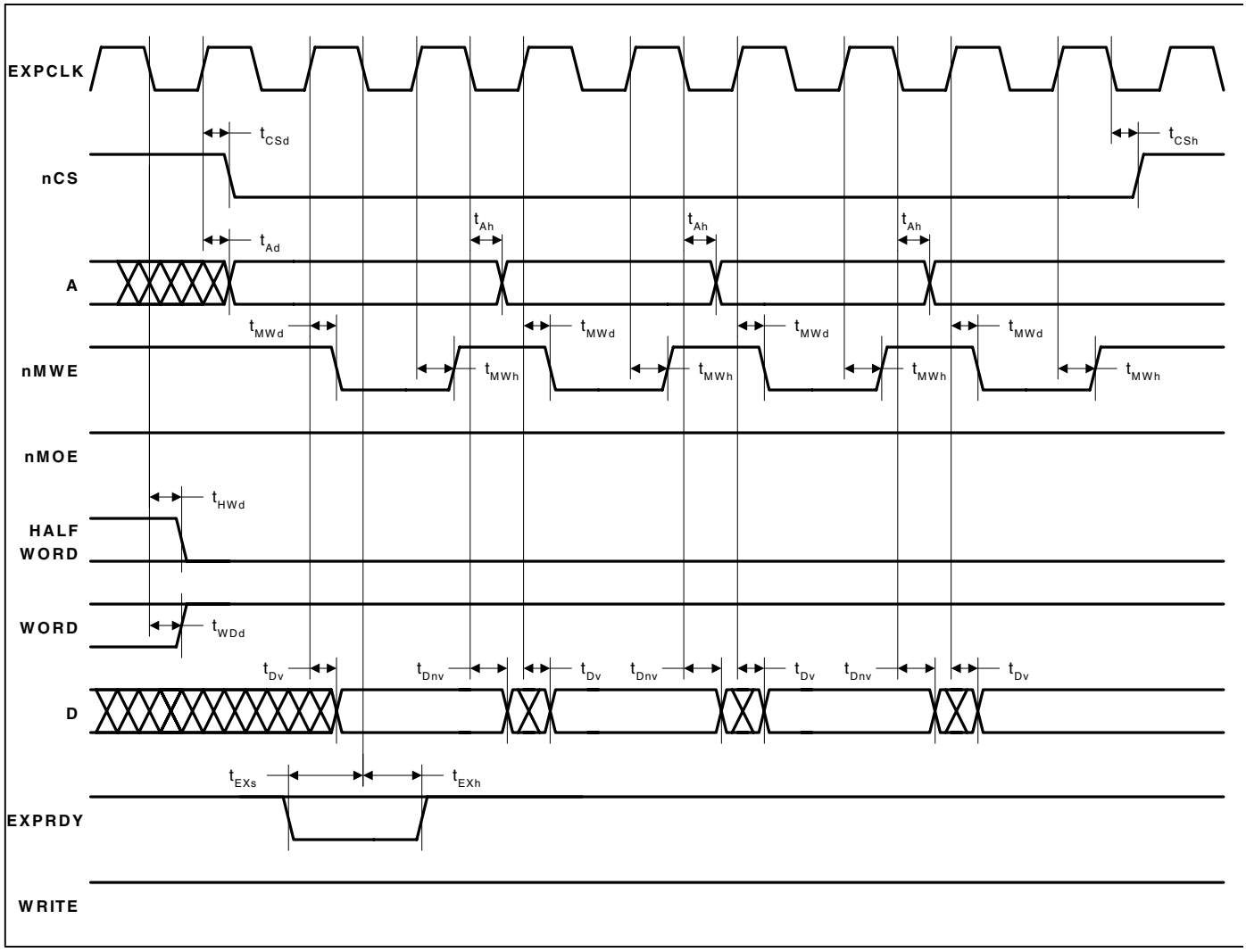

Figure 10. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.
4. Address, Data, Halfword, Word, and Write hold state until next cycle.

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SSI1 Interface

Parameter	Symbol	Min	Max	Unit
ADCCLK falling edge to nADCCSS deassert delay time	t_{Cd}	9	10	ms
ADCIN data setup to ADCCLK rising edge time	t_{INs}	-	15	ns
ADCIN data hold from ADCCLK rising edge time	t_{INh}	-	14	ns
ADCCLK falling edge to data valid delay time	t_{Ovd}	– 7	13	ns
ADCCLK falling edge to data invalid delay time	t_{Od}	– 2	3	ns

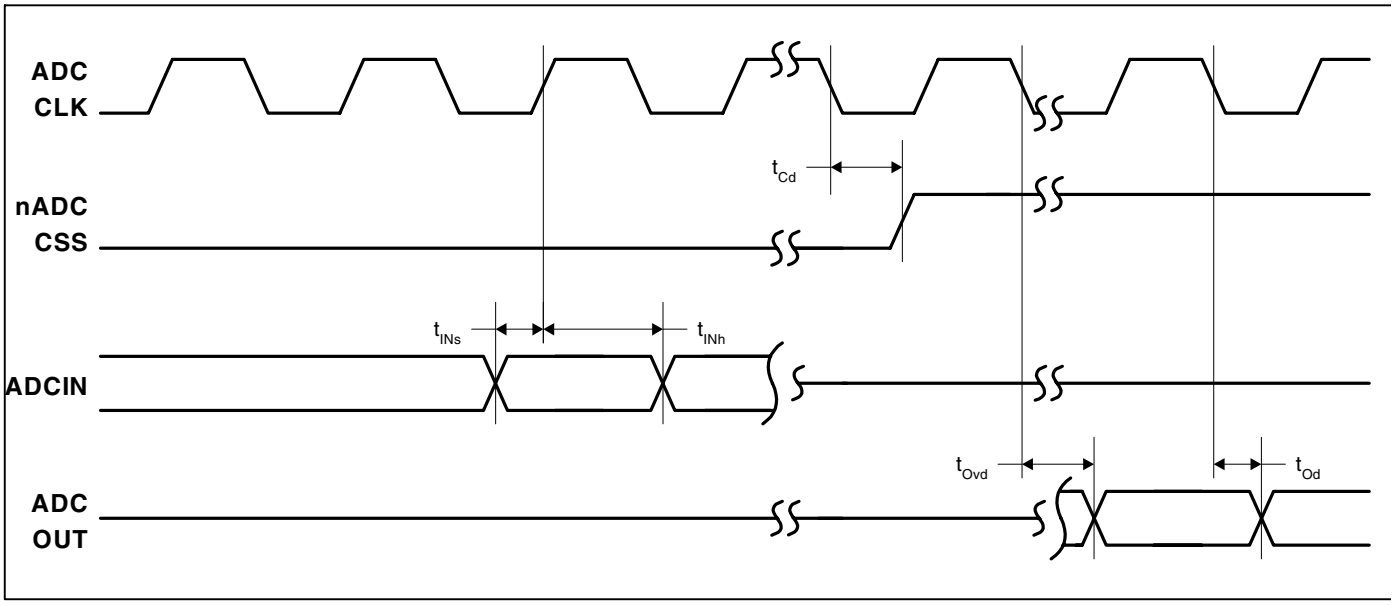

Figure 11. SSI1 Interface Timing Measurement

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SSI2 Interface

Parameter	Symbol	Min	Max	Unit
SSICLK period (slave mode)	t_{clk_per}	185	2050	ns
SSICLK high time	t_{clk_high}	925	1025	ns
SSICLK low time	t_{clk_low}	925	1025	ns
SSICLK rise/fall time	t_{clkrf}	3	18	ns
SSICLK rising edge to RX and/or TX frame sync high time	t_{FRd}	-	3	ns
SSICLK rising edge to RX and/or TX frame sync low time	t_{FRa}	-	8	ns
SSIRXFR and/or SSITXFR period	t_{FR_per}	960	990	ns
SSIRXDA setup to SSICLK falling edge time	t_{RXs}	3	7	ns
SSIRXDA hold from SSICLK falling edge time	t_{RXh}	3	7	ns
SSICLK rising edge to SSITXDA data valid delay time	t_{TXd}	-	2	ns
SSITXDA valid time	t_{TXv}	960	990	ns

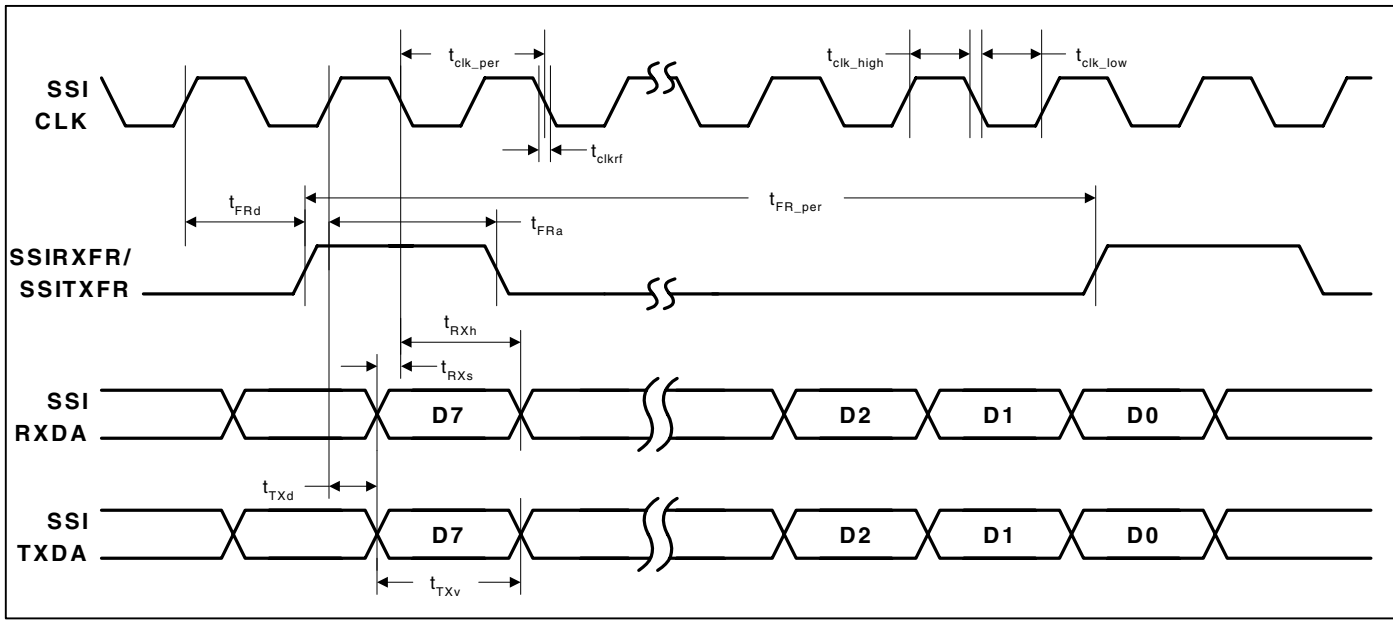

Figure 12. SSI2 Interface Timing Measurement

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LCD Interface

Parameter	Symbol	Min	Max	Unit
CL[2] falling to CL[1] rising delay time	t_{CL1d}	– 10	25	ns
CL[1] falling to CL[2] rising delay time	t_{CL2d}	80	3,475	ns
CL[1] falling to FRM transition time	t_{FRMd}	300	10,425	ns
CL[1] falling to M transition time	t_{Md}	– 10	20	ns
CL[2] rising to DD (display data) transition time	t_{DDd}	– 10	20	ns

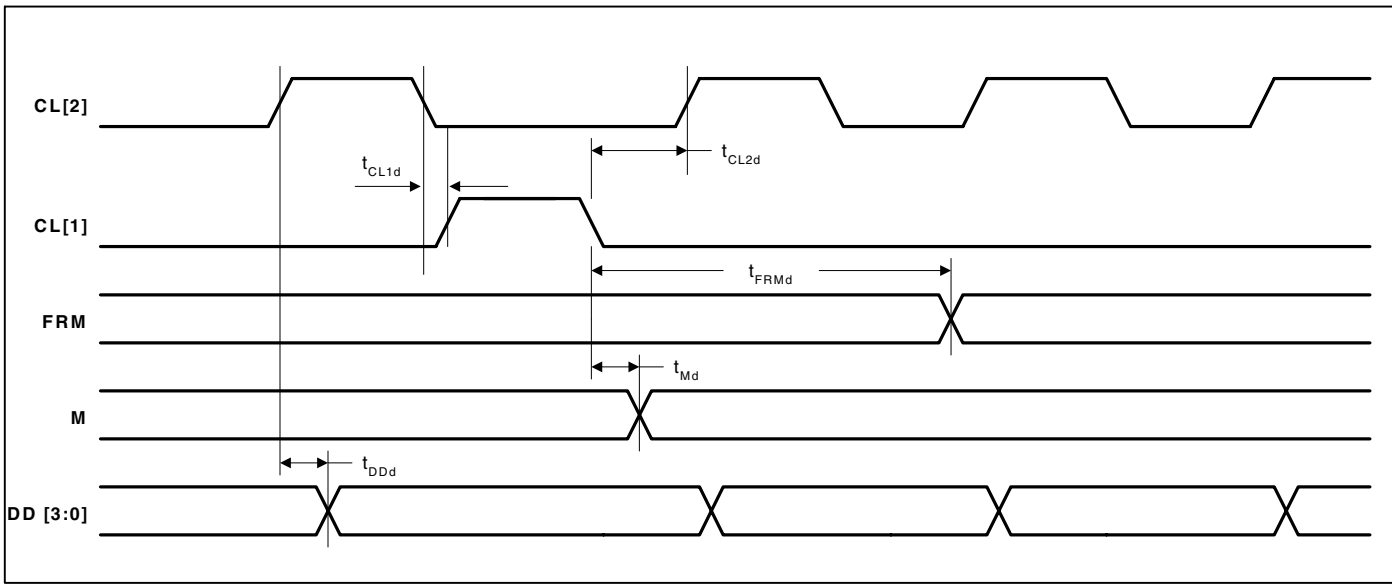

Figure 13. LCD Controller Timing Measurement

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JTAG Interface

Parameter	Symbol	Min	Max	Units
TCK clock period	t_{clk_per}	2	-	ns
TCK clock high time	t_{clk_high}	1	-	ns
TCK clock low time	t_{clk_low}	1	-	ns
JTAG port setup time	t_{JPs}	-	0	ns
JTAG port hold time	t_{JPh}	-	3	ns
JTAG port clock to output	t_{JPco}	-	10	ns
JTAG port high impedance to valid output	t_{JPzx}	-	12	ns
JTAG port valid output to high impedance	t_{JPxz}	-	19	ns

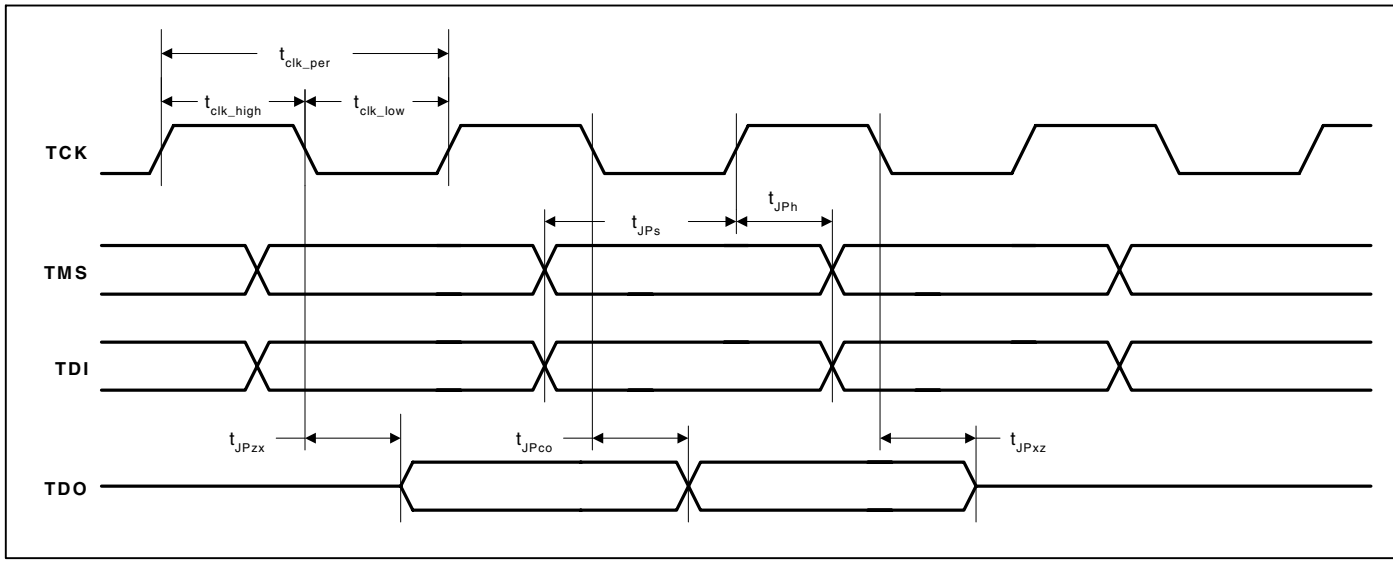

Figure 14. JTAG Timing Measurement

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Packages

208-Pin LQFP Package Characteristics

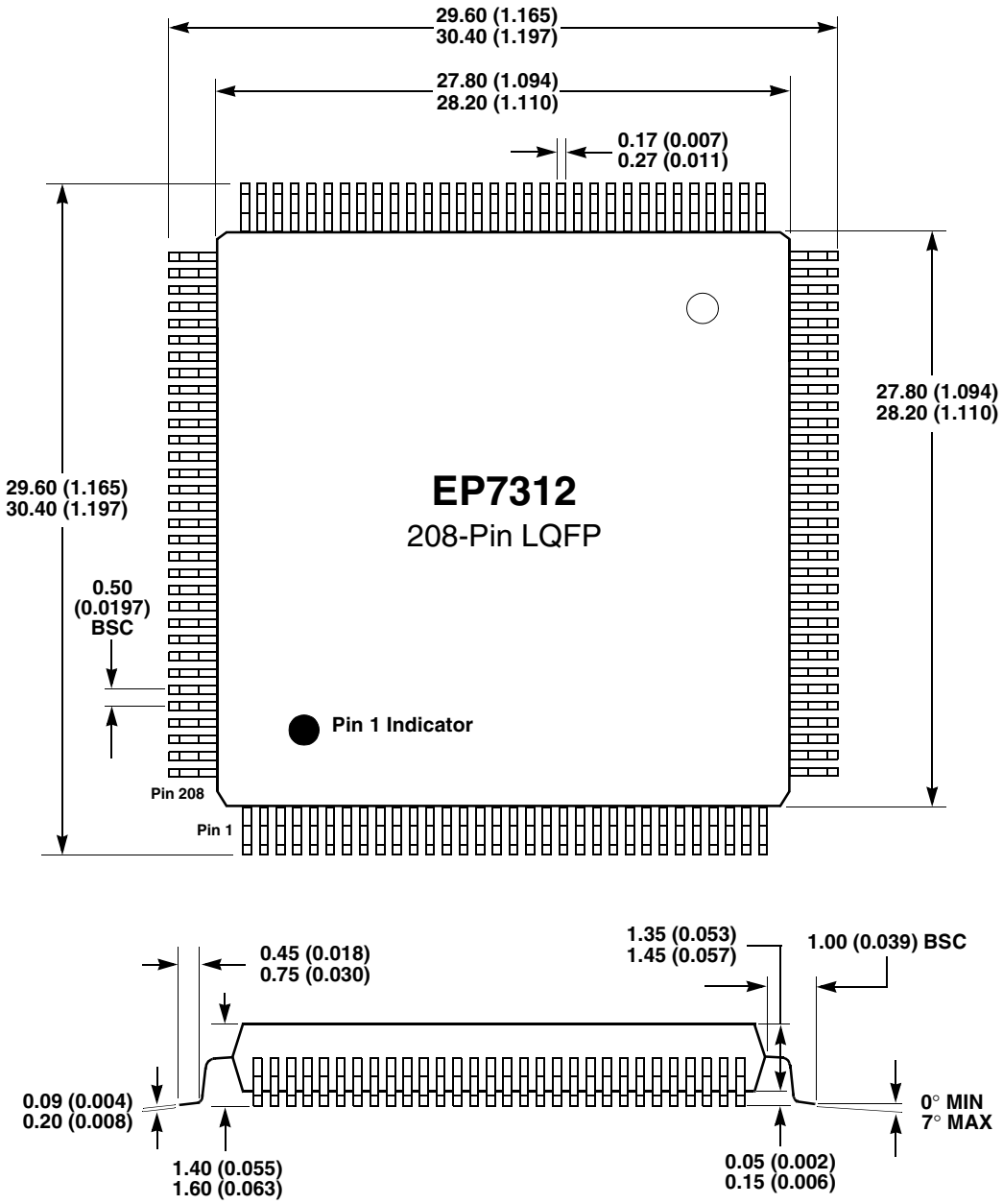

Figure 15. 208-Pin LQFP Package Outline Drawing

Note: 1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) For pin locations, please see Figure 16. For pin descriptions see the EP7312 User's Manual.

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208-Pin LQFP Pin Diagram

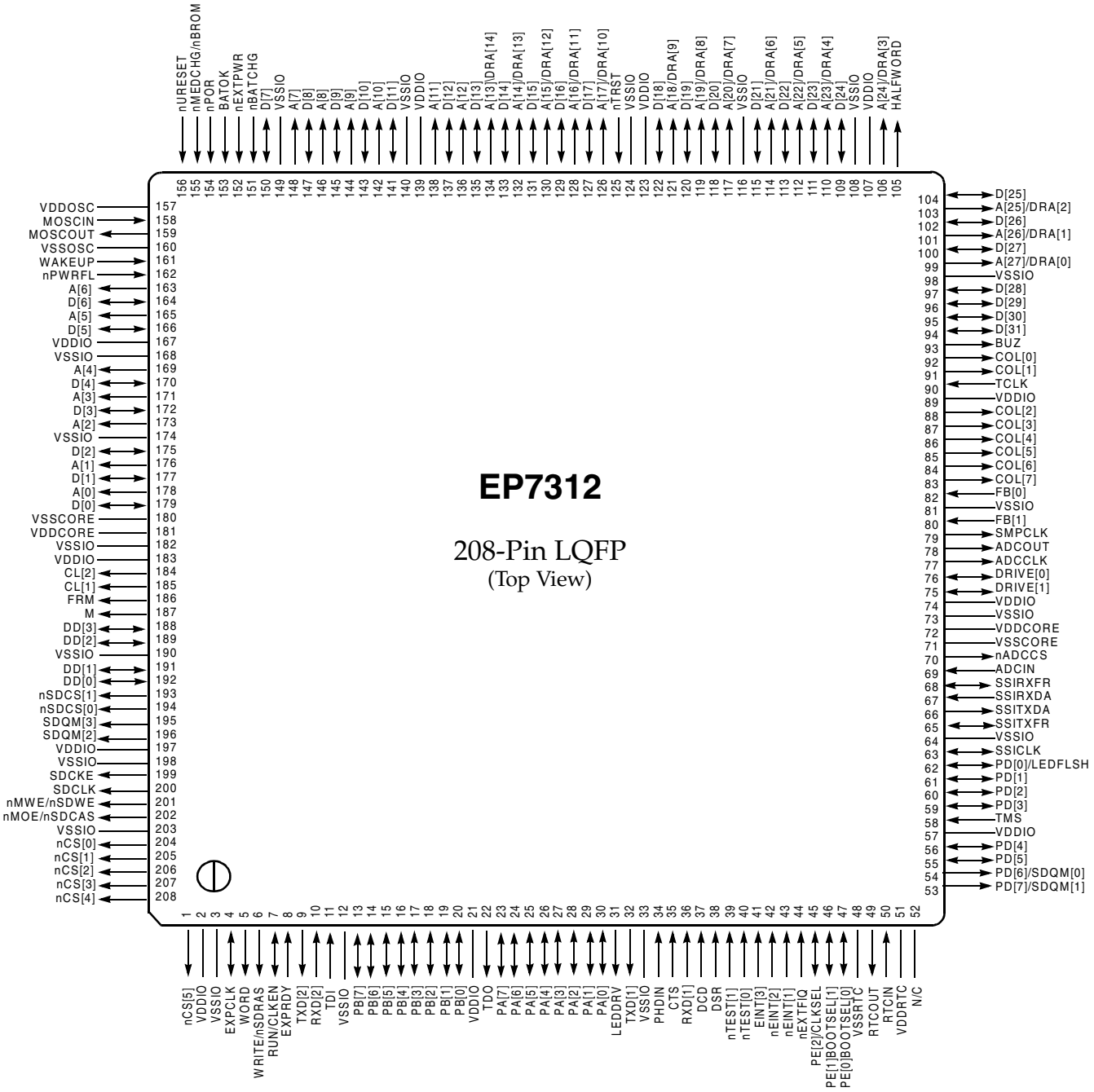

Figure 16. 208-Pin LQFP (Low Profile Quad Flat Pack) Pin Diagram

Note: 1. N/C should not be grounded but left as no connects.

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208-Pin LQFP Numeric Pin Listing

Table 20. 208-Pin LQFP Numeric Pin Listing

Pin No.	Signal	Strength†	Reset State	Type	Description
1	nCS[5]	1	Low	O	Chip select 5
2	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
3	VSSIO			Pad Gnd	I/O ground
4	EXPCLK	1		I	Expansion clock input
5	WORD	1	Low	O	Word access select output
6	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
7	RUN/CLKEN	1	Low	O	Run output / clock enable output
8	EXPRDY	1		I	Expansion port ready input
9	TXD[2]	1	High	O	UART 2 transmit data output
10	RXD[2]			I	UART 2 receive data input
11	TDI	with p/u*		I	JTAG data input
12	VSSIO			Pad Gnd	I/O ground
13	PB[7]	1	Input‡	I/O	GPIO port B
14	PB[6]	1	Input‡	I/O	GPIO port B
15	PB[5]	1	Input‡	I/O	GPIO port B
16	PB[4]	1	Input‡	I/O	GPIO port B
17	PB[3]	1	Input‡	I/O	GPIO port B
18	PB[2]	1	Input‡	I/O	GPIO port B
19	PB[1]	1	Input‡	I/O	GPIO port B
20	PB[0]	1	Input‡	I/O	GPIO port B
21	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
22	TDO	1	Input‡	O	JTAG data out
23	PA[7]	1	Input‡	I/O	GPIO port A
24	PA[6]	1	Input‡	I/O	GPIO port A
25	PA[5]	1	Input‡	I/O	GPIO port A
26	PA[4]	1	Input‡	I/O	GPIO port A
27	PA[3]	1	Input‡	I/O	GPIO port A
28	PA[2]	1	Input‡	I/O	GPIO port A
29	PA[1]	1	Input‡	I/O	GPIO port A
30	PA[0]	1	Input‡	I/O	GPIO port A
31	LEDDRV	1	Low	O	IR LED drive
32	TXD[1]	1	High	O	UART 1 transmit data out
33	VSSIO	1	High	Pad Gnd	I/O ground
34	PHDIN			I	Photodiode input
35	CTS			I	UART 1 clear to send input
36	RXD[1]			I	UART 1 receive data input
37	DCD			I	UART 1 data carrier detect

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Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
38	DSR			I	UART 1 data set ready input
39	nTEST[1]	With p/u*		I	Test mode select input
40	nTEST[0]	With p/u*		I	Test mode select input
41	EINT[3]			I	External interrupt
42	nEINT[2]			I	External interrupt input
43	nEINT[1]			I	External interrupt input
44	nEXTFIQ			I	External fast interrupt input
45	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
46	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
47	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / Boot mode select
48	VSSRTC			RTC Gnd	Real time clock ground
49	RTCOUT			O	Real time clock oscillator output
50	RTCIN			I	Real time clock oscillator input
51	VDDRTC			RTC power	Real time clock power, 2.5 V
52	N/C				
53	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
54	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
55	PD[5]	1	Low	I/O	GPIO port D
56	PD[4]	1	Low	I/O	GPIO port D
57	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
58	TMS	with p/u*		I	JTAG mode select
59	PD[3]	1	Low	I/O	GPIO port D
60	PD[2]	1	Low	I/O	GPIO port D
61	PD[1]	1	Low	I/O	GPIO port D
62	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
63	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
64	VSSIO			Pad Gnd	I/O ground
65	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 serial clock
66	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
67	SSIRXDA			I	DAI/CODEC/SSI2 serial data input
68	SSIRXFR		Input‡	I/O	DAI/CODEC/SSI2 frame sync
69	ADCIN			I	SSI1 ADC serial input
70	nADCCS	1	High	O	SSI1 ADC chip select
71	VSSCORE			Core ground	Core ground
72	VDDCORE			Core Pwr	Core power, 2.5 V
73	VSSIO			Pad Gnd	I/O ground
74	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
75	DRIVE[1]	2	High / Low	I/O	PWM drive output
76	DRIVE[0]	2	High / Low	I/O	PWM drive output
77	ADCCLK	1	Low	O	SSI1 ADC serial clock
78	ADCOUT	1	Low	O	SSI1 ADC serial data output

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Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
79	SMPCLK	1	Low	O	SSI1 ADC sample clock
80	FB[1]			I	PWM feedback input
81	VSSIO			Pad Gnd	I/O ground
82	FB[0]			I	PWM feedback input
83	COL[7]	1	High	O	Keyboard scanner column drive
84	COL[6]	1	High	O	Keyboard scanner column drive
85	COL[5]	1	High	O	Keyboard scanner column drive
86	COL[4]	1	High	O	Keyboard scanner column drive
87	COL[3]	1	High	O	Keyboard scanner column drive
88	COL[2]	1	High	O	Keyboard scanner column drive
89	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
90	TCLK			I	JTAG clock
91	COL[1]	1	High	O	Keyboard scanner column drive
92	COL[0]	1	High	O	Keyboard scanner column drive
93	BUZ	1	Low	O	Buzzer drive output
94	D[31]	1	Low	I/O	Data I/O
95	D[30]	1	Low	I/O	Data I/O
96	D[29]	1	Low	I/O	Data I/O
97	D[28]	1	Low	I/O	Data I/O
98	VSSIO			Pad Gnd	I/O ground
99	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
100	D[27]	1	Low	I/O	Data I/O
101	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
102	D[26]	1	Low	I/O	Data I/O
103	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address
104	D[25]	1	Low	I/O	Data I/O
105	HALFWORD	1	Low	O	Halfword access select output
106	A[24]/DRA[3]	1	Low	O	System byte address / SDRAM address
107	VDDIO		—	Pad Pwr	Digital I/O power, 3.3 V
108	VSSIO		—	Pad Gnd	I/O ground
109	D[24]	1	Low	I/O	Data I/O
110	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
111	D[23]	1	Low	I/O	Data I/O
112	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
113	D[22]	1	Low	I/O	Data I/O
114	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
115	D[21]	1	Low	I/O	Data I/O
116	VSSIO			Pad Gnd	I/O ground
117	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address

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Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
118	D[20]	1	Low	I/O	Data I/O
119	A[19]/DRA[8]	1	Low	O	System byte address / SDRAM address
120	D[19]	1	Low	I/O	Data I/O
121	A[18]/DRA[9]	1	Low	O	System byte address / SDRAM address
122	D[18]	1	Low	I/O	Data I/O
123	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
124	VSSIO			Pad Gnd	I/O ground
125	nTRST			I	JTAG async reset input
126	A[17]/DRA[10]	1	Low	O	System byte address / SDRAM address
127	D[17]	1	Low	I/O	Data I/O
128	A[16]/DRA[11]	1	Low	O	System byte address / SDRAM address
129	D[16]	1	Low	I/O	Data I/O
130	A[15]/DRA[12]	1	Low	O	System byte address / SDRAM address
131	D[15]	1	Low	I/O	Data I/O
132	A[14]/DRA[13]	1	Low	O	System byte address / SDRAM address
133	D[14]	1	Low	I/O	Data I/O
134	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
135	D[13]	1	Low	I/O	Data I/O
136	A[12]	1	Low	O	System byte address
137	D[12]	1	Low	I/O	Data I/O
138	A[11]	1	Low	O	System byte address
139	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
140	VSSIO			Pad Gnd	I/O ground
141	D[11]	1	Low	I/O	Data I/O
142	A[10]	1	Low	O	System byte address
143	D[10]	1	Low	I/O	Data I/O
144	A[9]	1	Low	O	System byte address
145	D[9]	1	Low	I/O	Data I/O
146	A[8]	1	Low	O	System byte address
147	D[8]	1	Low	I/O	Data I/O
148	A[7]	1	Low	O	System byte address
149	VSSIO			Pad Gnd	I/O ground
150	D[7]	1	Low	I/O	Data I/O
151	nBATCHG			I	Battery changed sense input
152	nEXTPWR			I	External power supply sense input
153	BATOK			I	Battery OK input
154	nPOR	Schmitt		I	Power-on reset input
155	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
156	nURESET	Schmitt		I	User reset input
157	VDDOSC			Oscillator Power	Oscillator power in, 2.5 V
158	MOSCIN			I	Main oscillator input
159	MOSCOUT			O	Main oscillator output
160	VSSOSC			Oscillator Ground	Oscillator Ground

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Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
161	WAKEUP	Schmitt		I	System wake up input
162	nPWRFL			I	Power fail sense input
163	A[6]	1	Low	O	System byte address
164	D[6]	1	Low	I/O	Data I/O
165	A[5]	1	Low	Out	System byte address
166	D[5]	1	Low	I/O	Data I/O
167	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
168	VSSIO			Pad Gnd	I/O ground
169	A[4]	1	Low	O	System byte address
170	D[4]	1	Low	I/O	Data I/O
171	A[3]	2	Low	O	System byte address
172	D[3]	1	Low	I/O	Data I/O
173	A[2]	2	Low	O	System byte address
174	VSSIO			Pad Gnd	I/O ground
175	D[2]	1	Low	I/O	Data I/O
176	A[1]	2	Low	O	System byte address
177	D[1]	1	Low	I/O	Data I/O
178	A[0]	2	Low	O	System byte address
179	D[0]	1	Low	I/O	Data I/O
180	VSSCORE			Core ground	Core ground
181	VDDCORE			Core Pwr	Core power, 2.5 V
182	VSSIO			Pad ground	I/O ground
183	VDDIO			Pad Power	Digital I/O power, 3.3 V
184	CL[2]	1	Low	O	LCD pixel clock out
185	CL[1]	1	Low	O	LCD line clock
186	FRM	1	Low	O	LCD frame synchronization pulse
187	M	1	Low	O	LCD AC bias drive
188	DD[3]	1	Low	I/O	LCD serial display data
189	DD[2]	1	Low	I/O	LCD serial display data
190	VSSIO			Pad Gnd	I/O ground
191	DD[1]	1	Low	I/O	LCD serial display data
192	DD[0]	1	Low	I/O	LCD serial display data
193	nSDCS[1]	1	High	O	SDRAM chip select 1
194	nSDCS[0]	1	High	O	SDRAM chip select 0
195	SDQM[3]	2	Low	I/O	SDRAM byte lane mask
196	SDQM[2]	2	Low	I/O	SDRAM byte lane mask
197	VDDIO			Pad Pwr	Digital I/O power, 3.3 V
198	VSSIO			Pad Gnd	I/O ground
199	SDCKE	2	Low	I/O	SDRAM clock enable output
200	SDCLK	2	Low	I/O	SDRAM clock out
201	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
202	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
203	VSSIO			Pad Gnd	I/O ground
204	nCS[0]	1	High	O	Chip select 0
205	nCS[1]	1	High	O	Chip select 1

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Table 20. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Strength†	Reset State	Type	Description
206	nCS[2]	1	High	O	Chip select 2
207	nCS[3]	1	High	O	Chip select 3
208	nCS[4]	1	High	O	Chip select 4

*"With p/u" means with internal pull-up of 100 KOhms on the pin.

† Strength 1 = 4 ma
Strength 2 = 12 ma

‡Input. Port A,B,D,E GPIOs default to input at nPOR and URESET conditions.

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204-Ball TFBGA Package Characteristics

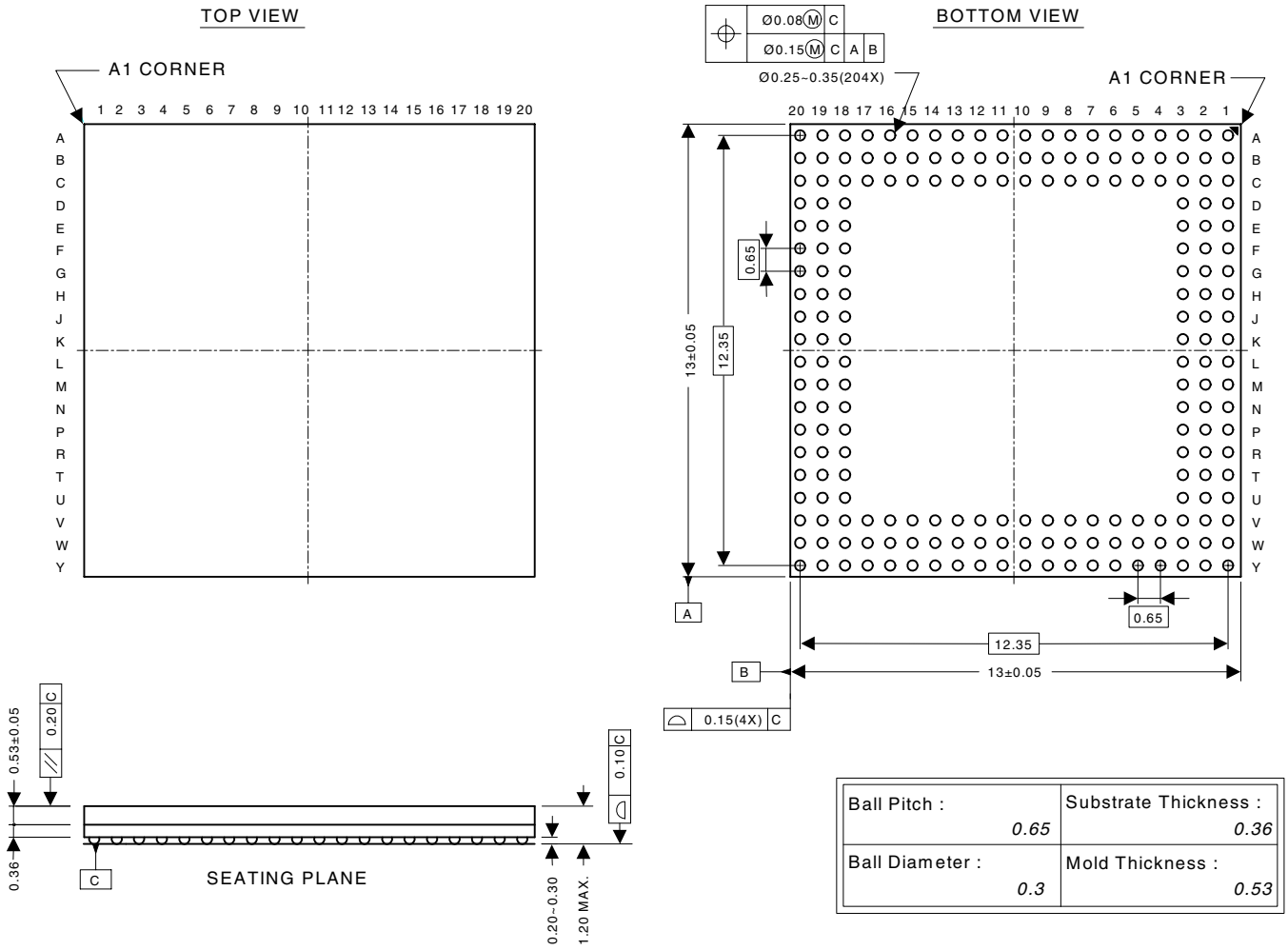

Figure 17. 204-Ball TFBGA Package

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204-Ball TFBGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VDDIO	EXPCLK	nCS[3]	nCS[1]	nMWE/ nSDWE	SDQM[2]	nSDCS[1]	DD[2]	FRM	CL[1]	GNDCORE	D[1]	A[2]	D[4]	A[5]	nPWRFL	MOSCOUT	GNDIO	GNDIO	GNDIO	A
B	WORD	VDDIO	nCS[5]	nCS[2]	nMOE/ nSDCAS	SDCKE	nSDCS[0]	DD[1]	M	CL[2]	D[0]	A[1]	D[3]	A[4]	D[6]	WAKEUP	MOSCIN	GNDIO	GNDIO	nURESET	B
C	RUN/ CLKEN	EXPRDY	VDDIO	nCS[4]	nCS[0]	SDCLK	SDQM[3]	DD[0]	DD[3]	VDDCORE	A[0]	D[2]	A[3]	D[5]	A[6]	GNDOSC	VDDOSC	GNDIO	BATOK	nPOR	C
D	PB[7]	RXD[2]	VDDIO															GNDIO	nBATCHG	A[7]	D
E	PB[4]	TXD[2]	WRITE/ nSDRAS															nMEDCHG/n BROM	nEXTPWR	D[9]	E
F	PB[3]	PB[6]	TDI															D[7]	A[8]	D[10]	F
G	PB[1]	PB[2]	PB[5]															D[8]	A[9]	D[11]	G
H	PA[7]	TDO	PB[0]															A[10]	D[12]	A[12]	H
J	PA[4]	PA[5]	PA[6]															A[11]	D[13]	A[13]/ DRA[14]	J
K	PA[1]	PA[2]	VDDIO															D[14]	A[14]/ DRA[13]	D[15]	K
L	TXD[1]	LEDDRV	PA[3]															VDDIO	D[16]	A[16]/ DRA[11]	L
M	RXD[1]	CTS	PA[0]															A[15]/ DRA[12]	A[17]/ DRA[10]	nTRST	M
N	DSR	nTEST[1]	PHDIN															D[17]	D[19]	A[18]/ DRA[9]	N
P	EINT[3]	nEINT[2]	DCD															D[18]	A[20]/ DRA[7]	D[20]	P
R	nEXTFIQ	PE2/ CLKSEL	nTEST[0]															A[19]/ DRA[8]	D[22]	A[21]/ DRA6	R
T	PE[1]/ BOOT SEL[1]	PE[0]/ BOOT SEL[0]	nEINT[1]															D[21]	D[23]	A[22]/ DRA5	T
U	GNDRTC	RTCOUT	RTCIN															HALF WORD	D[24]	A[23]/ DRA4	U
V	VDDRTC	GNDIO	GNDIO	PD[7]/ SDQM[1]	PD[4]	PD[2]	SSICLK	SSIRXDA	nADCCS	VDDIO	ADCCLK	COL[7]	COL[4]	TCLK	BUZ	D[29]	A[26]/ DRA[1]	VDDIO	VDDIO	A[24]/ DRA3	V
W	GNDIO	GNDIO	GNDIO	PD[6]/ SDQM[0]	TMS	PD[1]	SSITXFR	SSIRXFR	GNDCORE	DRIVE[1]	ADCOUT	FB[0]	COL[5]	COL[2]	COL[0]	D[30]	A[27]/ DRA[0]	D[26]	VDDIO	D[25]	W
Y	GNDIO	GNDIO	GNDIO	PD[5]	PD[3]	PD[0]/ LED FLSH	SSITXDA	ADCIN	VDDCORE	DRIVE[0]	SMPCLK	FB[1]	COL[6]	COL[3]	COL[1]	D[31]	D[28]	D[27]	A[25]/ DRA[2]	VDDIO	Y

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204-Ball TFBGA Ball Listing

The list is ordered by ball location.

Table 21. 204-Ball TFBGA Ball Listing

Ball Location	Name	Strength†	Reset State	Type	Description
A1	VDDIO			Pad power	Digital I/O power, 3.3 V
A2	EXPCLK	1		I	Expansion clock input
A3	nCS[3]	1	High	O	Chip select 3
A4	nCS[1]	1	High	O	Chip select 1
A5	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
A6	SDQM[2]	2	Low	O	SDRAM byte lane mask
A7	nSDCS[1]	1	High	O	SDRAM chip select 2
A8	DD[2]	1	Low	O	LCD serial display data
A9	FRM	1	Low	O	LCD frame synchronization pulse
A10	CL[1]	1	Low	O	LCD line clock
A11	VSSCORE			Core ground	Core ground
A12	D[1]	1	Low	I/O	Data I/O
A13	A[2]	2	Low	O	System byte address
A14	D[4]	1	Low	I/O	Data I/O
A15	A[5]	1	Low	O	System byte address
A16	nPWRFL			I	Power fail sense input
A17	MOSCOUT			O	Main oscillator out
A18	VSSIO			Pad ground	I/O ground
A19	VSSIO			Pad ground	I/O ground
A20	VSSIO			Pad ground	I/O ground
B1	WORD	1	Low	O	Word access select output
B2	VDDIO			Pad power	Digital I/O power, 3.3 V
B3	nCS[5]	1	Low	O	Chip select 5
B4	nCS[2]	1	High	O	Chip select 2
B5	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
B6	SDCKE	2	Low	O	SDRAM clock enable output
B7	nSDCS[0]	1	High	O	SDRAM chip select 0

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Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
B8	DD[1]	1	Low	O	LCD serial display data
B9	M	1	Low	O	LCD AC bias drive
B10	CL[2]	1	Low	0	LCD pixel clock out
B11	D[0]	1	Low	I/O	Data I/O
B12	A[1]	2	Low	O	System byte address
B13	D[3]	2	Low	I/O	Data I/O
B14	A[4]	1	Low	O	System byte address
B15	D[6]	1	Low	I/O	Data I/O
B16	WAKEUP	Schmitt		I	System wake up input
B17	MOSCIN			I	Main oscillator input
B18	VSSIO			Pad ground	I/O ground
B19	VSSIO			Pad ground	I/O ground
B20	nURESET	Schmitt		I	User reset input
C1	RUN/CLKEN	1	Low	0	Run output / clock enable output
C2	EXPRDY	1		I	Expansion port ready input
C3	VDDIO			Pad power	Digital I/O power, 3.3 V
C4	nCS[4]	1	High	O	Chip select 4
C5	nCS[0]	1	High	O	Chip select 0
C6	SDCLK	2	Low	O	SDRAM clock out
C7	SDQM[3]	2	Low	O	SDRAM byte lane mask
C8	DD[0]	1	Low	O	LCD serial display data
C9	DD[3]	1	Low	O	LCD serial display data
C10	VDDCORE			Core power	Digital core power, 2.5 V
C11	A[0]	2	Low	O	System byte address
C12	D[2]	1	Low	I/O	Data I/O
C13	A[3]	2	Low	O	System byte address
C14	D[5]	1	Low	I/O	Data I/O
C15	A[6]	1	Low	O	System byte address
C16	VSSOSC			Oscillator ground	PLL ground
C17	VDDOSC			Oscillator power	Oscillator power in, 2.5V
C18	VSSIO			Pad ground	I/O ground
C19	BATOK			I	Battery ok input

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Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C20	nPOR	Schmitt		I	Power-on reset input
D1	PB[7]	1	Input‡	I	GPIO port B
D2	RXD[2]			I	UART 2 receive data input
D3	VDDIO			Pad power	Digital I/O power, 3.3V
D18	VSSIO			Pad ground	I/O ground
D19	nBATCHG			I	Battery changed sense input
D20	A[7]	1	Low	O	System byte address
E1	PB[4]	1	Input‡	I	GPIO port B
E2	TXD[2]	1	High	O	UART 2 transmit data output
E3	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
E18	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E19	nEXTPWR			I	External power supply sense input
E20	D[9]	1	Low	I/O	Data I/O
F1	PB[3]	1	Input‡	I/O	GPIO port B
F2	PB[6]	1	Input‡	I/O	GPIO port B
F3	TDI	with p/u*		I	JTAG data input
F18	D[7]	1	Low	I/O	Data I/O
F19	A[8]	1	Low	O	System byte address
F20	D[10]	1	Low	I/O	Data I/O
G1	PB[1]	1	Input‡	I/O	
G2	PB[2]	1	Input‡	I/O	GPIO port B
G3	PB[5]	1	Input‡	I/O	GPIO port B
G18	D[8]	1	Input‡	I/O	Data I/O
G19	A[9]	1	Low	O	System byte address
G20	D[11]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H[2]	TDO	1	Input‡	O	JTAG data out
H[3]	PB[0]	1	Input‡	I/O	GPIO port B
H[18]	A[10]	1	Low	O	System byte address

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Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
H19	D[12]	1	Low	I/O	Data I/O
H20	A[12]	1	Low	O	System byte address
J1	PA[4]	1	Input‡	I/O	GPIO port A
J2	PA[5]	1	Input‡	I/O	GPIO port A
J3	PA[6]	1	Input‡	I/O	GPIO port A
J18	A[11]	1	Low	O	System byte address
J19	D[13]	1	Low	I/O	Data I/O
J20	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
K1	PA[1]	1	Input‡	I/O	GPIO port A
K2	PA[2]	1	Input‡	I/O	GPIO port A
K3	VDDIO			Pad power	Digital I/O power, 3.3V
K18	D[14]	1	Low	I/O	Data I/O
K19	A[14]/DRA[13]	1	Low	O	System byte address / SDRAM address
K20	D[15]	1	Low	I/O	Data I/O
L1	TXD[1]	1	High	O	UART 1 transmit data out
L2	LEDDRV	1	Low	O	IR LED drive
L3	PA[3]	1	Input‡	I/O	GPIO port A
L18	VDDIO			Pad power	Digital I/O power, 3.3V
L19	D[16]	1	Low	I/O	Data I/O
L20	A[16]/DRA[11]	1	Low	O	System byte address / SDRAM address
M1	RXD[1]			I	UART 1 receive data input
M2	CTS			I	UART 1 clear to send input
M3	PA[0]	1	Input‡	I/O	GPIO port A
M18	A[15]/DRA[12]	1	Low	O	System byte address / SDRAM address
M19	A[17]/DRA[10]	1	Low	O	System byte address / SDRAM address
M20	nTRST			I	JTAG async reset input
N1	DSR			I	UART 1 data set ready input
N2	nTEST[1]	With p/u*		I	Test mode select input
N3	PHDIN			I	Photodiode input

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Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
N18	D[17]	1	Low	I/O	Data I/O
N19	D[19]	1	Low	I/O	Data I/O
N20	A[18]/DRA[9]	1	Low	O	System byte address / SDRAM address
P1	EINT[3]			I	External interrupt
P2	nEINT[2]			I	External interrupt input
P3	DCD			I	UART 1 data carrier detect
P18	D[18]	1	Low	I/O	Data I/O
P19	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
P20	D[20]	1	Low	I/O	Data I/O
R1	nEXTFIQ			I	External fast interrupt input
R2	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
R3	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
R18	A[19]/DRA[8]	1	Low	O	System byte address / SDRAM address
R19	D[22]	1	Low	I/O	Data I/O
R20	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
T1	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
T2	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / boot mode select
T3	nEINT[1]			I	External interrupt input
T18	D[21]	1	Low	I/O	Data I/O
T19	D[23]	1	Low	I/O	Data I/O
T20	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
U1	VSSRTC			RTC ground	Real time clock ground
U2	RTCOUT			O	Real time clock oscillator output
U3	RTCIN			I/O	Real time clock oscillator input
U18	HALFWORD	1	Low	O	Halfword access select output
U19	D[24]	1	Low	I/O	Data I/O
U20	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
V1	VDDRTC			RTC power	Real time clock power, 2.5V

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Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
V2	VSSIO			Pad ground	I/O ground
V3	VSSIO			Pad ground	I/O ground
V4	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
V5	PD[4]	1	Low	I/O	GPIO port D
V6	PD[2]	1	Low	I/O	GPIO port D
V7	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
V8	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
V9	nADCCS	1	High	O	SSI1 ADC chip select
V10	VDDIO			Pad power	Digital I/O power, 3.3V
V11	ADCCLK	1	Low	O	SSI1 ADC serial clock
V12	COL[7]	1	High	O	Keyboard scanner column drive
V13	COL[4]	1	High	O	Keyboard scanner column drive
V14	TCLK			I	JTAG clock
V15	BUZ	1	Low	O	Buzzer drive output
V16	D[29]	1	Low	I/O	Data I/O
V17	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
V18	VDDIO			Pad power	Digital I/O power, 3.3 V
V19	VDDIO			Pad power	Digital I/O power, 3.3 V
V20	A[24]/DRA[3]	‘	Low	O	System byte address / SDRAM address
W1	VSSIO			Pad ground	I/O ground
W2	VSSIO			Pad ground	I/O ground
W3	VSSIO			Pad ground	I/O ground
W4	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
W5	TMS	with p/u*		I	JTAG mode select
W6	PD[1]	1	Low	I/O	GPIO port D
W7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
W8	SSIRXFR	1	Input‡	I/O	DAI/CODEC/SSI2 frame sync
W9	VSSCORE			Core Ground	Core Ground
W10	DRIVE[1]	2	High / Low	I/O	PWM drive output

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Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
W11	ADCOUT	1	Low	O	SSI1 ADC serial data output
W12	FB[0]			I	PWM feedback input
W13	COL[5]	1	High	O	Keyboard scanner column drive
W14	COL[2]	1	High	O	Keyboard scanner column drive
W15	COL[0]	1	High	O	Keyboard scanner column drive
W16	D[30]	1	Low	I/O	Data I/O
W17	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
W18	D[26]	1	Low	I/O	Data I/O
W19	VDDIO			Pad power	Digital I/O power, 3.3V
W20	D[25]	1	Low	I/O	Data I/O
Y1	VSSIO			Pad ground	I/O ground
Y2	VSSIO			Pad ground	I/O ground
Y3	VSSIO			Pad ground	I/O ground
Y4	PD[5]	1	Low	I/O	GPIO port D
Y5	PD[3]	1	Low	I/O	GPIO port D
Y6	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
Y7	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
Y8	ADCIN			I	SSI1 ADC serial input
Y9	VDDCORE			Core power	Digital core power, 2.5V
Y10	DRIVE[0]	2	Input‡	I/O	PWM drive output
Y11	SMPCLK	1	Low	O	SSI1 ADC sample clock
Y12	FB[1]			I	PWM feedback input
Y13	COL[6]	1	High	O	Keyboard scanner column drive
Y14	COL[3]	1	High	O	Keyboard scanner column drive
Y15	COL[1]	1	High	O	Keyboard scanner column drive
Y16	D[31]	1	Low	I/O	Data I/O
Y17	D[28]	1	Low	I/O	Data I/O
Y18	D[27]	1	Low	I/O	Data I/O
Y19	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address

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Table 21. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
Y20	VDDIO			Pad power	Digital I/O power, 3.3V

*"With p/u" means with internal pull-up of 100 KOhms on the pin.

† Strength 1 = 4 ma
Strength 2 = 12 ma

‡Input. Port A,B,D,E GPIOs default to input at nPOR and URESET conditions.

256-Ball PBGA Package Characteristics

Figure 18. 256-Ball PBGA Package

Note: 1) For pin locations see Table 22.
2) Dimensions are in millimeters (inches), and controlling dimension is millimeter
3) Before beginning any new EP7312 design, contact Cirrus Logic for the latest package information.

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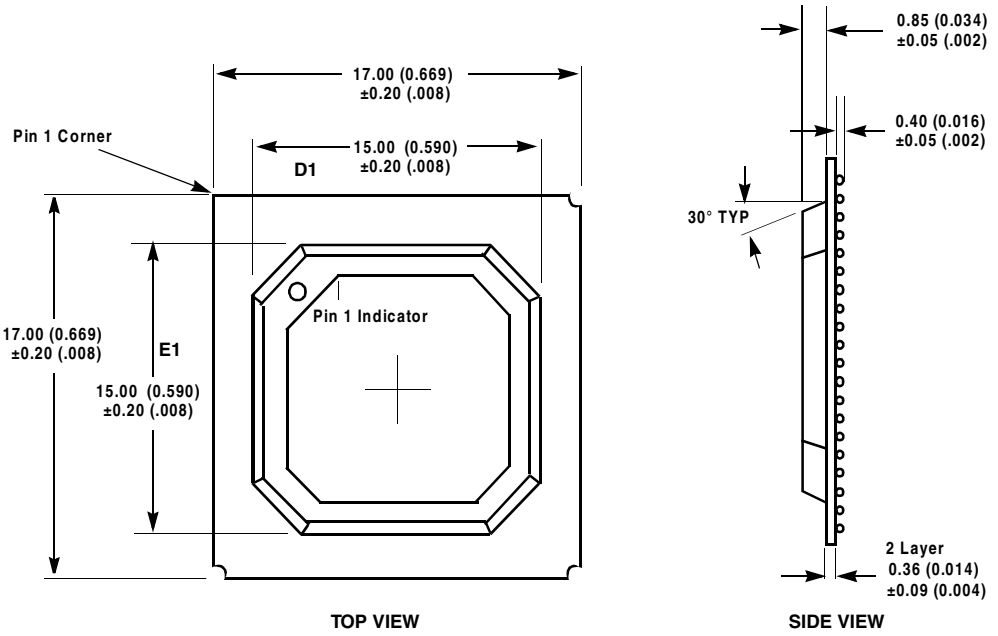

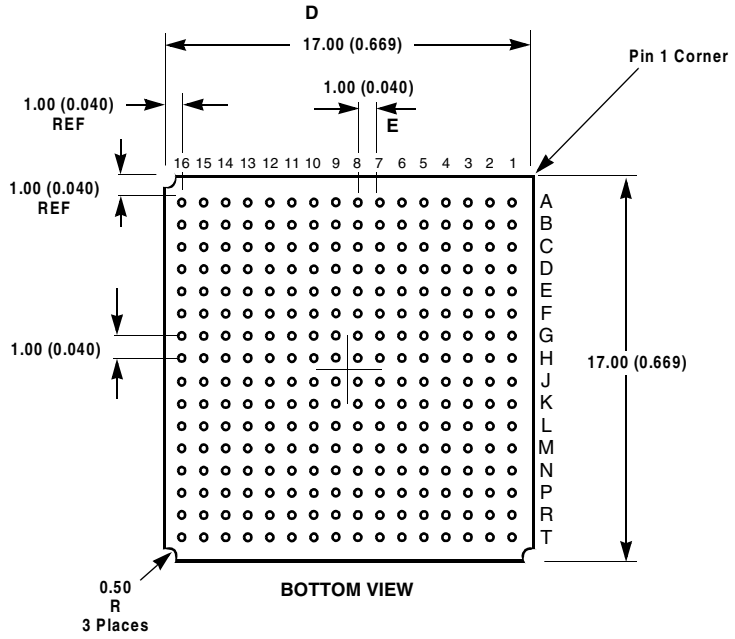

JEDEC #: MO-151
Ball Diameter: 0.50 mm ± 0.10 mm
17 ¥ 17 ¥ 1.61 mm body

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256-Ball PBGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VDDIO	nCS[4]	nCS[1]	SDCLK	SDQM[3]	DD[1]	M	VDDIO	D[0]	D[2]	A[3]	VDDIO	A[6]	MOSCOUT	VDDOSC	VSSIO	A
B	nCS[5]	VDDIO	nCS[3]	nMOE/ nSDCAS	VDDIO	nSDCS[1]	DD[2]	CL[1]	VDDCORE	D[1]	A[2]	A[4]	A[5]	WAKEUP	VDDIO	nURESET	B
C	VDDIO	EXPCLK	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	nPOR	nEXTPWR	C
D	WRITE/ nSDRAS	EXPRDY	VSSIO	VDDIO	nCS[2]	nMWE/ nSDWE	nSDCS[0]	CL[2]	VSSRTC	D[4]	nPWRFL	MOSCIN	VDDIO	VSSIO	D[7]	D[8]	D
E	RXD[2]	PB[7]	TDI	WORD	VSSIO	nCS[0]	SDQM[2]	FRM	A[0]	D[5]	VSSOSC	VSSIO	nMEDCHG/ nBROM	VDDIO	D[9]	D[10]	E
F	PB[5]	PB[3]	VSSIO	TXD[2]	RUN/ CLKEN	VSSIO	SDCKE	DD[3]	A[1]	D[6]	VSSRTC	BATOK	nBATCHG	VSSIO	D[11]	VDDIO	F
G	PB[1]	VDDIO	TDO	PB[4]	PB[6]	VSSCore	VSSRTC	DD[0]	D[3]	VSSRTC	A[7]	A[8]	A[9]	VSSIO	D[12]	D[13]	G
H	PA[7]	PA[5]	VSSIO	PA[4]	PA[6]	PB[0]	PB[2]	VSSRTC	VSSRTC	A[10]	A[11]	A[12]	A[13]/ DRA[14]	VSSIO	D[14]	D[15]	H
J	PA[3]	PA[1]	VSSIO	PA[2]	PA[0]	TXD[1]	CTS	VSSRTC	VSSRTC	A[17]/ DRA[10]	A[16]/ DRA[11]	A[15]/ DRA[12]	A[14]/ DRA[13]	nTRST	D[16]	D[17]	J
K	LEDDRV	PHDIN	VSSIO	DCD	nTEST[1]	EINT[3]	VSSRTC	ADCIN	COL[4]	TCLK	D[20]	D[19]	D[18]	VSSIO	VDDIO	VDDIO	K
L	RXD[1]	DSR	VDDIO	nEINT[1]	PE[2]/ CLKSEL	VSSRTC	PD[0]/ LEDFLSH	VSSRTC	COL[6]	D[31]	VSSRTC	A[22]/ DRA[5]	A[21]/ DRA[6]	VSSIO	A[18]/ DRA[9]	A[19]/ DRA[8]	L
M	nTEST[0]	nEINT[2]	VDDIO	PE[0]/ BOOTSEL[0]	TMS	VDDIO	SSITXFR	DRIVE[1]	FB[0]	COL[0]	D[27]	VSSIO	A[23]/ DRA[4]	VDDIO	A[20]/ DRA[7]	D[21]	M
N	nEXTFIQ	PE[1]/ BOOTSEL[1]	VSSIO	VDDIO	PD[5]	PD[2]	SSIRXDA	ADCCLK	SMPCLK	COL[2]	D[29]	D[26]	HALFWORD	VSSIO	D[22]	D[23]	N
P	VSSRTC	RTCOUT	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	D[24]	VDDIO	P
R	RTCIN	VDDIO	PD[4]	PD[1]	SSITXDA	nADCCS	VDDIO	ADCOUT	COL[7]	COL[3]	COL[1]	D[30]	A[27]/ DRA[0]	A[25]/ DRA[2]	VDDIO	A[24]\ DRA[3]	R
T	VDDRTC	PD[7]/ SDQM[1]	PD[6]/ SDQM[0]	PD[3]	SSICLK	SSIRXFR	VDDCORE	DRIVE[0]	FB[1]	COL[5]	VDDIO	BUZ	D[28]	A[26]/ DRA[1]	D[25]	VSSIO	T

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256-Ball PBGA Ball Listing

The list is ordered by ball location.

Table 22. 256-Ball PBGA Ball Listing

Ball Location	Name	Strength†	Reset State	Type	Description
A1	VDDIO			Pad power	Digital I/O power, 3.3 V
A2	nCS[4]	1	High	O	Chip select 4
A3	nCS[1]	1	High	O	Chip select 1
A4	SDCLK	2	Low	O	SDRAM clock out
A5	SDQM[3]	2	Low	O	SDRAM byte lane mask
A6	DD[1]	1	Low	O	LCD serial display data
A7	M	1	Low	O	LCD AC bias drive
A8	VDDIO			Pad power	Digital I/O power, 3.3 V
A9	D[0]	1	Low	I/O	Data I/O
A10	D[2]	1	Low	I/O	Data I/O
A11	A[3]	2	Low	O	System byte address
A12	VDDIO			Pad power	Digital I/O power, 3.3V
A13	A[6]	1	Low	O	System byte address
A14	MOSCOUT			O	Main oscillator out
A15	VDDOSC			Oscillator power	Oscillator power in, 2.5 V
A16	VSSIO			Pad ground	I/O ground
B1	nCS[5]	1	Low	O	Chip select 5
B2	VDDIO			Pad power	Digital I/O power, 3.3 V
B3	nCS[3]	1	High	O	Chip select 3
B4	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
B5	VDDIO			Pad power	Digital I/O power, 3.3 V
B6	nSDCS[1]	1	High	O	SDRAM chip select 1
B7	DD[2]	1	Low	O	LCD serial display data
B8	CL[1]	1	Low	O	LCD line clock
B9	VDDCORE			Core power	Digital core power, 2.5V
B10	D[1]	1	Low	I/O	Data I/O
B11	A[2]	2	Low	O	System byte address
B12	A[4]	1	Low	O	System byte address
B13	A[5]	1	Low	O	System byte address
B14	WAKEUP	Schmitt		I	System wake up input
B15	VDDIO			Pad power	Digital I/O power, 3.3 V
B16	nURESET	Schmitt		I	User reset input
C1	VDDIO			Pad power	Digital I/O power, 3.3V
C2	EXPCLK	1		I	Expansion clock input
C3	VSSIO			Pad ground	I/O ground
C4	VDDIO			Pad power	Digital I/O power, 3.3 V
C5	VSSIO			Pad ground	I/O ground
C6	VSSIO			Pad ground	I/O ground
C7	VSSIO			Pad ground	I/O ground
C8	VDDIO			Pad power	Digital I/O power, 3.3 V
C9	VSSIO			Pad ground	I/O ground
C10	VSSIO			Pad ground	I/O ground
C11	VSSIO			Pad ground	I/O ground
C12	VDDIO			Pad power	Digital I/O power, 3.3 V

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Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C13	VSSIO			Pad ground	I/O ground
C14	VSSIO			Pad ground	I/O ground
C15	nPOR	Schmitt		I	Power-on reset input
C16	nEXTPWR			I	External power supply sense input
D1	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
D2	EXPRDY	1		I	Expansion port ready input
D3	VSSIO			Pad ground	I/O ground
D4	VDDIO			Pad power	Digital I/O power, 3.3V
D5	nCS[2]	1	High	O	Chip select 2
D6	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
D7	nSDCS[0]	1	High	O	SDRAM chip select 2
D8	CL[2]	1	Low	O	LCD pixel clock out
D9	VSSRTC			Core ground	Real time clock ground
D10	D[4]	1	Low	I/O	Data I/O
D11	nPWRFL			I	Power fail sense input
D12	MOSCIN			I	Main oscillator input
D13	VDDIO			Pad power	Digital I/O power, 3.3V
D14	VSSIO			Pad ground	I/O ground
D15	D[7]	1	Low	I/O	Data I/O
D16	D[8]	1	Low	I/O	Data I/O
E1	RXD[2]			I	UART 2 receive data input
E2	PB[7]	1	Input‡	I	GPIO port B
E3	TDI	with p/u*		I	JTAG data input
E4	WORD	1	Low	O	Word access select output
E5	VSSIO			Pad ground	I/O ground
E6	nCS[0]	1	High	O	Chip select 0
E7	SDQM[2]	2	Low	O	SDRAM byte lane mask
E8	FRM	1	Low	O	LCD frame synchronization pulse
E9	A[0]	2	Low	O	System byte address
E10	D[5]	1	Low	I/O	Data I/O
E11	VSSOSC			Oscillator ground	PLL ground
E12	VSSIO			Pad ground	I/O ground
E13	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E14	VDDIO			Pad power	Digital I/O power, 3.3V
E15	D[9]	1	Low	I/O	Data I/O
E16	D[10]	1	Low	I/O	Data I/O
F1	PB[5]	1	Input‡	I	GPIO port B
F2	PB[3]	1	Input‡	I	GPIO port B
F3	VSSIO			Pad ground	I/O ground
F4	TXD[2]	1	High	O	UART 2 transmit data output
F5	RUN/CLKEN	1	Low	O	Run output / clock enable output
F6	VSSIO			Pad ground	I/O ground
F7	SDCKE	2	Low	O	SDRAM clock enable output
F8	DD[3]	1	Low	O	LCD serial display data
F9	A[1]	2	Low	O	System byte address

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Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
F10	D[6]	1	Low	I/O	Data I/O
F11	VSSRTC			RTC ground	Real time clock ground
F12	BATOK			I	Battery OK input
F13	nBATCHG			I	Battery changed sense input
F14	VSSIO			Pad ground	I/O ground
F15	D[11]	1	Low	I/O	Data I/O
F16	VDDIO			Pad power	Digital I/O power, 3.3V
G1	PB[1]	1	Input‡	I	GPIO port B
G2	VDDIO			Pad power	Digital I/O power, 3.3V
G3	TDO	1	Input‡	O	JTAG data out
G4	PB[4]	1	Input‡	I	GPIO port B
G5	PB[6]	1	Input‡	I	GPIO port B
G6	VSSCore			Core ground	Core ground
G7	VSSRTC			RTC ground	Real time clock ground
G8	DD[0]	1	Low	O	LCD serial display data
G9	D[3]	1	Low	I/O	Data I/O
G10	VSSRTC			RTC ground	Real time clock ground
G11	A[7]	1	Low	O	System byte address
G12	A[8]	1	Low	O	System byte address
G13	A[9]	1	Low	O	System byte address
G14	VSSIO			Pad ground	I/O ground
G15	D[12]	1	Low	I/O	Data I/O
G16	D[13]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H2	PA[5]	1	Input‡	I/O	GPIO port A
H3	VSSIO			Pad ground	I/O ground
H4	PA[4]	1	Input‡	I/O	GPIO port A
H5	PA[6]	1	Input‡	I/O	GPIO port A
H6	PB[0]	1	Input‡	I/O	GPIO port B
H7	PB[2]	1	Input‡	I/O	GPIO port B
H8	VSSRTC			RTC ground	Real time clock ground
H9	VSSRTC			RTC ground	Real time clock ground
H10	A[10]	1	Low	O	System byte address
H11	A[11]	1	Low	O	System byte address
H12	A[12]	1	Low	O	System byte address
H13	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
H14	VSSIO			Pad ground	I/O ground
H15	D[14]	1	Low	I/O	Data I/O
H16	D[15]	1	Low	I/O	Data I/O
J1	PA[3]	1	Input‡	I/O	GPIO port A
J2	PA[1]	1	Input‡	I/O	GPIO port A
J3	VSSIO			Pad ground	I/O ground
J4	PA[2]	1	Input‡	I/O	GPIO port A

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Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
J5	PA[0]	1	Input‡	I/O	GPIO port A
J6	TXD[1]	1	High	O	UART 1 transmit data out
J7	CTS			I	UART 1 clear to send input
J8	VSSRTC			RTC ground	Real time clock ground
J9	VSSRTC			RTC ground	Real time clock ground
J10	A[17]/DRA[10]	1	Low	O	System byte address / SDRAM address
J11	A[16]/DRA[11]	1	Low	O	System byte address / SDRAM address
J12	A[15]/DRA[12]	1	Low	O	System byte address / SDRAM address
J13	A[14]/DRA[13]	1	Low	O	System byte address / SDRAM address
J14	nTRST			I	JTAG async reset input
J15	D[16]	1	Low	I/O	Data I/O
J16	D[17]	1	Low	I/O	Data I/O
K1	LEDDRV	1	Low	O	IR LED drive
K2	PHDIN			I	Photodiode input
K3	VSSIO			Pad ground	I/O ground
K4	DCD			I	UART 1 data carrier detect
K5	nTEST[1]	With p/u*		I	Test mode select input
K6	EINT[3]			I	External interrupt
K7	VSSRTC			RTC ground	Real time clock ground
K8	ADCIN			I	SSI1 ADC serial input
K9	COL[4]	1	High	O	Keyboard scanner column drive
K10	TCLK			I	JTAG clock
K11	D[20]	1	Low	I/O	Data I/O
K12	D[19]	1	Low	I/O	Data I/O
K13	D[18]	1	Low	I/O	Data I/O
K14	VSSIO			Pad ground	I/O ground
K15	VDDIO			Pad power	Digital I/O power, 3.3V
K16	VDDIO			Pad power	Digital I/O power, 3.3V
L1	RXD[1]			I	UART 1 receive data input
L2	DSR			I	UART 1 data set ready input
L3	VDDIO			Pad power	Digital I/O power, 3.3V
L4	nEINT[1]			I	External interrupt input
L5	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
L6	VSSRTC			RTC ground	Real time clock ground
L7	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
L8	VSSRTC			Core ground	Real time clock ground
L9	COL[6]	1	High	O	Keyboard scanner column drive
L10	D[31]	1	Low	I/O	Data I/O
L11	VSSRTC			RTC ground	Real time clock ground
L12	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
L13	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
L14	VSSIO			Pad ground	I/O ground
L15	A[18]/DRA[9]	1	Low	O	System byte address / SDRAM address
L16	A[19]/DRA[8]	1	Low	O	System byte address / SDRAM address
M1	nTEST[0]	With p/u*		I	Test mode select input
M2	nEINT[2]			I	External interrupt input
M3	VDDIO			Pad power	Digital I/O power, 3.3V

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Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
M4	PE[0]/BOOTSEL[0]	1	Input‡	I	GPIO port E / Boot mode select
M5	TMS	with p/u*		I	JTAG mode select
M6	VDDIO			Pad power	Digital I/O power, 3.3V
M7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
M8	DRIVE[1]	2	High / Low	I/O	PWM drive output
M9	FB[0]			I	PWM feedback input
M10	COL[0]	1	High	O	Keyboard scanner column drive
M11	D[27]	1	Low	I/O	Data I/O
M12	VSSIO			Pad ground	I/O ground
M13	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
M14	VDDIO			Pad power	Digital I/O power, 3.3V
M15	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address
M16	D[21]	1	Low	I/O	Data I/O
N1	nEXTFIQ			I	External fast interrupt input
N2	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
N3	VSSIO			Pad ground	I/O ground
N4	VDDIO			Pad power	Digital I/O power, 3.3V
N5	PD[5]	1	Low	I/O	GPIO port D
N6	PD[2]	1	Low	I/O	GPIO port D
N7	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
N8	ADCCLK	1	Low	O	SSI1 ADC serial clock
N9	SMPCLK	1	Low	O	SSI1 ADC sample clock
N10	COL[2]	1	High	O	Keyboard scanner column drive
N11	D[29]	1	Low	I/O	Data I/O
N12	D[26]	1	Low	I/O	Data I/O
N13	HALFWORD	1	Low	O	Halfword access select output
N14	VSSIO			Pad ground	I/O ground
N15	D[22]	1	Low	I/O	Data I/O
N16	D[23]	1	Low	I/O	Data I/O
P1	VSSRTC			RTC ground	Real time clock ground
P2	RTCOUT			O	Real time clock oscillator output
P3	VSSIO			Pad ground	I/O ground
P4	VSSIO			Pad ground	I/O ground
P5	VDDIO			Pad power	Digital I/O power, 3.3V
P6	VSSIO			Pad ground	I/O ground
P7	VSSIO			Pad ground	I/O ground
P8	VDDIO			Pad power	Digital I/O power, 3.3V
P9	VSSIO			Pad ground	I/O ground
P10	VDDIO			Pad power	Digital I/O power, 3.3V
P11	VSSIO			Pad ground	I/O ground
P12	VSSIO			Pad ground	I/O ground
P13	VDDIO			Pad power	Digital I/O power
P14	VSSIO			Pad ground	I/O ground
P15	D[24]	1	Low	I/O	Data I/O
P16	VDDIO			Pad power	Digital I/O power, 3.3V
R1	RTCIN			I/O	Real time clock oscillator input
R2	VDDIO			Pad power	Digital I/O power, 3.3V

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Table 22. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
R3	PD[4]	1	Low	I/O	GPIO port D
R4	PD[1]	1	Low	I/O	GPIO port D
R5	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
R6	nADCCS	1	High	O	SSI1 ADC chip select
R7	VDDIO			Pad power	Digital I/O power, 3.3V
R8	ADCOUT	1	Low	O	SSI1 ADC serial data output
R9	COL[7]	1	High	O	Keyboard scanner column drive
R10	COL[3]	1	High	O	Keyboard scanner column drive
R11	COL[1]	1	High	O	Keyboard scanner column drive
R12	D[30]	1	Low	I/O	Data I/O
R13	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
R14	A[25]/DRA[2]	2	Low	O	System byte address / SDRAM address
R15	VDDIO			Pad power	Digital I/O power, 3.3V
R16	A[24]/DRA[3]	1	Low	O	System byte address / SDRAM address
T1	VDDRTC			RTC power	Real time clock power, 2.5V
T2	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
T3	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
T4	PD[3]	1	Low	I/O	GPIO port D
T5	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
T6	SSIRXFR	1	Input‡	I/O	DAI/CODEC/SSI2 frame sync
T7	VDDCORE			Core power	Core power, 2.5V
T8	DRIVE[0]	2	High / Low	I/O	PWM drive output
T9	FB[1]			I	PWM feedback input
T10	COL[5]	1	High	O	Keyboard scanner column drive
T11	VDDIO			Pad power	Digital I/O power, 3.3V
T12	BUZ	1	Low	O	Buzzer drive output
T13	D[28]	1	Low	I/O	Data I/O
T14	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
T15	D[25]	1	Low	I/O	Data I/O
T16	VSSIO			Pad ground	I/O ground

*"With p/u" means with internal pull-up of 100 KOhms on the pin.

† Strength 1 = 4 ma
Strength 2 = 12 ma

‡Input. Port A,B,D,E GPIOs default to input at nPOR and URESET conditions.

JTAG Boundary Scan Signal Ordering

Table 23. JTAG Boundary Scan Signal Ordering

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
1	B3	B1	nCS[5]	O	1
4	A2	C2	EXPCLK	I/O	3
5	B1	E4	WORD	O	6
6	E3	D1	WRITE/nSDRAS	O	8

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Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
7	C1	F5	RUN/CLKEN	O	10
8	C2	D2	EXPRDY	I	13
9	E2	F4	TXD2	O	14
10	D2	E1	RXD2	I	16
13	F3	E2	PB[7]	I/O	17
14	D1	G5	PB[6]	I/O	20
15	F2	F1	PB[5]	I/O	23
16	E1	G4	PB[4]	I/O	26
17	F1	F2	PB[3]	I/O	29
18	G2	H7	PB[2]	I/O	32
19	G1	G1	PB[1]	I/O	35
20	H3	H6	PB[0]	I/O	38
23	H1	H1	PA[7]	I/O	41
24	J3	H5	PA[6]	I/O	44
25	J2	H2	PA[5]	I/O	47
26	J1	H4	PA[4]	I/O	50
27	L3	J1	PA[3]	I/O	53
28	K2	J4	PA[2]	I/O	56
29	K1	J2	PA[1]	I/O	59
30	M3	J5	PA[0]	I/O	62
31	L2	K1	LEDDRV	O	65
32	L1	J6	TXD1	O	67
34	N3	K2	PHDIN	I	69
35	M2	J7	CTS	I	70
36	M1	L1	RXD1	I	71
37	P3	K4	DCD	I	72
38	N1	L2	DSR	I	73
39	N2	K5	nTEST1	I	74
40	R3	M1	nTEST0	I	75
41	P1	K6	EINT3	I	76
42	P2	M2	nEINT2	I	77
43	T3	L4	nEINT1	I	78
44	R1	N1	nEXTFIQ	I	79
45	R2	L5	PE[2]/CLKSEL	I/O	80
46	T1	N2	PE[1]/ BOOTSEL[1]	I/O	83
47	T2	M4	PE[0]/BOOTSEL0	I/O	86
53	V4	T2	PD[7]/SDQM[1]	I/O	89
54	W4	T3	PD[6/SDQM[0]]	I/O	92

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Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
55	Y4	N5	PD[5]	I/O	95
56	V5	R3	PD[4]	I/O	98
59	Y5	T4	PD[3]	I/O	101
60	V6	N6	PD[2]	I/O	104
61	W6	R4	PD[1]	I/O	107
62	Y6	L7	PD[0]/LEDFLSH	O	110
68	W8	T6	SSIRXFR	I/O	122
69	Y8	K8	ADCIN	I	125
70	V9	R6	nADCCS	O	126
75	W10	M8	DRIVE1	I/O	128
76	Y10	T8	DRIVE0	I/O	131
77	V11	N8	ADCCLK	O	134
78	W11	R8	ADCOUT	O	136
79	Y11	N9	SMPCLK	O	138
80	Y12	T9	FB1	I	140
82	Y11	M9	FB0	I	141
83	Y12	R9	COL7	O	142
84	Y13	L9	COL6	O	144
85	W13	T10	COL5	O	146
86	V13	K9	COL4	O	148
87	Y14	R10	COL3	O	150
88	W14	N10	COL2	O	152
91	Y15	R11	COL1	O	154
92	W15	M10	COL0	O	156
93	V15	T12	BUZ	O	158
94	Y16	L10	D[31]	I/O	160
95	W16	R12	D[30]	I/O	163
96	V16	N11	D[29]	I/O	166
97	Y17	T13	D[28]	I/O	169
99	Y16	R13	A[27]/DRA[0]	Out	172
100	Y18	M11	D[27]	I/O	174
101	V17	T14	A[26]/DRA[1]	O	177
102	W18	N12	D[26]	I/O	179
103	Y19	R14	A[25]/DRA[2]	O	182
104	Y20	T15	D[25]	I/O	184
105	U18	N13	HALFWORD	O	187
106	V209	R16	A[24]/DRA[3]	O	189
109	U19	P15	D[24]	I/O	191

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Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
110	U20	M13	A[23]/DRA[4]	O	194
111	T19	N16	D[23]	I/O	196
112	T20	L12	A[22]/DRA[5]	O	199
113	R19	N15	D[22]	I/O	201
114	R20	L13	A[21]/DRA[6]	O	204
115	T18	M16	D[21]	I/O	206
117	P19	M15	A[20]/DRA[7]	O	209
118	P20	K11	D[20]	I/O	211
119	R18	L16	A[19]/DRA[8]	O	214
120	N19	K12	D[19]	I/O	216
121	N20	L15	A[18]/DRA[9]	O	219
122	P18	K13	D[18]	I/O	221
126	M19	J10	A[17]/DRA[10]	O	224
127	N18	J16	D[17]	I/O	226
128	L20	J11	A[16]/DRA[11]	O	229
129	L19	J15	D[16]	I/O	231
130	M18	J12	A[15]/DRA[12]	O	234
131	K20	H16	D[15]	I/O	236
132	K19	J13	A[14]/DRA[13]	O	239
133	K18	H15	D[14]	I/O	241
134	J20	H13	A[13]/DRA[14]	O	244
135	J19	G16	D[13]	I/O	246
136	H20	H12	A[12]	O	249
137	H19	G15	D[12]	I/O	251
138	J18	H11	A[11]	O	254
141	G20	F15	D[11]	I/O	256
142	H18	H10	A[10]	O	259
143	F20	E16	D[10]	I/O	261
144	G19	G13	A[9]	O	264
145	E20	E15	D[9]	I/O	266
146	F19	G12	A[8]	O	269
147	G18	D16	D[8]	I/O	271
148	D20	G11	A[7]	O	274
150	F18	D15	D[7]	I/O	276
151	D19	F13	nBATCHG	I	279
152	E19	C16	nEXTPWR	I	280
153	C19	F12	BATOK	I	281
154	C20	C15	nPOR	I	282

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Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
155	E18	E13	nMEDCHG/nBROM	I	283
156	B20	B16	nURESET	I	284
161	B16	B14	WAKEUP	I	285
162	A16	D11	nPWRFL	I	286
163	C15	A13	A[6]	O	287
164	B15	F10	D[6]	I/O	289
165	A15	B13	A[5]	O	292
166	C14	E10	D[5]	I/O	294
169	B14	B12	A[4]	O	297
170	A14	D10	D[4]	I/O	299
171	C13	A11	A[3]	O	302
172	B13	G9	D[3]	I/O	304
173	A13	B11	A[2]	O	307
175	C12	A10	D[2]	I/O	309
176	B12	F9	A[1]	O	312
177	A12	B10	D[1]	I/O	314
178	C11	E9	A[0]	O	317
179	B11	A9	D[0]	I/O	319
184	B10	D8	CL2	O	322
185	A10	B8	CL1	O	324
186	A9	E8	FRM	O	326
187	B9	A7	M	O	328
188	C9	F8	DD[3]	O	330
189	A8	B7	DD[2]	O	333
191	B8	A6	DD[1]	O	336
192	C8	G8	DD[0]	O	339
193	A7	B6	nSDCS[1]	O	342
194	B7	D7	nSDCS[0]	O	344
195	C7	A5	SDQM[3]	I/O	346
196	A6	E7	SDQM[2]	I/O	349
199	B6	F7	SDCKE	I/O	352
200	C6	A4	SDCLK	I/O	355
201	A5	D6	nMWE/nSDWE	O	358
202	B5	B4	nMOE/nSDCAS	O	360
204	C5	E6	nCS[0]	O	362
205	A4	A3	nCS[1]	O	364

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Table 23. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
206	B4	D5	nCS[2]	O	366
207	A3	B3	nCS[3]	O	368
208	C4	A2	nCS[4]	O	370

1) See EP7312 Users' Manual for pin naming / functionality.

2) For each pad, the JTAG connection ordering is input, output, then enable as applicable.

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CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data sheet.

Acronyms and Abbreviations

Table 24 lists abbreviations and acronyms used in this data sheet.

Table 24. Acronyms and Abbreviations

Acronym/ Abbreviation	Definition
A/D	analog-to-digital
ADC	analog-to-digital converter
CODEC	coder / decoder
D/A	digital-to-analog
DMA	direct-memory access
EPB	embedded peripheral bus
FCS	frame check sequence
FIFO	first in / first out
FIQ	fast interrupt request
GPIO	general purpose I/O
ICT	in circuit test
IR	infrared
IRQ	standard interrupt request
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	liquid crystal display
LED	light-emitting diode
LQFP	low profile quad flat pack
LSB	least significant bit
MIPS	millions of instructions per second
MMU	memory management unit
MSB	most significant bit
PBGA	plastic ball grid array
PCB	printed circuit board
PDA	personal digital assistant
PLL	phase locked loop
p/u	pull-up resistor
RISC	reduced instruction set computer
RTC	Real-Time Clock
SIR	slow (9600–115.2 kbps) infrared
SRAM	static random access memory
SSI	synchronous serial interface

Table 24. Acronyms and Abbreviations (Continued)

Acronym/ Abbreviation	Definition
TAP	test access port
TLB	translation lookaside buffer
UART	universal asynchronous receiver

Units of Measurement

Table 25. Unit of Measurement

Symbol	Unit of Measure
°C	degree Celsius
fs	sample frequency
Hz	hertz (cycle per second)
kbps	kilobits per second
KB	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilo Ohm
Mbps	megabits (1,048,576 bits) per second
MB	megabyte (1,048,576 bytes)
MBps	megabytes per second
MHz	megahertz (1,000 kilohertz)
µA	microampere
µF	microfarad
µW	microwatt
µs	microsecond (1,000 nanoseconds)
mA	milliampere
mW	milliwatt
ms	millisecond (1,000 microseconds)
ns	nanosecond
V	volt
W	watt

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General Conventions

Hexadecimal numbers are presented with all letters in uppercase and a lowercase "h" appended or with a 0x at the beginning. For example, 0x14 and 03CAh are hexadecimal numbers. Binary numbers are enclosed in single quotation marks when in text (for example, '11' designates a binary number). Numbers not indicated by an "h", 0x or quotation marks are decimal.

Registers are referred to by acronym, with bits listed in brackets separated by a colon (:) (for example, CODR[7:0]), and are described in the *EP7312 User's Manual*. The use of "TBD" indicates values that are "to be determined," "n/a" designates "not available," and "n/c" indicates a pin that is a "no connect."

Pin Description Conventions

Abbreviations used for signal directions are listed in Table 26.

Table 26. Pin Description Conventions

Abbreviation	Direction
I	Input
O	Output
I/O	Input or Output

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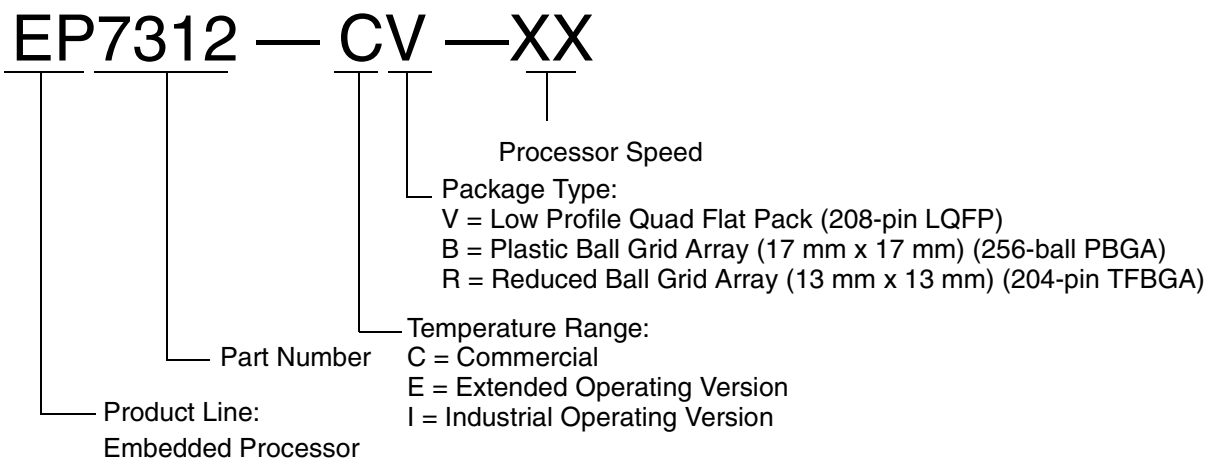
Ordering Information

Here is the list of EP7312 parts that are available:

- EP7312-CV
- EP7312-IV
- EP7312-CB
- EP7312-CR
- EP7312-CV-90
- EP7312-CB-90
- EP7312-CR-90
- EP7312-IB
- EP7312-IR
- EP7312-IV-90
- EP7312-IB-90
- EP7312-IR-90

Ordering Information Legend

Here is the legend for understanding the ordering information on page 1.



Note: Go to the Cirrus Logic Internet site at http://cirrus.com/corporate/contacts to find contact information for your local sales representative.

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