



**THE DATASHEET OF
EP1AGX20CF780C6N**



Introduction

The Arria® GX family of devices combines 3.125 Gbps serial transceivers with reliable packaging technology and a proven logic array. Arria GX devices include 4 to 12 high-speed transceiver channels, each incorporating clock data recovery (CDR) technology and embedded SERDES circuitry designed to support PCI-Express, Gigabit Ethernet, SDI, SerialLite II, XAUI, and Serial RapidIO protocols, along with the ability to develop proprietary, serial-based IP using its Basic mode. The transceivers build upon the success of the Stratix® II GX family. The Arria GX FPGA technology offers a 1.2-V logic array with the right level of performance and dependability needed to support these mainstream protocols.

Features

The key features of Arria GX devices include:

- Transceiver block features
 - High-speed serial transceiver channels with CDR support up to 3.125 Gbps.
 - Devices available with 4, 8, or 12 high-speed full-duplex serial transceiver channels
 - Support for the following CDR-based bus standards—PCI Express, Gigabit Ethernet, SDI, SerialLite II, XAUI, and Serial RapidIO, along with the ability to develop proprietary, serial-based IP using its Basic mode
 - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
 - 1.2- and 1.5-V pseudo current mode logic (PCML) support on transmitter output buffers
 - Receiver indicator for loss of signal (available only in PCI Express [PIPE] mode)
 - Hot socketing feature for hot plug-in or hot swap and power sequencing support without the use of external devices
 - Dedicated circuitry that is compliant with PIPE, XAUI, Gigabit Ethernet, Serial Digital Interface (SDI), and Serial RapidIO
 - 8B/10B encoder/decoder performs 8-bit to 10-bit encoding and 10-bit to 8-bit decoding
 - Phase compensation FIFO buffer performs clock domain translation between the transceiver block and the logic array
 - Channel aligner compliant with XAUI

- Main device features:
 - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 380 MHz
 - Up to 16 global clock networks with up to 32 regional clock networks per device
 - High-speed DSP blocks provide dedicated implementation of multipliers, multiply-accumulate functions, and finite impulse response (FIR) filters
 - Up to four enhanced phase-locked loops (PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, and advanced multiplication and phase shifting
 - Support for numerous single-ended and differential I/O standards
 - High-speed source-synchronous differential I/O support on up to 47 channels
 - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
 - Support for high-speed external memory including DDR and DDR2 SDRAM, and SDR SDRAM
 - Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPPSM)
 - Support for remote configuration updates

Table 1-1 lists Arria GX device features for FineLine BGA (FBGA) with flip chip packages.

Table 1-1. Arria GX Device Features (Part 1 of 2)

| Feature | EP1AGX20C | EP1AGX35C/D | | EP1AGX50C/D | | EP1AGX60C/D/E | | | EP1AGX90E |
|-------------------------------------|------------------------------------|------------------------|------------------------|------------------------|-------------------------------------|------------------------|------------------------|-------------------------|-------------------------|
| | C | C | D | C | D | C | D | E | E |
| Package | 484-pin, 780-pin (Flip chip) | 484-pin (Flip chip) | 780-pin (Flip chip) | 484-pin (Flip chip) | 780-pin, 1152-pin (Flip chip) | 484-pin (Flip chip) | 780-pin (Flip chip) | 1152-pin (Flip chip) | 1152-pin (Flip chip) |
| ALMs | 8,632 | 13,408 | | 20,064 | | 24,040 | | | 36,088 |
| Equivalent logic elements (LEs) | 21,580 | 33,520 | | 50,160 | | 60,100 | | | 90,220 |
| Transceiver channels | 4 | 4 | 8 | 4 | 8 | 4 | 8 | 12 | 12 |
| Transceiver data rate | 600 Mbps to 3.125 Gbps | 600 Mbps to 3.125 Gbps | | 600 Mbps to 3.125 Gbps | | 600 Mbps to 3.125 Gbps | | | 600 Mbps to 3.125 Gbps |
| Source-synchronous receive channels | 31 | 31 | 31 | 31 | 31, 42 | 31 | 31 | 42 | 47 |

Table 1-1. Arria GX Device Features (Part 2 of 2)

| Feature | EP1AGX20C | EP1AGX35C/D | | EP1AGX50C/D | | EP1AGX60C/D/E | | | EP1AGX90E |
|--------------------------------------|-----------|-------------|-----|-------------|----------|---------------|-----|-----|-----------|
| | C | C | D | C | D | C | D | E | E |
| Source-synchronous transmit channels | 29 | 29 | 29 | 29 | 29, 42 | 29 | 29 | 42 | 45 |
| M512 RAM blocks (32 × 18 bits) | 166 | 197 | | 313 | | 326 | | | 478 |
| M4K RAM blocks (128 × 36 bits) | 118 | 140 | | 242 | | 252 | | | 400 |
| M-RAM blocks (4096 × 144 bits) | 1 | 1 | | 2 | | 2 | | | 4 |
| Total RAM bits | 1,229,184 | 1,348,416 | | 2,475,072 | | 2,528,640 | | | 4,477,824 |
| Embedded multipliers (18 × 18) | 40 | 56 | | 104 | | 128 | | | 176 |
| DSP blocks | 10 | 14 | | 26 | | 32 | | | 44 |
| PLLs | 4 | 4 | | 4 | 4, 8 | 4 | | 8 | 8 |
| Maximum user I/O pins | 230, 341 | 230 | 341 | 229 | 350, 514 | 229 | 350 | 514 | 538 |

Arria GX devices are available in space-saving FBGA packages (refer to [Table 1-2](#)). All Arria GX devices support vertical migration within the same package. With vertical migration support, designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross-reference the available I/O pins with the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

Table 1-2. Arria GX Package Options (Pin Counts and Transceiver Channels) (Part 1 of 2)

| Device | Transceiver Channels | Source-Synchronous Channels | | Maximum User I/O Pin Count | | |
|-----------|----------------------|-----------------------------|----------|----------------------------|----------------------|-----------------------|
| | | Receive | Transmit | 484-Pin FBGA (23 mm) | 780-Pin FBGA (29 mm) | 1152-Pin FBGA (35 mm) |
| EP1AGX20C | 4 | 31 | 29 | 230 | 341 | — |
| EP1AGX35C | 4 | 31 | 29 | 230 | — | — |
| EP1AGX50C | 4 | 31 | 29 | 229 | — | — |
| EP1AGX60C | 4 | 31 | 29 | 229 | — | — |
| EP1AGX35D | 8 | 31 | 29 | — | 341 | — |
| EP1AGX50D | 8 | 31, 42 | 29, 42 | — | 350 | 514 |

Table 1-2. Arria GX Package Options (Pin Counts and Transceiver Channels) (Part 2 of 2)

| Device | Transceiver Channels | Source-Synchronous Channels | | Maximum User I/O Pin Count | | |
|-----------|----------------------|-----------------------------|----------|----------------------------|----------------------|-----------------------|
| | | Receive | Transmit | 484-Pin FBGA (23 mm) | 780-Pin FBGA (29 mm) | 1152-Pin FBGA (35 mm) |
| EP1AGX60D | 8 | 31 | 29 | — | 350 | — |
| EP1AGX60E | 12 | 42 | 42 | — | — | 514 |
| EP1AGX90E | 12 | 47 | 45 | — | — | 538 |

Table 1-3 lists the Arria GX device package sizes.

Table 1-3. Arria GX FBGA Package Sizes

| Dimension | 484 Pins | 780 Pins | 1152 Pins |
|--------------------------|----------|----------|-----------|
| Pitch (mm) | 1.00 | 1.00 | 1.00 |
| Area (mm ²) | 529 | 841 | 1225 |
| Length × width (mm × mm) | 23 × 23 | 29 × 29 | 35 × 35 |

Document Revision History

Table 1-4 lists the revision history for this chapter.

Table 1-4. Document Revision History

| Date and Document Version | Changes Made | Summary of Changes |
|---------------------------|--|--------------------|
| December 2009, v2.0 | <ul style="list-style-type: none"> ■ Document template update. ■ Minor text edits. | — |
| May 2008, v1.2 | Included support for SDI, SerialLite II, and XAUI. | — |
| June 2007, v1.1 | Included GIGE information. | — |
| May 2007, v1.0 | Initial Release | — |

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