EMC2102

RPM-Based Fan Controller with HW Thermal Shutdown

PRODUCT FEATURES

Datasheet

General Description

The EMC2102 is an SMBus, closed-loop, RPM-based fan controller/driver with hardware (HW) thermal shutdown and reset controller. The EMC2102 is packaged in a thermally enhanced, compact, 5x5, 28-pin lead-free RoHS compliant QFN package.

The EMC2102 utilizes Beta Compensation (an implementation of the BJT or transistor model for thermal diodes) and Resistance Error Correction (REC) to accurately monitor three external temperature zones. These features allow great accuracy for CPU substrate thermal diodes on multiple process geometries as well as with discrete diode-connected transistors. Both Beta Compensation and REC can be disabled on the EMC2102 to maintain accuracy when monitoring AMD thermal diodes.

The EMC2102 includes a closed-loop RPM based Fan Control Algorithm that integrates a linear fan driver capable of sourcing 600mA of current. The fan control algorithm is designed to work with fans that operate up to 16,000 RPMs.

The EMC2102 provides a stand-alone HW thermal shutdown block. The HW thermal shutdown logic can be configured for a few common configurations based on the strapping level of the SHDN_SEL pin on the PCB. The HW thermal shutdown point can be set in 1°C increments by using a discrete resistor divider implemented on the TRIP_SET pin.

The EMC2102 also provides 5V supply 'power good' function with a threshold of 4.5V. This function is provided on the RESET# pin.

Features

- Designed to support 45nm, 65nm, and 90nm CPU Diodes
- Supports BJT and transistor models for diode channels
- Closed-Loop RPM Based Fan Controller
  - Accepts External Clock Source To Achieve 2% Accuracy
- Integrated Linear Fan Driver
  - 600mA Drive Capability
- HW Thermal Shutdown (SYS_SHDN#)
  - 1°C Incremental Set Points For Thermal Shutdown
  - Cannot be disabled by software
- Provides Reset Function (RESET#) On 5V Supply
- Three Remote Thermal Zones
  - ±1°C Accuracy (60°C to 100°C)
  - 1°C Resolution
- Resistance Error Correction On Thermal Diode Channels
  - Eliminates Temperature Offset Due To Series Resistance From PCB Traces And Thermal 'Diode'
- Thermally Enhanced, 28-pin, 5x5 QFN Lead-free RoHS Compliant Package
- Operates From Single 3.0 - 3.6V Supply
  - 5V Supply For Linear Fan Driver
- Software Configurable ALERT# Signal For Diode Fault, Fan Stall Or System Warning

Applications

- Notebook Computers
- Desktop Computers
- Embedded Applications

ORDER NUMBER:

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Table of Contents

Chapter 1 Block Diagram 7

Chapter 2 Pinout 8
2.1 Pin Layout for EMC2102 8
2.2 Pin Description for EMC2102 9

Chapter 3 Electrical Specifications 11
3.1 Absolute Maximum Ratings 11
3.2 Electrical Specifications 11
3.3 SMBus Electrical Specifications 13

Chapter 4 System Management Bus Interface Protocol 15
4.1 Write Byte 15
4.2 Read Byte 16
4.3 Send Byte 16
4.4 Receive Byte 16
4.5 Alert Response Address 16
4.6 SMBus Address 17
4.7 SMBus Time-out 17

Chapter 5 General Description 18
5.1 Temperature Monitoring 20
5.1.1 Resistance Error Correction 20
5.1.2 Beta Compensation 20
5.1.3 Fault Queue 20
5.2 Fan Control Modes of Operation 21
5.3 RPM based Fan Control Algorithm 21
5.3.1 Programming the RPM based Fan Control Algorithm 23
5.3.2 TACH Measurement 23
5.3.2.1 Stalled Fan23
5.3.3 Spin Up Routine 23
5.3.4 FAN_MODE Pin 25
5.3.5 32.768KHz Clock Source 25
5.4 Watchdog Timer 25
5.5 High Side Fan Driver 26
5.5.1 Overcurrent Limit 26
5.6 Internal Thermal Shutdown (TSD) 26
5.7 Critical/Thermal Shutdown 26
5.7.1 TRIP_SET 28
5.7.2 SHDN_SEL Pin 28
5.7.3 Internal HW_SHDN Signal 29
5.8 5V Reset Controller 30

Chapter 6 Register Set 31
6.1 Register Map 31
6.1.1 Lock Entries 32
6.2 Temperature Data Registers 33
6.3 Critical/Thermal Shutdown Temperature Register 34
6.4 Configuration Register 34
6.5 Conversion Rate Register 35
6.6 Interrupt Status Register 1 36

6.7 Interrupt Status Register 2 37
6.8 Interrupt Mask Register 37
6.9 Beta Configuration Registers 38
6.10 REC Configuration Register 39
6.11 Temperature Limit Registers 40
6.12 Fan Driver Setting Register 40
6.13 Fan Configuration Register 41
6.14 Fan Spin Up Configuration Register 42
6.15 Fan Step Register 43
6.16 Fan Minimum Drive Register 43
6.17 Valid TACH Count Register 44
6.18 TACH Target Register 44
6.19 TACH Reading Register 44
6.20 Product ID Register 45
6.21 Revision Register 46

Chapter 7 Package Drawing 47

Appendix A TACH Reading Table - 2000 RPM Range. 48

Appendix B TACH Reading Table - 500RPM Range 51

List of Figures

Figure 1.1 EMC2102 Block Diagram 7
Figure 2.1 EMC2102 Pin Diagram 8
Figure 4.1 SMBus Timing Diagram 15
Figure 5.1 EMC2102 System Diagram 19
Figure 5.2 RPM based Fan Control Algorithm 22
Figure 5.3 Spin Up Routine 24
Figure 5.4 EMC2102 Critical/Thermal Shutdown Block Diagram 27
Figure 5.5 HW_SHDN Operation 29
Figure 5.6 5V Reset Controller Timing 30
Figure 7.1 EMC2102 28-Pin 5x5mm QFN Package Outline and Parameters 47

List of Tables

Table 2.1 Pin Description . . . 9
Table 3.1 Absolute Maximum Ratings . . . 11
Table 3.2 Electrical Specifications . . . 11
Table 3.3 SMBus Electrical Specifications . . . 13
Table 4.1 Protocol Format . . . 15
Table 4.2 Write Byte Protocol . . . 15
Table 4.3 Read Byte Protocol . . . 16
Table 4.4 Send Byte Protocol . . . 16
Table 4.5 Receive Byte Protocol . . . 16
Table 4.6 Alert Response Address Protocol . . . 16
Table 5.1 Fan Controls Active for Operating Mode . . . 21
Table 5.2 FAN_MODE Pin Functions . . . 25
Table 5.3 CLK_SEL Pin Functions . . . 25
Table 5.4 SHDN_SEL Pin Configuration . . . 28
Table 6.1 EMC2102 Register Set . . . 31
Table 6.2 Temperature data Registers . . . 33
Table 6.3 Temperature Data Format . . . 33
Table 6.4 Critical/Thermal Shutdown Temperature Register . . . 34
Table 6.5 Configuration Register . . . 34
Table 6.6 Fault Queue . . . 34
Table 6.7 Conversion Rate Register . . . 35
Table 6.8 Conversion Rate . . . 36
Table 6.9 Interrupt Status Register 1 . . . 36
Table 6.10 Interrupt Status Register 2 . . . 37
Table 6.11 Interrupt Mask Register . . . 37
Table 6.12 Beta Configuration Registers . . . 38
Table 6.13 Beta Compensation Look Up Table . . . 39
Table 6.14 REC Configuration Register . . . 39
Table 6.15 Temperature Limit Registers . . . 40
Table 6.16 Fan Driver Setting Register . . . 40
Table 6.17 Fan Control Configuration Register . . . 41
Table 6.18 Minimum Edges for Fan Rotation . . . 41
Table 6.19 Update Time . . . 42
Table 6.20 Fan TACH Configuration Register . . . 42
Table 6.21 Spin Time . . . 42
Table 6.22 Fan Step Register . . . 43
Table 6.23 Minimum Fan Drive Register . . . 43
Table 6.24 Valid TACH Count Register . . . 44
Table 6.25 TACH Reading Registers . . . 44
Table 6.26 TACH Reading Register . . . 44
Table 6.27 Example TACH Reading for Specific Fan Speeds . . . 45
Table 6.28 Product ID Register . . . 45
Table 6.29 Revision Register . . . 46
Table 7.1 TACH Count to RPM (2k Range) . . . 48
Table 7.2 TACH Count to RPM (500 Range) . . . 51

Chapter 1 Block Diagram

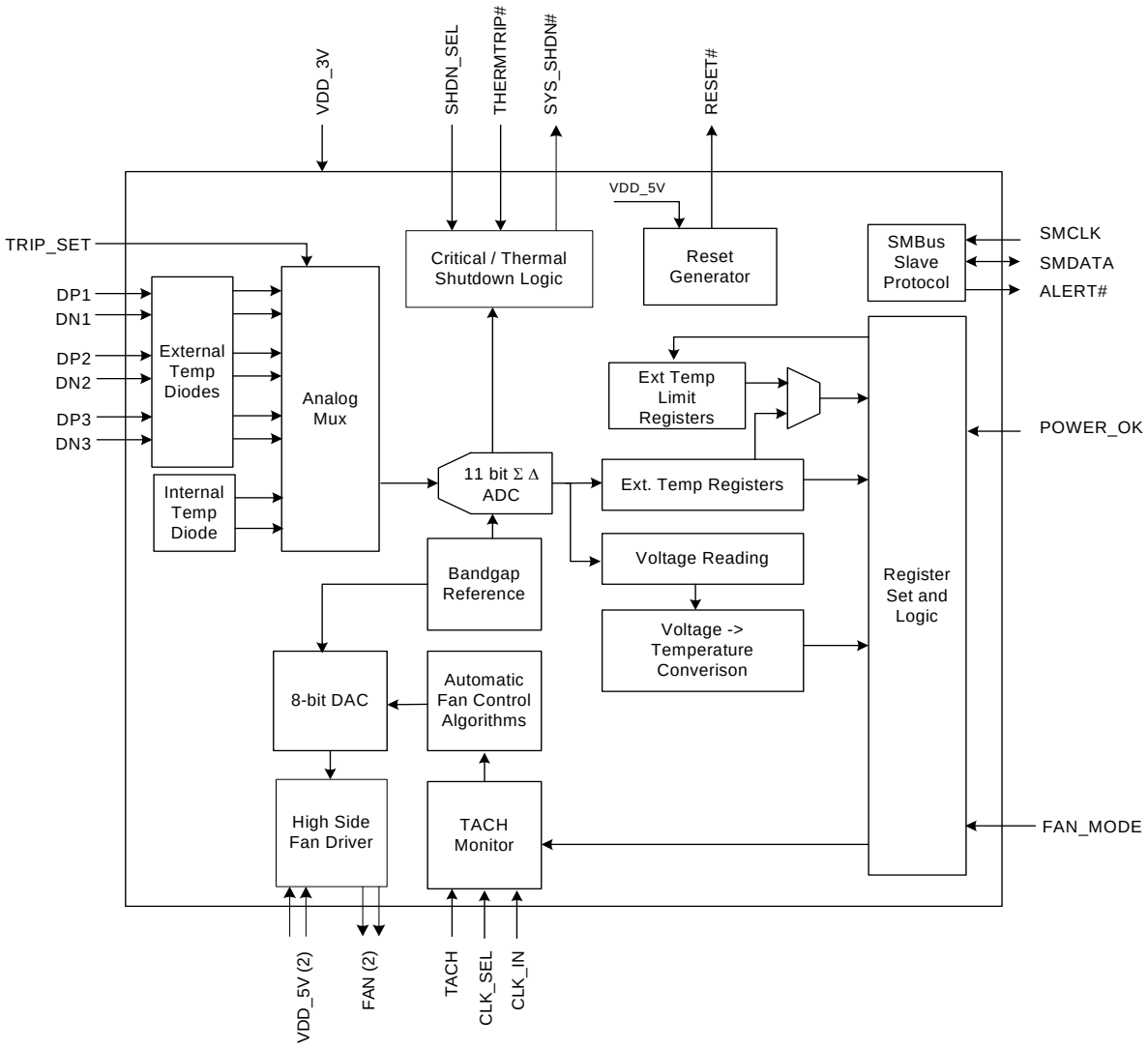

Figure 1.1 EMC2102 Block Diagram

Chapter 2 Pinout

2.1 Pin Layout for EMC2102

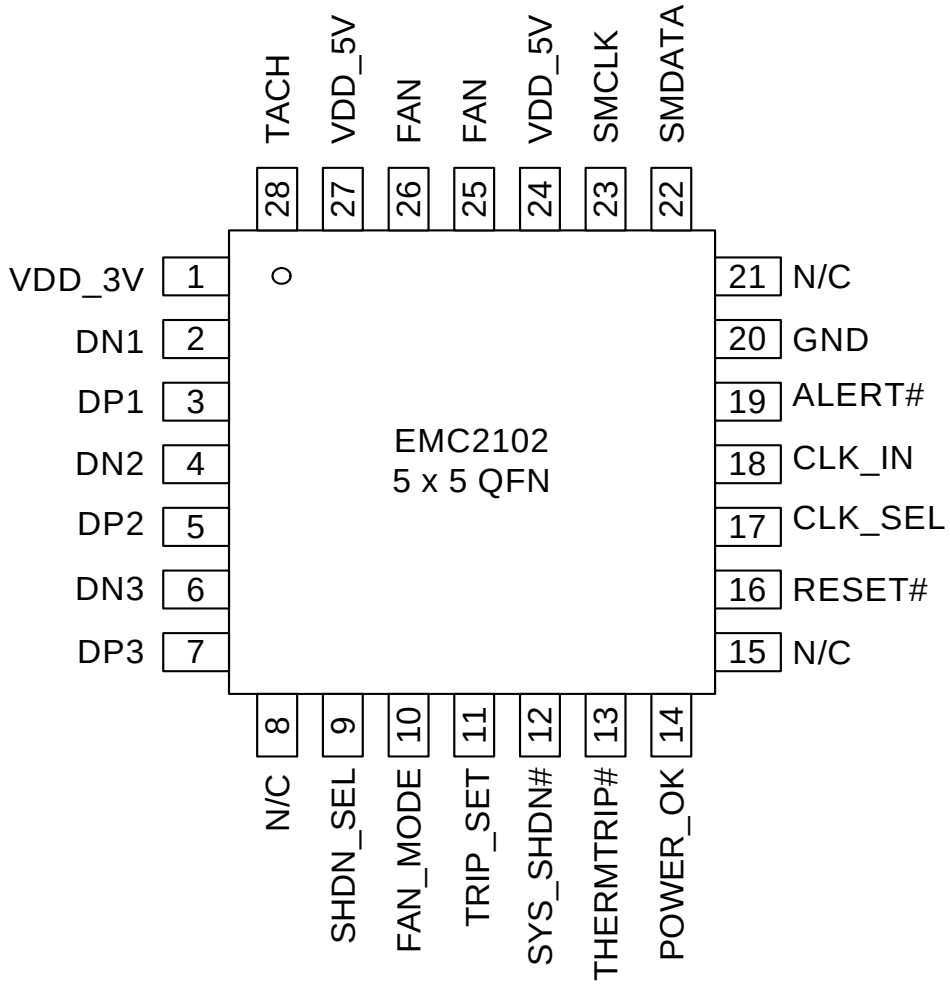

Figure 2.1 EMC2102 Pin Diagram

2.2 Pin Description for EMC2102

Table 2.1 Pin Description

PIN	NAME	FUNCTION	TYPE
1	VDD_3V	Supply Connection of 3.3V.	Power
2	DN1	Negative (cathode) Analog Input for External Diode 1.	AIO
3	DP1	Positive (anode) Analog Input for External Diode 1.	AIO
4	DN2	Negative (cathode) Analog Input for External Diode 2.	AIO
5	DP2	Positive (anode) Analog Input for External Diode 2.	AIO
6	DN3	Negative (cathode) Analog Input for External Diode 3.	AIO
7	DP3	Positive (anode) Analog Input for External Diode 3.	AIO
8	N/C	Not internally connected.	N/A
9	SHDN_SEL	Determines HW Shutdown temperature channel (see Table 5.4, "SHDN_SEL Pin Configuration".)	DIT
10	FAN_MODE	Selects power-up default for fan drive setting.	DIT
11	TRIP_SET	Voltage input to determine HW Shutdown threshold temperature	AI
12	SYS_SHDN#	Active low Critical System Shutdown output	OD (5V)
13	THERMTRIP#	Active low Critical temperature limit signal from the CPU or chipset.	IP
14	POWER_OK	Active high power good input.	DI (5V)
15	N/C	Not internally connected.	N/A
16	RESET#	Active low reset output.	DO
17	CLK_SEL	Selects internal oscillator or external clock.	DI (5V)
18	CLK_IN	32.768KHz clock input.	DI (5V)
19	ALERT#	Active low interrupt.	OD (5V)
20	GND	GND connection.	Power
21	N/C	Not internally connected.	N/A
22	SMDATA	SMBus data input/output.	DIOD (5V) - requires external upll-up resistor
23	SMCLK	SMBus clock input.	DI (5V) - requires external pull-up resistor

Table 2.1 Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
24	VDD_5V	5V supply input for the linear fan driver. Both VDD_5V pins should be connected to same 5V supply.	Power
25	FAN	Linear fan drive signal. Both FAN pins should be connected together.	AO
26	FAN	Linear fan drive signal. Both FAN pins should be connected together.	AO
27	VDD_5V	5V supply input for the linear fan driver. Both VDD_5V pins should be connected to same 5V supply.	Power
28	TACH	Input from the tachometer pin of the fan.	DI (5V)

The pin type are described in detail below. All pins labelled with (5V) are 5V tolerant.:

Power - this pin is used to supply power to the device.

DI - Digital Input - this pin is used as a digital input. This pin is 5V tolerant.

AI - Analog Input - this pin is used as an input for analog signals.

AO - Analog Output - this pin is used as an output for analog signals.

AIO - Analog Input / Output - this pin is used as an I/O for analog signals.

DO - Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current and doesn't require a pull-up resistor.

DIOD - Open Drain Digital Input / Output - this pin is used as an digital I/O. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

OD - Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor.

DIT - Tri-stated Digital Input - this pin is a digital input that supports 3 logic levels at the input: logic high, logic low, or high impedance (open).

IP - Digital Input - this pin has an internal 30uA pull-up current to VDD_3V.

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

Voltage on VDD_5V Pins and 5V tolerant pins (see Table 2.1, "Pin Description")	-0.3 to 6.5	V
Voltage on VDD_3V pin	-0.3 to 4	V
Voltage on FAN pins	-0.3 to VDD_5V + 0.3	V
Voltage on any other pin to GND	-0.3 to VDD_3V + 0.3	V
Package Power Dissipation	0.9 up to T_A = 85°C Note 3.2	W
Junction to Ambient (θ_{JA}) Note 3.3	37	°C/W
Operating Ambient Temperature Range	0 to 85	°C
Operating Die Temperature Range	0 to 125	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating, All Pins, HBM	2000	V

These ratings are absolute maximum values. Exceeding these values or operating at these values for an extended period of time may cause permanent damage to the device.

Note 3.1 All voltages are relative to ground.

Note 3.2 The Package Power Dissipation specification assumes a thermal via design consisting of four 20mil vias connected to the ground plane with a 3.1mm x 3.1mm thermal landing.

Note 3.3 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 60°C/W including localized PCB temperature increase.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

VDD_3V = 3V to 3.6V, VDD_5V = 4.6V - 5.5V, T_A = 0°C to 85°C all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
3.3V Supply Voltage	V_{DD_3V}	3	3.3	3.6	V	
5V Supply Voltage	V_{DD_5V}	4.6	5	5.5	V	
Supply Current from VDD_3V pin	I_{DD3}		500	750	uA	Fan Driver enabled
Supply Current from VDD_5V pin	I_{DD5}		200		uA	Fan Driver enabled

Table 3.2 Electrical Specifications (continued)

VDD_3V = 3V to 3.6V, VDD_5V = 4.6V - 5.5V, T_A = 0°C to 85°C all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
External Temperature Monitors						
Temperature Accuracy			±1	±1.5	°C	60°C < T_{DIODE} < 100°C 30°C < T_{DIE} < 85°C (Note 3.4)
			±1	±3	°C	0°C < T_{DIODE} < 125°C, 0°C < T_{DIE} < 115°C (Note 3.4)
Temperature Resolution			1		°C	
Diode decoupling capacitor	C_{FILTER}			2200	pF	Connected across external 2N3904 diode or AMD diode (Note 3.5)
				470	pF	Connected across CPU or GPU thermal diode (Note 3.5)
Resistance Error Corrected	R_{SERIES}			100	Ohm	Series resistance in DP and DN lines
Internal Temperature Monitor						
Temperature Accuracy			±3		°C	(Note 3.4)
Temperature Resolution			1		°C	
Reset Generator						
Reset Voltage	V_{RESET}	4.3	4.4	4.5	V	V_{DD_5V} rising edge 3V < V_{DD_3V} < 3.6V
Hysteresis	ΔV_{RESET}		100		mV	
Time Delay	t_{RESET}		220		ms	
High Side Fan Driver						
Output High Voltage from 5V supply	V_{OH_5V}			VDD_5 V - 0.4	V	I_{SOURCE} = 600mA, VDD_5V = 5V
Fan Drive Current	I_{SOURCE}			600	mA	
Overcurrent Limit	I_{OVER}		1500		mA	Momentary Current drive at startup for < 2 seconds
DC Short Circuit Current Limit	I_{SHORT}		800		mA	Sourcing current, Thermal shutdown not triggered, FAN_OUT = 0V
Short circuit delay	t_{DFS}		2		s	
Output Capacitive Load	C_{LOAD}			100	uF	
ESR on C_{LOAD}	R_{ESR}	0		2	Ohm	
RPM Based Fan Controller						

Table 3.2 Electrical Specifications (continued)

VDD_3V = 3V to 3.6V, VDD_5V = 4.6V - 5.5V, T_A = 0°C to 85°C all Typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
TACH Range	TACH	480		16000	RPM	
TACH Setting Accuracy	Δ_{TACH}		±1	±2	%	External oscillator 32.768kHz
	Δ_{TACH}		±5	±7.5	%	Internal Oscillator 40°C < T_{DIE} < 100°C
Thermal Shutdown						
Thermal Shutdown Threshold	TSD_{TH}		150		°C	
Thermal Shutdown Hysteresis	TSD_{HYST}		50		°C	
SMBus and Digital I/O pins						
Output High Voltage	V_{OH}	VDD _3V 0.4			V	2 mA current drive
Output Low Voltage	V_{OL}			0.5	V	4mA current sink

Note 3.4 T_{DIE} refers to the internal die temperature and may not match T_A due to self heating of the device. The internal temperature sensor will return T_{DIE}.

Note 3.5 Contact SMSC for Application Notes and guidelines when measuring GPU processor diodes and CPU processor diodes.

3.3 SMBus Electrical Specifications

Table 3.3 SMBus Electrical Specifications

VDD_3V = 3V to 3.6V, VDD_5V = 4.6 to 5.5V, T_A = 0°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High/Low Current	I_{IH} / I_{IL}	-1		1	uA	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current			4		mA	SMDATA = 0.5V
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	

Table 3.3 SMBus Electrical Specifications (continued)

VDD_3V = 3V to 3.6V, VDD_5V = 4.6 to 5.5V, T_A = 0°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Bus free time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.6		6	us	
Data Setup Time	$t_{SU:DAT}$	0.6		72	us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 4 System Management Bus Interface Protocol

The EMC2102 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1. Stretching of the SMCLK signal is supported, however the EMC2102 will not stretch the clock signal.

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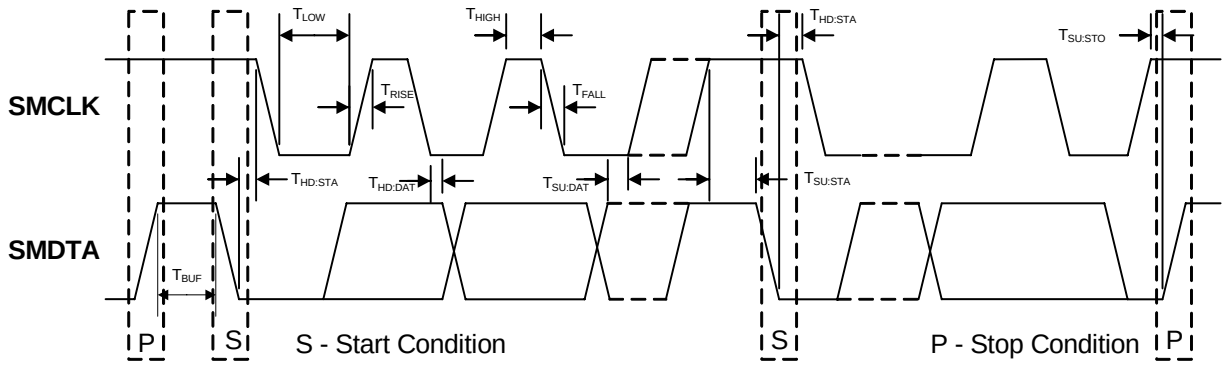


Figure 4.1 SMBus Timing Diagram

The EMC2102 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte and Write Byte as valid protocols as shown below. It will respond to the Alert Response Address protocol but is not in full compliance.

All of the below protocols use the convention in Table 4.1.

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

4.1 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2:

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1	7	1	1	8	1	8	1	1

4.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	W R	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1	7	1	1	8	1	1	7	1	1	8	1	1

4.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1	7	1	1	8	1	1

4.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1	7	1	1	8	1	1

4.5 Alert Response Address

The ALERT# output can be used as a processor interrupt or as an $\overline{\text{SMBALERT}}$.

When it detects that the $\overline{\text{SMBALERT}}$ pin is asserted, the host will send the Alert Response Address (general address of 000_1100b) on the bus. All devices with active interrupts will respond with their client address as shown in Table 4.6.

..

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1	7	1	1	8	1	1

The EMC2102 will respond to the ARA command if the ALERT# pin has been asserted but will not immediately release the ALERT# pin. The ALERT# pin is released under the following conditions.

1. The Interrupt Status Registers are read and the error condition has been removed.
2. The specific error condition is masked from asserting the ALERT# pin.

4.6 SMBus Address

The EMC2102-1 is addressed on the SMBus as 011_1101b.

Attempting to communicate with the EMC2102 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents.

4.7 SMBus Time-out

The EMC2102 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

Chapter 5 General Description

The EMC2102 monitors three external temperature channels. Two of the external temperature channels can employ both Beta Compensation (an implementation of the BJT or transistor model for thermal diodes) and Resistance Error Correction for use with thermal diodes while the third channel is hardwired to measure a discrete diode connected NPN or PNP transistor. The temperature data is available over a standard 2-wire serial interface using SMBus read commands. The temperature monitoring is described in more detail in Section 5.1, "Temperature Monitoring".

The EMC2102 integrates a closed-loop RPM based Fan Control Algorithm. A host writes the desired fan speed into a register of the EMC2102 via the SMBus and the integrated fan controller will maintain the fan at the desired speed using fan speed feedback from the TACH output from a 3-wire fan. The fan control algorithm controls an integrated 5V, 600mA, linear fan driver. The fan control algorithm functionality is described in more detail in Section 5.3, "RPM based Fan Control Algorithm"

The EMC2102 provides the system with a hardware based critical/thermal shutdown function. This critical/thermal shutdown function integrates critical signals from both the CPU and power supply and the analog circuitry to monitor a specific temperature channel based on the system configuration. The critical/thermal shutdown temperature threshold is configured on the PCB through a simple discrete resistor divider. The Critical/Thermal Shutdown function is described in more detail in Section 5.7, "Critical/Thermal Shutdown".

An example of a typical system configuration for the EMC2102 is provided in Figure 5.1.

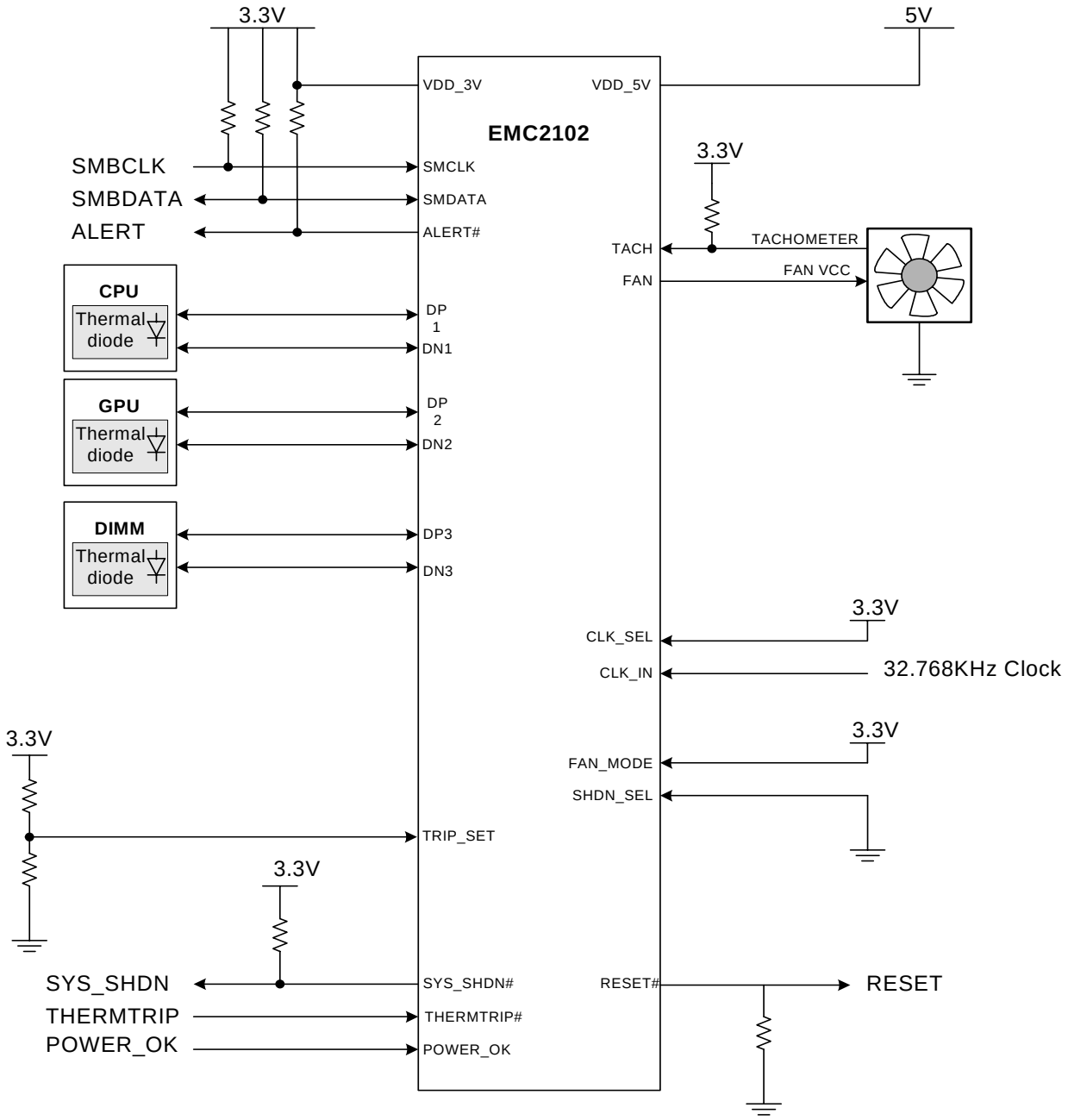


Figure 5.1 EMC2102 System Diagram

5.1 Temperature Monitoring

External diode channels one and two can be configured to monitor either discrete thermal diodes or a CPU / GPU thermal diode. External diode channel three is always configured to monitor a discrete diode-connected transistor (such as a 2N3904) or an AMD thermal diode. Each channel can enable the Resistance Error Correction functionality and external diode channels one and two can adjust the Beta Compensation settings (disabling it if desired). The disabling of these features is only recommended in two situations:

1. An AMD thermal diode is being monitored. The AMD thermal diode is physically a 2-terminal diode and will not function with either Beta Compensation or Resistance Error Correction. Because of this, when an EMC2102 temperature channel is interfacing an AMD thermal diode, both Beta Compensation and Resistance Error Correction must be disabled.
2. A discrete diode connected transistor (such as 2N3904) is used. In this configuration, Beta Compensation must be disabled, but Resistance Error Correction should remain enabled.

5.1.1 Resistance Error Correction

The EMC2102 includes active Resistance Error Correction to remove the effect of up to 100 ohms of series resistance. Without this automatic feature, voltage developed across the parasitic resistance in the remote diode path causes the temperature to read higher than the true temperature is. The error induced by parasitic resistance is approximately +0.7°C per ohm. Sources of parasitic resistance include bulk resistance in the remote temperature transistor junctions, series resistance in the CPU, and resistance in the printed circuit board traces and package leads. Resistance error correction in the EMC2102 eliminates the need to characterize and compensate for parasitic resistance in the remote diode path.

5.1.2 Beta Compensation

The forward current gain, or beta, of a transistor is not constant as emitter currents change. As well, it is not constant over changes in temperature. The variation in beta causes an error in temperature reading that is proportional to absolute temperature. This correction is done by implementing the BJT or transistor model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The Beta Compensation circuitry in the EMC2102 corrects for this beta variation to eliminate any error which would normally be induced.

5.1.3 Fault Queue

To avoid spurious interrupts and Critical/Thermal Trip events induced by thermal spikes and noise injection, the selected Thermal / Critical Shutdown Temperature channel (see Section 5.7.2) is filtered through a fault queue. This fault queue requires that a user-defined number of consecutive out-of-limit errors be recorded before it will cause an interrupt or trigger the Critical/Thermal trip event.

The fault queue only applies to the measurement channels that will cause the SYS_SHDN# pin to be asserted including any software configured channels (see Section 5.7). In addition, the fault queue applies to all enabled channels simultaneously and will trigger the SYS_SHDN# pin if there are the desired number of consecutive measurements with any or all channels exceeding their corresponding limits.

5.2 Fan Control Modes of Operation

The EMC2102 has two modes of operation for the High Side Fan Driver. They are:

1. Manual Mode - in this mode of operation, the user directly controls the fan drive setting. Updating the Fan Driver Setting Register (see Section 6.12) will instantly update the fan drive.

- The Manual Mode is enabled by clearing the EN bit in the Fan Configuration Register (see Section 6.13).
- Whenever the Manual Mode is enabled the current drive will be changed to what was last written into the Fan Driver Setting Register.
- Setting the drive value to 00h will disable the High Side Fan Driver for lower power operation.

2. Using RPM based Fan Control Algorithm - in this mode of operation, the user determines a target TACH count and the drive setting is automatically updated to achieve this target speed. The algorithm uses the Spin Up Routine and has user definable ramp rate controls.

Table 5.1 Fan Controls Active for Operating Mode

MANUAL MODE	ALGORITHM
Fan Driver Setting (read / write)	Fan Driver Setting (read only)
EDGES[1:0]	EDGES[1:0] (Fan Configuration)
-	UPDATE[2:0] (Fan Configuration)
-	LEVEL (Spin Up Configuration)
-	SPINUP_TIME[1:0] (Spin Up Configuration)
-	Fan Step
-	Fan Minimum Drive
Valid TACH Count	Valid TACH Count
-	TACH Target
TACH Reading	TACH Reading

5.3 RPM based Fan Control Algorithm

The EMC2102 includes a RPM based Fan Control Algorithm that controls an integrated linear High Side Fan Driver. This fan control algorithm automatically approaches and maintains the system's desired fan speed to an accuracy directly proportional to the accuracy of the clock source. Figure 5.2, "RPM based Fan Control Algorithm" shows a simple flow diagram of the RPM based Fan Control Algorithm operation.

The desired TACH count is set by the user inputting the desired number of 32.768KHz cycles that occur per fan revolution. The user may change the target count at any time. The user may also set the target count to FFh in order to disable the fan driver for lower current operation.

For example, if a desired RPM rate for a 2-pole fan is 3000RPMs, then the user would input the hexidecimal equivalent of 655 (29h in the TACH Target Register). This number represents the number of 32.768KHz cycles that would occur during the time it takes the fan to complete a single revolution when it is spinning at 3000RPMs (see Equation [4] in Section 6.19).

The EMC2102's RPM based Fan Control Algorithm has programmable configuration settings for parameters such as ramp-rate control and spin up conditions. The fan driver automatically detects and attempts to alleviate a stalled/stuck fan condition while also asserting the ALERT# pin. The EMC2102 works with fans that operate up to 16,000 RPMs and provide a valid tachometer signal. The fan controller will function either with an externally supplied 32.768KHz clock source or with it's own internal 32.768KHz oscillator depending on the required accuracy.

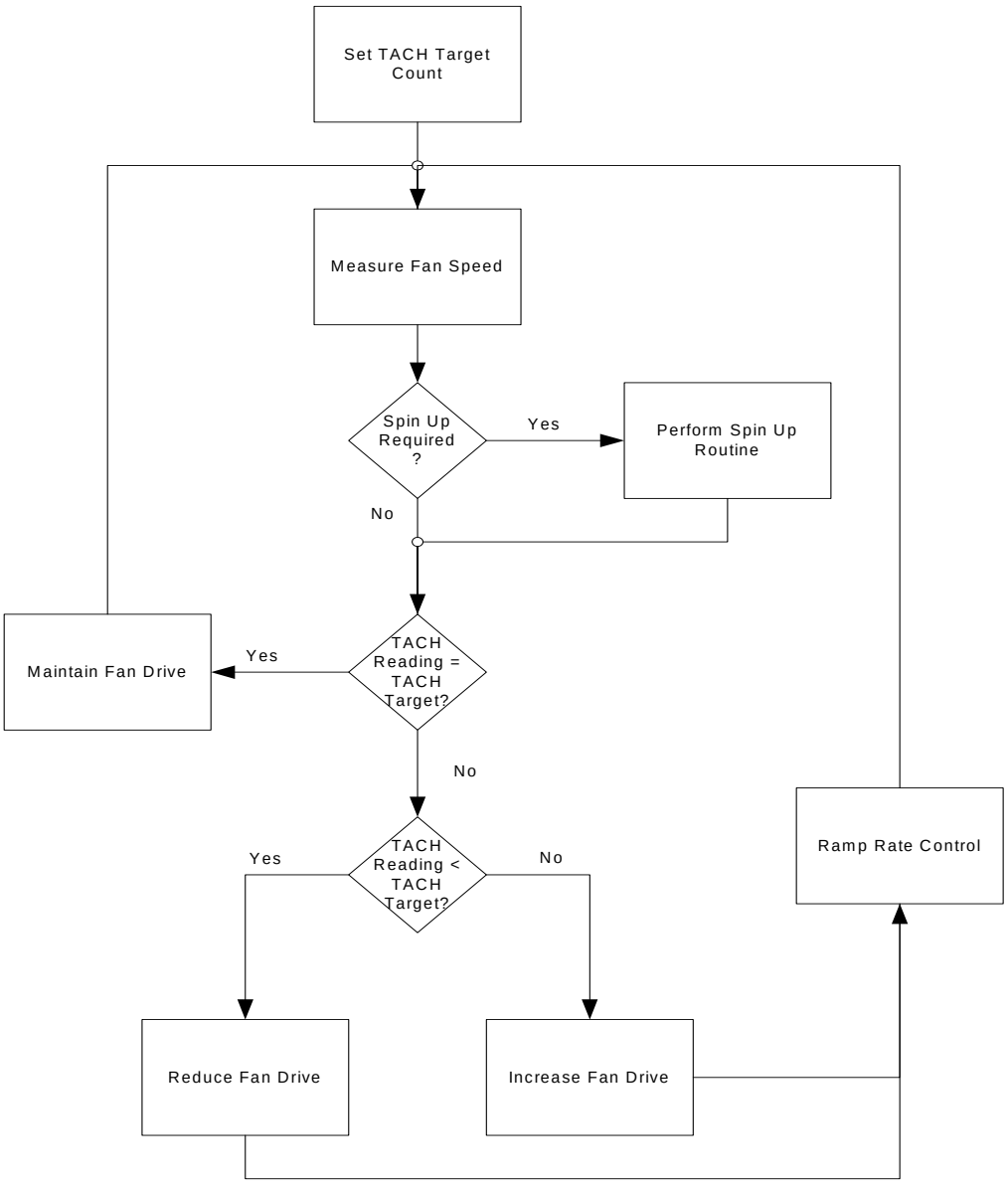


Figure 5.2 RPM based Fan Control Algorithm

5.3.1 Programming the RPM based Fan Control Algorithm

The RPM based Fan Control Algorithm powers-up enabled and active. The following registers control the algorithm. The EMC2102 fan control registers are preloaded with defaults that will work for a wide variety of fans so only the TACH Target Register is required to set a fan speed. The other fan control registers can be used to fine-tune the algorithm behavior based on application requirements.

1. Set the Valid TACH Count Register to the minimum TACH count that indicates the fan is spinning.
2. Set the Spin Up Configuration Register to the spin up level and Spin Time desired.
3. Set the Fan Step Register to the desired step size.
4. Set the Fan Minimum Drive Register to the minimum drive value that will maintain fan operation.
5. Set the Update Time, and Edges options in the Fan Configuration Register.
6. Set the TACH Target Register to the desired TACH count.

5.3.2 TACH Measurement

In both modes of operation, the TACH measurement will work normally. Any TACH count that is higher than the Valid TACH Count (see Section 6.17) will flag a stalled fan and trigger an interrupt.

The EMC2102 includes a TACH measurement circuit. The TACH signal must be valid at all times to ensure proper operation. The TACH measurement circuitry is programmable to detect the fan speed of a variety of fan configurations and architectures including 1-pole, 2-pole (default), 3-pole, and 4-pole fans.

APPLICATION NOTE: The TACH measurement works independently of the drive settings. If the device is put into manual mode and the fan drive is set at a level that is lower than the fan can operate (including zero drive), then the TACH measurement may signal a Stalled Fan condition and assert an interrupt.

5.3.2.1 Stalled Fan

If the TACH counter exceeds the user-programmable Valid TACH Count setting then it will flag the fan as stalled and trigger an interrupt. If the RPM based Fan Control Algorithm is enabled, the algorithm will automatically attempt to restart the fan until it detects a valid TACH level or is disabled.

The FAN_STALL Status bit indicates that a stalled fan was detected. This bit is checked conditionally depending on the mode of operation.

- Whenever the Manual Mode is enabled, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time (see Table 6.21, "Spin Time") to allow the fan opportunity to reach a valid speed without generating unnecessary interrupts.
- In Manual Mode, whenever the drive value is changed from 00h, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time to allow the fan opportunity to reach a valid speed without generating unnecessary interrupts.
- In Manual Mode, whenever the TACH count exceeds the Valid TACH Count Register setting, the FAN_STALL status bit will be set.
- When the RPM based Fan Control Algorithm, the stalled fan condition is checked whenever the Update Time is met and the fan drive setting is updated. It is not a continuous check.

5.3.3 Spin Up Routine

The EMC2102 also contains programmable circuitry to control the spin up behavior of the fan driver to ensure proper fan operation. During Manual Mode, the Spin Up Routine will not control the fan drive settings under any conditions.

When the RPM based Fan Control Algorithm is running, the Spin Up Routine is initiated under the following conditions:

APPLICATION NOTE: When the device is operating in manual mode, the FAN_SPIN status bit may be set if the fan drive is set at a level that is lower than the fan can operate (including zero drive). If the FAN_SPIN interrupt is unmasked, then this condition will trigger an errant interrupt.

1. The TACH Target Register value changes from a value of FFh to a value that is less than the Valid TACH Count (see Section 6.18, "TACH Target Register" and Section 6.17, "Valid TACH Count Register").
2. At power-up if the FAN_MODE setting is '1' or 'open' indicating 75% drive or 60% drive respectively. If the FAN_MODE setting is '0' indicating 0% drive, then the Spin Up Routine is not initiated until another condition is met.
3. The RPM based Fan Control Algorithm is started and the FAN_MODE setting is '0' indicating 0% drive prior to algorithm control.
4. The RPM based Fan Control Algorithm's measured TACH count is greater than the Valid TACH Count.

When the Spin Up Routine is operating, the fan driver is set to full scale for one quarter of the total user defined spin up time. For the remaining spin up time, the fan driver output is set a a user defined level (60% or 75% drive).

After the Spin Up Routine has finished, the EMC2102 measures the TACH. If the measured TACH count is higher than the Valid TACH Count Register setting, the FAN_SPIN status bit is set and the Spin Up Routine will automatically attempt to restart the fan.

Figure 5.3 shows an example of the Spin Up Routine in response to a programmed fan speed change based on the first condition above.

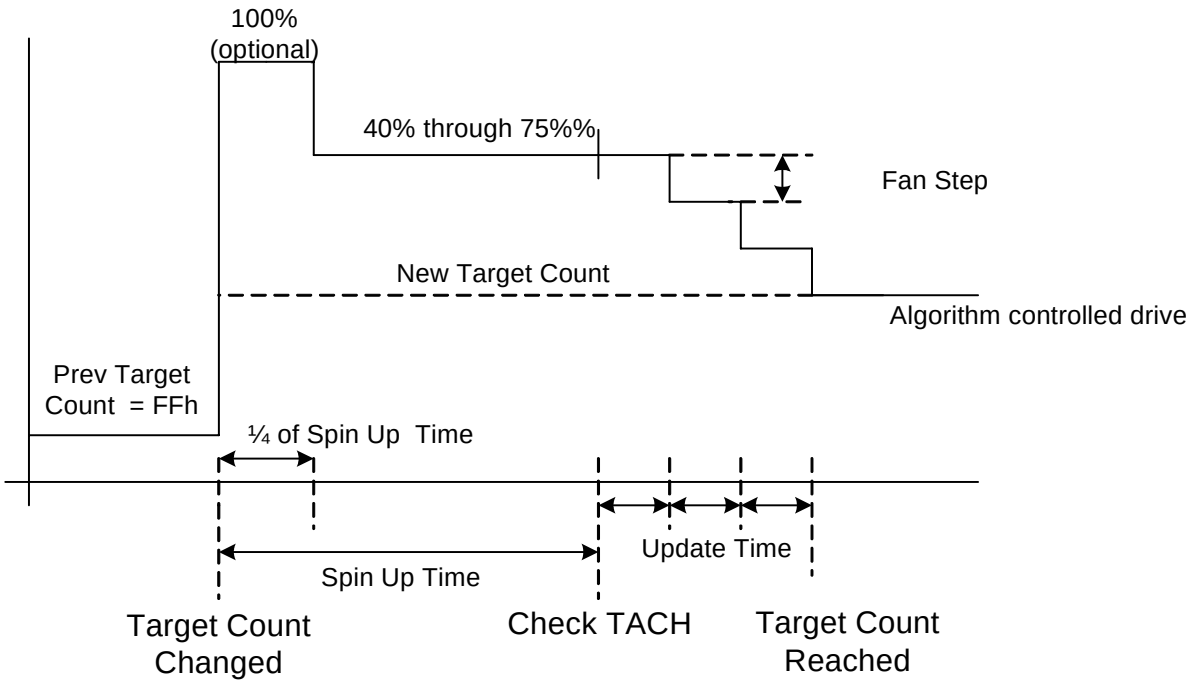


Figure 5.3 Spin Up Routine

5.3.4 FAN_MODE Pin

The FAN_MODE pin is used to determine the fan driver output levels at power-up before the EMC2102 has been programmed. After power-up, the fan driver will be set at the selected drive until the RPM based Fan Control Algorithm is started or disabled.

The level on the pin determines the function as shown in Table 5.2, "FAN_MODE Pin Functions".

Table 5.2 FAN_MODE Pin Functions

FAN_MODE	FUNCTION
0	Fan Driver set at 0% drive
open	Fan Driver set at 60% drive after Spin Up Routine
1	Fan Driver set at 75% drive after Spin Up Routine

5.3.5 32.768KHz Clock Source

The EMC2102 allows the user to choose between supplying an external 32.768KHz clock or use of the internal 32.768KHz oscillator to measure the TACH signal. This clock source is used by the RPM based Fan Control Algorithm to calculate the current fan speed. This fan controller accuracy is directly proportional to the accuracy of the clock source.

To enable the external clock source, the CLK_SEL pin must be pulled to VDD_3V at power-up (see Table 5.3). The CLK_SEL pin is must be in a known state at all times (either pulled high or pulled low) and is latched upon power-up.

Table 5.3 CLK_SEL Pin Functions

CLK_SEL	FUNCTION
0	Internal oscillator used
1	External clock used

5.4 Watchdog Timer

The EMC2102 contains an internal Watchdog Timer. Once the device has powered up the watchdog timer monitors the bus traffic for signs of activity. The Watchdog Timer starts when the VDD_5V supply has reached its operating point. The Watchdog Timer only starts immediately after power-up and once it has been triggered or deactivated will not restart.

If four (4) seconds elapse without the system host programming the device, then the following will occur:

1. The WATCH status bit will be set.
2. The High Side Fan Driver will be set to full scale drive. It will remain at full scale drive until one of the two conditions listed below are met.

If the Watchdog Timer is triggered, the following two operations will disable the timer and return the device to normal operation.

1. Writing the RPM based Fan Control Algorithm TACH Target Register will disable the Watchdog Timer regardless of the value. If a value is written that is greater than the Valid TACH Count Register setting (other than FFh), the fan drive setting will be set based on the FAN_MODE pin

condition (0%, 60% or 75% drive). If a value of FFh is written, then the fan driver will be disabled until a valid setting is written.

2. Disabling the RPM based Fan Control Algorithm by clearing the EN bit will disable the Watchdog Timer. The fan driver will be set to the programmed setting written in the Fan Driver Setting Register.

Writing any other configuration registers will not disable the Watchdog Timer. If the VDD_5V supply drops below the reset threshold, then the Watchdog Timer will be stopped but not reset.

5.5 High Side Fan Driver

The EMC2102's fan controller integrates a 5V, 600mA, linear high side fan driver to directly drive a 5V fan. By fully integrating the linear fan driver, the typical requirement for the discrete pass device and other external linearization circuitry is completely eliminated. The linear fan driver is driven by an 8-bit DAC providing better than 20mV resolution between steps.

5.5.1 Overcurrent Limit

The High Side Fan Driver contains circuitry to allow for significant overcurrent levels to accommodate transient conditions on the FAN pins. The overcurrent limit is dependent upon the output voltage with the limit dropping as the voltage nears 0V.

If the fan driver current detects a short-circuit condition for longer than 2 seconds, then the I_SHORT status bit is set and an interrupt generated. Additionally, the fan driver will be disabled (by setting the drive level to 00h).

In both Manual Mode and when using the RPM based Fan Control Algorithm, the device will attempt to restart the fan after a time equal to the spin-up time programmed in the Fan Spin Up Configuration Register (see Section 6.14, "Fan Spin Up Configuration Register"). If the High Side Fan Driver is configured to operate in Manual Mode, when it attempts to restart the fan after a overcurrent condition, it will set the Fan Drive Setting Register to the most recently written value (prior to the overcurrent condition). If the High Side Fan Driver is configured to use the RPM based Fan Control Algorithm, it will invoke the Spin Up Routine described in Section 5.3.3, "Spin Up Routine".

If the overcurrent condition persists, the fan driver will continue to attempt to restart the fan until the overcurrent condition is removed or the High Side Fan Driver is disabled by setting the TACH Target to FFh (when using the RPM based Fan Control Algorithm) or by writing the Fan Setting Register to a value of 00h (when operating in Manual Mode)

5.6 Internal Thermal Shutdown (TSD)

The EMC2102 contains an internal thermal shutdown circuit that monitors the internal die temperature. If the die temperature exceeds the Thermal Shutdown Threshold (see Table 3.2, "Electrical Specifications"), then the following will occur:

1. The High Side Fan Driver is disabled. It will remain disabled until the internal temperature drops below the threshold temperature minus 50°C.
2. The TSD Status bit will be set and the $\overline{\text{ALERT}}$ pin asserted. This signal cannot be masked.
3. The $\overline{\text{SYS_SHDN}}$ pin is asserted.

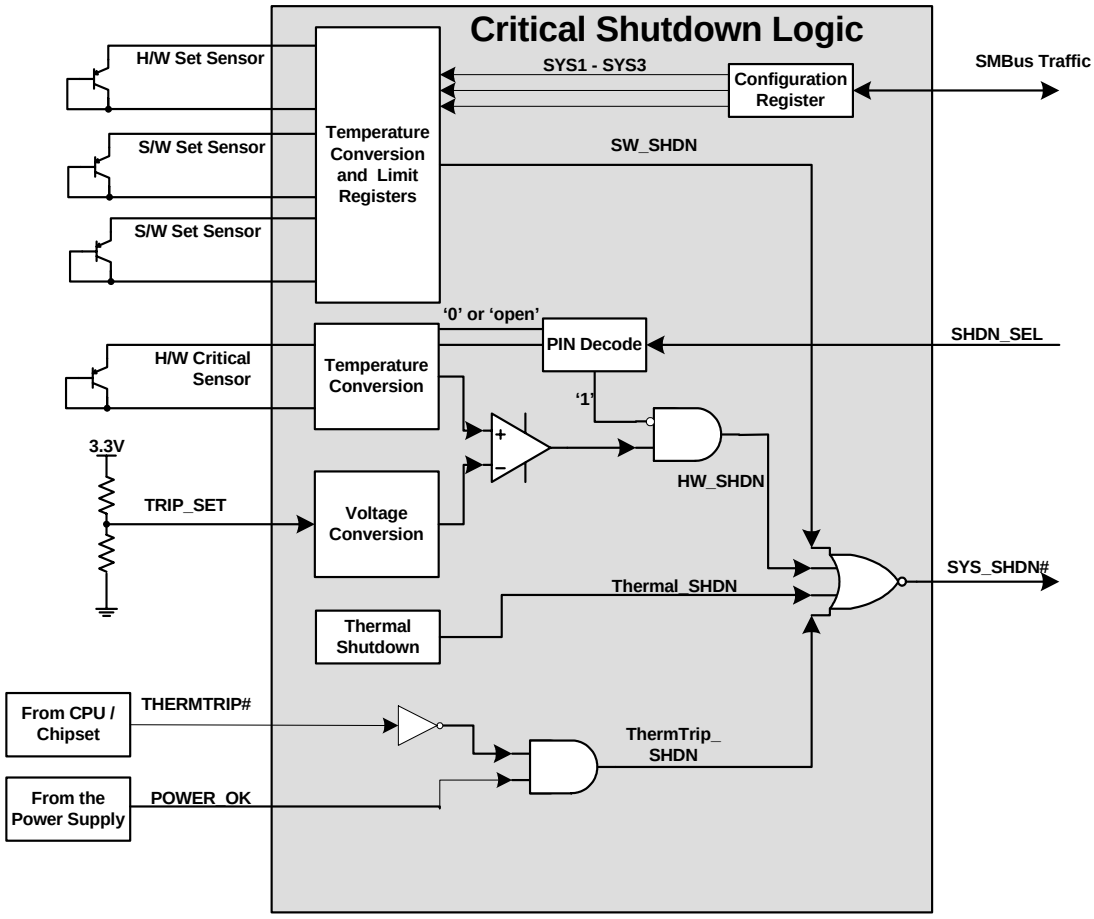
5.7 Critical/Thermal Shutdown

The EMC2102 provides a hardware Critical/Thermal Shutdown function for systems. Figure 5.4, "EMC2102 Critical/Thermal Shutdown Block Diagram" is a block diagram of this Critical/Thermal Shutdown function. The Critical/Thermal Shutdown function in the EMC2102 consists of both analog and digital functions. It accepts digital inputs from the CPU (THERMTRIP#) and power supply

(POWER_OK) and configuration information from the fixed states of the SHDN_SEL pins as described in Section 5.7.2, "SHDN_SEL Pin".

In addition, each of the temperature limits can be configured to act as inputs to the Critical / Thermal Shutdown independent of the hardware shutdown operation.

The analog portion of the Critical/Thermal Shutdown function monitors a specific remote temperature channel (configured with the SHDN_SEL pin). This measured temperature is then compared with the TRIP_SET point. This TRIP_SET point is created by the system designer with a simple resistor divider and is discussed in detail in Section 5.7.1, "TRIP_SET".



ThermTrip#	Power_OK	ThermTrip_SHDN
0	0	0
0	1	1
1	0	0
1	1	0

Figure 5.4 EMC2102 Critical/Thermal Shutdown Block Diagram

5.7.1 TRIP_SET

The EMC2102's TRIP_SET pin is an analog input to the Critical/Thermal Shutdown block which sets the Thermal Shutdown temperature. The system designer creates a voltage level at this input through a simple resistor divider between the 3.3V supply and GND. This input voltage is valid between 0V and 1.5V which corresponds to Thermal Shutdown temperature setpoints between 75°C and 106°C as described in the following equation.

$$TRIP_SET \text{ Pin Voltage} = \frac{T_{TRIP} - 75}{21} \quad \textbf{[1]}$$

Where:

T_{TRIP} is the desired trip point temperature

TRIPSET is the voltage on the TRIP_SET pin

5.7.2 SHDN_SEL Pin

The EMC2102 has one 'strappable' input (SHDN_SEL) allowing for configuration of the hardware Critical/Thermal Shutdown. This pin has 3 possible states and is monitored and decoded by the EMC2102 at power-up. The three possible states are 0 (tied to GND), 1 (tied to 3.3V) or High-Z (open). The states of this pin determine which remote temperature channel and configuration is used by the Critical/Thermal Shutdown function. The different configurations of SHDN_SEL pin are described in Table 5.4

A channel that is configured via the SHDN_SEL pin for the Critical/Thermal Shutdown is locked and none of the configuration registers associated with it can be updated via the SMBus. The other two temperature channels, however, are still configurable via the SMBus.

Table 5.4 SHDN_SEL Pin Configuration

SHDN_SEL	FUNCTION NAME	REMOTE CHANNEL INPUT TO THERMAL SHUTDOWN	CRITICAL/THERMAL SHUTDOWN DETAILS
0	Intel Mode	1	Channel 1 is configured and locked with both Beta Compensation and Resistance Error Correction enabled which is optimized for an Intel thermal diode.
High-Z	Diode Mode	3	Channel 3 is configured and locked with Resistance Error Correction enabled which is optimal for interfacing a discrete diode-connected NPN transistor.
1	Disabled,	NA	The Critical/Thermal Shutdown function will not assert SYS_SHDN# based on a temperature channel. This does not include software configured inputs (see Section 6.4, "Configuration Register")

5.7.3 Internal HW_SHDN Signal

The HW_SHDN output from the Critical/Thermal Shutdown Monitor is a logical indicator of the temperature state of the chosen external diode channel. HW_SHDN is an internal signal routed as an input to the Thermal / Critical Shutdown logic.

The HW_SHDN output is set to logic '1' when the indicated temperature exceeds the temperature threshold (T_P) established by the TRIP_SET input pin (as shown in Figure 5.5, "HW_SHDN Operation") for a number of consecutive measurements defined by the fault queue. If the HW_SHDN output is asserted and the temperature drops below T_P, then it will be set to a logic '0' state.

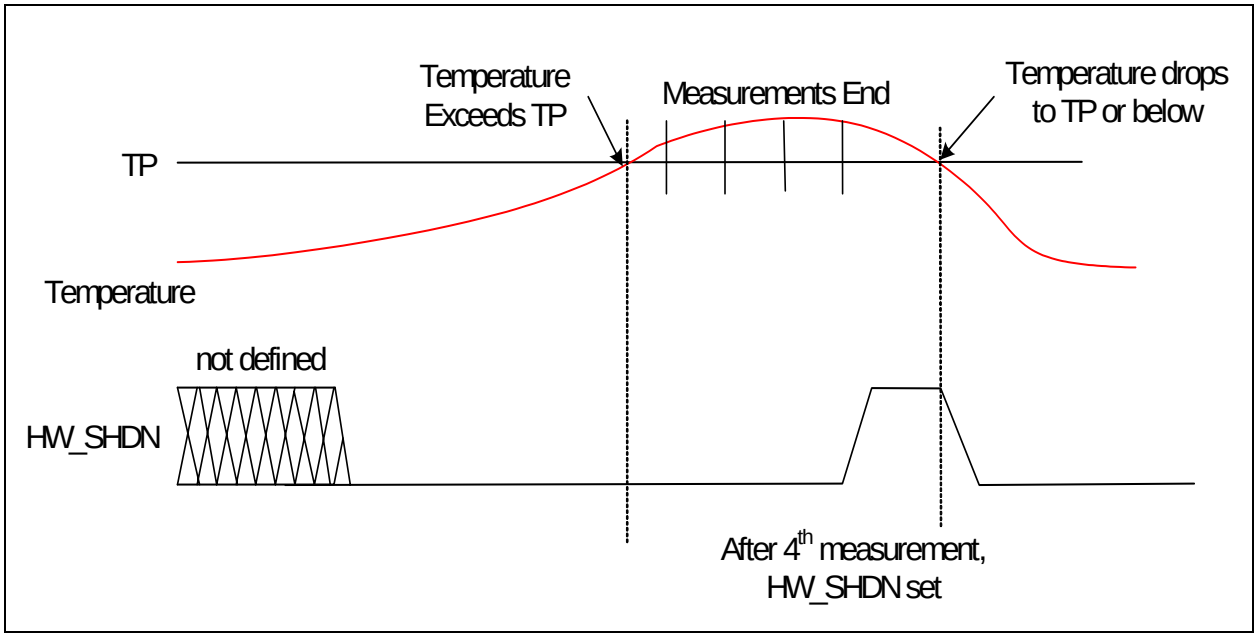


Figure 5.5 HW_SHDN Operation

5.8 5V Reset Controller

The EMC2102 also provides a ‘power-good’ reset controller for the system’s 5V supply rail. The reset controller will set the RESET# pin to a logic ‘0’ after power-up and set the RESET# pin to a logic ‘1’ 220ms after the VDD_5V supply rises above its threshold voltage (see Table 3.2, "Electrical Specifications").

If the VDD_5V supply drops below the reset threshold, then the RESET# pin will be set to ‘0’ immediately.

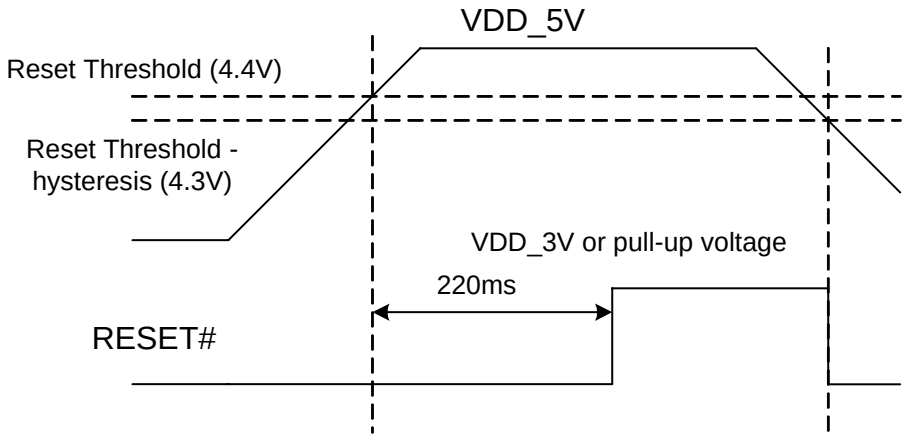


Figure 5.6 5V Reset Controller Timing

Chapter 6 Register Set

6.1 Register Map

The following registers are accessible through the SMBus Interface. All register bits marked as '-' will always read '0'. A write to these bits will have no effect.

Table 6.1 EMC2102 Register Set

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
Temperature Registers						
00h	R	Internal Temp Reading	Stores the integer data of the Internal Temp Reading	00h	No	Page 33
01h	R	External Diode 1 Temp Reading	Stores the integer data of External Diode 1	00h	No	Page 33
02h	R	External Diode 2 Temp Reading	Stores the integer data of External Diode 2	00h	No	
03h	R	External Diode 3 Temp Reading	Stores the integer data of External Diode 3	00h	No	
04h	R	Critical/Thermal Shutdown Temperature	Stores the calculated Critical/Thermal Shutdown temperature high limit derived from the voltage on TRIP_SET.	7Fh	No	Page 34
Configuration and control						
20h	R/W	Configuration	Configures the Thermal / Critical Shutdown masking options and software lock	80h	SWL	Page 34
21h	R/W	Conversion Rate	Configures the conversion rate	02h	SWL	Page 35
22h	R-C	Interrupt Status Register 1	Stores the status bits for temperature channels	80h	No	Page 36
23h	R-C	Interrupt Status Register 2	Stores the status bits for the thermal shutdown and RPM based Fan Control Algorithm	00h	No	Page 37
24h	R/W	Interrupt Mask Register	Controls the masking of interrupts on all maskable channels	10h	No	Page 37
Diode Configuration						
30h	R/W	External Diode 1 Beta Configuration	Configures the beta compensation settings for External Diode 1	03h	SWL	Page 38
31h	R/W	External Diode 2 Beta Configuration	Configures the beta compensation settings for External Diode 2	03h	SWL	
32h	R/W	External Diode REC Configuration	Configures the Resistance Error Correction functionality for all external diodes	07h	SWL	Page 39

Table 6.1 EMC2102 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
Temperature Limit Registers						
41h	R/W	External Diode 1 Temp High Limit	High limit for External Diode 1	55h (+85°C)	SWL	Page 40
42h	R/W	External Diode 2 Temp High Limit	High limit for External Diode 2	55h (+85°C)	SWL	
43h	R/W	External Diode 3 Temp High Limit	High limit for External Diode 3	55h (+85°C)	SWL	
Fan Control Registers						
51h	R/W	Fan Driver Setting	Always displays the most recent fan driver input setting. If the RPM based Fan Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	Page 40
52h	R/W	Fan Configuration	Sets configuration values for the RPM based Fan Control Algorithm	CBh	No	Page 41
53h	R/W	Fan Spin Up Configuration	Sets the configuration values for Spin Up Routine of the High Side Fan Driver	01h	SWL	Page 42
54h	R/W	Fan Step	Sets the maximum change per update for the High Side Fan Driver	10h	SWL	Page 43
55h	R/W	Fan Minimum Drive	Sets the minimum drive value for the High Side Fan Driver	80h	SWL	Page 43
56h	R/W	Fan Valid TACH Count	Holds the minimum TACH value that indicates the fan is spinning properly	F5h	SWL	Page 44
57h	R/W	TACH Target	Holds the target TACH count for the fan	FAh	No	Page 44
58h	R	TACH Reading	Holds the TACH count for the fan	FFh	No	Page 44
Revision Registers						
FDh	R	Product ID	Stores the unique Product ID	14h	No	Page 45
FFh	R	Revision	Revision	00h	No	Page 46

During Power-On-Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the VDD_3V supply surpasses the POR level as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

6.1.1 Lock Entries

The Lock Column describes the locking mechanism, if any, used for individual registers. All SWL registers are Software Locked and therefore made read-only when the LOCK bit is set.

6.2 Temperature Data Registers

Table 6.2 Temperature data Registers

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	Internal Diode	Sign	64	32	16	8	4	2	1	00h
01h	External Diode 1	Sign	64	32	16	8	4	2	1	00h
02h	External Diode 2	Sign	64	32	16	8	4	2	1	00h
03h	External Diode 3	Sign	64	32	16	8	4	2	1	00h

The temperature measurement range is from 0°C to +191°C. The data format can be selected between pure 2's complement format which displays data from 0°C to +127°C, or in offset 2's complement format that displays data over the entire data range. The temperature format is shown below:

Table 6.3 Temperature Data Format

TEMPERATURE (°C)	2'S COMPLEMENT FORMAT		OFFSET 2'S COMPLEMENT FORMAT	
	BINARY	HEX	BINARY	HEX
Diode Fault	1000 0000	80h	1000 0000	80h
<= 0	0000 0000	00h	1100 0000	C0h
1	0000 0001	01h	1100 0001	C1h
63	0011 1111	3Fh	1111 1111	FFh
64	0100 0000	40h	0000 0000	00h
65	0100 0001	41h	0000 0001	01h
127	0111 1111	7Fh	0011 1111	3Fh
128 (Note 6.1)	0111 1111	7Fh	0100 0000	40h
190	0111 1111	7Fh	0111 1110	7Eh
191	0111 1111	7Fh	0111 1111	7Fh

Note 6.1 In 2's complement format, any temperature above +127°C will be displayed as +127°C

If the High Side Fan Driver is active, then self-heating of the large current drive device will affect the internal temperature reading. Therefore, it is not recommended that the Internal temperature channel be used to monitor the ambient air temperature.

6.3 Critical/Thermal Shutdown Temperature Register

Table 6.4 Critical/Thermal Shutdown Temperature Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
04h	Critical/Thermal Shutdown Temperature	Sign	64	32	16	8	4	2	1	7Fh (+127°C)

The Critical/Thermal Shutdown Temperature Register is a read-only register that stores the Voltage Programmable Threshold temperature used in the Thermal / Critical Shutdown circuitry. The contents of the register reflect the calculated temperature based on the TRIP_SET voltage. This register is updated at the end of every monitoring cycle based on the current value of TRIP_SET. The register value reflects the exact threshold temperature.

The data format will match the selected format of the temperature data registers as shown in Table 6.3, "Temperature Data Format".

6.4 Configuration Register

Table 6.5 Configuration Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
20h	Configuration	QUEUE[1:0]		SYS3	SYS2	SYS1	FORMAT	-	LOCK	80h

The Configuration Register controls the basic functionality of the EMC2102. The bits are described below. The Configuration Register is software locked.

Bit 7-6 - QUEUE[1:0] - determines how many consecutive out-of-limit errors must occur on the hardware selected and software enabled temperature channels before the SYS_SHDN# pin is asserted (see Table 5.2, "FAN_MODE Pin Functions"). The queue applies to all enabled channels simultaneously and will trigger the SYS_SHDN# pin if there are four consecutive measurements with any or all channels exceeding their corresponding limits.

Table 6.6 Fault Queue

QUEUE1:0]		NUMBER OF FAULTS
1	0	
0	0	1
0	1	2
1	0	4 (default)
1	1	8

Bit 5 - SYS3 - enables the high temperature limit for the External Diode 3 channel to trigger the Critical / Thermal Shutdown circuitry (see Section 5.7, "Critical/Thermal Shutdown").

- '0' (default) - the External Diode 3 channel high limit will not be linked to the SYS_SHDN# pin. If the temperature exceeds the limit, the ALERT# pin will be asserted normally.

- '1' - the External Diode 3 channel high limit will be linked to the SYS_SHDN# pin. If the temperature exceeds the limit then the SYS_SHDN# pin will be asserted. The ALERT# pin will be asserted normally.

Bit 4 - SYS2 - enables the high temperature limit for the External Diode 2 channel to trigger the Critical / Thermal Shutdown circuitry (see Section 5.7, "Critical/Thermal Shutdown").

- '0' (default) - the External Diode 2 channel high limit will not be linked to the SYS_SHDN# pin. If the temperature exceeds the limit, the ALERT# pin will be asserted normally.
- '1' - the External Diode 2 channel high limit will be linked to the SYS_SHDN# pin. If the temperature exceeds the limit then the SYS_SHDN# pin will be asserted. The ALERT# pin will be asserted normally.

Bit 3 - SYS1 - enables the high temperature limit for the External Diode 1 channel to trigger the Critical / Thermal Shutdown circuitry (see Section 5.7).

- '0' (default) - the External Diode 1channel high limit will not be linked to the SYS_SHDN# pin. If the temperature exceeds the limit, the ALERT# pin will be asserted normally.
- '1' - the External Diode 1 channel high limit will be linked to the SYS_SHDN# pin. If the temperature exceeds the limit then the SYS_SHDN# pin will be asserted. The ALERT# pin will be asserted normally.

Bit 2 - FORMAT - determines the data format that is displayed in the Temperature Data Registers. The data format for the Critical Thermal Shutdown Threshold Register will not be changed. If the temperature data format is changed, the limit register values must be changed to match the newer format.

- '0' (default) - the temperature data will be in standard 2's complement format.
- '1' - the temperature data will be in offset 2's complement format.

Bit 0 - LOCK - this bit acts on all registers that are designated SWL. When this bit is set, the locked registers become read only and cannot be updated.

- '0' (default) - all SWL registers can be updated normally.
- '1' - all SWL registers cannot be updated and a hard-reset is required to unlock them.

6.5 Conversion Rate Register

Table 6.7 Conversion Rate Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
21h	Conversion Rate	-	-	-	-	-	-	CONV[1:0]		02h

The Conversion Rate Register controls the conversion rate of the temperature monitoring as well as the fault queue. The Conversion Rate Register is software locked.

Bit 1 - 0 - CONV[1:0] - determines the conversion rate of the temperature monitoring. This conversion rate does not affect the fan driver. The supply current from VDD_3V is nominally dependent upon the conversion rate and the average current will increase as the conversion rate increases.

Table 6.8 Conversion Rate

CONV[1:0]		CONVERSION RATE
1	**0**	
0	0	1 / sec
0	1	2 / sec
1	0	4 / sec (default)
1	1	8 / sec

6.6 Interrupt Status Register 1

Table 6.9 Interrupt Status Register 1

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
22h	Interrupt Status Register 1	RESET	TSD	ERR3	TRD3	ERR2	TRD2	ERR1	TRD1	80h

The Interrupt Status Registers report the operating condition of the EMC2102. If any of the bits are set to a logic ‘1’ (other than the RESET pin) then the ALERT# pin will be asserted low. Reading from the status register clears all status bits if the error conditions is removed. If there are no set status bits, then the ALERT# pin will be released.

The bits that cause the ALERT# pin to be asserted can be masked based on the channel they are associated with unless stated otherwise.

Bit 7 - RESET - this bit mirrors the output of the RESET# pin. When the RESET# pin is set to a logic ‘0’ (indicating that the VDD_5V supply is lower than the reset threshold), this bit is set to a logic ‘1’ as well. This bit will not cause the ALERT# pin to be asserted.

Bit 6 - TSD - this bit is asserted ‘1’ if there is a thermal shutdown condition. This bit cannot be masked.

Bit 5 - ERR3 - this bit is asserted ‘1’ if there is a diode fault on External Diode 3.

Bit 4 - TRD3 - this bit is asserted ‘1’ if the External Diode 3 Temperature measurement exceeds the high limit.

Bit 3 - ERR2 - this bit is asserted ‘1’ if there is a diode fault on External Diode 2.

Bit 2 - TRD2 - this bit is asserted ‘1’ if the External Diode 2 Temperature measurement exceeds the high limit.

Bit 1 - ERR1 - this bit is asserted ‘1’ if there is a diode fault on External Diode 1.

Bit 0 - TRD1 - this bit is asserted ‘1’ if the External Diode 1 Temperature measurement exceeds the high limit.

6.7 Interrupt Status Register 2

Table 6.10 Interrupt Status Register 2

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
23h	Interrupt Status Register 2	PWROK	THERM	HWS	-	WATCH	FAN_SPIN	FAN_STALL	I_SHORT	00h

The Interrupt Status Registers report the operating condition of the EMC2102. If any of the bits (except the PWROK, THERM, and HWS bits) are asserted then the ALERT# pin will be asserted low. Reading from the status register clears all status bits if the error conditions is removed. If there are no set status bits, then the ALERT# pin will be released.

Bit 7 - PWROK - this bit is set if the POWER_OK pin is set to a logic ‘1’ state. When this bit is set, it will not cause the ALERT# pin to be asserted.

Bit 6 - THERM - this bit is set if the THERMTRIP# pin is set to a logic ‘0’ state. When this bit is set, it will not cause the ALERT# pin to be asserted however will coincide with SYS_SHDN# pin being asserted. The THERMTRIP# pin can only cause the SYS_SHDN# pin to be asserted if the POWER_OK pin is set to a logic ‘1’ (see Figure 5.4, "EMC2102 Critical/Thermal Shutdown Block Diagram").

Bit 5 - HWS - this bit is set if the internal HW_SHDN signal is set (see Section 5.7.3, "Internal HW_SHDN Signal") based on the TRIP_SET voltage and the SHDN_SEL pin conditions. When this bit is set, it will not cause the ALERT# pin to be asserted however will coincide with SYS_SHDN# pin being asserted.

Bit 3 - WATCH - this bit is asserted ‘1’ if the Watchdog Timer circuit does not detect the fan being programmed within 4 seconds after power-up. This bit cannot be masked.

Bit 2 - FAN_SPIN - this bit is asserted ‘1’ if the Spin up Routine for Fan cannot detect a valid TACH within its maximum time window. This bit can be masked from asserting the ALERT# pin.

Bit 1 - FAN_STALL - this bit is asserted ‘1’ if the TACH measurement on fan detects a stalled fan. This bit can be masked from asserting the ALERT# pin.

Bit 0 - I_SHORT - this bit is asserted ‘1’ if the High Side Fan Driver circuit detects a short circuit condition. This bit cannot be masked.

6.8 Interrupt Mask Register

Table 6.11 Interrupt Mask Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
24h	Interrupt Mask	-	-	-	SPIN_MASK	STALL_MASK	EXT3_MSK	EXT2_MSK	EXT1_MSK	10h

The Interrupt Mask Register controls the masking for each temperature channel and the TACH monitor. When a channel is masked, it will not cause the ALERT# pin to be asserted when an error condition is detected.

Bit 4 - SPIN_MASK - masks the FAN_SPIN bit from asserting the ALERT# pin.

- ‘0’ - the FAN_SPIN bit will assert the ALERT# pin if set in the Interrupt Status Register 2.
- ‘1’ - (default) - the FAN_SPIN bit will not assert the ALERT# pin though will still update the Interrupt Status Register 2 normally.

Bit 3 - STALL_MASK - masks the FAN_STALL bit from asserting the ALERT# pin.

- '0' (default) - the FAN_STALL bit will assert the ALERT# pin if set in the Interrupt Status Register 2.
- '1' - the FAN_STALL bit will not assert the ALERT# pin though will still update the Interrupt Status Register 2 normally.

Bit 2 - EXT3_MASK - masks the ERR3 and TRD3 bits from asserting the ALERT# pin.

- '0' (default) - the ERR3 and TRD3 bits will assert the ALERT# pin if they are set in the Interrupt Status Register 1.
- '1' - the ERR3 and TRD3 bits will not assert the ALERT# pin though they will still update the Interrupt Status Register 1 normally.

Bit 1 - EXT2_MASK - masks the ERR2 and TRD2 bits from asserting the ALERT# pin.

- '0' (default) - the ERR2 and TRD2 bits will assert the ALERT# pin if they are set in the Interrupt Status Register 1.
- '1' - the ERR2 and TRD2 bits will not assert the ALERT# pin though they will still update the Interrupt Status Register 1 normally.

Bit 0 - EXT1_MASK - masks the ERR1 and TRD1 bits from asserting the ALERT# pin.

- '0' (default) - the ERR1 and TRD1 bits will assert the ALERT# pin if they are set in the Interrupt Status Register 1.
- '1' - the ERR1 and TRD1 bits will not assert the ALERT# pin though they will still update the Interrupt Status Register 1 normally.

6.9 Beta Configuration Registers

Table 6.12 Beta Configuration Registers

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
30h	External Diode 1 Beta Configuration	-	-	-	-	-	BETA1[2:0]			03h
31h	External Diode 2 Beta Configuration	-	-	-	-	-	BETA2[2:0]			03h

The Beta Configuration Registers control advanced temperature measurement features for each External Diode channel. The Beta Configuration Registers are software locked.

When the External Diode 1 Channel is selected by the SHDN_SEL pin to be the hardware shutdown input channel (see Table 5.4, "SHDN_SEL Pin Configuration"), the External Diode 1 Beta Configuration Register becomes read only. Writing to the register will have no affect and reading from it will always reflect the current beta settings (05h).

For the External Diode 3 Channel, the beta compensation setting is fixed at '111b' indicating that the beta compensation is disabled.

Bit 2 - 0 - BETAx[2:0] - hold a value that corresponds to a range of betas that the Beta Compensation circuitry can compensate for. The Beta Configuration Registers activate the Beta Compensation circuitry if any value besides 111 is written. The register should be set with a value corresponding to the lowest expected value of beta for the PNP transistor being used as a temperature sensing device.

See Figure 6.13, "Beta Compensation Look Up Table" for supported beta ranges. The default setting is calibrated for 65nm CPU's. For 90nm CPU's the optimal beta setting is 04h.

When the Beta Compensation circuitry is disabled, the diode channels will function with default current levels and will not automatically adjust for beta variation. This mode is used when measuring a discrete 2N3904 transistor or AMD thermal diode.

All of the Beta Configuration Registers are Software Locked.

Table 6.13 Beta Compensation Look Up Table

BETAX[2:0]			MINIMUM BETA
2	**1**	**0**	
0	0	0	0.1111
0	0	1	0.1765
0	1	0	0.25
0	1	1	0.333 (default)
1	0	0	0.4285
1	0	1	1.0
1	1	0	2.333
1	1	1	Disabled

6.10 REC Configuration Register

Table 6.14 REC Configuration Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
32h	REC Configuration	-	-	-	-	-	REC3	REC2	REC1	07h

The REC Configuration Register determines whether Resistance Error Correction is used for each external diode channel. The REC Configuration Register is software locked.

If either the External Diode 1 channel or External Diode 3 channel is selected by the SHDN_SEL pin to be the hardware shutdown input channel (see Table 5.4, "SHDN_SEL Pin Configuration"), then the corresponding RECx bit will be locked. Writing to the bit will have no affect and reading from it will always report the current setting.

Bit 2 - REC3 - Controls the Resistive Error Correction functionality of External Diode 3

- '0' - the REC functionality for External Diode 3 is disabled
- '1' (default) - the REC functionality for External Diode 3 is enabled.

Bit 1 - REC2 - Controls the Resistive Error Correction functionality of External Diode 1

- '0' - the REC functionality for External Diode 2 is disabled
- '1' (default) - the REC functionality for External Diode 2 is enabled.

Bit 0 - REC1 - Controls the Resistive Error Correction functionality of External Diode 1

- '0' - the REC functionality for External Diode 1 is disabled
- '1' (default) - the REC functionality for External Diode 1 is enabled.

6.11 Temperature Limit Registers

Table 6.15 Temperature Limit Registers

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
41h	External Diode 1 High Limit	Sign	64	32	16	8	4	2	1	55h (+85°C)
42h	External Diode 2 High Limit	Sign	64	32	16	8	4	2	1	55h (+85°C)
43h	External Diode 3 High Limit	Sign	64	32	16	8	4	2	1	55h (+85°C)

The EMC2102 contains high limits for all temperature channels.If any particular temperature channel exceeds the high limit then the appropriate status bit is set.

Each temperature channel software limit can be individually enabled to assert the SYS_SHDN# pin if the temperature exceeds this limit.

All Temperature Limit Registers are Software Locked.

6.12 Fan Driver Setting Register

Table 6.16 Fan Driver Setting Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
51h	Fan Driver Setting	128	64	32	16	8	4	2	1	00h

The Fan Driver Setting Register always displays the current setting of the High Side Fan Driver. If the RPM based Fan Control Algorithm is disabled, this register can be written to manually control the fan driver (manual mode). See Section 5.2, "Fan Control Modes of Operation".

If this register is written to while the RPM based Fan Control Algorithm is active, it will not affect the current output drive. The value that is written will be retained however and used as the current drive if the RPM based Fan Control algorithm is disabled.

Reading from this register will report the current fan speed setting regardless of the operating mode. Therefore it is possible that reading from this register will not report data that was previously written into this register.

The contents of the register represent the weighting of each bit in determining the final output voltage. The output voltage is given by Equation [2].

$$FAN_OUT = \left(\frac{VALUE}{255}\right) \times VDD_5V \quad \textbf{[2]}$$

6.13 Fan Configuration Register

Table 6.17 Fan Control Configuration Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
52h	FAN Configuration	EN	LIMIT2K	-	EDGES[1:0]		UPDATE[2:0]			CBh

The Fan Configuration Register controls the general operation of the RPM based Fan Control Algorithm used for the High Side Fan Driver.

Bit 7 - EN - enables the RPM based Fan Control Algorithm.

- '0' - the control circuitry is disabled and the fan driver output is determined by the Fan Driver Setting Register.
- '1' (default) - the control circuitry is enabled and the Fan Driver output will be automatically updated to maintain the programmed fan speed as indicated by the TACH Target Register.

Bit 6 - LIMIT2K - Adjusts the range of reported and programmed TACH count values.

- '0' - the range of reported and programmable TACH values allows for a minimum speed of approximately 500 RPM with reduced resolution to report lower speed values. The TACH Reading count value is multiplied by a value of factor of '1x'.
- '1' (default) - the range of reported and programmable TACH values allows for a minimum speed of approximately 2000 RPM with increased resolution to report higher speed values. he TACH Reading count value is multiplied by a value of factor of '4x'.

Bit 4-3 - EDGES[1:0] - determines the minimum number of edges that must be detected on the TACH signal to determine a single rotation. A typical fan measured 5 edges (for a 2-pole fan). For more accurate TACH measurement, the minimum number of poles may be increased, however the TACH measurement will be artificially higher than expected as denoted in the Effective TACH multiplier. Additionally, some fans have more than 2-poles and therefore require more edges to be measured as shown in the Number of Fan Poles

The EDGES[1:0] bits are shown in Table 6.18, "Minimum Edges for Fan Rotation".

Table 6.18 Minimum Edges for Fan Rotation

EDGES[1:0]		MINIMUM TACH EDGES	NUMBER OF FAN POLES	EFFECTIVE TACH MULTIPLIER (BASED ON 2 POLE FANS)
1	0			
0	0	3	1 pole	0.5
0	1	5	2 poles (default)	2
1	0	7	3 poles	1.5
1	1	9	4 poles	2

Bit 2-0 - UPDATE - determines the base time between fan driver updates. The Update Time, along with the Fan Step Register, is used to control the ramp rate of the drive response to provide a cleaner transition of the actual fan operation as the desired fan speed changes. The Update Time is set as shown in Table 6.19, "Update Time".

Table 6.19 Update Time

UPDATE[2:0]			UPDATE TIME
2	**1**	**0**	
0	0	0	100ms
0	0	1	200ms
0	1	0	300ms
0	1	1	400ms (default)
1	0	0	500ms
1	0	1	800ms
1	1	0	1200ms
1	1	1	1600ms

6.14 Fan Spin Up Configuration Register

Table 6.20 Fan TACH Configuration Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
53h	Fan Spin Up Configuration	-	-	-	-	-	LEVEL	SPINUP_TIME [1:0]		01h

The Fan Spin Up Configuration Register controls the settings of Spin Up Routine used by the RPM based Fan Control Algorithm. The Fan Spin Up Configuration Register is software locked.

Bit 2 - LEVEL - determines the spin up level that is used whenever the Spin Up Routine is initiated after power-up

- '0' (default) - the spin up level will be 60% of full scale.
- '1' - the spin up level will be 75% of full scale.

Bit 1 -0 - SPINUP_TIME[2:0] - determines the maximum Spin Time that the Spin Up Routine will run for (see Section 5.3.3, "Spin Up Routine"). If a valid TACH is not detected before the Spin Time has elapsed, then an interrupt will be generated. When the RPM based Fan Control Algorithm is active, the fan driver will attempt to re-start the fan immediately after the end of the last spin up attempt.

The Spin Time is set as shown in Table 6.21, "Spin Time".

Table 6.21 Spin Time

SPINUP_TIME[1:0]		TOTAL SPIN UP TIME
1	**0**	
0	0	250 ms
0	1	500 ms (default)

Table 6.21 Spin Time (continued)

SPINUP_TIME[1:0]		TOTAL SPIN UP TIME
1	**0**	
1	0	1 sec
1	1	2 sec

6.15 Fan Step Register

Table 6.22 Fan Step Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
54h	Fan Step	-	-	32	16	8	4	2	1	10h

The Fan Step Register, along with the Update Time, controls the ramp rate of the fan driver response calculated by the RPM based Fan Control Algorithm. The value of the register represents the maximum step size the fan driver will take between update times (see Section 6.13, "Fan Configuration Register").

The Fan Step Register setting can be translated to a maximum voltage step as shown in Equation [2].

If the necessary fan driver delta is larger than the Fan Step, it will be capped at the Fan Step setting and updated every Update Time ms.

The Fan Step Register is software locked.

6.16 Fan Minimum Drive Register

Table 6.23 Minimum Fan Drive Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
55h	Fan Minimum Drive	128	64	32	16	8	4	2	1	80h

The Fan Minimum Drive Register stores the minimum drive setting for the RPM based Fan Control Algorithm. The RPM based Fan Control Algorithm will not drive the fan at a level lower than the minimum drive unless the target Fan Speed is set at FFh (see Section 6.18, "TACH Target Register")

During normal operation, if the fan stops for any reason (including low drive), the RPM based Fan Control Algorithm will attempt to restart the fan. Setting the Fan Minimum Drive Registers to a setting that will maintain fan operation is a useful way to avoid potential fan oscillations as the control circuitry attempts to drive it at a level that cannot support fan operation.

The Fan Minimum Drive Register is software locked.

6.17 Valid TACH Count Register

Table 6.24 Valid TACH Count Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
56h	Valid TACH Count	2048	1024	512	256	128	64	32	16	F5h

The Valid TACH Count Register stores the maximum TACH count to indicate that the fan is spinning properly. The value is referenced at the end of the Spin Up Routine to determine if the fan has started operating and decide if the device needs to retry. See Equation [4] for translating the count to an RPM.

If the TACH count exceeds the Valid TACH Count Register (indicating that the Fan RPM is below the threshold set by this count), then a stalled fan is detected. In this condition, the algorithm will automatically begin its Spin Up Routine.

If a TACH Target Count is set above the Valid TACH Count setting, then that setting will be ignored and the algorithm will use the current fan drive setting.

The Valid TACH Count Register is software locked.

6.18 TACH Target Register

Table 6.25 TACH Reading Registers

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
57h	TACH Target	2048	1024	512	256	128	64	32	16	FAh

The TACH Target Register holds the target TACH count that is maintained by the RPM based Fan Control Algorithm.

If the algorithm is enabled, setting the Fan Target to FFh will immediately disable the High Side Fan Driver. Setting the Fan Target to any other value will cause the algorithm to invoke the Spin Up Routine after which it will function normally.

6.19 TACH Reading Register

Table 6.26 TACH Reading Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
58h	Fan TACH	2048	1024	512	256	128	64	32	16	FFh

The TACH Reading Register contents describe the current TACH setting of the fan. The data represents the fan speed as the number of 32.768kHz clock periods that occur for a single revolution of the fan.

Equation [3] shows the detailed conversion from TACH measurement (COUNT) to RPM while Equation [4] shows the simplified translation of TACH Reading Register count to RPM assuming a 2-pole fan, measuring 5 edges, with a frequency of 32.768kHz.

$$RPM = \frac{1}{(2 \times poles)} \times \frac{(n-1)}{COUNT \times \frac{1}{m}} \times \frac{1}{period} \times 1e6 \times 60 \times \frac{1}{y} \quad \textbf{[3]}$$

where:

poles = number of poles of the fan (typically 2)

period = period of oscillation (30.5175us is the period for a 32.768khz clock)

n = number of edges measured (typically 5)

m = TACH multiplier term set by LIMIT2K
'0' = 1
'1' = 4

y = Scaling factor set by EDGES[1:0] bits

$$RPM = \frac{1{,}966{,}080 \times m}{COUNT} \quad \textbf{[4]}$$

COUNT = TACH Reading Register value (in decimal)

Table 6.27 Example TACH Reading for Specific Fan Speeds

TACH READING REGISTER	LIMIT2K	RPM
F6h	0	500
FFh (Note 6.2)	1	1920
3Dh	0	2000
F5h	1	2000
0Fh	0	8000
3Dh	1	8000
07h	0	16000
1Eh	1	16000

Note 6.2 If the LIMIT2K bit is set, the minimum fan speed that can be measured is approximately 1920RPM. Any fan speed lower than this value will be reported as FFh.

6.20 Product ID Register

Table 6.28 Product ID Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	Product ID Register (EMC2102-1)	0	0	0	1	0	1	0	0	14h

The Product ID Register contains a unique 8 bit word that identifies the product.

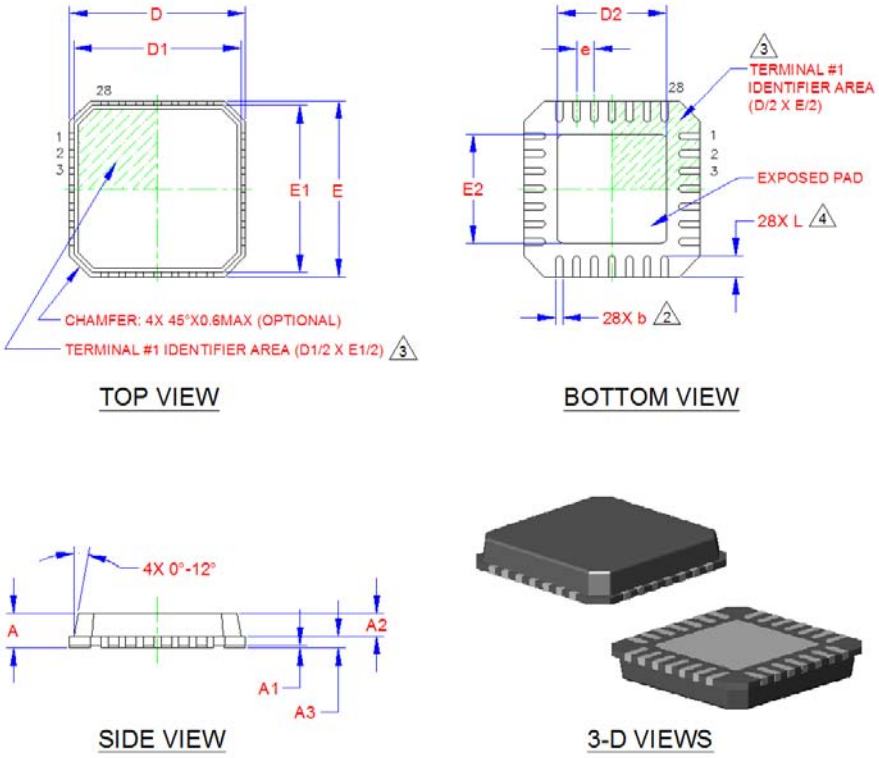
6.21 Revision Register

Table 6.29 Revision Register

ADDRESS	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	Revision	0	0	0	0	0	0	0	0	00h

The Revision Register contains a 8 bit word that identifies the die revision.

Chapter 7 Package Drawing



COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	-	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	0.60	-	0.80	-	MOLD CAP THICKNESS
A3	0.20			-	LEADFRAME THICKNESS
D/E	4.85	5.00	5.15	-	X/Y BODY SIZE
D1/E1	4.55	-	4.95	-	X/Y MOLD CAP SIZE
D2/E2	SEE VARIATIONS			2	X/Y EXPOSED PAD SIZE
L	0.50	-	0.75	4	TERMINAL LENGTH
b	0.18	-	0.30	2	TERMINAL WIDTH
e	0.50 BSC			-	TERMINAL PITCH

D2/E2 VARIATIONS				
MIN	NOM	MAX	NOTE	CATALOG PART #
2.95	3.10	3.25	2	EMC2102

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.
4. ROUNDED INNER TIPS ON TERMINALS ARE OPTIONAL.

Figure 7.1 EMC2102 28-Pin 5x5mm QFN Package Outline and Parameters

Appendix A TACH Reading Table - 2000 RPM Range

Table 7.1 TACH Count to RPM (2k Range)

DEC	REGISTER READING HEX	RPM
16	01h	491520
32	02h	245760
48	03h	163840
64	04h	122880
80	05h	98304
96	06h	81920
112	07h	70217
128	08h	61440
144	09h	54613
160	0Ah	49152
176	0Bh	44684
192	0Ch	40960
208	0Dh	37809
224	0Eh	35109
240	0Fh	32768
256	10h	30720
272	11h	28913
288	12h	27307
304	13h	25869
320	14h	24576
336	15h	23406
352	16h	22342
368	17h	21370
384	18h	20480
400	19h	19661
416	1Ah	18905
432	1Bh	18204
448	1Ch	17554
464	1Dh	16949

Table 7.1 TACH Count to RPM (2k Range) (continued)

DEC	REGISTER READING HEX	RPM
480	1Eh	16384
496	1Fh	15855
512	20h	15360
528	21h	14895
544	22h	14456
560	23h	14043
576	24h	13653
592	25h	13284
608	26h	12935
624	27h	12603
640	28h	12288
656	29h	11988
672	2Ah	11703
688	2Bh	11431
704	2Ch	11171
720	2Dh	10923
736	2Eh	10685
752	2Fh	10458
768	30h	10240
784	31h	10031
800	32h	9830
816	33h	9638
832	34h	9452
848	35h	9274
864	36h	9102
880	37h	8937
896	38h	8777
912	39h	8623
928	3Ah	8474
944	3Bh	8331

Table 7.1 TACH Count to RPM (2k Range) (continued)

DEC	REGISTER READING HEX	RPM
960	3Ch	8192
976	3Dh	8058
992	3Eh	7928
1008	3Fh	7802
1024	40h	7680
1040	41h	7562
1056	42h	7447
1072	43h	7336
1088	44h	7228
1104	45h	7123
1120	46h	7022
1136	47h	6923
1152	48h	6827
1168	49h	6733
1184	4Ah	6642
1200	4Bh	6554
1216	4Ch	6467
1232	4Dh	6383
1248	4Eh	6302
1264	4Fh	6222
1280	50h	6144
1296	51h	6068
1312	52h	5994
1328	53h	5922
1344	54h	5851
1360	55h	5783
1376	56h	5715
1392	57h	5650
1408	58h	5585
1424	59h	5523

Table 7.1 TACH Count to RPM (2k Range) (continued)

DEC	REGISTER READING HEX	RPM
1440	5Ah	5461
1456	5Bh	5401
1472	5Ch	5343
1488	5Dh	5285
1504	5Eh	5229
1520	5Fh	5174
1536	60h	5120
1552	61h	5067
1568	62h	5016
1584	63h	4965
1600	64h	4915
1616	65h	4867
1632	66h	4819
1648	67h	4772
1664	68h	4726
1680	69h	4681
1696	6Ah	4637
1712	6Bh	4594
1728	6Ch	4551
1744	6Dh	4509
1760	6Eg	4468
1776	6Fh	4428
1792	70	4389
1808	71h	4350
1824	72h	4312
1840	73h	4274
1856	74h	4237
1872	75h	4201
1888	76h	4165
1904	77h	4130
1920	78h	4096

Table 7.1 TACH Count to RPM (2k Range) (continued)

DEC	REGISTER READING HEX	RPM
1936	79h	4062
1952	7Ah	4029
1968	7Bh	3996
1984	7Ch	3964
2000	7Dh	3932
2016	7Eh	3901
2032	7Fh	3870
2048	80h	3840
2064	81h	3810
2080	82h	3781
2096	83h	3752
2112	84h	3724
2128	85h	3696
2144	86h	3668
2160	87h	3641
2176	88h	3614
2192	89h	3588
2208	8Ah	3562
2224	8Bh	3536
2240	8Ch	3511
2256	8Dh	3486
2272	8Eh	3461
2288	8Fh	3437
2304	90h	3413
2320	91h	3390
2336	92h	3367
2352	93h	3344
2368	94h	3321
2384	95h	3299
2400	96h	3277
2416	97h	3255

Table 7.1 TACH Count to RPM (2k Range) (continued)

DEC	REGISTER READING HEX	RPM
2432	98h	3234
2448	99h	3213
2464	9Ah	3192
2480	9Bh	3171
2496	9Ch	3151
2512	9Dh	3131
2528	9Eh	3111
2544	9Fh	3091
2560	A0h	3072
2576	A1h	3053
2592	A2h	3034
2608	A3h	3015
2624	A4h	2997
2640	A5h	2979
2656	A6h	2961
2672	A7h	2943
2688	A8h	2926
2704	A9h	2908
2720	AAh	2891
2736	ABh	2874
2752	ACh	2858
2768	ADh	2841
2784	AEh	2825
2800	AFh	2809
2816	B0h	2793
2832	B1h	2777
2848	B2h	2761
2864	B3h	2746
2880	B4h	2731
2896	B5h	2716
2912	B6h	2701

Table 7.1 TACH Count to RPM (2k Range) (continued)

DEC	REGISTER READING HEX	RPM
2928	B7h	2686
2944	B8h	2671
2960	B9h	2657
2976	BAh	2643
2992	BBh	2628
3008	BCh	2614
3024	BDh	2601
3040	BEh	2587
3056	BFh	2573
3072	C0h	2560
3088	C1h	2547
3104	C2h	2534
3120	C3h	2521
3136	C4h	2508
3152	C5h	2495
3168	C6h	2482
3184	C7h	2470
3200	C8h	2458
3216	C9h	2445
3232	CAh	2433
3248	CBh	2421
3264	CCh	2409
3280	CDh	2398
3296	CEh	2386
3312	CFh	2374
3328	D0h	2363
3344	D1h	2352
3360	D2h	2341
3376	D3h	2329
3392	D4h	2318
3408	D5h	2308

Table 7.1 TACH Count to RPM (2k Range) (continued)

DEC	REGISTER READING HEX	RPM
3424	D6h	2297
3440	D7h	2286
3456	D8h	2276
3472	D9h	2265
3488	DAh	2255
3504	DBh	2244
3520	DCh	2234
3536	DDh	2224
3552	DEh	2214
3568	DFh	2204
3584	E0h	2194
3600	E1h	2185
3616	E2h	2175
3632	E3h	2165
3648	E4h	2156
3664	E5h	2146
3680	E6h	2137
3696	E7h	2128
3712	E8h	2119
3728	E9h	2110
3744	EAh	2101
3760	EBh	2092
3776	ECh	2083
3792	EDh	2074
3808	EEh	2065
3824	EFh	2057
3840	F0h	2048
3856	F1h	2040
3872	F2h	2031
3888	F3h	2023
3904	F4h	2014

Table 7.1 TACH Count to RPM (2k Range) (continued)

DEC	REGISTER READING HEX	RPM
3920	F5h	2006
3936	F6h	1998
3952	F7h	1990
3968	F8h	1982
3984	F9h	1974
4000	FAh	1966
4016	FBh	1958
4032	FCh	1950
4048	FDh	1943
4064	FEh	1935
4080	FFh	1928

Appendix B TACH Reading Table - 500RPM Range

Table 7.2 TACH Count to RPM (500 Range)

DEC	REGISTER READING HEX	RPM
16	01h	122880
32	02h	61440
48	03h	40960
64	04h	30720
80	05h	24576
96	06h	20480
112	07h	17554
128	08h	15360
144	09h	13653
160	0Ah	12288
176	0Bh	11171
192	0Ch	10240
208	0Dh	9452
224	0Eh	8777
240	0Fh	8192
256	10h	7680
272	11h	7228
288	12h	6827
304	13h	6467
320	14h	6144
336	15h	5851
352	16h	5585
368	17h	5343
384	18h	5120
400	19h	4915
416	1Ah	4726
432	1Bh	4551
448	1Ch	4389

Table 7.2 TACH Count to RPM (500 Range) (continued)

DEC	REGISTER READING HEX	RPM
464	1Dh	4237
480	1Eh	4096
496	1Fh	3964
512	20h	3840
528	21h	3724
544	22h	3614
560	23h	3511
576	24h	3413
592	25h	3321
608	26h	3234
624	27h	3151
640	28h	3072
656	29h	2997
672	2Ah	2926
688	2Bh	2858
704	2Ch	2793
720	2Dh	2731
736	2Eh	2671
752	2Fh	2614
768	30h	2560
784	31h	2508
800	32h	2458
816	33h	2409
832	34h	2363
848	35h	2318
864	36h	2276
880	37h	2234
896	38h	2194
912	39h	2156

Table 7.2 TACH Count to RPM (500 Range) (continued)

DEC	REGISTER READING HEX	RPM
928	3Ah	2119
944	3Bh	2083
960	3Ch	2048
976	3Dh	2014
992	3Eh	1982
1008	3Fh	1950
1024	40h	1920
1040	41h	1890
1056	42h	1862
1072	43h	1834
1088	44h	1807
1104	45h	1781
1120	46h	1755
1136	47h	1731
1152	48h	1707
1168	49h	1683
1184	4Ah	1661
1200	4Bh	1638
1216	4Ch	1617
1232	4Dh	1596
1248	4Eh	1575
1264	4Fh	1555
1280	50h	1536
1296	51h	1517
1312	52h	1499
1328	53h	1480
1344	54h	1463
1360	55h	1446
1376	56h	1429

Table 7.2 TACH Count to RPM (500 Range) (continued)

DEC	REGISTER READING HEX	RPM
1392	57h	1412
1408	58h	1396
1424	59h	1381
1440	5Ah	1365
1456	5Bh	1350
1472	5Ch	1336
1488	5Dh	1321
1504	5Eh	1307
1520	5Fh	1293
1536	60h	1280
1552	61h	1267
1568	62h	1254
1584	63h	1241
1600	64h	1229
1616	65h	1217
1632	66h	1205
1648	67h	1193
1664	68h	1182
1680	69h	1170
1696	6Ah	1159
1712	6Bh	1148
1728	6Ch	1138
1744	6Dh	1127
1760	6Eg	1117
1776	6Fh	1107
1792	70	1097
1808	71h	1087
1824	72h	1078
1840	73h	1069
1856	74h	1059
1872	75h	1050

Table 7.2 TACH Count to RPM (500 Range) (continued)

DEC	REGISTER READING HEX	RPM
1888	76h	1041
1904	77h	1033
1920	78h	1024
1936	79h	1016
1952	7Ah	1007
1968	7Bh	999
1984	7Ch	991
2000	7Dh	983
2016	7Eh	975
2032	7Fh	968
2048	80h	960
2064	81h	953
2080	82h	945
2096	83h	938
2112	84h	931
2128	85h	924
2144	86h	917
2160	87h	910
2176	88h	904
2192	89h	897
2208	8Ah	890
2224	8Bh	884
2240	8Ch	878
2256	8Dh	871
2272	8Eh	865
2288	8Fh	859
2304	90h	853
2320	91h	847
2336	92h	842
2352	93h	836
2368	94h	830

Table 7.2 TACH Count to RPM (500 Range) (continued)

DEC	REGISTER READING HEX	RPM
2384	95h	825
2400	96h	819
2416	97h	814
2432	98h	808
2448	99h	803
2464	9Ah	798
2480	9Bh	793
2496	9Ch	788
2512	9Dh	783
2528	9Eh	778
2544	9Fh	773
2560	A0h	768
2576	A1h	763
2592	A2h	759
2608	A3h	754
2624	A4h	749
2640	A5h	745
2656	A6h	740
2672	A7h	736
2688	A8h	731
2704	A9h	727
2720	AAh	723
2736	ABh	719
2752	ACh	714
2768	ADh	710
2784	AEh	706
2800	AFh	702
2816	B0h	698
2832	B1h	694
2848	B2h	690
2864	B3h	686

Table 7.2 TACH Count to RPM (500 Range) (continued)

DEC	REGISTER READING HEX	RPM
2880	B4h	683
2896	B5h	679
2912	B6h	675
2928	B7h	671
2944	B8h	668
2960	B9h	664
2976	BAh	661
2992	BBh	657
3008	BCh	654
3024	BDh	650
3040	BEh	647
3056	BFh	643
3072	C0h	640
3088	C1h	637
3104	C2h	633
3120	C3h	630
3136	C4h	627
3152	C5h	624
3168	C6h	621
3184	C7h	617
3200	C8h	614
3216	C9h	611
3232	CAh	608
3248	CBh	605
3264	CCh	602
3280	CDh	599
3296	CEh	597
3312	CFh	594
3328	D0h	591
3344	D1h	588
3360	D2h	585

Table 7.2 TACH Count to RPM (500 Range) (continued)

DEC	REGISTER READING HEX	RPM
3376	D3h	582
3392	D4h	580
3408	D5h	577
3424	D6h	574
3440	D7h	572
3456	D8h	569
3472	D9h	566
3488	DAh	564
3504	DBh	561
3520	DCh	559
3536	DDh	556
3552	DEh	554
3568	DFh	551
3584	E0h	549
3600	E1h	546
3616	E2h	544
3632	E3h	541
3648	E4h	539
3664	E5h	537
3680	E6h	534
3696	E7h	532
3712	E8h	530
3728	E9h	527
3744	EAh	525
3760	EBh	523
3776	ECh	521
3792	EDh	518
3808	EEh	516
3824	EFh	514
3840	F0h	512
3856	F1h	510

Table 7.2 TACH Count to RPM (500 Range) (continued)

DEC	REGISTER READING HEX	RPM
3872	F2h	508
3888	F3h	506
3904	F4h	504
3920	F5h	502
3936	F6h	500
3952	F7h	497
3968	F8h	495
3984	F9h	493
4000	FAh	492
4016	FBh	490
4032	FCh	488
4048	FDh	486
4064	FEh	484
4080	FFh	482

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