



**THE DATASHEET OF  
EL8102ISZ**



EL8102, EL8103

500MHz Rail-to-Rail Amplifiers

OBSOLETE PRODUCT  
POSSIBLE SUBSTITUTE PRODUCT  
EL8100 AND EL8101

FN7104  
Rev 7.00  
August 10, 2007

The EL8102, EL8103 represent single rail-to-rail amplifiers with a -3dB bandwidth of 500MHz and slew rate of 600V/ $\mu$ s. Running off a very low 5.6mA supply current, the EL8102, EL8103 also feature inputs that go to 0.15V below the  $V_{S-}$  rail.

The EL8102 includes a fast-acting disable/power-down circuit. With a 25ns disable and a 200ns enable, the EL8102 is ideal for multiplexing applications.

The EL8102, EL8103 are designed for a number of general purpose video, communication, instrumentation, and industrial applications. The EL8102 is available in 8 Ld SOIC and 6 Ld SOT-23 packages and the EL8103 is available in a 5 Ld SOT-23 package. All are specified for operation over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
EL8102IS	8102IS	8 Ld SOIC	MDP0027
EL8102IS-T7	8102IS	8 Ld SOIC	MDP0027
EL8102IS-T13	8102IS	8 Ld SOIC	MDP0027
EL8102ISZ (Note)	8102ISZ	8 Ld SOIC (Pb-free)	MDP0027
EL8102ISZ-T7 (Note)	8102ISZ	8 Ld SOIC (Pb-free)	MDP0027
EL8102ISZ-T13 (Note)	8102ISZ	8 Ld SOIC (Pb-free)	MDP0027
EL8102IW-T7	4	6 Ld SOT-23	MDP0038
EL8102IW-T7A	4	6 Ld SOT-23	MDP0038
EL8102IWZ-T7 (Note)	BAVA	6 Ld SOT-23 (Pb-free)	MDP0038
EL8102IWZ-T7A (Note)	BAVA	6 Ld SOT-23 (Pb-free)	MDP0038
EL8103IW-T7	5	5 Ld SOT-23	MDP0038
EL8103IW-T7A	5	5 Ld SOT-23	MDP0038
EL8103IWZ-T7 (Note)	BAWA	5 Ld SOT-23 (Pb-free)	MDP0038
EL8103IWZ-T7A (Note)	BAWA	5 Ld SOT-23 (Pb-free)	MDP0038

\*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

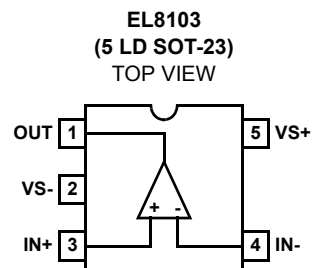
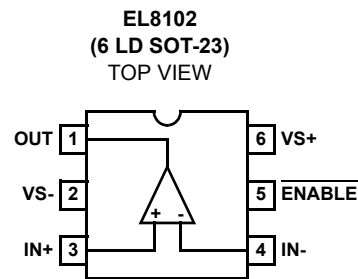
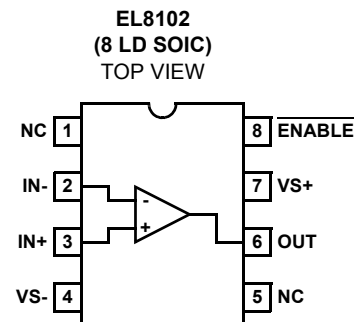
Features

- 500MHz -3dB bandwidth
- 600V/ $\mu$ s slew rate
- Low supply current = 5.6mA
- Supplies from 3V to 5.0V
- Rail-to-rail output
- Input to 0.15V below  $V_{S-}$
- Fast 25ns disable (EL8102 only)
- Low cost
- Pb-Free available (RoHS compliant)

Applications

- Video amplifiers
- Portable/hand-held products
- Communications devices

Pinouts



**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

Supply Voltage from $V_{S+}$ to $V_{S-}$ .....	5.5V
Input Voltage .....	$V_{S+} + 0.3\text{V}$ to $V_{S-} - 0.3\text{V}$
Differential Input Voltage .....	.2V
Continuous Output Current .....	40mA

**Thermal Information**

Power Dissipation .....	See Curves
Storage Temperature .....	$-65^\circ\text{C}$ to $+125^\circ\text{C}$
Ambient Operating Temperature .....	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Operating Junction Temperature .....	$+125^\circ\text{C}$
Pb-free reflow profile .....	see link below
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**Electrical Specifications**  $V_{S+} = 5\text{V}$ ,  $V_{S-} = \text{GND}$ ,  $T_A = +25^\circ\text{C}$ ,  $V_{\text{CM}} = 2.5\text{V}$ ,  $R_L$  to 2.5V,  $A_V = 1$ , Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
<b>INPUT CHARACTERISTICS</b>						
$V_{\text{OS}}$	Offset Voltage		-8	-0.8	+8	mV
$\text{TCV}_{\text{OS}}$	Offset Voltage Temperature Coefficient	Measured from $T_{\text{MIN}}$ to $T_{\text{MAX}}$		3		$\mu\text{V}/^\circ\text{C}$
$I_{\text{B}}$	Input Bias Current	$V_{\text{IN}} = 0\text{V}$	-9	-6		$\mu\text{A}$
$I_{\text{OS}}$	Input Offset Current	$V_{\text{IN}} = 0\text{V}$		0.1	0.6	$\mu\text{A}$
$\text{TCI}_{\text{OS}}$	Input Bias Current Temperature Coefficient	Measured from $T_{\text{MIN}}$ to $T_{\text{MAX}}$		2		$\text{nA}/^\circ\text{C}$
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -0.15\text{V}$ to $+3.5\text{V}$	70	95		dB
CMIR	Common Mode Input Range		$V_{\text{S-}} - 0.15$		$V_{\text{S+}} - 1.5$	V
$R_{\text{IN}}$	Input Resistance	Common Mode		3.5		$\text{M}\Omega$
$C_{\text{IN}}$	Input Capacitance			0.5		pF
AVOL	Open Loop Gain	$V_{\text{OUT}} = +1.5\text{V}$ to $+3.5\text{V}$ , $R_L = 1\text{k}\Omega$ to GND	75	90		dB
		$V_{\text{OUT}} = +1.5\text{V}$ to $+3.5\text{V}$ , $R_L = 150\Omega$ to GND		80		dB
<b>OUTPUT CHARACTERISTICS</b>						
$R_{\text{OUT}}$	Output Resistance	$A_V = +1$		30		$\text{m}\Omega$
$V_{\text{OP}}$	Positive Output Voltage Swing	$R_L = 1\text{k}\Omega$	4.85	4.9		V
		$R_L = 150\Omega$	4.6	4.7		V
$V_{\text{ON}}$	Negative Output Voltage Swing	$R_L = 150\Omega$		100	150	mV
		$R_L = 1\text{k}\Omega$		25	50	mV
$I_{\text{OUT}}$	Linear Output Current			65		mA
$I_{\text{SC}}$ (source)	Short Circuit Current	$R_L = 10\Omega$	70	80		mA
$I_{\text{SC}}$ (sink)	Short Circuit Current	$R_L = 10\Omega$	120	150		mA
<b>POWER SUPPLY</b>						
PSRR	Power Supply Rejection Ratio	$V_{\text{S+}} = 4.5\text{V}$ to $5.5\text{V}$	70	95		dB
$I_{\text{S-ON}}$	Supply Current - Enabled			5.6	6	mA
$I_{\text{S-OFF}}$	Supply Current - Disabled			30		$\mu\text{A}$
<b>ENABLE (EL8102 ONLY)</b>						
$t_{\text{EN}}$	Enable Time			200		ns
$t_{\text{DS}}$	Disable Time			25		ns
$V_{\text{IH-ENB}}$	ENABLE Pin Voltage for Power-up			0.8		V
$V_{\text{IL-ENB}}$	ENABLE Pin Voltage for Shut-down			2		V

**Electrical Specifications**  $V_{S+} = 5V$ ,  $V_{S-} = GND$ ,  $T_A = +25^{\circ}C$ ,  $V_{CM} = 2.5V$ ,  $R_L$  to 2.5V,  $A_V = 1$ , Unless Otherwise Specified. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
$I_{IH-ENB}$	ENABLE Pin Input Current High			8.6		$\mu A$
$I_{IL-ENB}$	ENABLE Pin Input for Current Low			0.01		$\mu A$
<b>AC PERFORMANCE</b>						
BW	-3dB Bandwidth	$A_V = +1$ , $R_F = 0\Omega$ , $C_L = 5pF$		500		MHz
		$A_V = -1$ , $R_F = 1k\Omega$ , $C_L = 5pF$		140		MHz
		$A_V = +2$ , $R_F = 1k\Omega$ , $C_L = 5pF$		165		MHz
		$A_V = +10$ , $R_F = 1k\Omega$ , $C_L = 5pF$		18		MHz
BW	$\pm 0.1dB$ Bandwidth	$A_V = +1$ , $R_F = 0\Omega$ , $C_L = 5pF$		35		MHz
Peak	Peaking	$A_V = +1$ , $R_L = 1k\Omega$ , $C_L = 5pF$		1		dB
GBWP	Gain Bandwidth Product			200		MHz
PM	Phase Margin	$R_L = 1k\Omega$ , $C_L = 5pF$		55		$^{\circ}$
SR	Slew Rate	$A_V = 2$ , $R_L = 100\Omega$ , $V_{OUT} = 0.5V$ to $4.5V$	500	600		$V/\mu s$
$t_R$	Rise Time	$2.5V_{STEP}$ , 20% to 80%		4		ns
$t_F$	Fall Time	$2.5V_{STEP}$ , 20% to 80%		2		ns
OS	Overshoot	200mV step		10		%
$t_{PD}$	Propagation Delay	200mV step		1		ns
$t_S$	0.1% Settling Time	200mV step		15		ns
dG	Differential Gain	$A_V = +2$ , $R_F = 1k\Omega$ , $R_L = 150\Omega$		0.01		%
dP	Differential Phase	$A_V = +2$ , $R_F = 1k\Omega$ , $R_L = 150\Omega$		0.01		$^{\circ}$
$e_N$	Input Noise Voltage	$f = 10kHz$		12		$nV/\sqrt{Hz}$
$i_{N+}$	Positive Input Noise Current	$f = 10kHz$		1.7		$pA/\sqrt{Hz}$
$i_{N-}$	Negative Input Noise Current	$f = 10kHz$		1.3		$pA/\sqrt{Hz}$

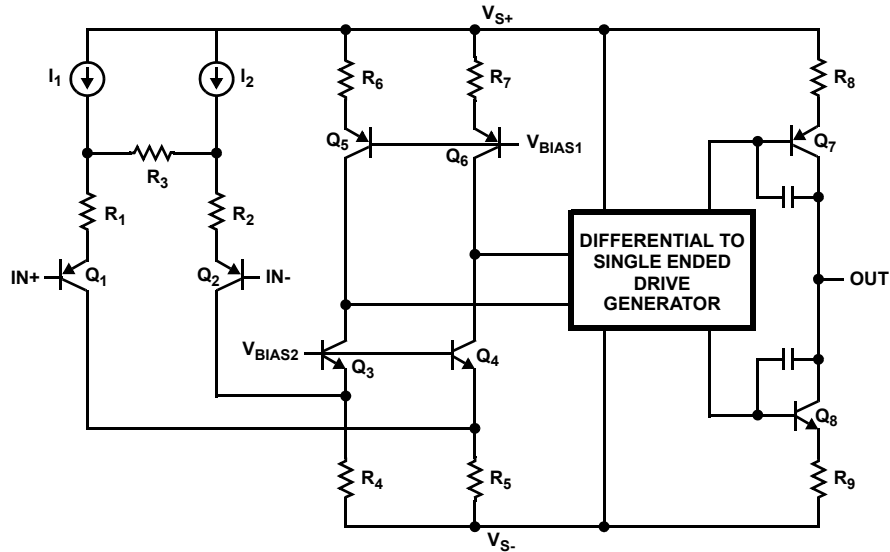
## NOTE:

- Parts are 100% tested at  $+25^{\circ}C$ . Over-temperature limits established by characterization and are not production tested.

**Pin Descriptions**

PIN			NAME	FUNCTION
EL8102IS	EL8102IW	EL8103IW		
1			NC	Not connected
2	4	4	IN-	Inverting input
3	3	3	IN+	Non-inverting input
4	2	2	VS-	Negative power supply
5			NC	Not connected
6	1	1	OUT	Amplifier output
7	6	5	VS+	Positive power supply
8	5		ENABLE	Enable and disable input

**Simplified Schematic Diagram**



**Typical Performance Curves**

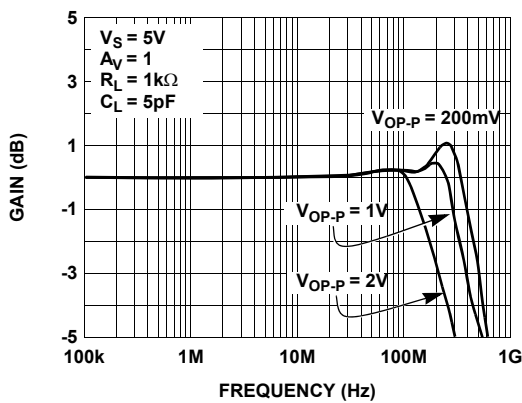


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGE LEVELS

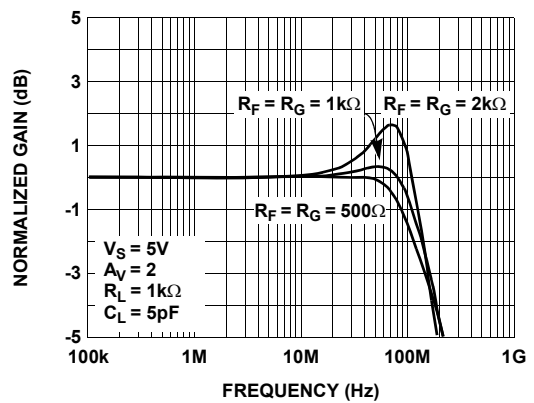


FIGURE 2. SMALL SIGNAL FREQUENCY RESPONSE vs  $R_F$  AND  $R_G$

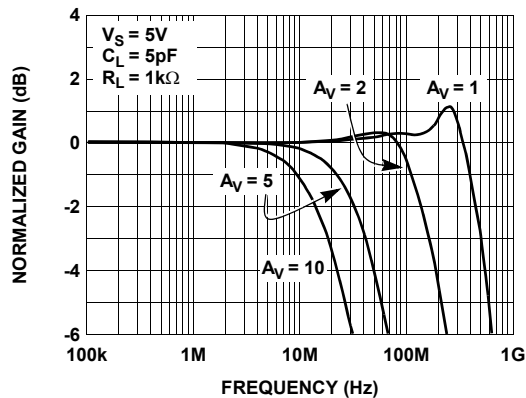


FIGURE 3. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS NON-INVERTING GAINS

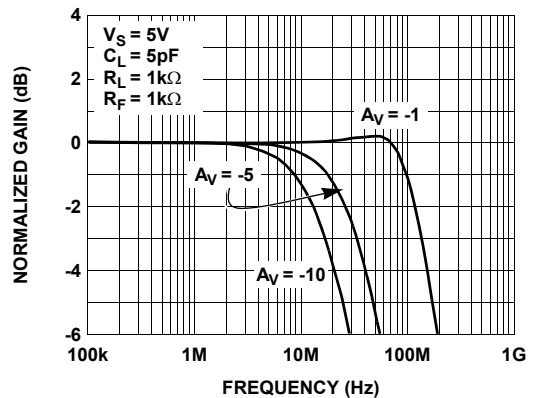


FIGURE 4. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS INVERTING GAINS

Typical Performance Curves (Continued)

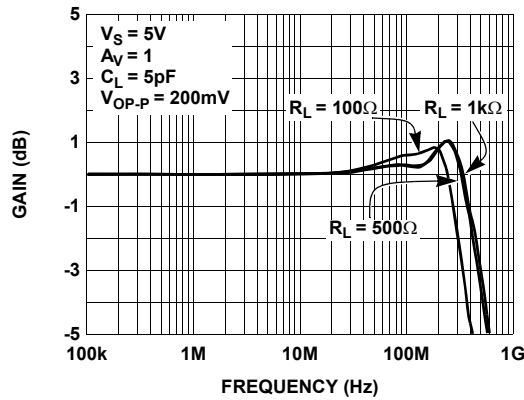


FIGURE 5. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS  $R_{LOAD}$

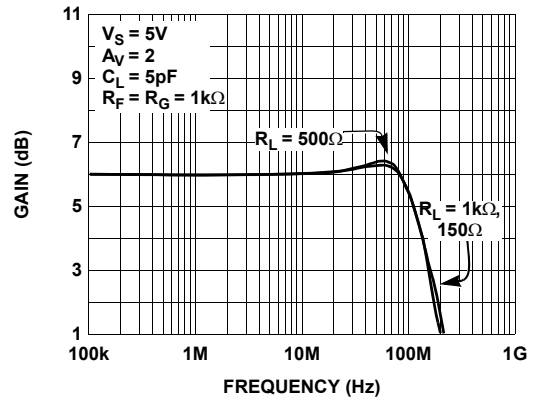


FIGURE 6. SMALL SIGNAL FREQUENCY RESPONSE vs VARIOUS  $R_{LOAD}$

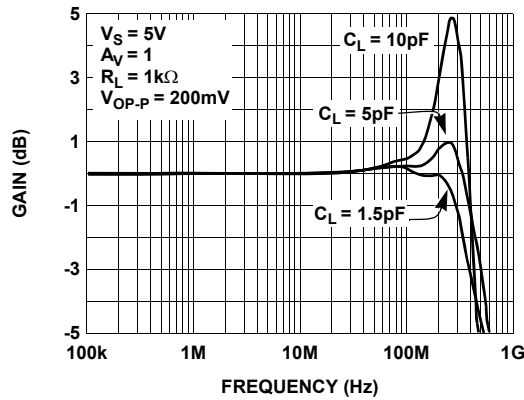


FIGURE 7. SMALL SIGNAL FREQUENCY RESPONSE vs  $C_L$

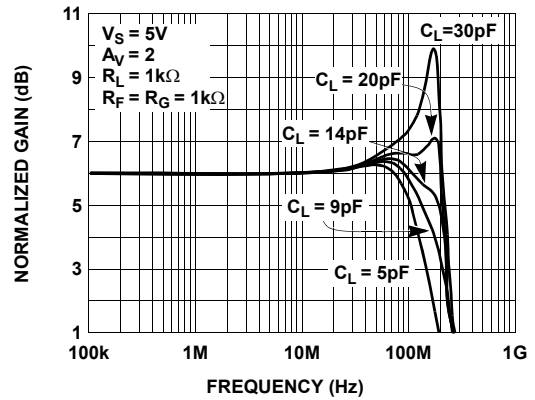


FIGURE 8. SMALL SIGNAL FREQUENCY RESPONSE FOR VARIOUS  $C_L$

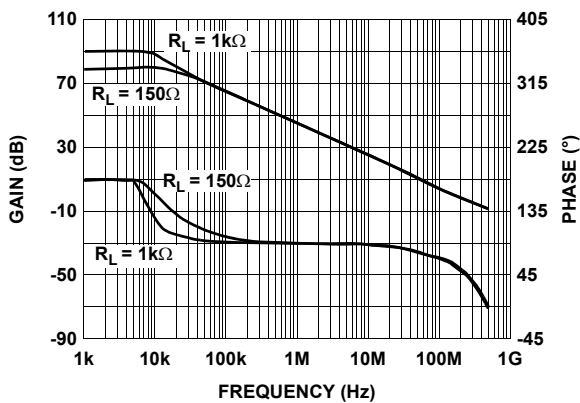


FIGURE 9. OPEN LOOP GAIN AND PHASE vs FREQUENCY

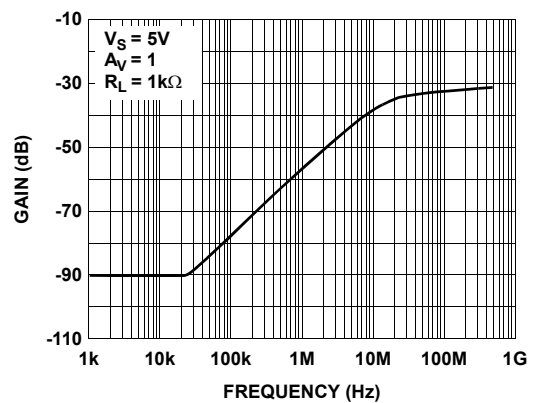


FIGURE 10. DISABLED OUTPUT ISOLATION FREQUENCY RESPONSE

Typical Performance Curves (Continued)

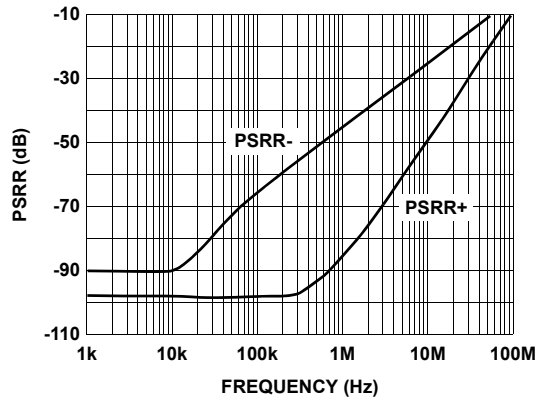


FIGURE 11. POWER SUPPLY REJECTION RATIO vs FREQUENCY

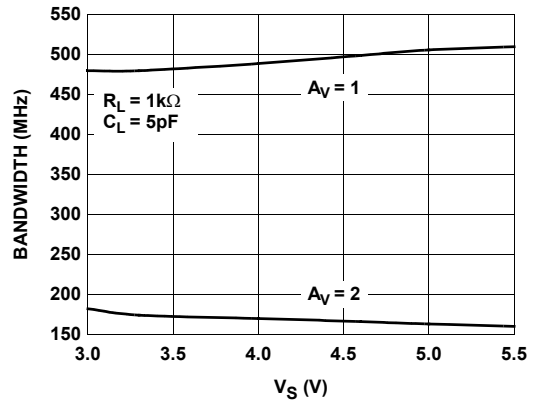


FIGURE 12. SMALL SIGNAL BANDWIDTH vs SUPPLY VOLTAGE

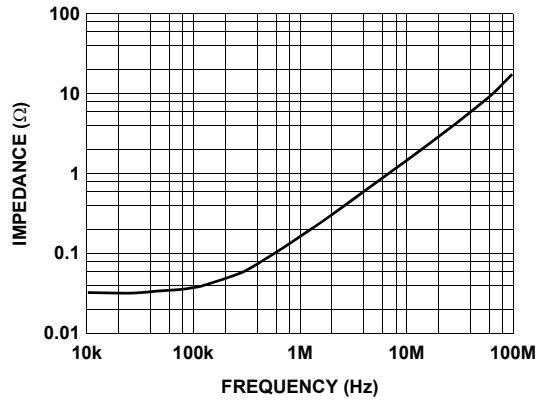


FIGURE 13. OUTPUT IMPEDANCE vs FREQUENCY

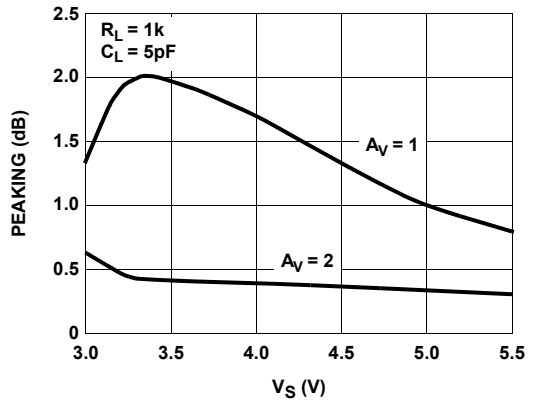


FIGURE 14. SMALL SIGNAL PEAKING vs SUPPLY VOLTAGE

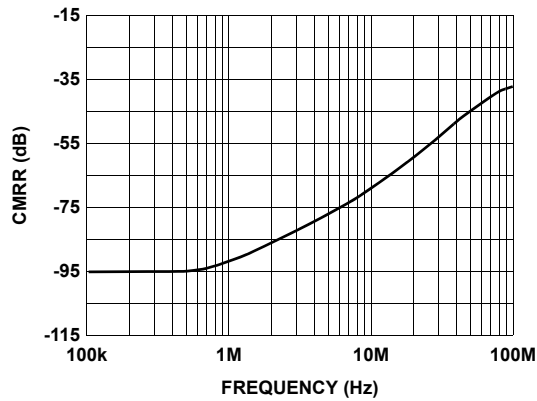


FIGURE 15. COMMON-MODE REJECTION RATIO vs FREQUENCY

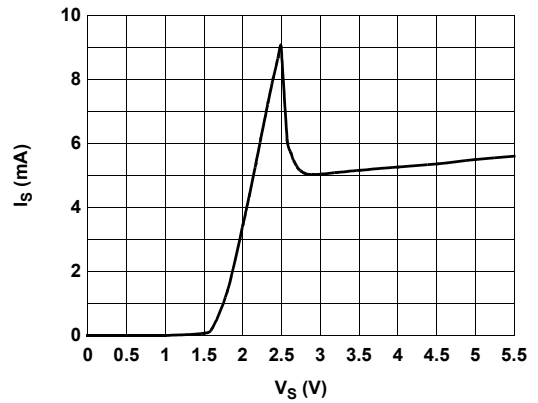


FIGURE 16. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

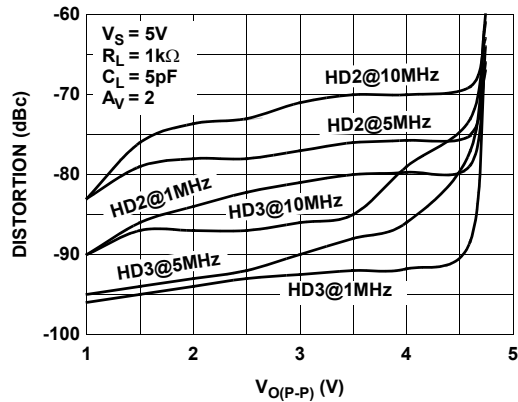


FIGURE 17. HARMONIC DISTORTION vs OUTPUT VOLTAGE

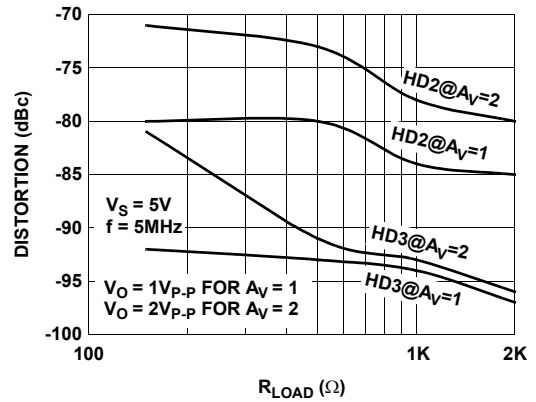


FIGURE 18. HARMONIC DISTORTION vs LOAD RESISTANCE

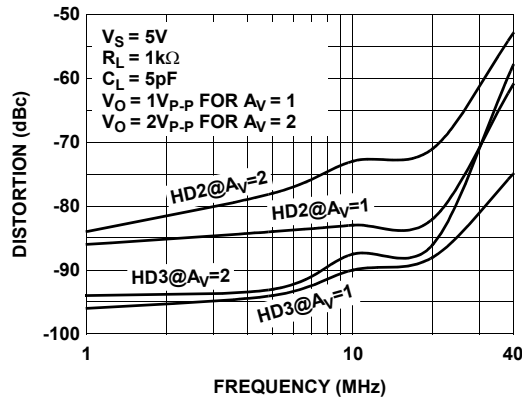


FIGURE 19. HARMONIC DISTORTION vs FREQUENCY

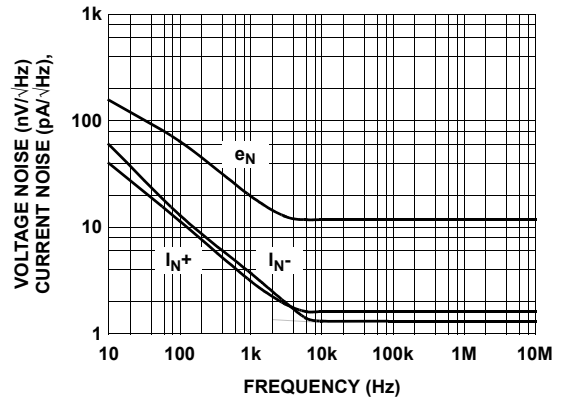


FIGURE 20. VOLTAGE AND CURRENT NOISE vs FREQUENCY

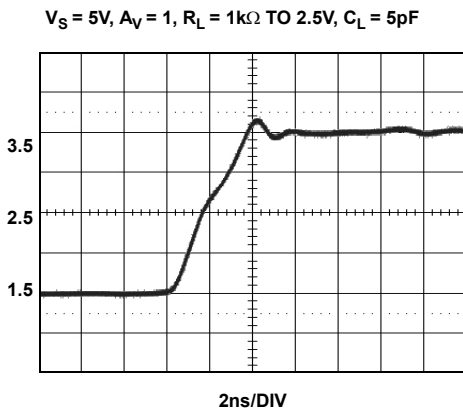


FIGURE 21. LARGE SIGNAL TRANSIENT RESPONSE - RISING

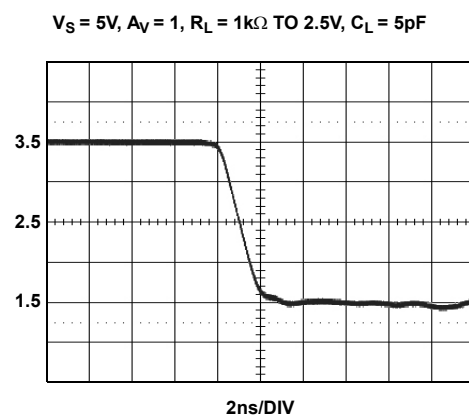


FIGURE 22. LARGE SIGNAL TRANSIENT RESPONSE - FALLING

Typical Performance Curves (Continued)

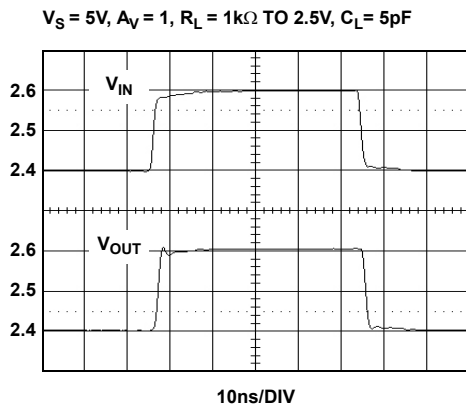


FIGURE 23. SMALL SIGNAL TRANSIENT REPNSE

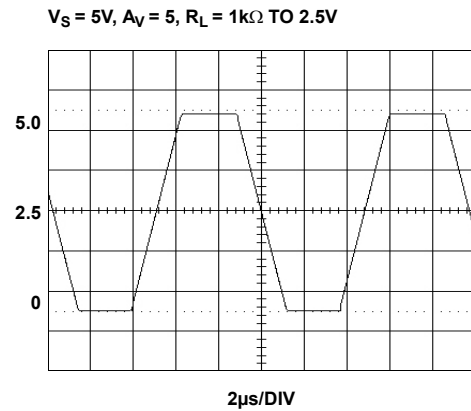


FIGURE 24. OUTPUT SWING

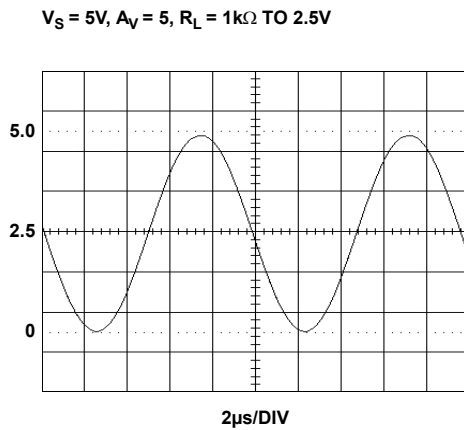


FIGURE 25. OUTPUT SWING

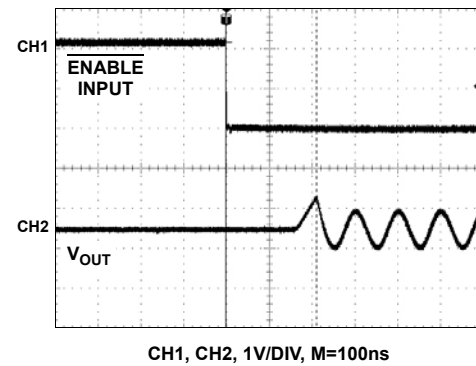


FIGURE 26. ENABLED RESPONSES

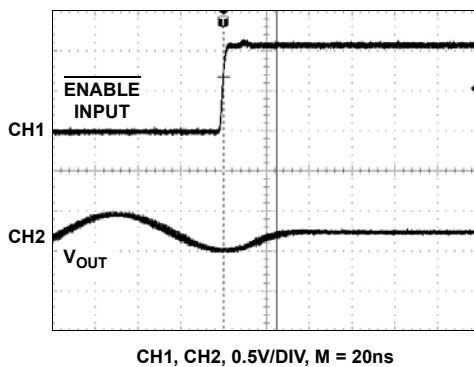


FIGURE 27. DISABLED RESPONSE

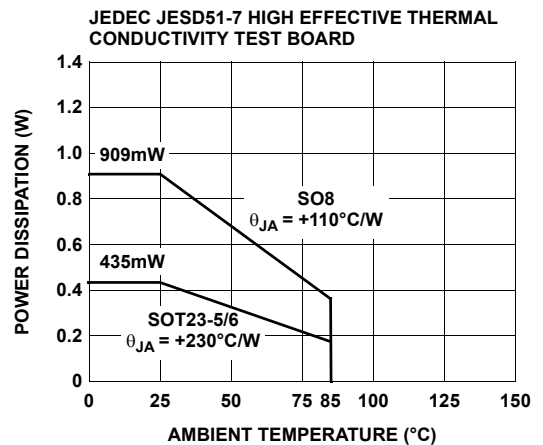


FIGURE 28. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

## Typical Performance Curves (Continued)

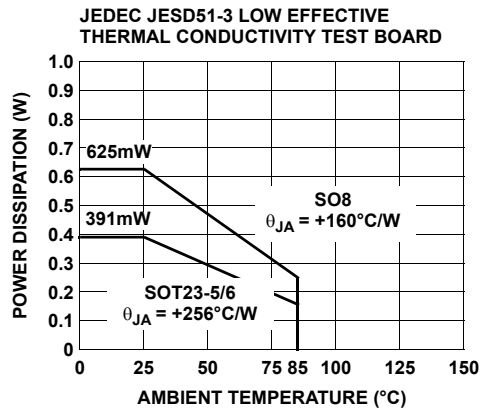


FIGURE 29. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

## Description of Operation and Application Information

### Product Description

The EL8102, EL8103 are wide bandwidth, single supply, low power and rail-to-rail output voltage feedback operational amplifiers. Both amplifiers are internally compensated for closed loop gain of +1 of greater. Connected in voltage follower mode and driving a 1k $\Omega$  load, the EL8102, EL8103 have a -3dB bandwidth of 500MHz. Driving a 150 $\Omega$  load, the bandwidth is about 350MHz while maintaining a 600V/ $\mu$ s slew rate. The EL8102 is available with a power-down pin to reduce power to 30 $\mu$ A typically while the amplifier is disabled.

### Input, Output and Supply Voltage Range

The EL8102, EL8103 have been designed to operate with a single supply voltage from 3V to 5.0V. Split supplies can also be used as long as their total voltage is within 3V to 5.0V. The amplifiers have an input common mode voltage range from 0.15V below the negative supply (VS- pin) to within 1.5V of the positive supply (VS+ pin). If the input signal is outside the above specified range, it will cause the output signal to be distorted.

The output of the EL8102, EL8103 can swing rail-to-rail. As the load resistance becomes lower, the ability to drive close to each rail is reduced. For the load resistor 1k $\Omega$ , the output swing is about 4.9V at a 5V supply. For the load resistor 150 $\Omega$ , the output swing is about 4.6V.

### Choice of Feedback Resistor and Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required. Just short the output pin to the inverting input pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain

and peaking in the frequency domain. Therefore, R<sub>F</sub> has some maximum value that should not be exceeded for optimum performance. If a large value of R<sub>F</sub> must be used, a small capacitor in the few pF range in parallel with R<sub>F</sub> can help to reduce the ringing and peaking at the expense of reducing the bandwidth.

As far as the output stage of the amplifier is concerned, the output stage is also a gain stage with the load. R<sub>F</sub> and R<sub>G</sub> appear in parallel with R<sub>L</sub> for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R<sub>F</sub> also has a minimum value that should not be exceeded for optimum performance. For a gain of +1, R<sub>F</sub> = 0 is optimum. For the gains other than +1, optimum response is obtained with R<sub>F</sub> between 300 $\Omega$  to 1k $\Omega$ .

The EL8102, EL8103 have a gain bandwidth product of 200MHz. For gains  $\geq 5$ , its bandwidth can be predicted by the Equation 1:

$$\text{Gain} \times \text{BW} = 200\text{MHz} \quad (\text{EQ. 1})$$

### Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150 $\Omega$  because the change in output current with DC level. Special circuitry has been incorporated in the EL8102, EL8103 to reduce the variation of the output impedance with the current output. This results in dG and dP specifications of 0.01% and 0.01 $^\circ$ , while driving 150 $\Omega$  at a gain of 2. Driving high impedance loads would give a similar or better dG and dP performance.

### Driving Capacitive Loads and Cables

The EL8102, EL8103 can drive 10pF loads in parallel with 1k $\Omega$  with less than 5dB of peaking at a gain of +1. If less peaking is desired in applications, a small series resistor (usually between 5 $\Omega$  to 50 $\Omega$ ) can be placed in series with the

output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor  $R_G$  can then be chosen to make up for any gain loss which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

### Disable/Power-Down

The EL8102 can be disabled and its output placed in a high impedance state. The turn-off time is about 25ns and the turn-on time is about 200ns. When disabled, the amplifier's supply current is reduced to 30 $\mu$ A typically, thereby effectively eliminating the power consumption. The amplifier's power down can be controlled by standard TTL or CMOS signal levels at the  $\overline{\text{ENABLE}}$  pin. The applied logic signal is relative to  $V_{S-}$  pin. Letting the  $\overline{\text{ENABLE}}$  pin float or applying a signal that is less than 0.8V above  $V_{S-}$  will enable the amplifier. The amplifier will be disabled when the signal at  $\overline{\text{ENABLE}}$  pin is 2V above  $V_{S-}$ .

### Output Drive Capability

The EL8102, EL8103 do not have internal short circuit protection circuitry. They have a typical short circuit current of 80mA sourcing and 150mA sinking for the output is connected to half way between the rails with a 10 $\Omega$  resistor. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds  $\pm 40$ mA. This limit is set by the design of the internal metal interconnections.

### Power Dissipation

With the high output drive capability of the EL8102, EL8103, it is possible to exceed the +125 $^{\circ}$ C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 2:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad (\text{EQ. 2})$$

Where:

$T_{JMAX}$  = Maximum junction temperature

$T_{AMAX}$  = Maximum ambient temperature

$\theta_{JA}$  = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

For sourcing, Equation 3:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L} \quad (\text{EQ. 3})$$

For sinking, Equation 4:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT} - V_{S-}) \times I_{LOAD} \quad (\text{EQ. 4})$$

Where:

$V_S$  = Total supply voltage

$I_{SMAX}$  = Maximum quiescent supply current

$V_{OUT}$  = Maximum output voltage of the application

$R_{LOAD}$  = Load resistance tied to ground

$I_{LOAD}$  = Load current

By setting the two  $PD_{MAX}$  equations equal to each other, we can solve the output current and  $R_{LOAD}$  to avoid the device overheat.

### Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the  $V_{S-}$  pin is connected to the ground plane, a single 4.7 $\mu$ F tantalum capacitor in parallel with a 0.1 $\mu$ F ceramic capacitor from  $V_{S+}$  to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the  $V_{S-}$  pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

**Typical Applications**

**VIDEO SYNC PULSE REMOVER**

Many CMOS analog to digital converters have a parasitic latch up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off. Figure 30 shows a gain of 2 connections for EL8102, EL8103. Figure 31 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.

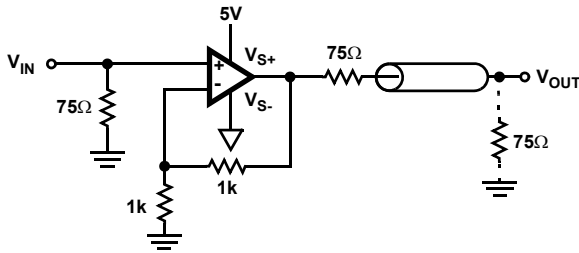


FIGURE 30. SYNC PULSE REMOVER

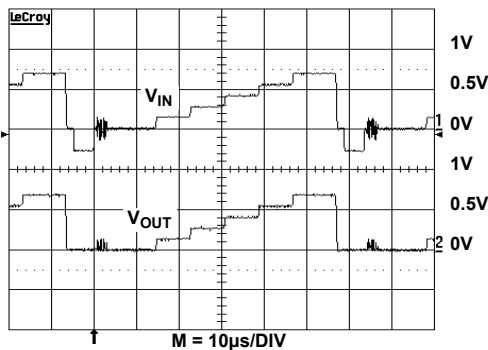


FIGURE 31. VIDEO SIGNAL

**MULTIPLEXER**

Besides the normal power-down usage, the ENABLE pin of the EL8102 can be used for multiplexing applications. Figure 32 shows two EL8102 with the outputs tied together, driving a back terminated 75Ω video load. A 2V<sub>P-P</sub> 2MHz sine wave is applied to Amp A and a 1V<sub>P-P</sub> 2MHz sine wave is applied to Amp B. Figure 33 shows the ENABLE signal and the resulting output waveform at V<sub>OUT</sub>. Observe the break-before-make operation of the multiplexing. Amp A is on and V<sub>IN1</sub> is passed through to the output when the ENABLE signal is low and turns off in about 25ns when the ENABLE signal is high. About 200ns later, Amp B turns on and V<sub>IN2</sub> is passed through to the output. The break-before-make operation ensures that more than one amplifier isn't trying to drive the bus at the same time.

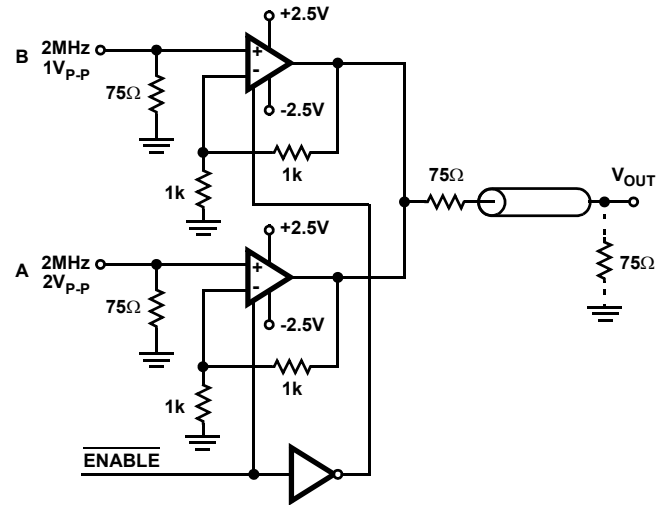


FIGURE 32. TWO TO ONE MULTIPLEXER

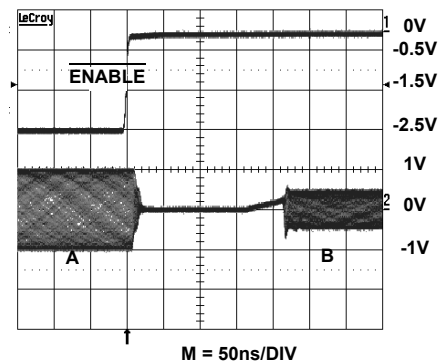


FIGURE 33.

**SINGLE SUPPLY VIDEO LINE DRIVER**

The EL8102 and EL8103 are wideband rail-to-rail output op amplifiers with large output current, excellent dG, dP, and low distortion that allow them to drive video signals in low supply applications. Figure 34 is the single supply non-inverting video line driver configuration and Figure 35 is the inverting video line driver configuration. The signal is AC coupled by C<sub>1</sub>. R<sub>1</sub> and R<sub>2</sub> are used to level shift the input and output to provide the largest output swing. R<sub>F</sub> and R<sub>G</sub> set the AC gain. C<sub>2</sub> isolates the virtual ground potential. R<sub>T</sub> and R<sub>3</sub> are the termination resistors for the line. C<sub>1</sub>, C<sub>2</sub> and C<sub>3</sub> are selected big enough to minimize the droop of the luminance signal.

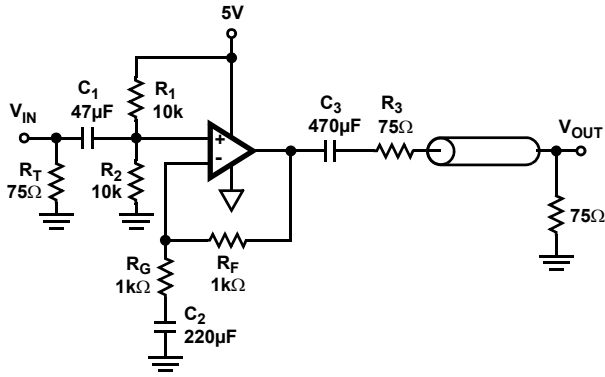


FIGURE 34. 5V SINGLE SUPPLY NON INVERTING VIDEO LINE DRIVER

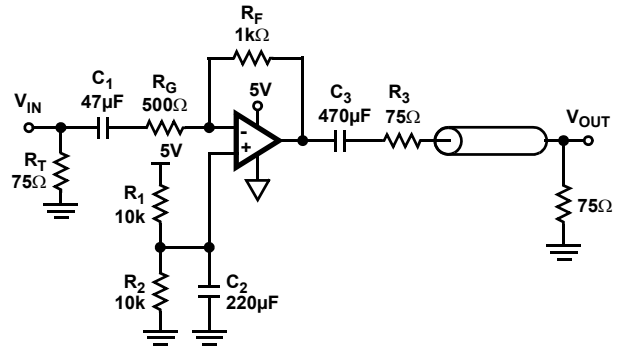


FIGURE 35. SINGLE SUPPLY INVERTING VIDEO LINE DRIVER

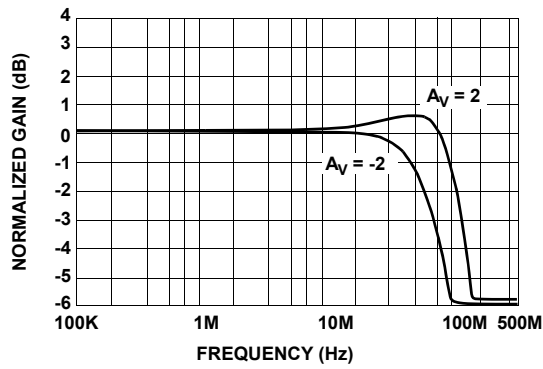
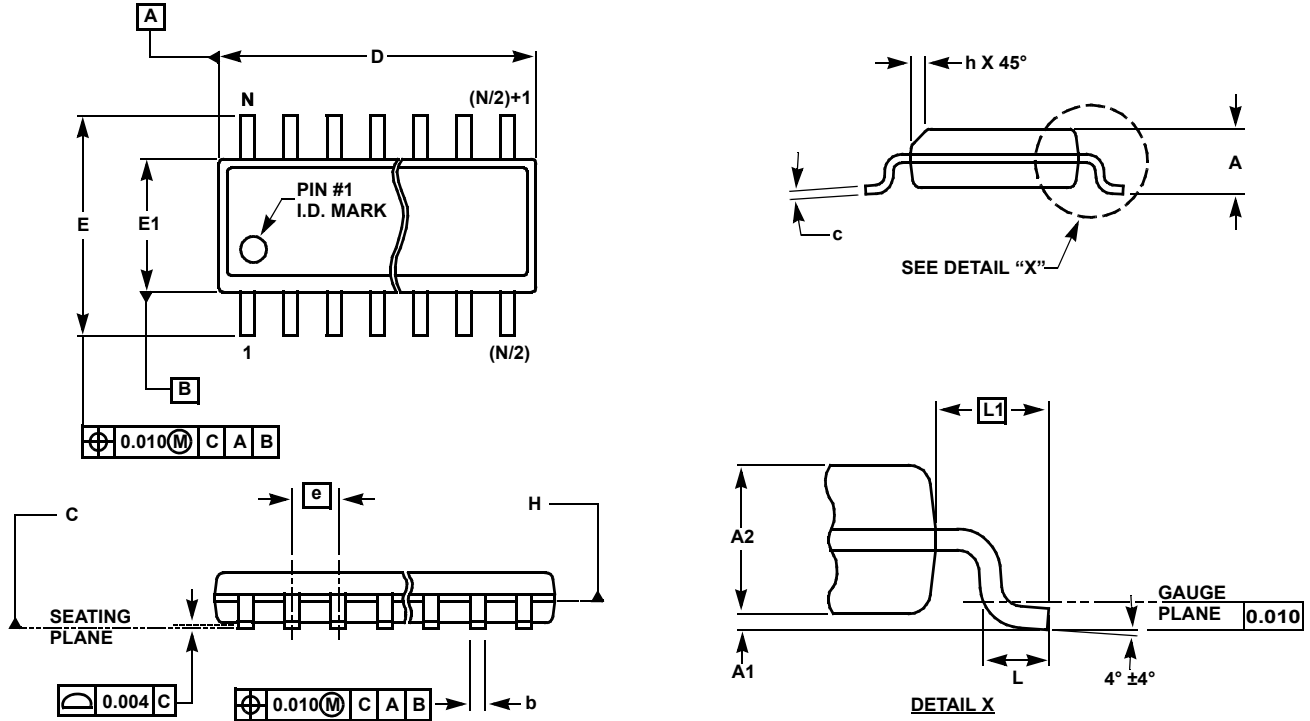


FIGURE 36. VIDEO LINE DRIVER FREQUENCY RESPONSE

**Small Outline Package Family (SO)**



**MDP0027**

**SMALL OUTLINE PACKAGE FAMILY (SO)**

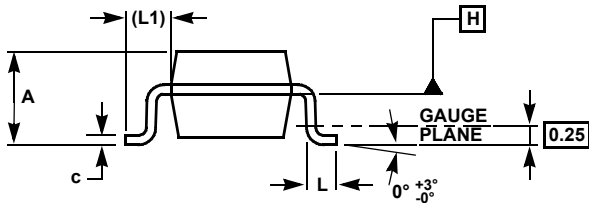
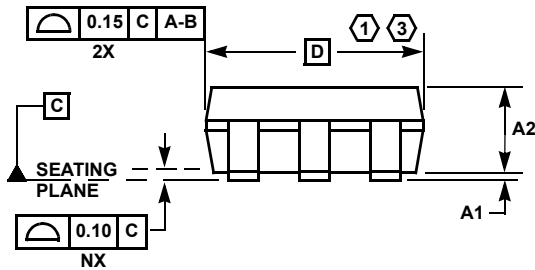
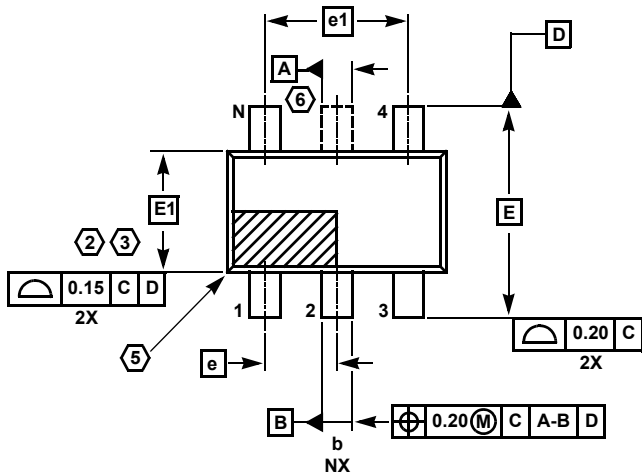
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

**SOT-23 Package Family**



**MDP0038**

**SOT-23 PACKAGE FAMILY**

SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

**NOTES:**

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

© Copyright Intersil Americas LLC 2003-2007. All Rights Reserved.  
 All trademarks and registered trademarks are the property of their respective owners.

For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at [www.intersil.com/en/support/qualandreliability.html](http://www.intersil.com/en/support/qualandreliability.html)

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View EL8102ISZ on WIN SOURCE](#)

 [Intersil Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management