



**THE DATASHEET OF  
EL4584CSZ-T7**



## EL4584

### Horizontal Genlock, 4F<sub>SC</sub>

FN7174  
Rev 3.00  
May 9, 2008

The EL4584 is a PLL (Phase Lock Loop) sub system, designed for video applications but also suitable for general purpose use up to 36MHz. In video applications, this device generates a TTL/CMOS compatible Pixel Clock (CLK OUT) which is a multiple of the TV horizontal scan rate and phase locked to it.

The reference signal is a horizontal sync signal, TTL/CMOS format, which can be easily derived from an analog composite video signal with the EL4583 Sync Separator. An input signal to "coast" is provided for applications where periodic disturbances are present in the reference video timing, such as VTR head switching. The Lock detector output indicates correct lock.

The divider ratio is four ratios for NTSC and four similar ratios for the PAL video timing standards, by external selection of three control pins. These four ratios have been selected for common video applications including 4F<sub>SC</sub>, 3F<sub>SC</sub>, 13.5MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate 8F<sub>SC</sub>, 6F<sub>SC</sub>, 27MHz (CCIR 601 format) etc. use the EL4585, which includes an additional divide-by-two stage.

For applications where these frequencies are inappropriate or for general purpose PLL applications, the internal divider can be bypassed and an external divider chain used.

**TABLE 1. FREQUENCIES AND DIVISORS**

FUNCTION	3F <sub>SC</sub> (Note 1)	CCIR 601 (Note 2)	SQUARE (Note 3)	4F <sub>SC</sub>
Divisor	851	864	944	1135
PAL F <sub>OSC</sub> (MHz)	13.301	13.5	14.75	17.734
Divisor	682	858	780	910
NTSC F <sub>OSC</sub> (MHz)	10.738	13.5	12.273	14.318

**NOTES:**

- 3F<sub>SC</sub> numbers do not yield integer divisors.
- CCIR 601 Divisors yield 720 pixels in the portion of each line for NTSC and PAL.
- Square pixels format gives 640 pixels for NTSC and 768 pixels for PAL in the active portion.

### Features

- 36MHz, general purpose PLL
- 4F<sub>SC</sub> based timing (use the EL4585 for 8F<sub>SC</sub>)
- Compatible with EL4583 sync separator
- VCXO, Xtal, or LC tank oscillator
- < 2ns jitter (VCXO)
- User controlled PLL capture and lock
- Compatible with NTSC and PAL TV formats
- 8 pre-programmed TV scan rate clock divisors
- Selectable external divide for custom ratios
- Single 5V, low current operation
- Pb-Free available (RoHS compliant)

### Applications

- Pixel clock regeneration
- Video compression engine (MPEG) clock generator
- Video capture or digitization
- PIP (Picture-in-Picture) timing generator
- Text or graphics overlay timing

### Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
EL4584CN	EL4584CN	16 Ld PDIP	MDP0031
EL4584CS*	EL4584CS	16 Ld SOIC	MDP0027
EL4584CSZ* (Note)	EL4584CSZ	16 Ld SOIC (Pb-free)	MDP0027

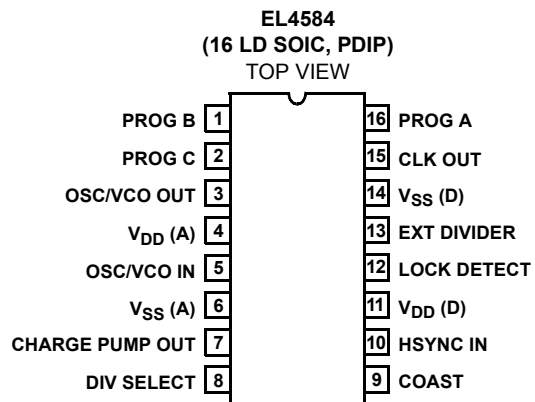
\*Add "-T7" or "-T13" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

\*\*For 6F<sub>SC</sub> and 8F<sub>SC</sub> clock frequencies, see EL4585 datasheet.  
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

### Demo Board

A demo PCB is available for this product.

**Pinout**



**Absolute Maximum Ratings** ( $T_A = +25^{\circ}\text{C}$ )

V<sub>CC</sub> Supply .....7V  
 Operating Junction Temperature ..... +125°C  
 Storage Temperature .....-65°C to +150°C  
 Power Dissipation .....400mW

Oscillator Frequency ..... 36MHz  
 Pin Voltages..... -0.5V to V<sub>CC</sub> +0.5V  
 Operating Ambient Temperature Range .....-40°C to +85°C  
 Pb-free reflow profile .....see link below  
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$*

**DC Electrical Specifications** V<sub>DD</sub> = 5V, T<sub>A</sub> = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>DD</sub>	V <sub>DD</sub> = 5V (Note 4)		2	4	mA
V <sub>IL</sub> Input Low Voltage				1.5	V
V <sub>IH</sub> Input High Voltage		3.5			V
I <sub>IL</sub> Input Low Current	All inputs except COAST, V <sub>IN</sub> = 1.5V	-100			nA
I <sub>IH</sub> Input High Current	All inputs except COAST, V <sub>IN</sub> = 3.5V			100	nA
I <sub>IL</sub> Input Low Current	COAST pin, V <sub>IN</sub> = 1.5V	-100	-60		μA
I <sub>IH</sub> Input High Current	COAST pin, V <sub>IN</sub> = 3.5V		60	100	μA
V <sub>OL</sub> Output Low Voltage	Lock Det, I <sub>OL</sub> = 1.6mA			0.4	V
V <sub>OH</sub> Output High Voltage	Lock Det, I <sub>OH</sub> = -1.6mA	2.4			V
V <sub>OL</sub> Output Low Voltage	CLK, I <sub>OL</sub> = 3.2mA			0.4	V
V <sub>OH</sub> Output High Voltage	CLK, I <sub>OH</sub> = -3.2mA	2.4			V
V <sub>OL</sub> Output Low Voltage	OSC Out, I <sub>OL</sub> = 200μA			0.4	V
V <sub>OH</sub> Output High Voltage	OSC Out, I <sub>OH</sub> = -200μA	2.4			V
I <sub>OL</sub> Output Low Current	Filter Out, V <sub>OUT</sub> = 2.5V	200	300		μA
I <sub>OH</sub> Output High Current	Filter Out, V <sub>OUT</sub> = 2.5V		-300	-200	μA
I <sub>OL</sub> /I <sub>OH</sub> Current Ratio	Filter Out, V <sub>OUT</sub> = 2.5V	1.05	1.0	0.95	
I <sub>LEAK</sub> Filter Out	Coast Mode, V <sub>DD</sub> > V <sub>OUT</sub> > 0V	-100	±1	100	nA

NOTE:

- 4. All inputs to 0V, COAST floating.

**AC Electrical Specifications** V<sub>DD</sub> = 5V, T<sub>A</sub> = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VCO Gain @ 20MHz	Test circuit 1		15.5		dB
H <sub>SYNC</sub> S/N Ratio	V <sub>DD</sub> = 5V (Note 5)	35			dB
Jitter	VCXO oscillator		1		ns
Jitter	LC oscillator (Typ)		10		ns

NOTE:

- 5. Noisy video signal input to EL4583, H<sub>SYNC</sub> input to EL4584. Test for positive signal lock.

## Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
1, 2, 16	PROG B, PROG C, PROG A	Digital inputs to select + N value for internal counter. See Table 2 for values.
3	OSC/VCO OUT	Output of internal inverter/oscillator. Connect to external crystal or LC tank VCO circuit.
4	VDD (A)	Analog positive supply for oscillator, PLL circuits.
5	OSC/VCO IN	Input from external VCO.
6	VSS (A)	Analog ground for oscillator, PLL circuits.
7	CHARGE PUMP OUT	Connect to loop filter. If the H <sub>SYNC</sub> phase is leading or H <sub>SYNC</sub> frequency > CLK ÷ N, current is pumped into the filter capacitor to increase VCO frequency. If H <sub>SYNC</sub> phase is lagging or frequency < CLK ÷ N, current is pumped out of the filter capacitor to decrease VCO frequency. During coast mode or when locked, charge pump goes to a high impedance state.
8	DIV SELECT	Divide select input. When high, the internal divider is enabled and EXT DIV becomes a test pin, outputting CLK ÷ N. When low, the internal divider is disabled and EXT DIV is an input from an external ÷ N.
9	COAST	Tri-state logic input. Low (<1/3*V <sub>CC</sub> ) = normal mode, Hi Z (or 1/3 to 2/3*V <sub>CC</sub> ) = fast lock mode, High (>2/3*V <sub>CC</sub> ) = coast mode.
10	HSYNC IN	Horizontal sync pulse (CMOS level) input.
11	VDD (D)	Positive supply for digital, I/O circuits.
12	LOCK DETECT	Lock Detect output. Low level when PLL is locked. Pulses high when out of lock.
13	EXT DIVIDER	External Divide input when DIV SEL is low, internal ÷N output when DIV SEL is high.
14	VSS (D)	Ground for digital, I/O circuits.
15	CLK OUT	Buffered output of the VCO.

TABLE 2. VCO DIVISORS

PROG A (PIN 16)	PROG B (PIN 1)	PROG C (PIN 2)	DIV VALUE (N)
0	0	0	851
0	0	1	864
0	1	0	944
0	1	1	1135
1	0	0	682
1	0	1	858
1	1	0	780
1	1	1	910

Timing Diagrams

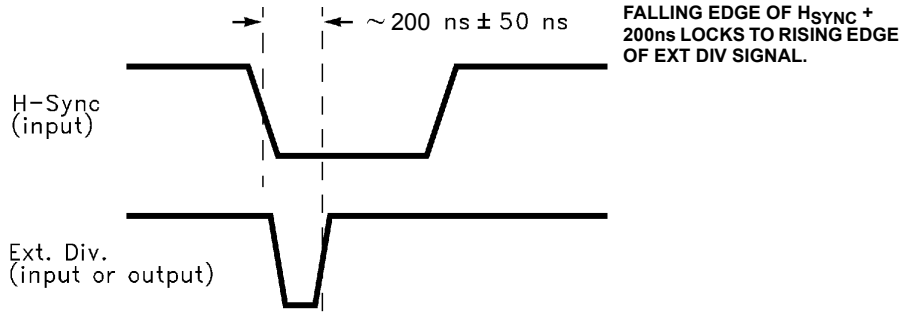


FIGURE 1. PLL LOCKED CONDITION (PHASE ERROR = 0)

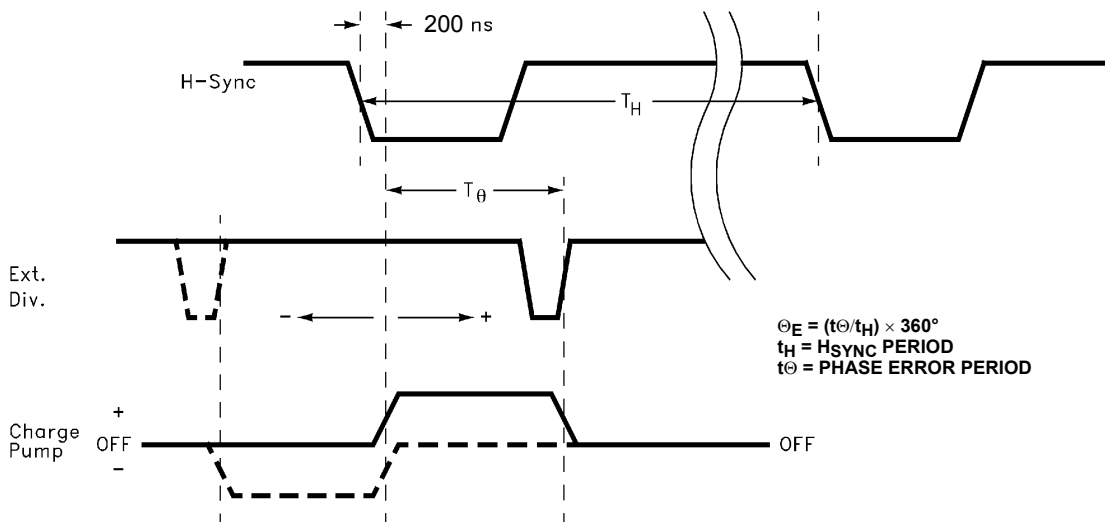


FIGURE 2. OUT OF LOCK CONDITION

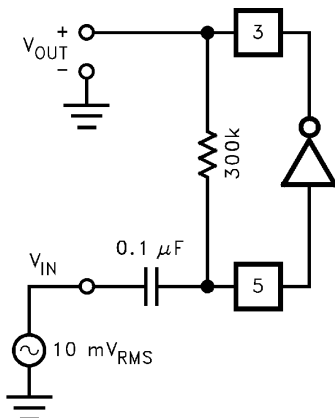
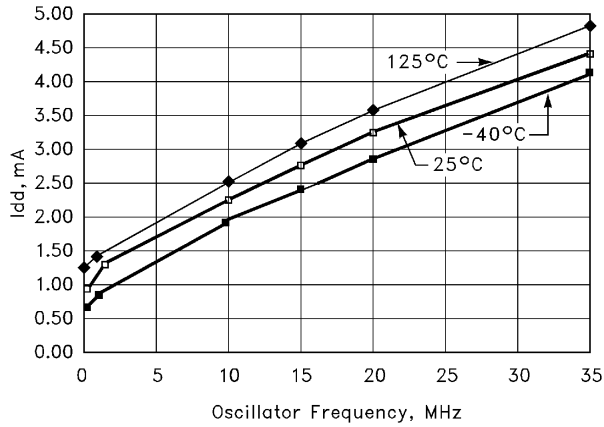
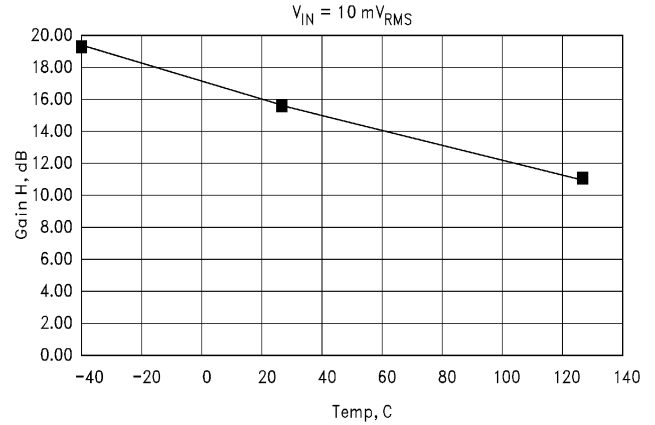


FIGURE 3. TEST CIRCUIT 1

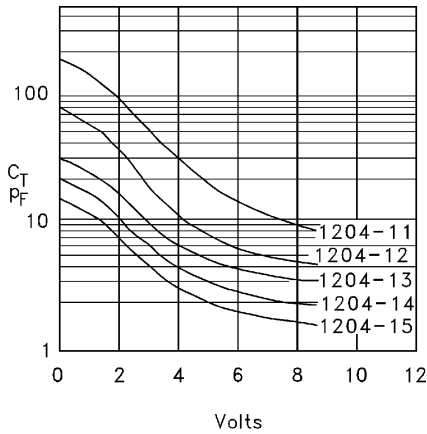
**Typical Performance Curves**



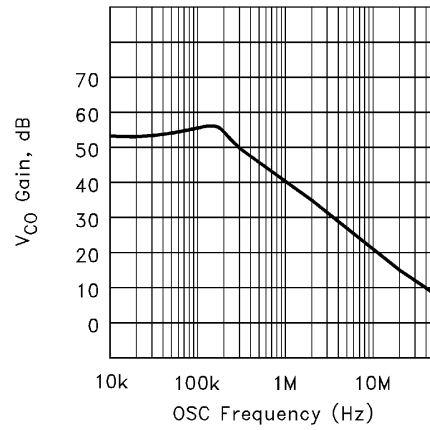
**FIGURE 4. I<sub>DD</sub> vs F<sub>osc</sub>**



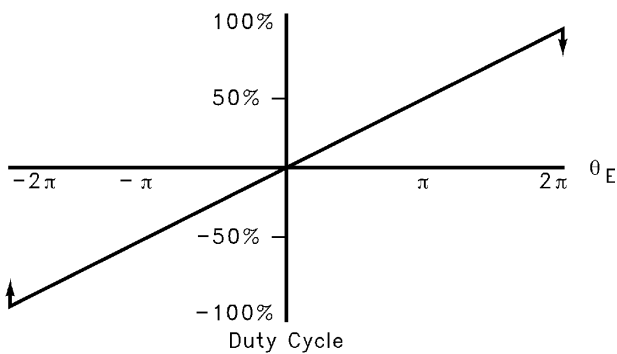
**FIGURE 5. EL4584 OSC GAIN @ 20MHz vs TEMPERATURE**



**FIGURE 6. TYPICAL VARACTOR**

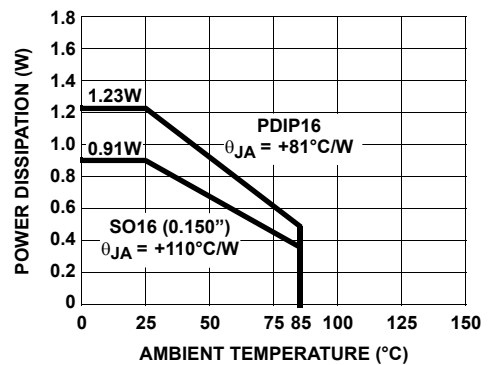


**FIGURE 7. OSC GAIN vs F<sub>osc</sub>**



**FIGURE 8. CHARGE PUMP DUTY CYCLE vs  $\theta_E$**

**JEDEC JESD51-3 LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD**



**FIGURE 9. PACKAGE POWER DISSIPATION VS AMBIENT TEMPERATURE**



must be accomplished with variable capacitance from the varactor within this range. Crystal oscillators are more stable than LC oscillators, which translates into lower jitter, but LC oscillators can be pulled from their mid-point values further, resulting in a greater capture and locking range. If the incoming horizontal sync signal is known to be very stable, then a crystal oscillator circuit can be used. If the H<sub>SYNC</sub> signal experiences frequency variations of greater than about 300ppm, an LC oscillator should be considered, as crystal oscillators are very difficult to pull this far. When H<sub>SYNC</sub> input frequency is greater than CLK ÷ N, charge pump output (pin 7) sources current into the filter capacitor, increasing the voltage across the varactor, which lowers its capacitance, thus tending to increase VCO frequency. Conversely, filter output pulls current from the filter capacitor when H<sub>SYNC</sub> frequency is less than CLK ÷ N, forcing the VCO frequency lower.

### Loop Filter

The loop filter controls how fast the VCO will respond to a change in filter output stimulus. Its components should be chosen so that fast lock can be achieved, yet with a minimum of VCO "hunting", preferably in one to two oscillations of charge pump output, assuming the VCO frequency starts within capture range. If the filter is under-damped, the VCO will over and under-shoot the desired operating point many times before a stable lock takes place. It is possible to under-damp the filter so much that the loop itself oscillates, and VCO lock is never achieved. If the filter is over-damped, the VCO response time will be excessive and many cycles will be required for a lock condition. Over-damping is also characterized by an easily unlocked system because the filter can't respond fast enough to perturbations in VCO frequency. A severely over-damped system will seem to endlessly oscillate, like a very large mass at the end of a long pendulum. Due to parasitic effects of PCB traces and component variables, it will take some trial and error experimentation to determine the best values to use for any given situation. Use the component tables as a starting point, but be aware that deviation from these values is not out of the ordinary.

### External Divide

DIV SELECT (pin 8) controls the use of the internal divider. When high, the internal divider is enabled and EXT DIVIDER (pin 13) outputs the CLK out divided by N. This is the signal to which the horizontal sync input will lock. When divide select is low, the internal divider output is disabled, and the external divide becomes an input from an external divider, so that a divisor other than one of the 8 pre-programmed internal divisors can be used.

### Normal Mode

Normal mode is enabled by pulling COAST (pin 9) low (below  $1/3 \cdot V_{CC}$ ). If H<sub>SYNC</sub> and CLK ÷ N have any phase or frequency difference, an error signal is generated and sent to the charge pump. The charge pump will either force current into or out of the filter capacitor in an attempt to modulate the

VCO frequency. Modulation will continue until the phase and frequency of CLK ÷ N exactly match the H<sub>SYNC</sub> input. When the phase and frequency match (with some offset in phase that is a function of the VCO characteristics), the error signal goes to zero, lock detect no longer pulses high, and the charge pump enters a high impedance state. The clock is now locked to the H<sub>SYNC</sub> input. As long as phase and frequency differences remain small, the PLL can adjust the VCO to remain locked and lock detect remains low.

### Fast Lock Mode

Fast Lock mode is enabled by either allowing coast to float, or pulling it to mid supply (between  $1/3$  and  $2/3 \cdot V_{CC}$ ). In this mode, lock is achieved much faster than in normal mode, but the clock divisor is modified on the fly to achieve this. If the phase detector detects an error of enough magnitude, the clock is either inhibited or reset to attempt a "fast" lock of the signals.

Forcing the clock to be synchronized to the H<sub>SYNC</sub> input this way allows a lock in approximately 2 H-cycles, but the clock spacing will not be regular during this time. Once the near lock condition is attained, charge pump output should be very close to its lock-on value and placing the device into normal mode should result in a normal lock very quickly. Fast Lock mode is intended to be used where H<sub>SYNC</sub> becomes irregular, until a stable signal is again obtained.

### Coast Mode

Coast mode is enabled by pulling the COAST (pin 9) high (above  $2/3 \cdot V_{CC}$ ). In coast mode, the internal phase detector is disabled and filter out remains in high impedance mode to keep filter out voltage and VCO frequency as constant as possible. VCO frequency will drift as charge leaks from the filter capacitor, and the voltage changes the VCO operating point. Coast mode is intended to be used when noise or signal degradation results in loss of horizontal sync for many cycles. The phase detector will not attempt to adjust to the resultant loss of signal so that when horizontal sync returns, sync lock can be re-established quickly. However, if much VCO drift has occurred, it may take as long to re-lock as when restarting.

### Lock Detect

LOCK DETECT (pin 12) will go low when lock is established. Any DC current path from charge pump out will skew EXT DIVIDER relative to H<sub>SYNC</sub> IN, tending to offset or add to the 200ns internal delay, depending on which way the extra current is flowing. This offset is called static phase error, and is always present in any PLL system. If, when the part stabilizes in a locked mode, lock detect is not low, adding or subtracting from the loop filter series resistor R<sub>2</sub> will change this static phase error to allow LDET to go low while in lock. The goal is to put the rising edge of EXT DIVIDER in sync with the falling edge of H<sub>SYNC</sub> + 200ns (see "Timing Diagrams" on page 5 and page 5). Increasing R<sub>2</sub> decreases phase error, while decreasing R<sub>2</sub> increases phase error (phase error is positive when EXT DIVIDER lags H<sub>SYNC</sub>.)

The resistance needed will depend on VCO design or VCXO module selection.

**Applications Information**

**Choosing External Components**

1. To choose LC VCO components, first pick the desired operating frequency. For our example, we will use 14.31818MHz, with an H<sub>SYNC</sub> frequency of 15.734kHz.
2. Choose a reasonable inductor value (10µH to 20µH works well). We choose 15µH.
3. Calculate C<sub>T</sub> needed to produce F<sub>OSC</sub>, as shown in Equations 1 and 2.

$$F_{OSC} = \frac{1}{2\pi\sqrt{LC_T}} \quad (EQ. 1)$$

$$C_T = \frac{1}{4\pi^2 F^2 L} = \frac{1}{4\pi^2 (14.318e6)^2 (15e-6)} = 8.2pF \quad (EQ. 2)$$

4. From the varactor data sheet find C<sub>V</sub> @ 2.5V, the desired lock voltage. C<sub>V</sub> = 23pF for our SMV1204-12, for example.
5. C<sub>2</sub> should be about 10C<sub>V</sub>, so we choose C<sub>2</sub> = 220pF for our example.
6. Calculate C<sub>1</sub> using Equations 3 and 4. Since:

$$C_T = \frac{C_1 C_2 C_V}{(C_1 C_2) + (C_1 C_V) + (C_2 C_V)} \quad (EQ. 3)$$

then:

$$C_1 = \frac{C_2 C_T C_V}{(C_2 C_V) - (C_2 C_T) - (C_T C_V)} \quad (EQ. 4)$$

For our example, C<sub>1</sub> = 14pF (a trim capacitor may be used for fine tuning). Examples for each frequency using the internal divider follow.

**Typical Application**

Horizontal genlock provides clock for an analog to digital converter, digitizing analog video.

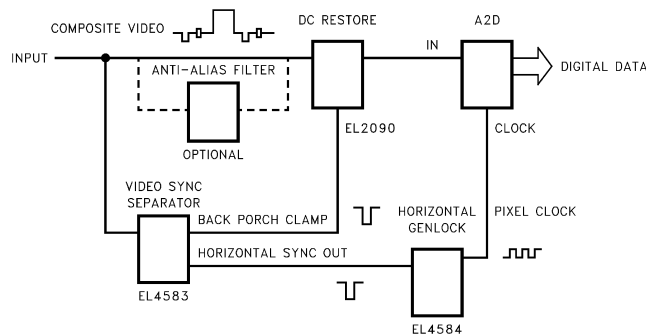


FIGURE 11.

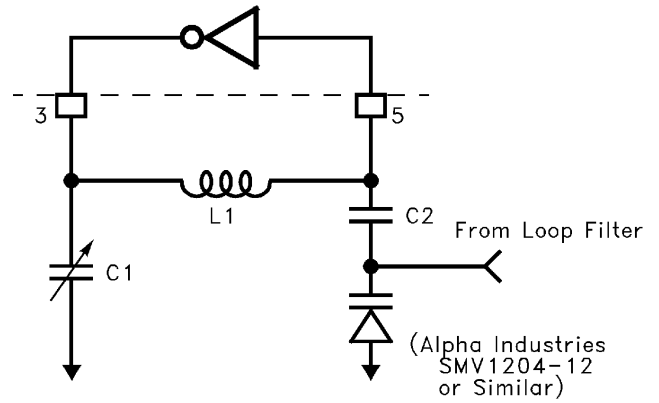


FIGURE 12. TYPICAL LC VCO

TABLE 3. LC VCO COMPONENT VALUES (APPROXIMATE) (NOTE)

FREQUENCY (MHZ)	L <sub>1</sub> (µH)	C <sub>1</sub> (pF)	C <sub>2</sub> (pF)
13.301	15	18	220
13.5	15	17	220
14.75	12	18	220
17.734	12	10	220
10.738	22	20	220
12.273	18	17	220
14.318	15	14	220

NOTE: Use shielded inductors for optimum performance.

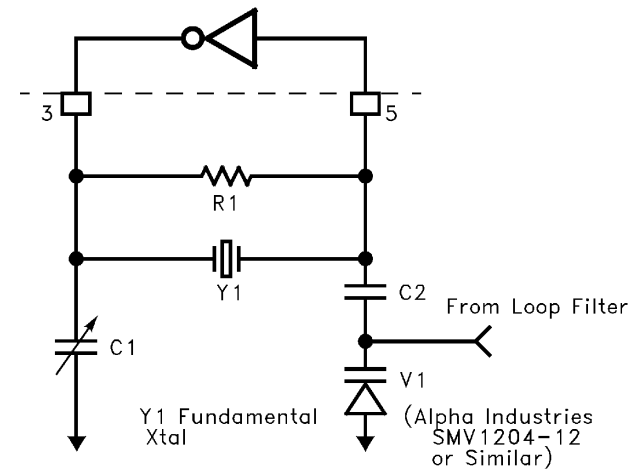


FIGURE 13. TYPICAL XTAL VCO

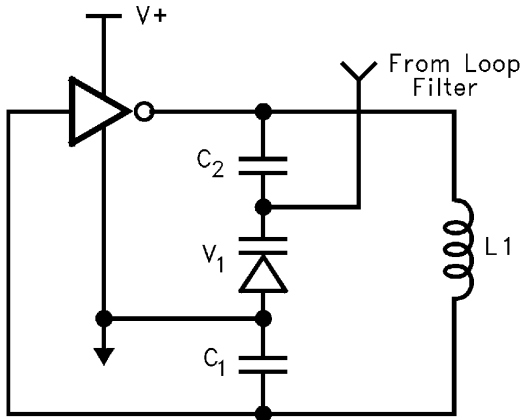
TABLE 4. XTAL VCO COMPONENT VALUES (APPROXIMATE)

FREQUENCY (MHZ)	R <sub>1</sub> (kΩ)	C <sub>1</sub> (pF)	C <sub>2</sub> (µF)
13.301	300	15	0.001
13.5	300	15	0.001
14.75	300	15	0.001

**TABLE 4. XTAL VCO COMPONENT VALUES (APPROXIMATE) (Continued)**

FREQUENCY (MHz)	R <sub>1</sub> (kΩ)	C <sub>1</sub> (pF)	C <sub>2</sub> (μF)
17.734	300	15	0.001
10.738	300	15	0.001
12.273	300	15	0.001
14.318	300	15	0.001

The above oscillators are arranged as Colpitts oscillators, and the structure is redrawn here to emphasize the split capacitance used in a Colpitts oscillator. It should be noted that this oscillator configuration is just one of literally hundreds possible, and the configuration shown here does not necessarily represent the best solution for all applications. Crystal manufacturers are very informative sources on the design and use of oscillators in a wide variety of applications, and the reader is encouraged to become familiar with them.



**FIGURE 14. COLPITTS OSCILLATOR**

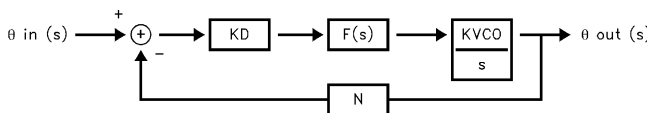
C<sub>1</sub> is to adjust the center frequency, C<sub>2</sub> DC isolates the control from the oscillator, and V<sub>1</sub> is the primary control device. C<sub>2</sub> should be much larger than C<sub>V</sub> so that V<sub>1</sub> has maximum modulation capability. The frequency of oscillation is given by Equations 5 and 6:

$$F = \frac{1}{12\pi\sqrt{LC_T}} \tag{EQ. 5}$$

$$C_T = \frac{C_1 C_2 C_V}{(C_1 C_2) + (C_1 C_V) + (C_2 C_V)} \tag{EQ. 6}$$

**Choosing Loop Filter Components**

The PLL, VCO, and loop filter can be represented in Figure 15:



**FIGURE 15.**

Where:

K<sub>d</sub> = phase detector gain in A/rad

F(s) = loop filter impedance in V/A

K<sub>VCO</sub> = VCO gain in rad/s/V

N = internal or external divisor

It can be shown that for the loop filter shown in Equation 7:

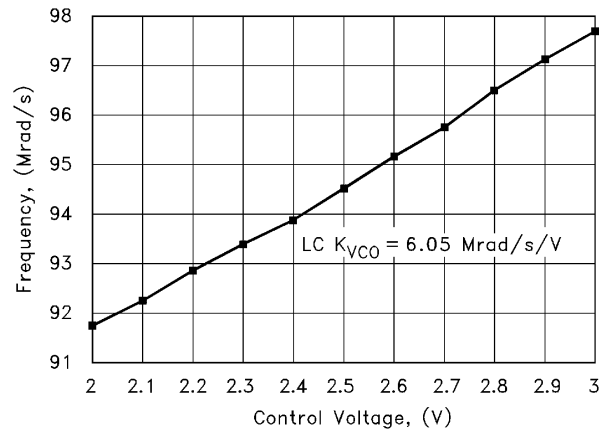
$$C_3 = \frac{K_d K_{VCO}}{N \omega_n^2}, C_4 = \frac{C_3}{10}, R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}} \tag{EQ. 7}$$

Where ω<sub>n</sub> = loop filter bandwidth, and ζ = loop filter damping factor.

1. K<sub>d</sub> = 300μA/2πrad = 4.77e-5A/rad for the EL4584.
2. The loop bandwidth should be about H<sub>SYNC</sub> frequency/20, and the damping ratio should be 1 for optimum performance. For our example, ω<sub>n</sub> = 15.734kHz/20 = 787Hz≈5000rad/S.
3. N = 910 from Table 2.

$$N = \frac{VCO\text{frequency}}{H-SYNC\text{frequency}} = \frac{14.31818M}{15.73426k} = 910 \tag{EQ. 8}$$

4. K<sub>VCO</sub> represents how much the VCO frequency changes for each volt applied at the control pin. It is assumed (but probably is not) linear about the lock point (2.5V). Its value depends on the VCO configuration and the varactor transfer function C<sub>V</sub> = F(V<sub>C</sub>), where V<sub>C</sub> is the reverse bias control voltage, and C<sub>V</sub> is varactor capacitance. Since F(V<sub>C</sub>) is nonlinear, it is probably best to build the VCO and measure K<sub>VCO</sub> about 2.5V. The results of one such measurement are shown in the following. The slope of the curve is determined by linear regression techniques and equals K<sub>VCO</sub>. For our example, K<sub>VCO</sub> = 6.05 Mrad/S/V.



**FIGURE 16. F<sub>OSC</sub> vs V<sub>C</sub>, LC VCO**

5. Now we can solve for C<sub>3</sub>, C<sub>4</sub>, and R<sub>3</sub>. We choose R<sub>3</sub> = 30kΩ for convenience.
6. Notice R<sub>2</sub> has little effect on the loop filter design. R<sub>2</sub> should be large, around 100k, and can be adjusted to compensate for any static phase error t<sub>0</sub> at lock, but if made too large, will slow loop response. If R<sub>2</sub> is made

smaller,  $t_0$  (see “Timing Diagrams” on page 5) increases, and if  $R_2$  increases,  $t_0$  decreases. For LDET to be low at lock,  $|t_0| < 50$  ns.  $C_4$  is used mainly to attenuate high frequency noise from the charge pump.

$$C_3 = \frac{K_d K_{VCO}}{N \omega_n^2} = \frac{(4.77e-5)(6.05e6)}{(910)(5000)^2} = 0.01 \mu F \quad (\text{EQ. 9})$$

$$C_4 = \frac{C_3}{10} = 0.0001 \mu F \quad (\text{EQ. 10})$$

$$R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}} = \frac{(2)(910)(1)(5000)}{(4.77e-5)(6.05e6)} = 31.5 k\Omega \quad (\text{EQ. 11})$$

**Lock Time**

Let  $\tau = R_3 C_3$ . As  $t$  increases, damping increases, but so does lock time. Decreasing  $t$  decreases damping and speeds up loop response, but increases overshoot and thus increases the number of hunting oscillations before lock. Critical damping ( $\zeta = 1$ ) occurs at minimum lock time. Because decreased damping also decreases loop stability, it is sometimes desirable to design slightly overdamped ( $\zeta > 1$ ), trading lock time for increased stability.

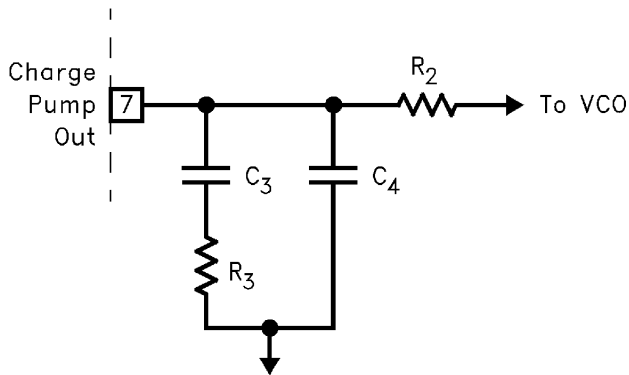


FIGURE 17. TYPICAL LOOP FILTER

TABLE 5. LC LOOP FILTER COMPONENTS (APPROXIMATE)

FREQUENCY (MHz)	R <sub>2</sub> (kΩ)	R <sub>3</sub> (kΩ)	C <sub>3</sub> (μF)	C <sub>4</sub> (μF)
13.301	100	30	0.01	0.001
13.5	100	30	0.01	0.001
14.75	100	33	0.01	0.001
17.734	100	39	0.01	0.001
10.738	100	22	0.01	0.001
12.273	100	27	0.01	0.001
14.318	100	30	0.01	0.001

TABLE 6. XTAL LOOP FILTER COMPONENTS (APPROXIMATE)

FREQUENCY (MHz)	R <sub>2</sub> (kΩ)	R <sub>3</sub> (MΩ)	C <sub>3</sub> (pF)	C <sub>4</sub> (pF)
13.301	100	4.3	68	6.8
13.5	100	4.3	68	6.8
14.75	100	4.3	68	6.8
17.734	100	4.3	68	6.8
10.738	100	4.3	68	6.8
12.273	100	4.3	68	6.8
14.318	100	4.3	68	6.8

**PCB Layout Considerations**

It is highly recommended that power and ground planes be used in layout. The oscillator and filter sections constitute a feedback loop and thus care must be taken to avoid any feedback signal influencing the oscillator except at the control input. The entire oscillator/filter section should be surrounded by copper ground to prevent unwanted influences from nearby signals. Use separate paths for analog and digital supplies, keeping the analog (oscillator section) as short and free from spurious signals as possible. Careful attention must be paid to correct bypassing. Keep lead lengths short and place bypass capacitors as close to the supply pins as possible. If laying out a PCB to use discrete components for the VCO section, care must be taken to avoid parasitic capacitance at the OSC pins 3 and 5, and FILTER out (pin 7). Remove ground and power plane copper above and below these traces to avoid making a capacitive connection to them. It is also recommended to enclose the oscillator section within a shielded cage to reduce external influences on the VCO, as they tend to be very sensitive to “handwaving” influences, the LC variety being more sensitive than crystal controlled oscillators. In general, the higher the operating frequency, the more important these considerations are. Self contained VCXO or VCO modules are already mounted in a shielding cage and therefore do not require as much consideration in layout. Many crystal manufacturers publish informative literature regarding use and layout of oscillators which should be helpful.

The VCO and loop filter section of the EL4583, EL4584, EL4585 demo board can be implemented in Figures 18, 19 and 20.

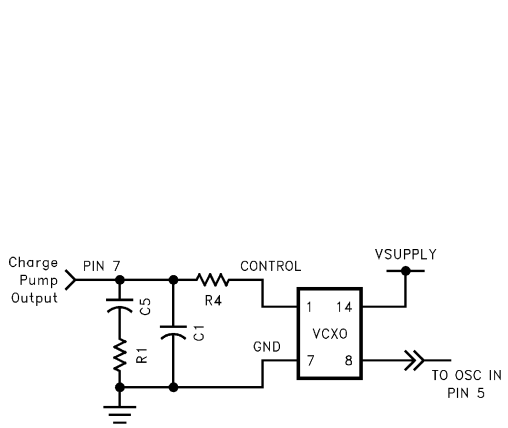


FIGURE 18. VCXO

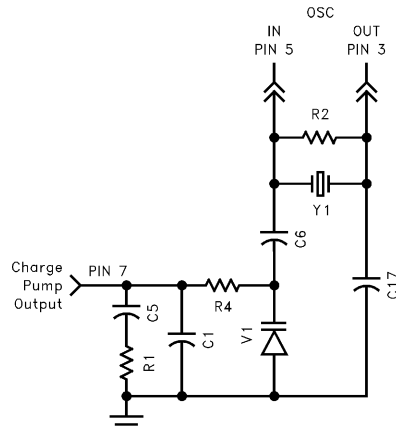


FIGURE 19. XTAL

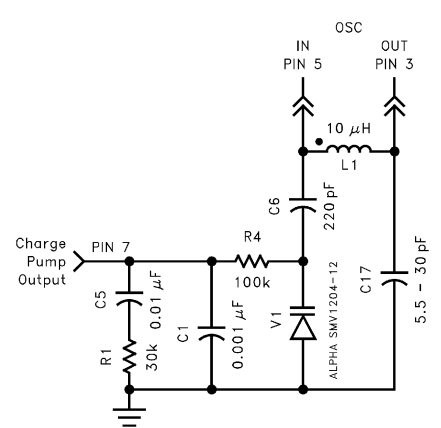
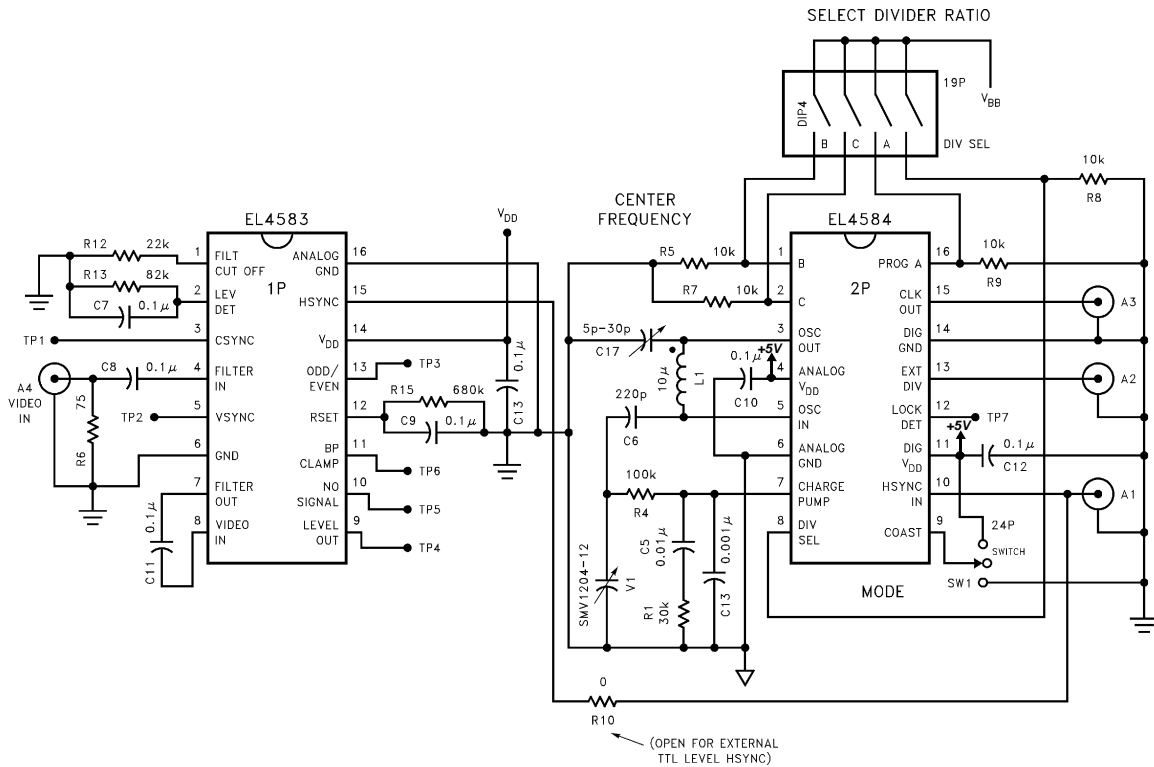


FIGURE 20. LC TANK

**Demo Board**



## **Component Sources**

### **Inductors**

- Dale Electronics  
E. Highway 50  
PO Box 180  
Yankton, SD 57078-0180  
(605) 665-9301

### **Crystals, VCXO, VCO Modules**

- Connor-Winfield  
2111 Comprehensive Drive  
Aurora, IL 60606  
(708) 851-4722
- Piezo Systems  
100 K Street  
PO Box 619  
Carlisle, PA 17013  
(717) 249-2151
- Reeves-Hoffman  
400 West North Street  
Carlisle, PA 17013  
(717) 243-5929

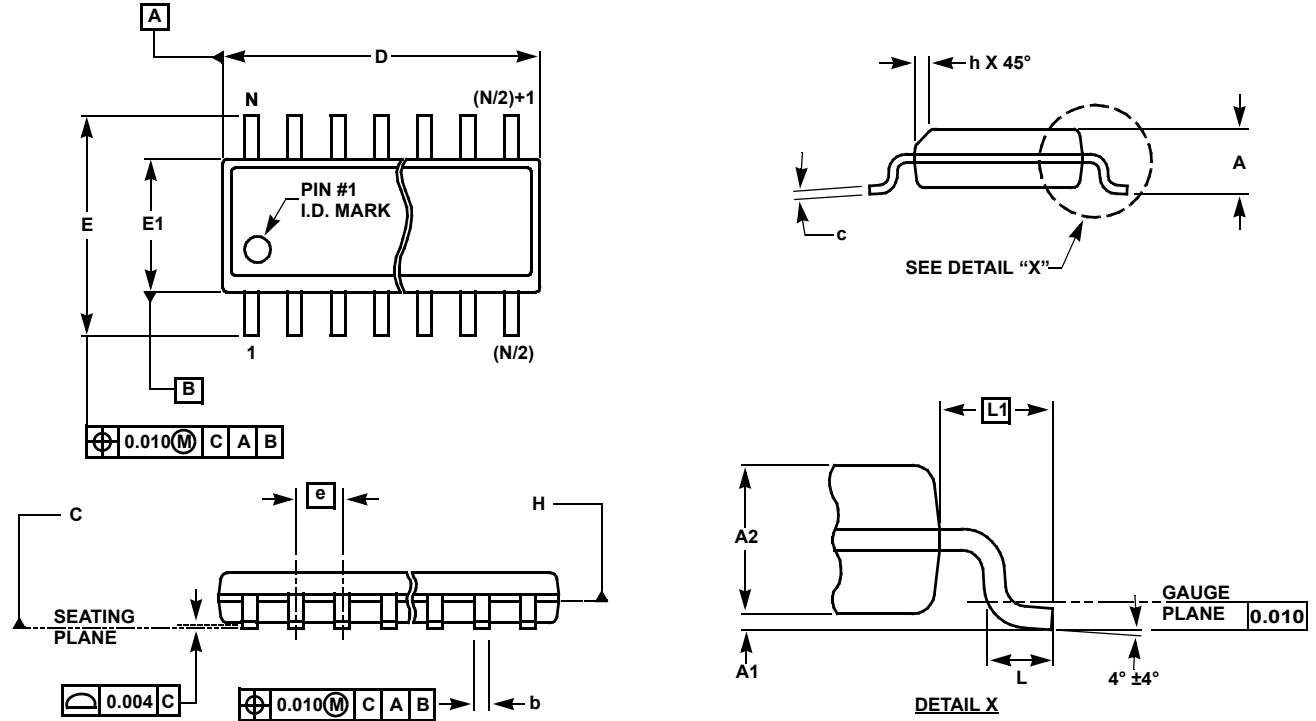
- SaRonix  
151 Laura Lane  
Palo Alto, CA 94043  
(415) 856-6900
- Standard Crystal  
9940 Baldwin Place  
El Monte, CA 91731  
(818) 443-2121

### **Varactors**

- Sky Works Solutions Inc.  
20 Sylvan Road  
Woburn, MA 01801  
(781) 376-3000  
[www.skyworksinc.com](http://www.skyworksinc.com)
- Motorola Semiconductor Products  
2100 E. Elliot  
Tempe, AZ 85284  
(602) 244-6900

Note: These sources are provided for information purposes only. No endorsement of these companies is implied by this listing.

**Small Outline Package Family (SO)**



**MDP0027**

**SMALL OUTLINE PACKAGE FAMILY (SO)**

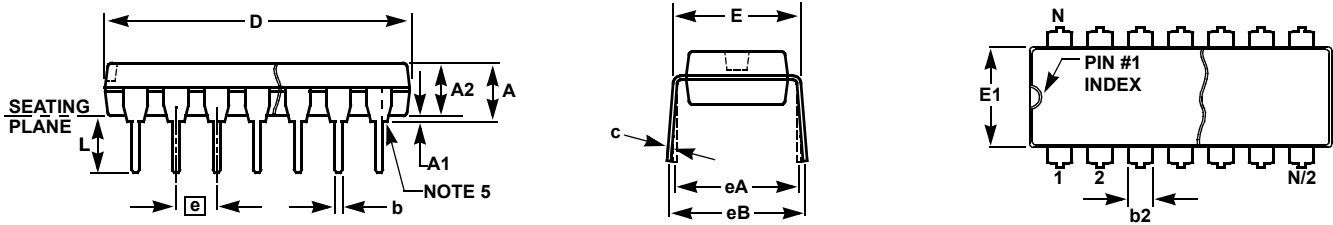
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

**Plastic Dual-In-Line Packages (PDIP)**



**MDP0031**

**PLASTIC DUAL-IN-LINE PACKAGE**

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

**NOTES:**

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

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