THE DATASHEET OF

DS92LV1021AMSA

DS92LV1021A 16-40 MHz 10 Bit Bus LVDS Serializer

Check for Samples: DS92LV1021A

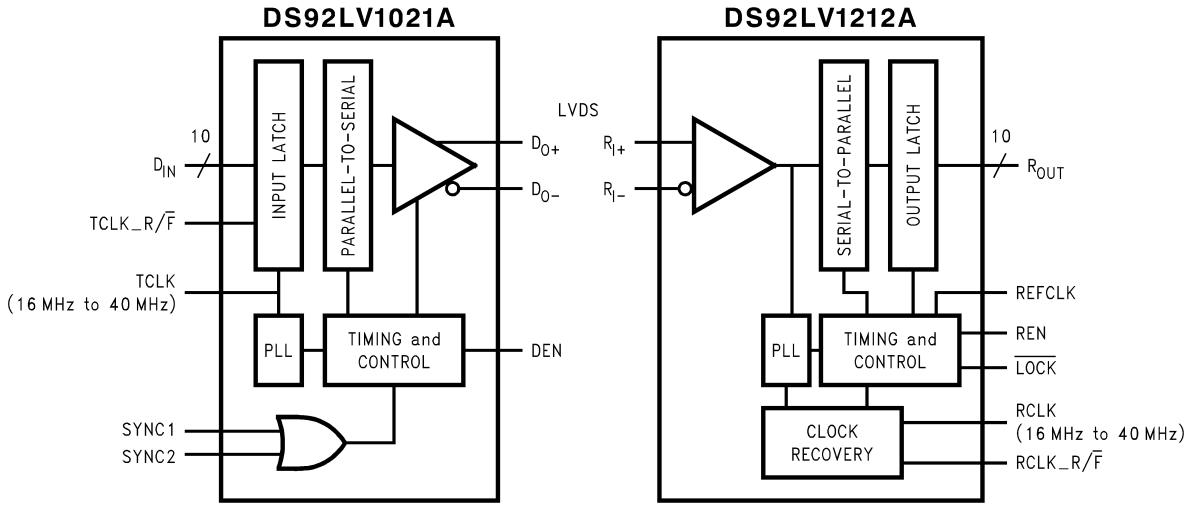
FEATURES

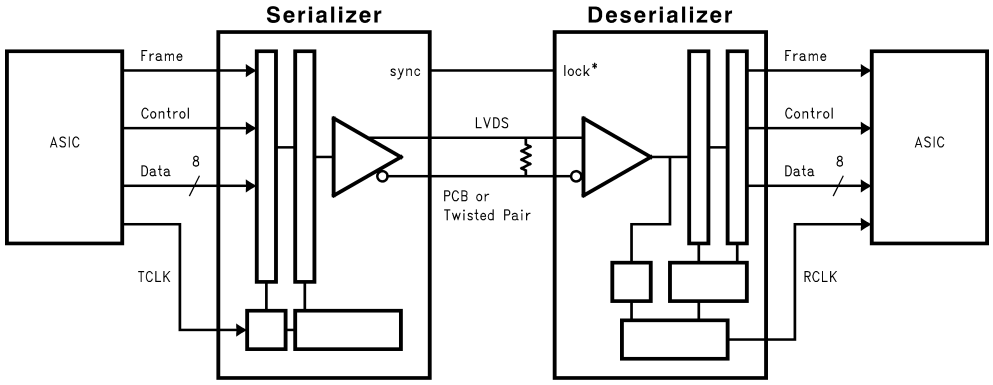
- **Specified Transition Every Data Transfer Cycle**
- **Single Differential Pair Eliminates Multi-Channel Skew**
- **Flow-Through Pinout for Easy PCB Layout**
- **400 Mbps Serial Bus LVDS Bandwidth (at 40 MHz Clock)**
- **10-bit Parallel Interface for 1 Byte Data Plus 2 Control Bits**
- **Programmable Edge Trigger on Clock**
- **Bus LVDS Serial Output Rated for 27Ω Load**
- **Small 28-Lead SSOP Package-DB**

DESCRIPTION

The DS92LV1021A transforms a 10-bit wide parallel LVCMOS/LVTTL data bus into a single high speed Bus LVDS serial data stream with embedded clock. The DS92LV1021A can transmit data over backplanes or cable. The single differential pair data path makes PCB design easier. In addition, the reduced cable, PCB trace count, and connector size tremendously reduce cost. Since one output transmits both clock and data bits serially, it eliminates clock-to-data and data-to-data skew. The powerdown pin saves power by reducing supply current when the device is not being used. Upon power up of the Serializer, you can choose to activate synchronization mode or use one of TI's Deserializers in the synchronization-to-random-data feature. By using the synchronization mode, the Deserializer will establish lock to a signal within specified lock times. In addition, the embedded clock specifies a transition on the bus every 12-bit cycle. This eliminates transmission errors due to charged cable conditions. Furthermore, you may put the DS92LV1021A output pins into TRI-STATE to achieve a high impedance state. The PLL can lock to frequencies between 16 MHz and 40 MHz.

Block Diagram





Functional Description

The DS92LV1021A is an upgrade to the DS92LV1021. The DS92LV1021A no longer has a power-up sequence requirement. Like the DS92LV1021, the DS92LV1021A is a 10-bit Serializer designed to transmit data over a differential backplane at clock speeds from 16 to 40MHz. It may also be used to drive data over Unshielded Twisted Pair (UTP) cable.

The DS92LV1021A can be used with any of TI's 10-bit BLVDS Deserializers (DS92LV1212A for example) and has three active states of operation: Initialization, Data Transfer, and Resynchronization; and two passive states: Powerdown and TRI-STATE.

The following sections describe each active and passive state.

Initialization

Before data can be transferred, the Serializer must be initialized. Initialization refers to synchronization of the Serializer's PLL to a local clock.

When V_{CC} is applied to the Serializer, the outputs are held in TRI-STATE and internal circuitry is disabled by on-chip power-on circuitry. When V_{CC} reaches V_{CC} OK (2.5V) the Serializer's PLL begins locking to the local clock. The local clock is the transmit clock, TCLK, provided by the source ASIC or other device.

Once the PLL locks to the local clock, the Serializer is ready to send data or SYNC patterns, depending on the levels of the SYNC1 and SYNC2 inputs. The SYNC pattern is composed of six ones and six zeros switching at the input clock rate.

Control of the SYNC pins is left to the user. One recommendation is a direct feedback loop from the $\overline{\text{LOCK}}$ pin. Under all circumstances, the Serializer stops sending SYNC patterns after both SYNC inputs return low.

Data Transfer

After initialization, the Serializer inputs DIN0–DIN9 may be used to input data to the Serializer. Data is clocked into the Serializer by the TCLK input. The edge of TCLK used to strobe the data is selectable via the TCLK_R/$\overline{\text{F}}$ pin. TCLK_R/$\overline{\text{F}}$ high selects the rising edge for clocking data and low selects the falling edge. If either of the SYNC inputs is high for 5*TCLK cycles, the data at DIN0-DIN9 is ignored regardless of the clock edge.

A start bit and a stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

Serialized data and clock bits (10+2 bits) are transmitted from the serial data output (DO±) at 12 times the TCLK frequency. For example, if TCLK is 40 MHz, the serial rate is 40 × 12 = 480 Mega bits per second. Since only 10 bits are from input data, the serial "payload" rate is ten times the TCLK frequency. For instance, if TCLK = 40 MHz, the payload data rate is 40 × 10 = 400 Mbps. TCLK is provided by the data source and must be in the range of 16 MHz to 40 MHz nominal.

The outputs (DO±) can drive a backplane or a point-to-point connection. The outputs transmit data when the enable pin (DEN) is high, $\overline{\text{PWRDN}}$ is high, and SYNC1 and SYNC2 are low. The DEN pin may be used to TRI-STATE the outputs when driven low.

Ideal Crossing Point

The ideal crossing point is the best case start and stop point for a normalized bit. Each ideal crossing point is found by dividing the clock period by twelve--two clock bits plus ten data bits. For example, a 40 MHz clock has a period of 25ns. The 25ns divided by 12 bits is approximately 2.08ns. This means that each bit width is approximately 2.08ns, and the ideal crossing points occur every 2.08ns. For a graphical representation, please see Figure 9.

Resynchronization

The Deserializer $\overline{\text{LOCK}}$ pin driven low indicates that the Deserializer PLL is locked to the embedded clock edge. If the Deserializer loses lock, the $\overline{\text{LOCK}}$ output will go high and the outputs (including RCLK) will be TRI-STATE.

The $\overline{\text{LOCK}}$ pin must be monitored by the system to detect a loss of synchronization, and the system must decide if it is necessary to pulse the Serializer SYNC1 or SYNC2 pin to resynchronize. There are multiple approaches possible. One recommendation is to provide a feedback loop using the $\overline{\text{LOCK}}$ pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). At the time of publication, other than the DS92LV1210, all other Deserializers from TI have random lock capability. This feature does not require the system user to send SYNC patterns upon loss of lock. However, lock times can only be specified with transmission of SYNC patterns. Dual SYNC pins are provided for multiple control in a multi-drop application.

Powerdown

The Powerdown state is a low power sleep mode that the Serializer and Deserializer may use to reduce power when no data is being transferred. The device enters Powerdown when the $\overline{\text{PWRDN}}$ pin is driven low on the Serializer. In Powerdown, the PLL stops and the outputs go into TRI-STATE, disabling load current and reducing supply current into the milliamp range. To exit Powerdown, $\overline{\text{PWRDN}}$ must be driven high.

Both the Serializer and Deserializer must reinitialize and resynchronize before data can be transferred. The Deserializer will initialize and assert $\overline{\text{LOCK}}$ high until it is locked to the Bus LVDS clock.

TRI-STATE

For the Serializer, TRI-STATE is entered when the DEN pin is driven low. This will TRI-STATE both driver output pins (DO+ and DO−). When DEN is driven high, the serializer will return to the previous state as long as all other control pins remain static (SYNC1, SYNC2, $\overline{\text{PWRDN}}$, TCLK_R/F).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} +0.3V)
CMOS/TTL Output Voltage	−0.3V to (V_{CC} +0.3V)
Bus LVDS Receiver Input Voltage	−0.3V to +3.9V
Bus LVDS Driver Output Voltage	−0.3V to +3.9V
Bus LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	+260°C
Maximum Package Power Dissipation Capacity @ 25°C Package: 28L SSOP	1.27 W
Package Derating: 28L SSOP	10.2 mW/°C above +25°C
ESD Rating (HBM)[3]	>2.0kV

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) With a limited Engineering sample size, ESD (HBM) testing passed 2.5kV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
Supply Noise Voltage (V_{CC})			100	mV_{P-P}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
SERIALIZER CMOS/TTL DC SPECIFICATIONS (apply to DIN0-9, TCLK, $\overline{PWRDN}$, TCLK_R/$\overline{F}$, SYNC1, SYNC2, DEN)							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V		−10	±2	+10	µA
SERIALIZER Bus LVDS DC SPECIFICATIONS (apply to pins DO+ and DO−)							
V_{OD}	Output Differential Voltage (DO+)–(DO−)	RL = 27Ω		200	270		mV
ΔV_{OD}	Output Differential Voltage Unbalance					35	mV
V_{OS}	Offset Voltage			0.78	1.1	1.3	V
ΔV_{OS}	Offset Voltage Unbalance					35	mV
I_{OS}	Output Short Circuit Current	D0 = 0V, DIN = High, $\overline{PWRDN}$ and DEN = 2.4V			−30	−40	mA
I_{OZ}	TRI-STATE Output Current	$\overline{PWRDN}$ or DEN = 0.8V, DO = 0V or VCC		−10	±1	+10	µA
I_{OX}	Power-Off Output Current	VCC = 0V, DO = 0V or VCC		−20	±1	+20	µA
SERIALIZER SUPPLY CURRENT (apply to pins DVCC and AVCC)							
I_{CCD}	Worst Case Serializer Supply Current	RL = 27Ω, Figure 1	f = 40 MHz		40	55	mA
			f = 16 MHz		28	35	mA
I_{CCXD}	Serializer Supply Current Powerdown	$\overline{PWRDN}$ = 0.8V			88	300	µA

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Serializer Timing Requirements for TCLK

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period		25	T	62.5	ns
t_{TCIH}	Transmit Clock High Time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Clock Low Time		0.4T	0.5T	0.6T	ns
t_{CLKT}	TCLK Input Transition Time			3	6	ns
t_{JIT}	TCLK Input Jitter				150	ps (RMS)

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{LLHT}	Bus LVDS Low-to-High Transition Time	R_L = 27Ω, Figure 2, C_L=10pF to GND			0.31	0.75	ns
t_{LHLT}	Bus LVDS High-to-Low Transition Time				0.30	0.75	ns
t_{DIS}	DIN (0-9) Setup to TCLK	See Figure 4, R_L = 27Ω, C_L=10pF to GND		0			ns
t_{DIH}	DIN (0-9) Hold from TCLK			4.0			ns
t_{HZD}	DO ± HIGH to TRI-STATE Delay	See Figure 5 , (3), R_L = 27Ω, C_L=10pF to GND			3.5	10	ns
t_{LZD}	DO ± LOW to TRI-STATE Delay				2.9	10	ns
t_{ZHD}	DO ± TRI-STATE to HIGH Delay				2.5	10	ns
t_{ZLD}	DO ± TRI-STATE to LOW Delay				2.7	10	ns
t_{SPW}	SYNC Pulse Width	See Figure 7, R_L = 27Ω		$5*t_{TCP}$			ns
t_{PLD}	Serializer PLL Lock Time	See Figure 6, R_L = 27Ω		$510*t_{TCP}$		$2049*t_{TCP}$	ns
t_{SD}	Serializer Delay	See Figure 8 , R_L = 27Ω		t_{TCP}+1.0	t_{TCP} + 2.0	t_{TCP}+4.0	ns
t_{BIT}	Bus LVDS Bit Width	R_L = 27Ω, C_L=10pF to GND			t_{CLK} / 12		ns
t_{DJIT}	Deterministic Jitter	R_L = 27Ω, C_L=10pF to GND, (4)	f = 40 MHz	−320	−110	150	ps
			f = 16 MHz	−800	−160	380	ps

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.
(3) Due to TRI-STATE of the Serializer, the Deserializer will lose PLL lock and have to resynchronize before data transfer.
(4) t_{DJIT} specifications are specified by design using statistical analysis.

AC Timing Diagrams and Test Circuits

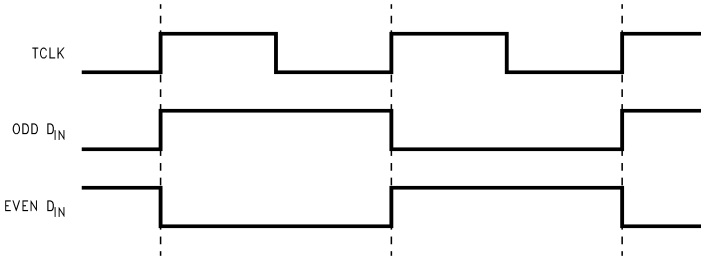


Figure 1. "Worst Case" Serializer ICC Test Pattern

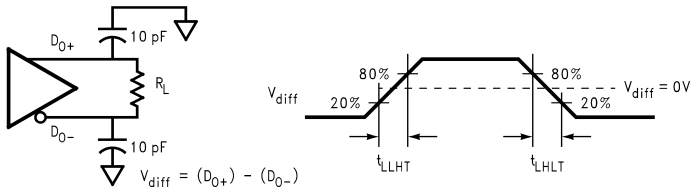


Figure 2. Serializer Bus LVDS Output Load and Transition Times

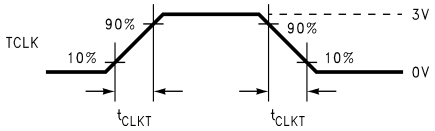
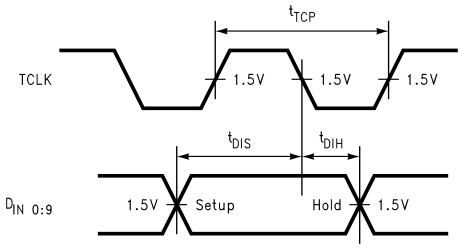
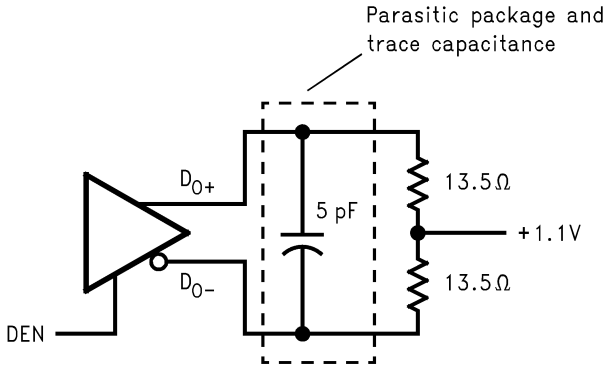


Figure 3. Serializer Input Clock Transition Time



Timing shown for TCLK_R/$\overline{F}$ = LOW

Figure 4. Serializer Setup/Hold Times



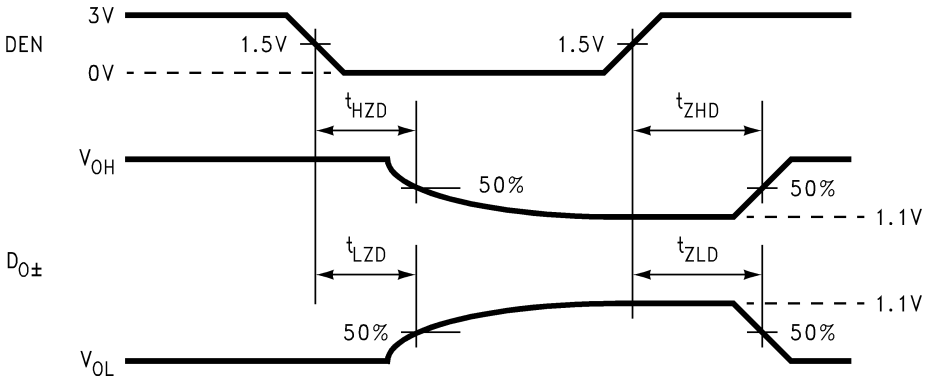


Figure 5. Serializer TRI-STATE Test Circuit and Timing

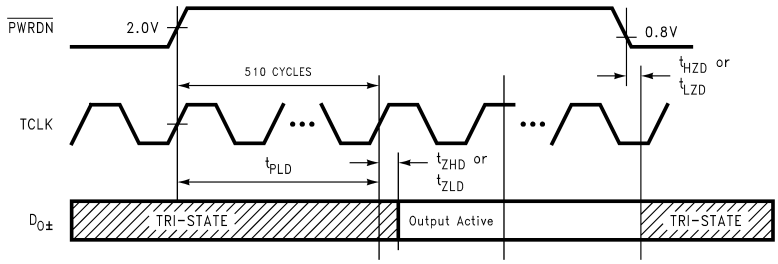


Figure 6. Serializer PLL Lock Time, and $\overline{\text{PWRDN}}$ TRI-STATE Delays

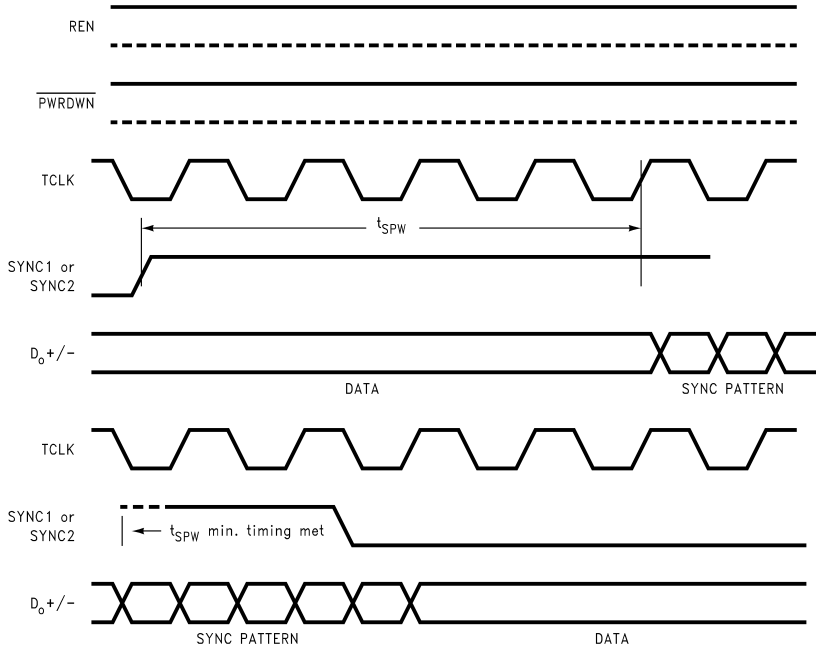


Figure 7. SYNC Timing Delays

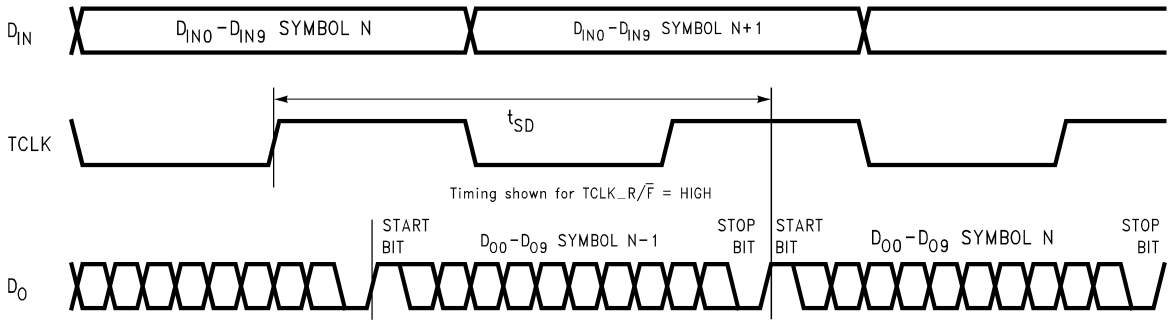
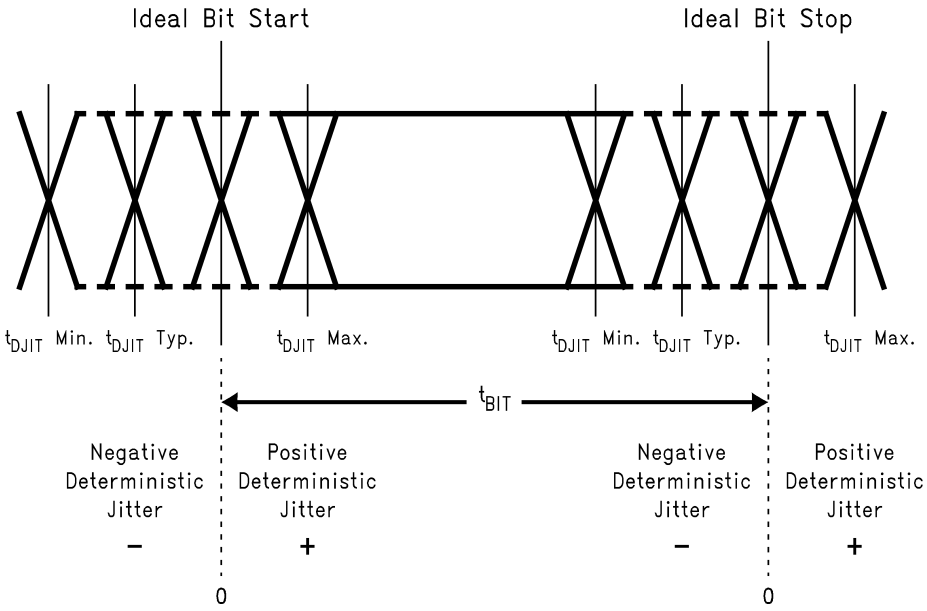


Figure 8. Serializer Delay



For an explanation of the Ideal Crossing Point, please see the Application Information Section.

Figure 9. Serializer Deterministic Jitter and Ideal Crossing Point

APPLICATION INFORMATION

DIFFERENCES BETWEEN THE DS92LV1021A AND THE DS92LV1021

The DS92LV1021A is an enhanced version of the DS92LV1021. The following enhancements are provided by the DS92LV1021A:

- TCLK may be applied before power
- TCLK may be halted
- Slower typical edge rates help to reduce reflections
- $\overline{\text{PWRDN}}$ pin includes an internal weak pull down device

Like the DS92LV1021, the DS92LV1021A is a 10-bit Serializer designed to transmit data over a differential backplane at clock speeds from 16 to 40MHz. It may also be used to drive data over Unshielded Twisted Pair (UTP) cable.

USING THE DS92LV1021A

The Serializer is an easy to use transmitter that sends 10 bits of parallel TTL data over a serial Bus LVDS link up to 400 Mbps. Serialization of the input data is accomplished using an onboard PLL which embeds two clock bits with the data.

POWER CONSIDERATIONS

An all CMOS design of the Serializer makes it an inherently low power device. Additionally, the constant current source nature of the Bus LVDS outputs minimize the slope of the speed vs. I_{CC} curve of CMOS designs.

DIGITAL AND ANALOG POWER PINS

Digital and Analog power supply pins should be at the same voltage levels. The user should verify that voltage levels at the digital and analog supply pins are at the same voltage levels after board layout and after bypass capacitors are added.

HOT INSERTION

All Bus LVDS devices are hot pluggable if you follow a few rules. When inserting, ensure the Ground pin(s) makes contact first, then the VCC pin(s), and then the I/O pins. When removing, the I/O pins should be unplugged first, then the VCC, then the Ground.

TRANSMITTING DATA

Once the Serializer and Deserializer are powered up and running they must be phase locked to each other in order to transmit data. Phase locking can be accomplished by the Serializer sending SYNC patterns to the Deserializer, or by using the Deserializer's random lock capability. SYNC patterns are sent by the Serializer whenever SYNC1 or SYNC2 inputs are held high. The $\overline{\text{LOCK}}$ output of the Deserializer is high whenever the Deserializer is not locked. Connecting the $\overline{\text{LOCK}}$ output of the Deserializer to one of the SYNC inputs of the Serializer will specifiy that enough SYNC patterns are sent to achieve Deserializer lock.

While the Deserializer $\overline{\text{LOCK}}$ output is low, data at the Deserializer outputs (ROUT0-9) is valid except for the specific case of loss of lock during transmission.

RECOVERING FROM LOCK LOSS

In the case where the Serializer loses lock during data transmission up to three cycles of data that was previously received can be invalid. This is due to the delay in the lock detection circuit. The lock detect circuit requires that invalid clock information be received 4 times in a row to indicate loss of lock. Since clock information has been lost it is possible that data was also lost during these cycles. When the Deserializer $\overline{\text{LOCK}}$ pin goes low, data from at least the previous three cycles should be resent upon regaining lock.

Lock can be regained at the Deserializer by causing the Serializer to resend SYNC patterns as described above.

PCB CONSIDERATIONS

The Bus LVDS devices Serializer and Deserializer should be placed as close to the edge connector as possible. In multiple Deserializer applications, the distance from the Deserializer to the slot connector appears as a stub to the Serializer driving the backplane traces. Longer stubs lower the impedance of the bus increasing the load on the Serializer and lowers threshold margin at the Deserializers. Deserializer devices should be placed no more than 1 inch from the slot connector.

TRANSMISSION MEDIA

The Serializer and Deserializer are designed for data transmission over a multi-drop bus. Multi-drop buses use a single Serializer and multiple Deserializer devices. Since the Serializer can be driving from any point on the bus, the bus must be terminated at both ends. For example, a 100 Ohm differential bus must be terminated at each end with 100 Ohms lowering the DC impedance that the Serializer must drive to 50 Ohms. This load is further lowered by the addition of multiple Deserializers. Adding up to 20 Deserializers to the bus (depending upon spacing) will lower the total load to about 27 Ohms (54 Ohm bus). The Serializer is designed for DC loads between 27 and 100 Ohms.

The Serializer and Deserializer can also be used in point-to-point configuration of a backplane, PCB trace or through a twisted pair cable. In point-to-point configurations the transmission media need only be terminated at the receiver end. In the point-to-point configuration the potential of offsetting the ground levels of the Serializer vs. the Deserializer must be considered. Bus LVDS provides a plus / minus one volt common mode range at the receiver inputs.

PIN DIAGRAM

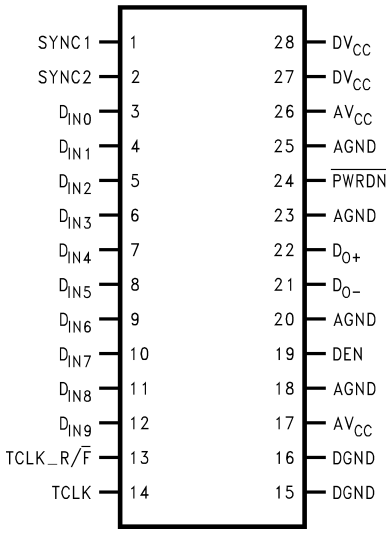


Figure 10. DS92LV1021AMSA - Serializer

Serializer Pin Description

Pin Name	I/O	No.	Description
DIN	I	3–12	Data Input. TTL levels inputs. Data on these pins are loaded into a 10-bit input register.
TCLK_R/$\overline{F}$	I	13	Transmit Clock Rising/Falling strobe select. TTL level input. Selects TCLK active edge for strobing of DIN data. High selects rising edge. Low selects falling edge.
DO+	O	22	+ Serial Data Output. Non-inverting Bus LVDS differential output.
DO−	O	21	− Serial Data Output. Inverting Bus LVDS differential output.
DEN	I	19	Serial Data Output Enable. TTL level input. A low, puts the Bus LVDS outputs in TRI-STATE.
$\overline{PWRDN}$	I	24	Powerdown. TTL level input. $\overline{PWRDN}$ driven low shuts down the PLL and TRI-STATEs the outputs putting the device into a low power sleep mode. This pin has an internal weak pull down.
TCLK	I	14	Transmit Clock. TTL level input. Input for 16 MHz–40 MHz (nominal) system clock.
SYNC	I	1, 2	Assertion of SYNC (high) for at least 1024 synchronization symbols to be transmitted on the Bus LVDS serial output. Synchronization symbols continue to be sent if SYNC continues asserted. TTL level input. The two SYNC pins are ORed.
DVCC	I	27, 28	Digital Circuit power supply. DVCC voltage level should be identical to the AVCC voltage level.
DGND	I	15, 16	Digital Circuit ground. Ground potential should be the same as AGND.
AVCC	I	17, 26	Analog power supply (PLL and Analog Circuits). AVCC voltage level should be identical to the DVCC voltage level.
AGND	I	18, 25, 20, 23	Analog ground (PLL and Analog Circuits). Ground potential should be the same as DGND.

Truth Table(1)

DIN (0–9)	TCLK_R/$\overline{F}$	TCLK	SYNC1/SYNC2	DEN	$\overline{PWRDN}$	DO+	DO−
X	X	X	X	X	0	Z	Z
X	X	X	X	0	1	Z	Z
X	X	SYSTEM CLK	1~	1	1	SYNC PTRN	SYNC PTRN*
DATA	1		0	1	1	DATA (0–9)	DATA (0–9)*
DATA	0		0	1	1	DATA (0–9)	DATA (0–9)*

RI	RI−	RCLK_R/$\overline{F}$	REFCLK	REN	$\overline{PWRDN}$	RCLK	$\overline{LOCK}$
X	X	X	X	X	0	Z	Z
X	X	X	X	0**	1	Z	Z
SYNC PTRN	SYNC PTRN*	X	SYSTEM CLK	1	1	CLK	1†
DATA (0–9)	DATA (0–9)*	1	SYSTEM CLK	1	1		0
DATA (0–9)	DATA (0–9)*	0	SYSTEM CLK	1	1		0

(1) ~ Pulse 5-bits
* Inverted
†Must be 1 before SYNC PTRN starts
** Device must be locked first

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS92LV1021AMSA	NRND	SSOP	DB	28	47	TBD	Call TI	Call TI	-40 to 85	DS92LV1021A MSA >B	
DS92LV1021AMSA/NOPB	LIFEBUY	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	DS92LV1021A MSA >B	
DS92LV1021AMSAX/NOPB	LIFEBUY	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	DS92LV1021A MSA >B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

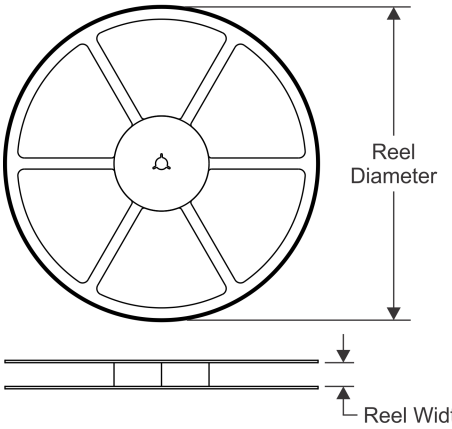
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

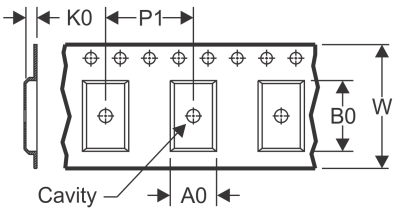
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

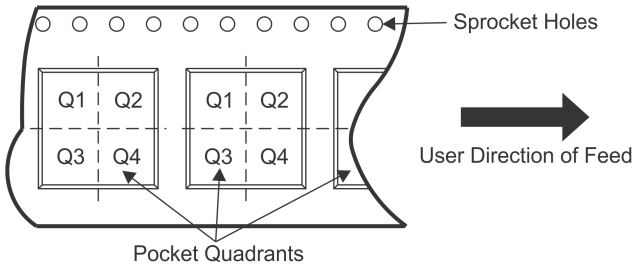


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

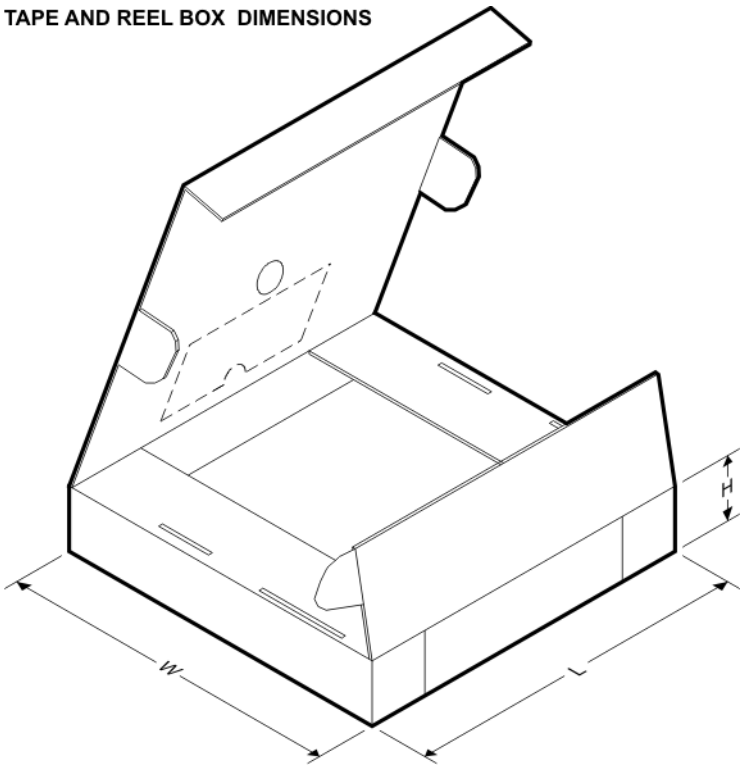
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV1021AMSAX/NOPB	SSOP	DB	28	2000	330.0	16.4	8.4	10.7	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

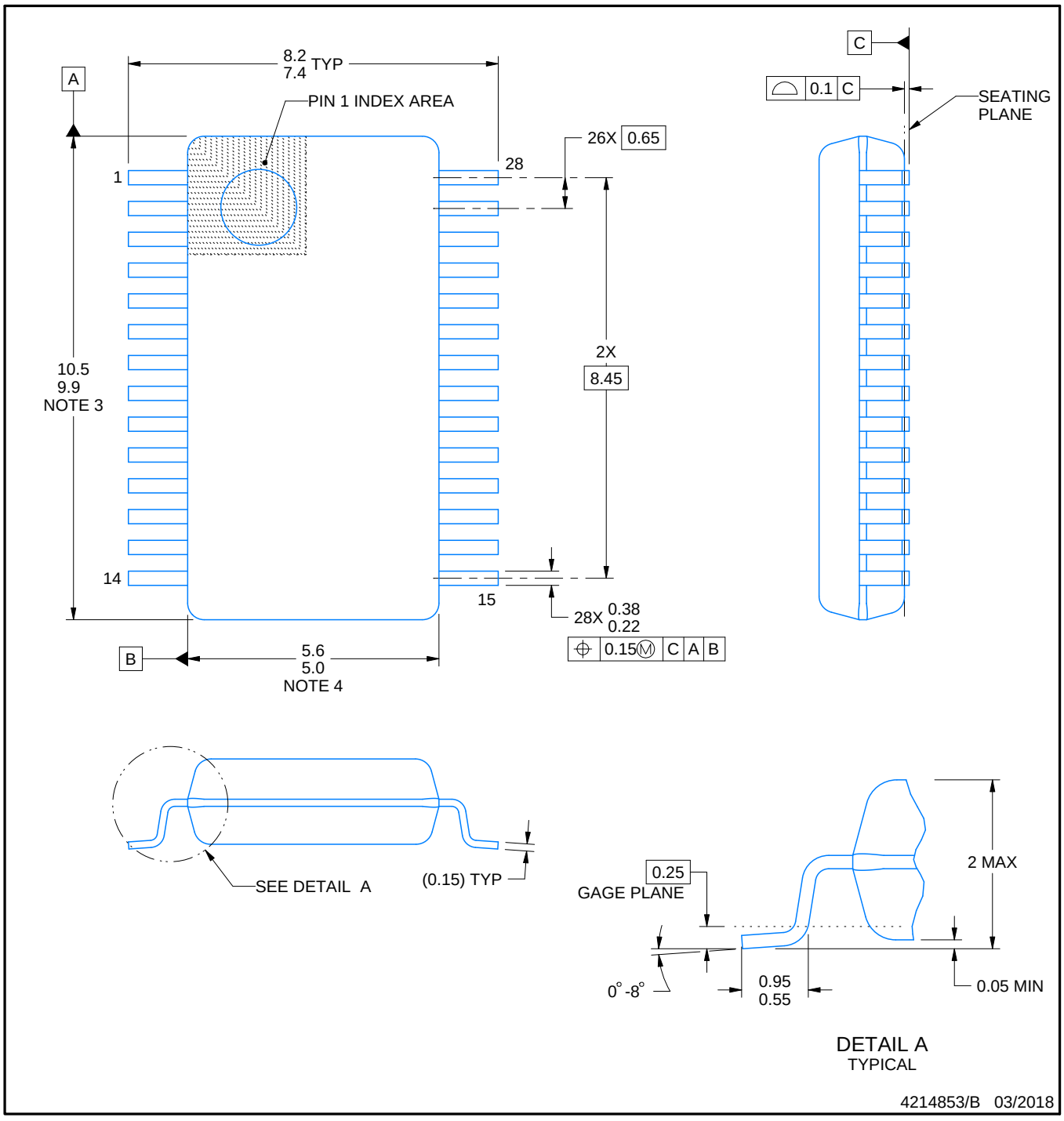
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV1021AMSAX/NOPB	SSOP	DB	28	2000	367.0	367.0	38.0

PACKAGE OUTLINE

DB0028A

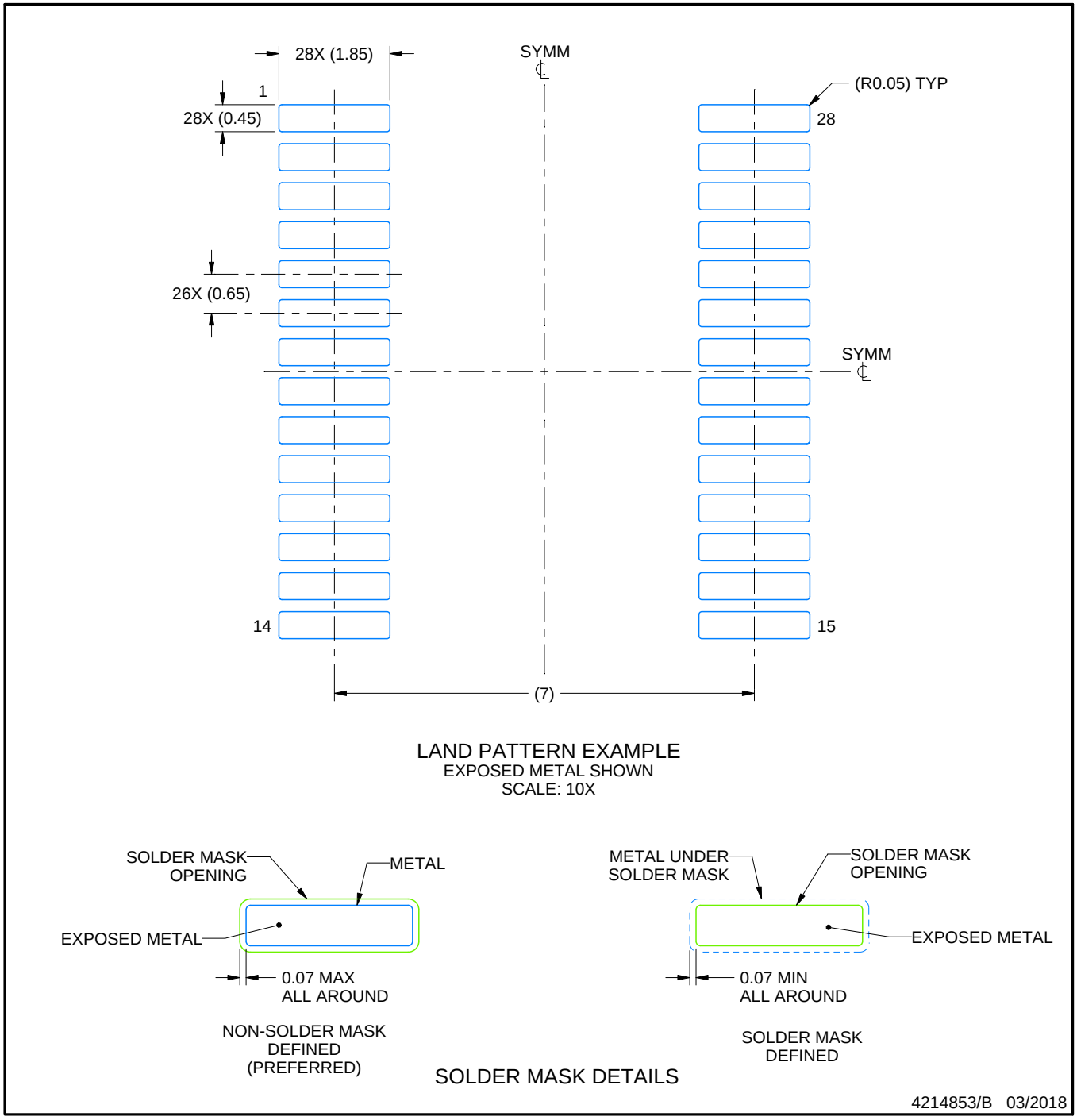
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



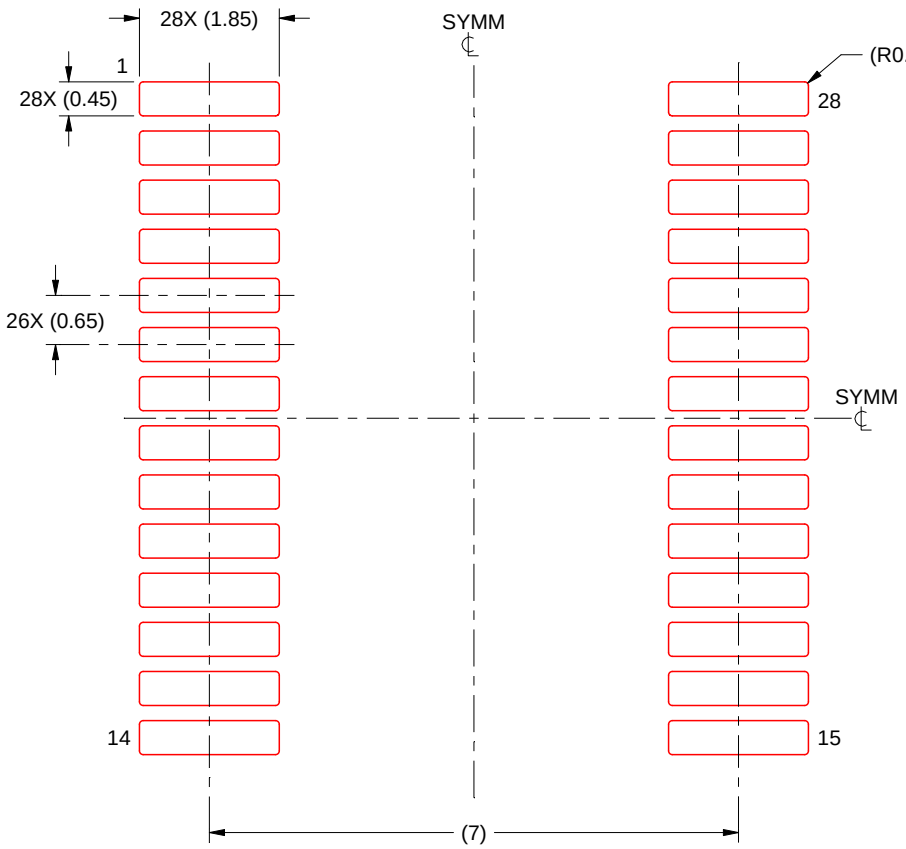
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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