THE DATASHEET OF

171040302

171040302

MagI³C Power Module

VDRM – Variable Step Down Regulator Module

2.95 – 6V / 4A / 0.8 – 3.6V Output

DESCRIPTION

The VDRM 1710x0302 series of the MagI³C Power Module family provide a fully integrated DC-DC power supply including the switching regulator with integrated MOSFETs, compensation and shielded inductor in one package. These modules require as few as 4 external components.

The 171040302 offers high efficiency and delivers up to 4A of output current. It operates with an input voltage from 2.95 to 6V and is designed for fast transient response.

It is available in a standard industrial high power density QFN package (11mm x 9mm x 2.8mm) with very good thermal performance.

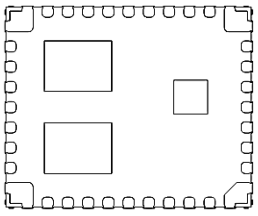
This module has an on-board protection circuitry to guard against thermal overstress and electrical damage featuring thermal shutdown, overcurrent, short circuit, overvoltage and undervoltage protections.

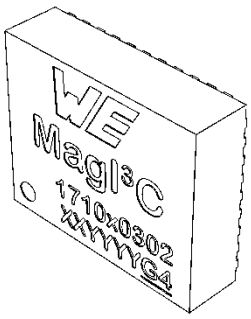
TYPICAL APPLICATIONS

- Point-of-load DC-DC applications from 5V and 3.3V rails
- Industrial, test & measurement, medical applications
- Communication infrastructure
- System power supplies
- DSPs, FPGAs, MCUs and MPU supply
- I/O interface power supply
- High density distributed power systems

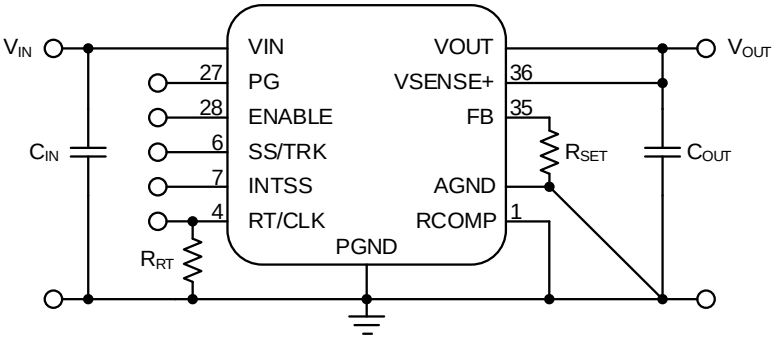
FEATURES

- Peak efficiency up to 96%
- Current capability up to 4A
- Input voltage range: 2.95 to 6V
- Output voltage range: 0.8 to 3.6V
- Continuous output power: 14.4W
- Integrated shielded inductor
- Low output voltage ripple: 5mV typ.
- Reference accuracy over temperature: 1% max.
- Adjustable switching frequency: 0.5 to 2 MHz
- Current Mode control
- Synchronous operation
- Forced continuous mode
- Undervoltage lockout protection (UVLO)
- Adjustable soft-start and voltage tracking
- Frequency synchronization to an external clock
- Sequencing
- Thermal shutdown
- Short circuit protection
- Cycle-by-cycle current limit
- Output overvoltage protection
- Power good indicator
- Pin compatible with 171020302 & 171060302
- Operating ambient temperature up to 85°C
- No derating within the operating temperature range
- Operating junction temp. range: -40 to 125°C
- UL94V-0 package material
- Complies with EN55022 class B radiated emissions standard





TYPICAL CIRCUIT DIAGRAM



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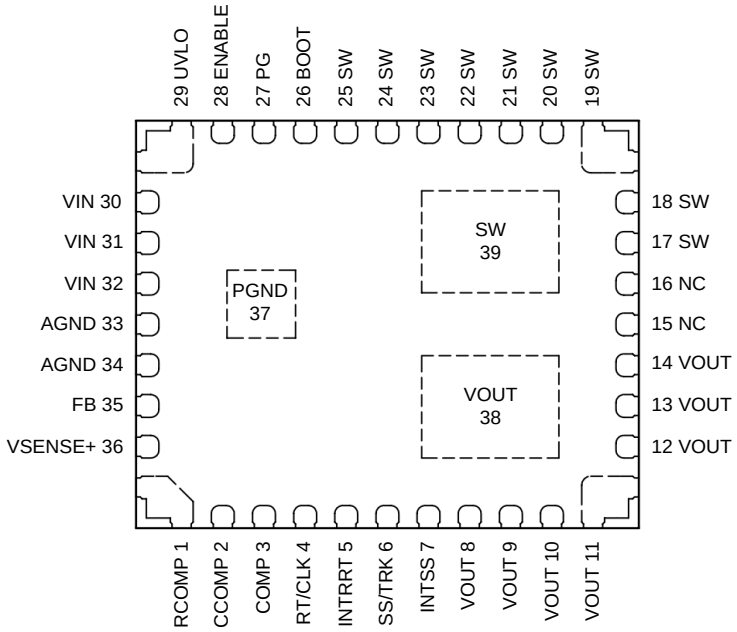
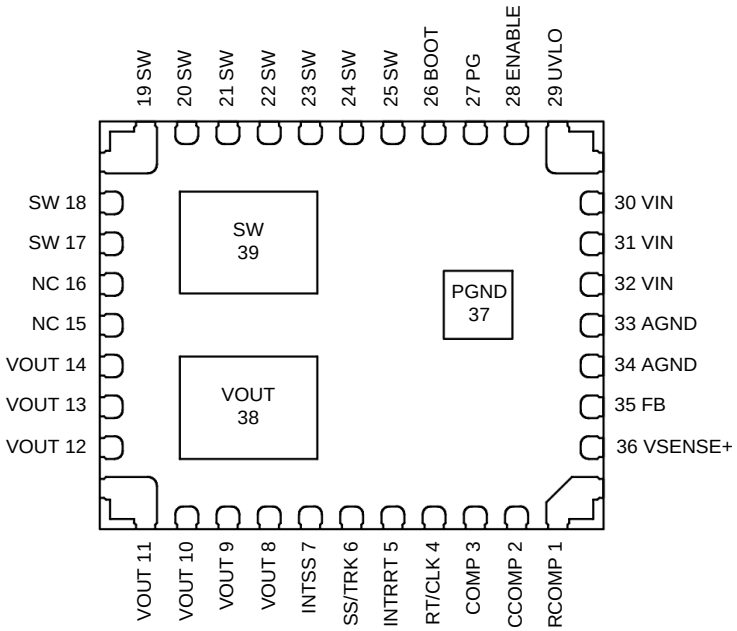
PACKAGE



Top View



Bottom View

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PIN DESCRIPTION

SYMBOL	NUMBER	TYPE	DESCRIPTION
VIN	30,31,32	Power	Input Voltage. Place input capacitors as close as possible
VOUT	8,9,10,11, 12,13,14, 38	Power	Output voltage. Place output capacitors as close as possible. For thermal performance use copper plane(s) at these pins.
AGND	33,34	Supply	Analog ground for internal circuitry. Connect to power ground
PGND	37	Power	Power ground for the internal switching circuitry. Connect to copper plane(s) with thermal vias for thermal performance.
VSENSE+	36	Input	Connect to positive terminal of the output capacitor. An internal resistor of 1430 Ω is connected internally between V_{SENSE+} and FB. This is the top resistor of the feedback voltage divider.
FB	35	Input	A resistor (R_{SET}) from FB to sets the output voltage. This is the bottom resistor of the feedback voltage divider.
RT/CLK	4	Input	An external resistor from RT/CLK to AGND adjusts the switching frequency of the device. This pin can also be used to synchronize the switching frequency of the module to an external clock.
INTRRT	5	Analog	Internal resistor which sets the default switching frequency.
RCOMP	1	Analog	Internal resistor of the compensation network. Must be connected to AGND.

OPTIONAL

SYMBOL	NUMBER	TYPE	DESCRIPTION
UVLO	29	Input	An internal undervoltage lock out resistor of 34kΩ is connected to the enable pin. If pin 29 is connected to analog ground, the internal UVLO resistor divider will be activated. For input voltages below 3.3V this pin should be left open and an optional resistor from enable to analog ground sets the UVLO to values between 2.95 and 3.3 V.
ENABLE	28	Input	Enable pin. Internally pull-up current source. Pull to analog ground to disable the module . Can be left floating to enable the module.
PG	27	Output	Open drain output. The PG pin pulls low during thermal shutdown, over-current, output overvoltage or undervoltage or disabled device. A pull-up resistor is required.
SS/TRK	6	Input	Internal current source to charge the soft start capacitor. Connect an external capacitor to optionally increase the soft-start time. A voltage applied to this pin allows tracking and sequencing.
INTSS	7	Analog	An internal 3.3nF capacitor is connected to this pin. If pin 7 is connected to analog ground, a 1.1ms soft start time is selected.

AUXILIARY

SYMBOL	NUMBER	TYPE	DESCRIPTION
COMP	3	Output	Output of the error amplifier. Do not connect this pin
CCOMP	2	Analog	Internal capacitor of the compensation network. Do not connect this pin.
BOOT	26	Supply	Internal bootstrap pin for the high side MOSFET.
SWITCH	17,18,19, 20,21,22, 23,24,25, 39	Power	Internal switch node. Do not connect these pins.
NC	15,16		Not connected to internal circuitry.

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ORDERING INFORMATION

ORDER CODE	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
171040302	4A / 14.4W version	BQFN-39	Tape and Reel, 250 pieces
178040302	4A / 14.4W version	Eval Board	1

PIN COMPATIBLE FAMILY MEMBERS

ORDER CODE	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
171020302	2A / 7.2W version	BQFN-39	Tape and Reel, 250 pieces
178020302	2A / 7.2W version	Eval Board	1
171060302	6A / 21.6W version	BQFN-39	Tape and Reel, 250 pieces
178060302	6A / 21.6W version	Eval Board	1

PACKAGE SPECIFICATIONS

Weight	Molding compound	UL class	Certificate number
0.54g	EME-G770H	UL94 V-0	E41429

SALES INFORMATION

SALES CONTACT
Würth Elektronik eiSos GmbH & Co. KG EMC & Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 7942 945 0 www.we-online.com/powermodules Technical support: powermodules@we-online.com

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ABSOLUTE MAXIMUM RATINGS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN (1)	MAX (1)	
VIN	Input pin voltage	-0.3	7	VIN
VOUT	Output pin voltage	-0.6	V_{IN}	VOUT
FB	Feedback pin voltage	-0.3	3	FB
UVLO	Undervoltage lockout pin voltage	-0.3	3.3	UVLO
EN	Enable pin Voltage	-0.3	7	EN
	Enable pin source current	-	100	
RT/CLK	RT/CLK pin voltage	-0.3	6	RT/CLK
	RT/CLK pin current	-	±100	
SS/TRK	SS/TRK pin voltage	-0.3	3	SS/TRK
	SS/TRK pin current	-	±100	
PG	Power Good pin voltage	-0.3	7	PG
	Power Good pin current	-	10	
COMP	COMP pin voltage	-0.3	3	COMP
	COMP pin current	-	100	
INTSS	INTSS pin voltage	-0.3	3	INTSS
INTRRT	INTRRT pin voltage	-0.3	6	INTRRT
RCOMP	RCOMP pin voltage	-0.3	3	RCOMP
CCOMP	CCOMP pin voltage	-0.3	3	CCOMP
VSENSE+	VSENSE+ pin voltage	-0.3	V_{out}	VSENSE+
SW	SW pin voltage	-0.6	7	SW
	10ns transient	-2	7	
BOOT	BOOT pin voltage	-	V_{SW} +8V	BOOT
$T_{storage}$	Assembled, non operating storage temperature	-65	150	$T_{storage}$
T_{SOLR}	Peak case/leads temperature during reflow soldering, max. 30sec. (JEDEC J-STD020) Maximum three cycles!	-	245±5	T_{SOLR}
Mechanical shock: Mil-STD-883D, Method 2002.2, 1ms, ½ sine, mounted		-	1500	G
Mechanical vibration: Mil-STD-883D, Method 2007.2, 20-2000Hz		-	20	G

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OPERATING CONDITIONS

Operating conditions are conditions under which operation of the device is intended to be functional. All values are referenced to GND.

MIN and MAX limits are valid for the recommended ambient temperature range of **-40°C to 85°C**. Typical values represents statistically the utmost probability at following conditions: V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 4A, C_{IN1} = 47µF ceramic, C_{IN2} = 220µF polymer electrolytic, C_{OUT1} = 47µF ceramic, C_{OUT2} = 100µF poly-tantalum unless otherwise noted.

SYMBOL	PARAMETER	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{IN}	Input voltage	2.95	-	6	V
V_{OUT}	Output voltage (depending on input voltage and switching frequency)	0.8	-	3.6	V
T_A	Ambient temperature range	-40	-	85 (3)	°C
T_{JOP}	Junction temperature range	-40	-	125	°C
I_{OUT}	Nominal output current			4	A

THERMAL SPECIFICATIONS

SYMBOL	PARAMETER	TYP (2)	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance (4)	12	°C/W
Ψ_{JT}	Junction-to-top(5)	2.2	°C/W
Ψ_{JB}	Junction-to-board(6)	9.7	°C/W
T_{SD}	Thermal shutdown, rising	175	°C
	Thermal shutdown hysteresis, falling	15	°C

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ELECTRICAL SPECIFICATIONS

MIN and MAX limits are valid for the recommended ambient temperature range of **-40°C to 85°C**. Typical values represents statistically the utmost probability at following conditions: V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 4A, C_{IN1} = 47µF ceramic, C_{IN2} = 220µF polymer electrolytic, C_{OUT1} = 47µF ceramic, C_{OUT2} = 100µF poly-tantalum unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
Output current						
I_{OCP}	Over current protection		-	7	-	A
Accuracy						
V_{FB}	Reference accuracy	T_A = 25°C, I_{OUT} = 0A with internal feedback resistor	-	-	±1(7)	%
	Temperature variation	-40°C≤T_A≤85°C, I_{OUT} = 0A	-	±0.3	-	%
V_{OUT}	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 0A	-	±0.1	-	%
	Load regulation	Over I_{OUT} range, T_A = 25°C	-	±0.1	-	%
	Total output voltage variation		-	-	±1.5	%
	Output voltage ripple	10µF ceramic, 20MHz BW (8)	-	5	-	mV_{pp}
Switching frequency						
f_{SW}	Switching frequency	Using RT mode	500	-	2000	kHz
		RT/CLK pin open	400	500	600	kHz
f_{CLK}	Synchronization clock frequency range	Using CLK mode	500	-	2000	kHz
	Minimum CLK pulse width		75	-	-	ns
V_{CLK-H}	RT/CLK high threshold	Relative to AGND	2.2	-	3.3	V
V_{CLK-L}	RT/CLK low threshold		-0.3	-	0.4	V
f_{CLK}	RT/CLK to switch node delay		-	90	-	ns
	PLL lock-in-time		-	14	-	µs
Enable and undervoltage lockout						
V_{UVLO}	V_{IN} undervoltage threshold	V_{IN} increasing, UVLO pin connected to AGND	-	3.05	3.135	V
		V_{IN} decreasing, UVLO pin connected to AGND	2.5	2.75	-	V
V_{ENABLE}	Enable threshold trip point	Enable logic high voltage	-	1.25	-	V
		Enable logic low voltage	-0.3	-	1.0	V
Power Good						
PG	Power Good threshold	V_{OUT} rising, V_{OUT} GOOD	-	93	-	%
		V_{OUT} rising, V_{OUT} FAULT	-	107	-	%
		V_{OUT} falling, V_{OUT} GOOD	-	105	-	%
		V_{OUT} falling, V_{OUT} FAULT	-	91	-	%
	Power Good low voltage	I_{PG} = 0.33mA	-	-	0.3	V

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ELECTRICAL SPECIFICATIONS

SYMBOL	PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
Efficiency							
η	Efficiency	V_{IN} = 5V I_{OUT} = 2A	V_{OUT} = 3.3V, f_{SW} = 1.0MHz	-	95	-	%
			V_{OUT} = 2.5V, f_{SW} = 1.0MHz	-	93	-	%
			V_{OUT} = 1.8V, f_{SW} = 1.0MHz	-	91	-	%
			V_{OUT} = 1.5V, f_{SW} = 1.0MHz	-	89	-	%
			V_{OUT} = 1.2V, f_{SW} = 750kHz	-	88	-	%
			V_{OUT} = 1.0V, f_{SW} = 650kHz	-	86	-	%
			V_{OUT} = 0.8V, f_{SW} = 650kHz	-	84	-	%
		V_{IN} = 3.3V I_{OUT} = 2A	V_{OUT} = 1.8V, f_{SW} = 1.0MHz	-	91	-	%
			V_{OUT} = 1.5V, f_{SW} = 1.0MHz	-	89	-	%
			V_{OUT} = 1.2V, f_{SW} = 750kHz	-	87	-	%
			V_{OUT} = 1.0V, f_{SW} = 650kHz	-	86	-	%
			V_{OUT} = 0.8V, f_{SW} = 650kHz	-	83	-	%
Input and output capacitors							
C_{IN}	External input capacitor		Ceramic, required	47 (9)	-	-	µF
			Non ceramic, recommended in addition to ceramic	-	220 (9)	-	µF
C_{OUT}	External output capacitor		Ceramic, optionally in addition to ceramic	47 (10)	150	650 (11)	µF
			Non ceramic	-	100 (10)	1000(11)	µF
	Output capacitor ESR			-	-	25	mΩ
Transient Response							
t_{TR}	Transient Response		Recovery time 1A/µs load step from 1A to 3A	-	80	-	µs
			V_{OUT} over/undershoot 1A/µs load step from 1A to 3A	-	90	-	mV
Input quiescent current							
I_{SD}	Shutdown quiescent current		V_{ENABLE} = 0V	-	70	100	µA

RELIABILITY

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
MTBF	Mean Time Between Failures	Confidence level 60%, T_A=55°C, Activation energy 0.7eV, 1000 hrs test duration, 128756 samples, 0 fail		$1 \cdot 10^{10}$		h

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NOTES

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
(2) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.
(3) Depending on heat sink design, number of PCB layers, copper thickness and air flow.
(4) Measured on a 100 x 100mm two layer board, with 35µm (1 ounce) copper, no air flow
(5) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \Psi_{JT} * P_{dis} + T_T$; where P_{dis} is the power dissipated in the device and T_T is the temperature of the top of the device.
(6) The junction-to-board characterization parameter, Ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \Psi_{JB} * P_{dis} + T_B$; where P_{dis} is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.
(7) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance is affected by the tolerance of the external R_{SET} resistor.
(8) The industry standard for comparison of the output voltage ripple between switching regulators or modules requires a 10µF ceramic (sometimes additional 1µF ceramic in parallel) at the point of load where the voltage measurement is done using an oscilloscope with its probe and probe jack for low voltage/high frequency (low impedance) measurement. The oscilloscopes bandwidth is limited at 20MHz.
(9) A minimum of 47µF of ceramic capacitance is required across the input for proper operation. Locate the capacitor directly at V_{IN} of the device. An additional 220µF of bulk capacitance is recommended.
(10) The amount of required output capacitance varies depending on the output voltage. The amount of required capacitance must include at least 47µF of ceramic capacitance. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients.
(11) When using both ceramic and non-ceramic output capacitance, the combined maximum must not exceed 1200µF.

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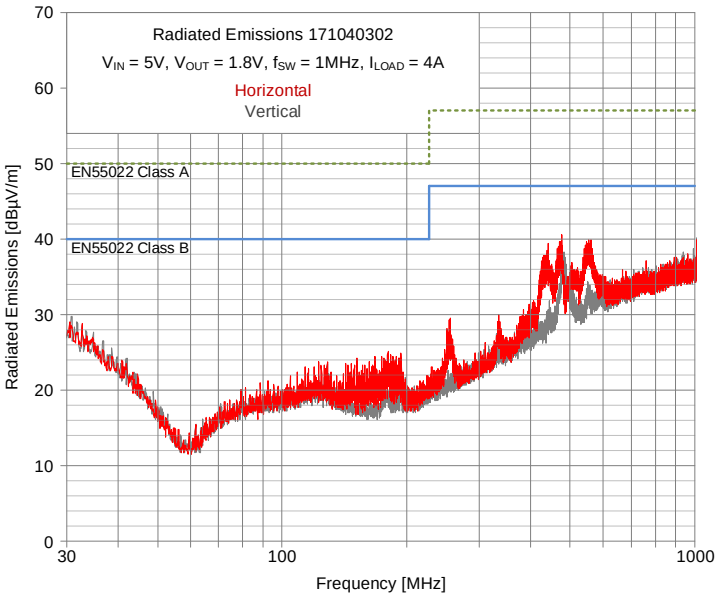
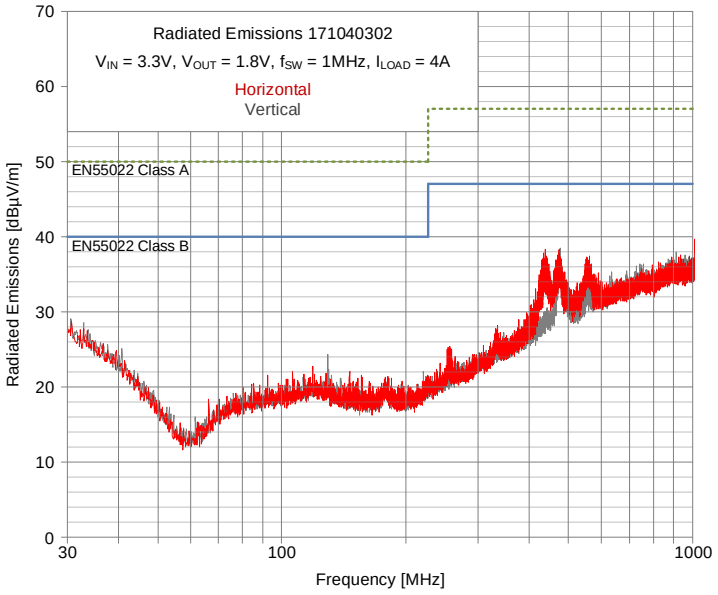
TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: V_{IN} = 3.3V - 5V; C_{IN} = 2 x 47µF X7R ceramic; C_{OUT} = 2x 47µF X7R ceramic, T_{AMB} = 25°C.

RADIATED EMISSIONS EN55022 (CISPR-22) CLASS B COMPLIANT

Measured on module with PCB and without external filters at 3m antenna distance





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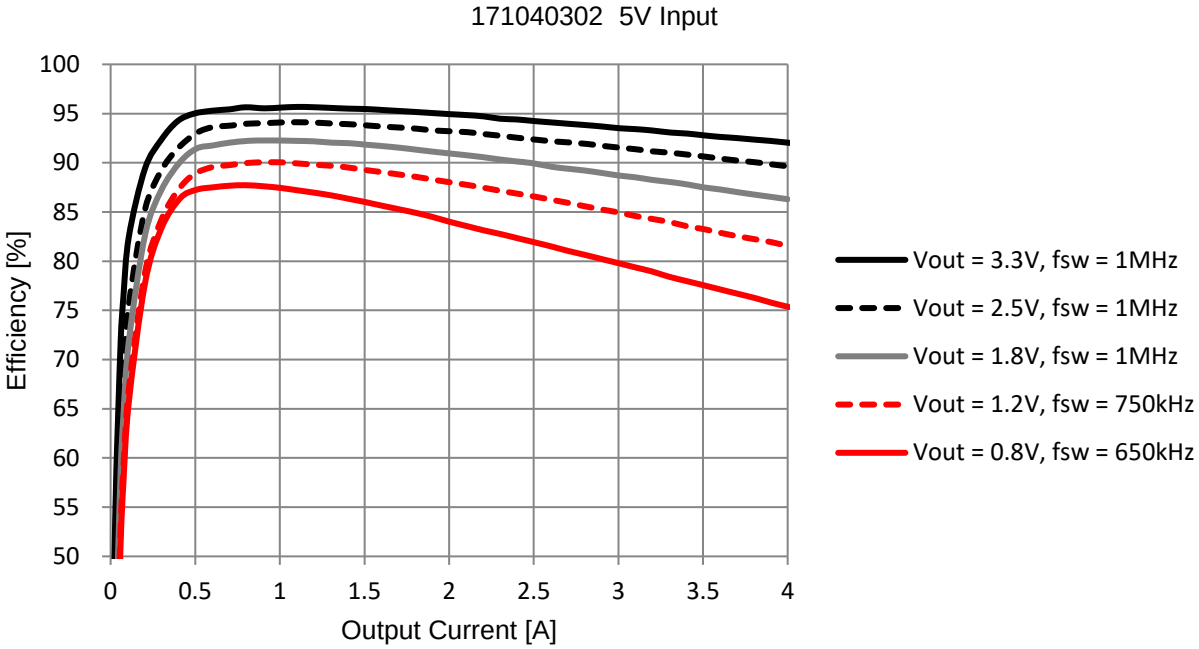
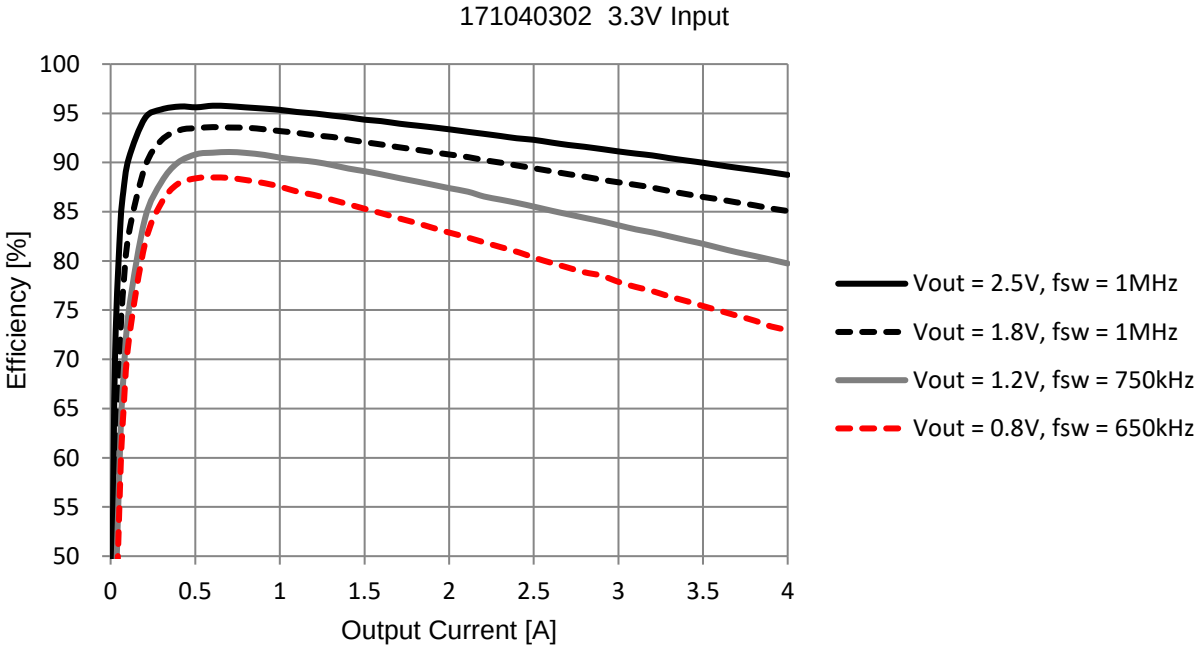
EFFICIENCY





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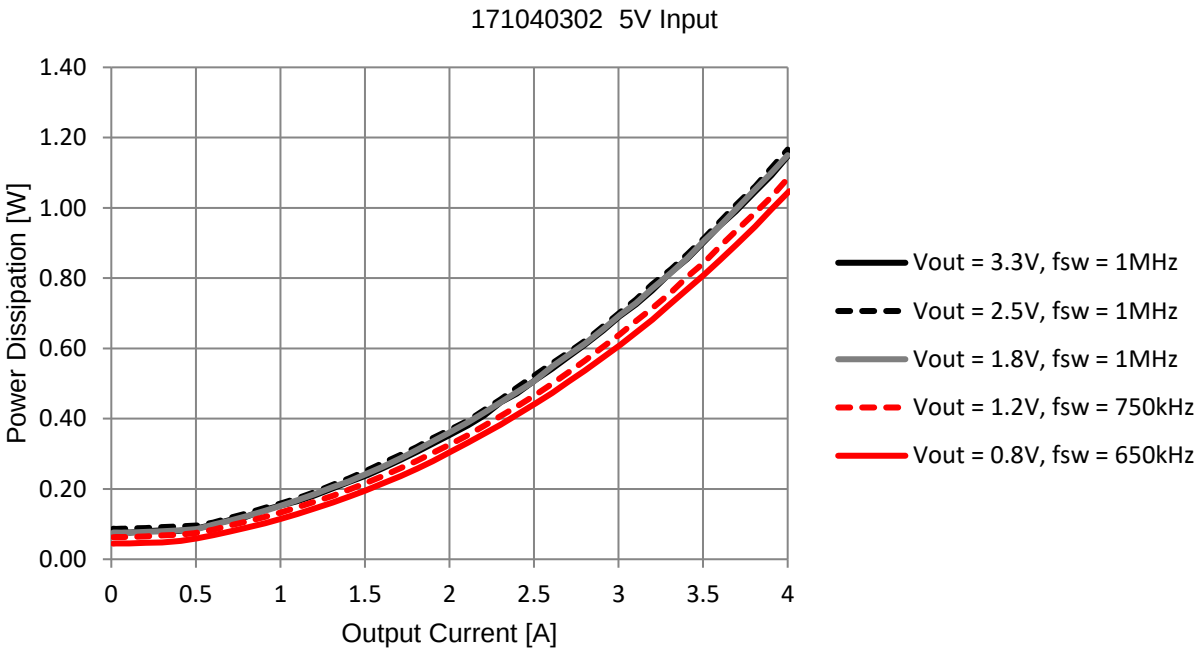
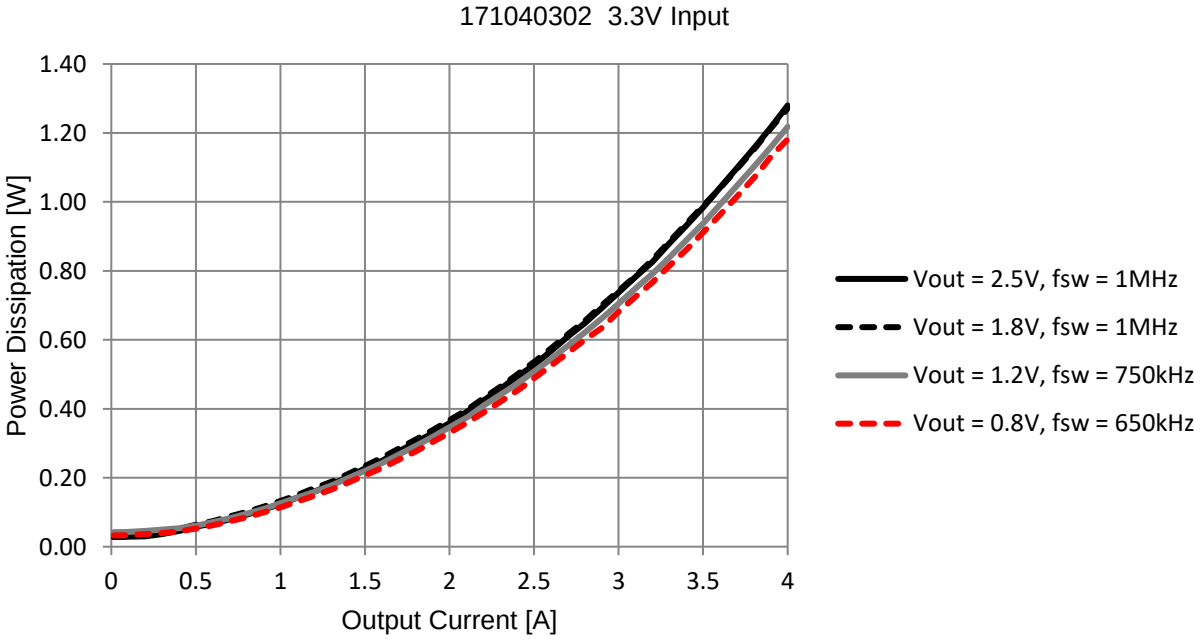
POWER DISSIPATION





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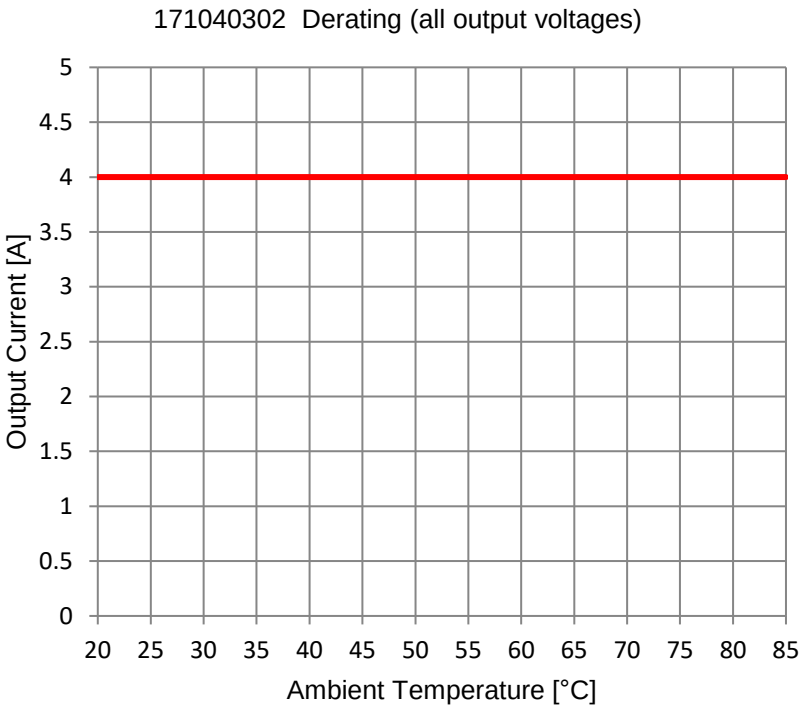
OUTPUT POWER DERATING



Note : see T_A limits in operating conditions on page 6.

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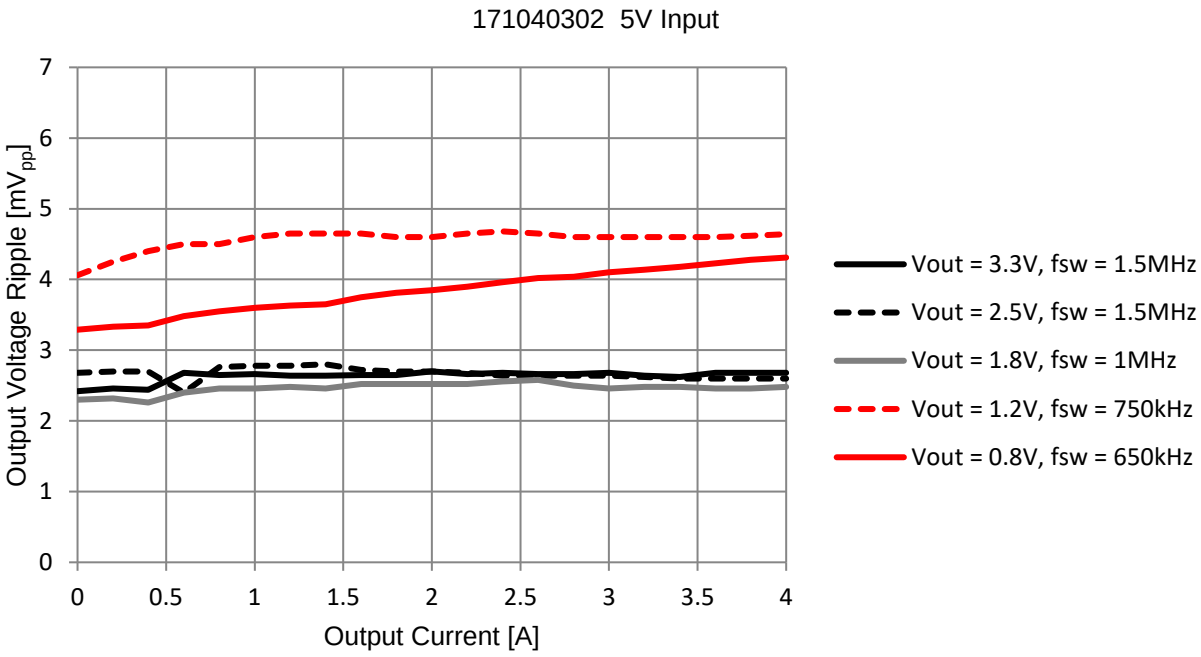
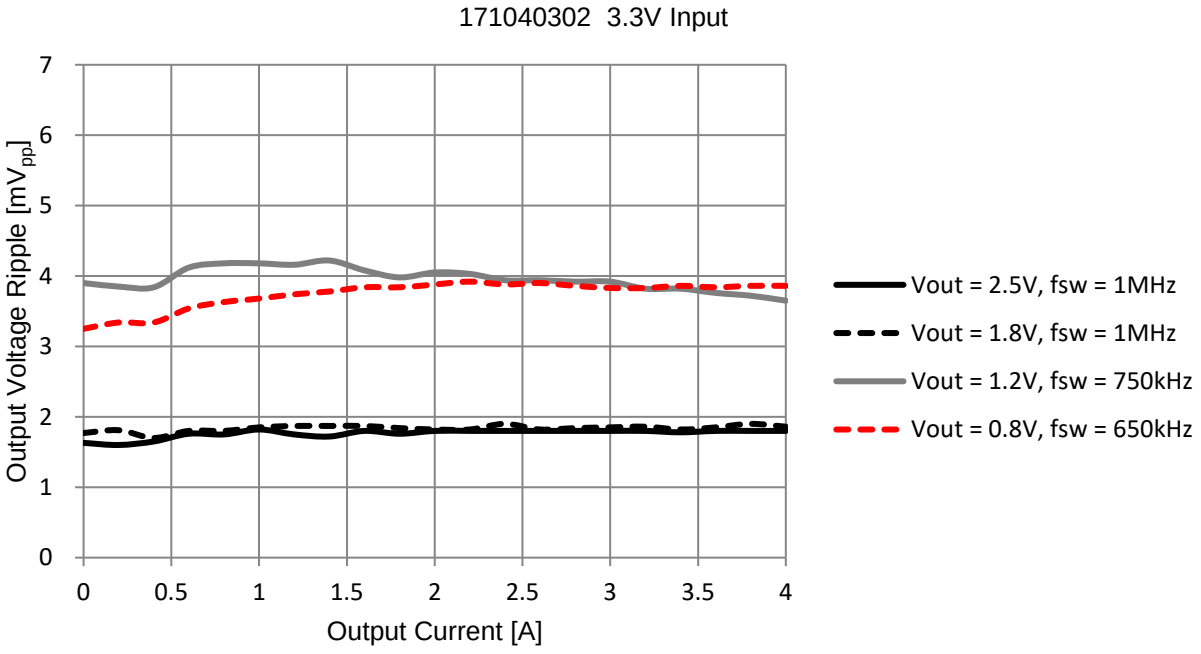
OUTPUT VOLTAGE RIPPLE





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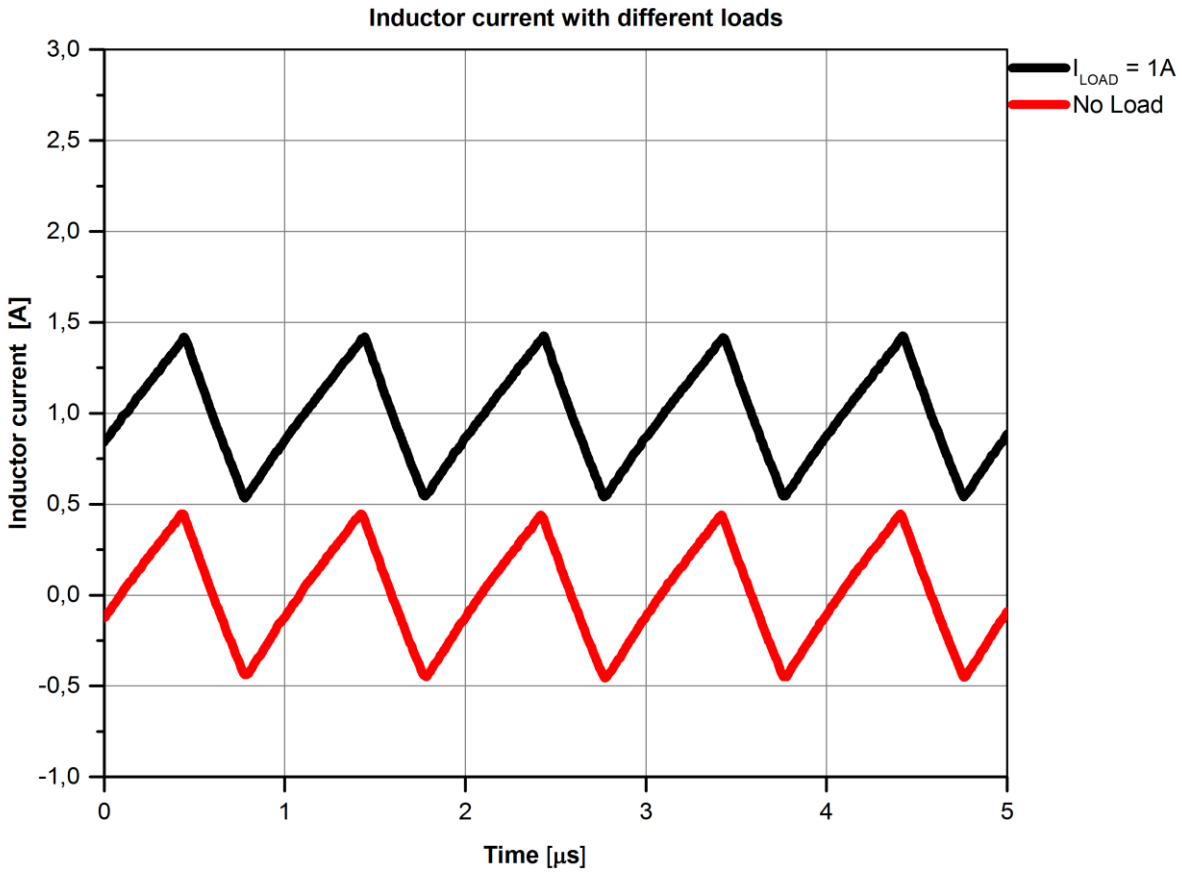
LIGHT LOAD OPERATION

The 171040302 forces the CCM (Continuous Conduction Mode) operation at light load (forced CCM). The inductor current during t_{OFF} can flow in the opposite direction, i.e. from the output capacitor and load to ground, through the low side MOSFET. In this way during t_{OFF} the output capacitor is discharged and loses the excess of charge gathered during t_{ON}.

In this way the switching frequency always remains constant, giving a relevant advantage in terms of filtering and avoiding interferences in undesired frequency ranges. Any load change will simply shift the inductor current up and down (see figure below).



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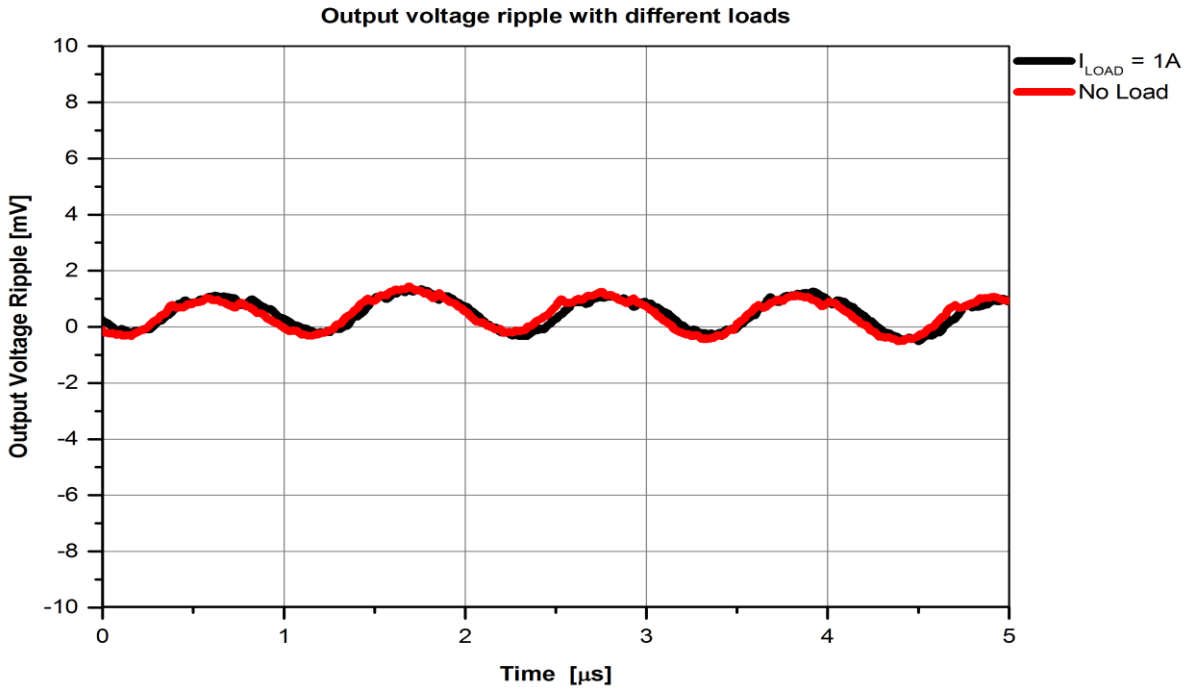
OUTPUT VOLTAGE RIPPLE AT LIGHT LOAD

In addition, the forced CCM implemented in the 171040302 keeps the output voltage ripple constant and low at all conditions (see figure below).



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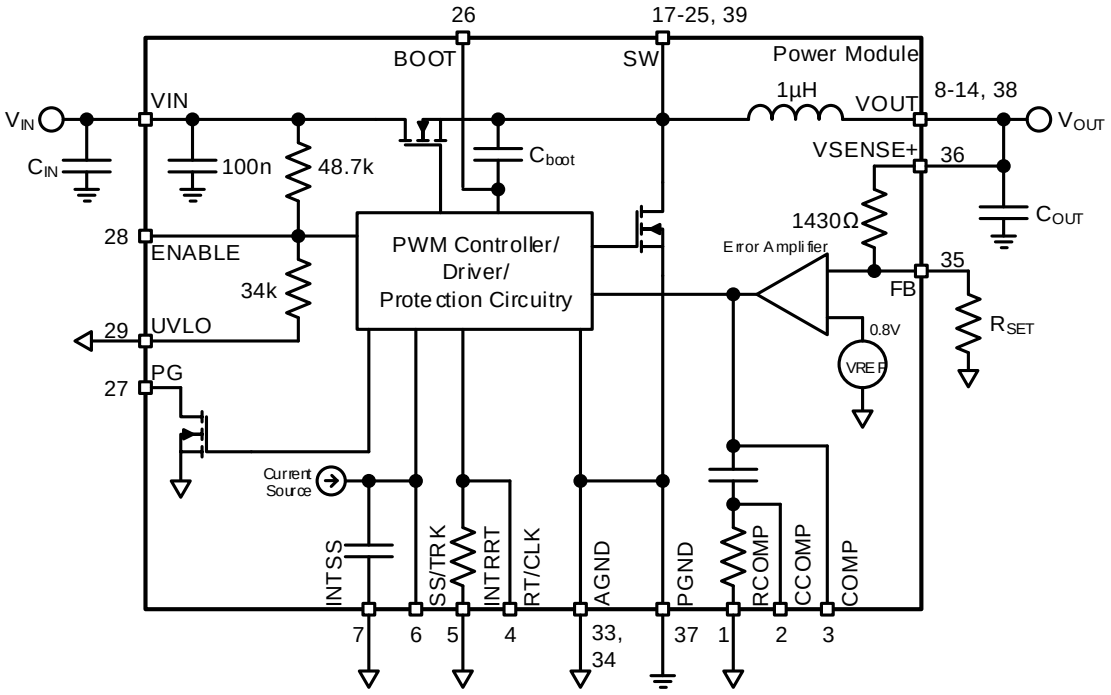
BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MagI³C Power Module series 1710x0302 is based on a synchronous step down regulator with integrated MOSFETs and a power inductor. The control scheme is based on a Current Mode (CM) regulation loop.

The V_{OUT} of the regulator is divided with the feedback resistor network of internal 1430Ω and external R_{SET} and fed into the FB pin. The error amplifier compares this signal with the internal 0.803V reference. The error signal is amplified and controls the on-time of a fixed frequency pulse width generator. This signal drives the power MOSFETs.

The Current Mode architecture features a constant frequency during load steps. Only the on-time is modulated. It is internally compensated and stable with low ESR output capacitors and requires no external compensation network.

This architecture supports fast transient response and very small output ripple values (less than 10mV) are achieved.

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DESIGN FLOW

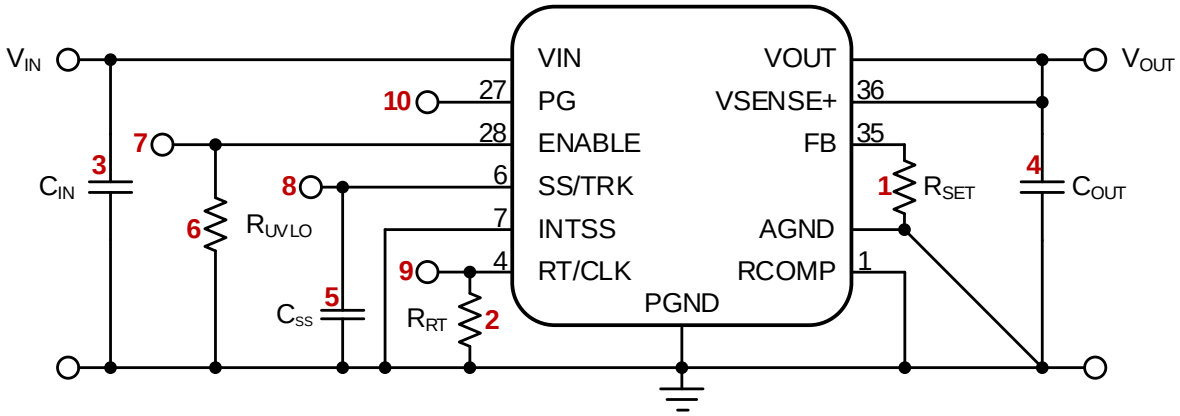
The next 10 simple steps will show how to select the external components to design your power application.

Essential Steps

1. Set output voltage
2. Set operating frequency
3. Select input capacitor
4. Select output capacitor

Optional Steps

5. Select soft-start capacitor
6. Select undervoltage lockout divider
7. Enable / Disable
8. Voltage tracking
9. Synchronization to an external clock
10. Power Good



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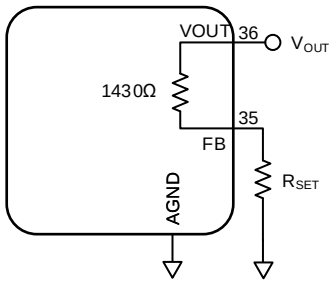
Step 1 Setting the output voltage (V_{OUT})

The output voltage is selected with a resistor divider across FB pin and AGND. The top resistor of 1430 Ω of the feedback voltage resistor divider is located inside the module. The output voltage adjustment range is from 0.8V to 3.6V.

$$R_{SET} = \frac{V_{REF} \bullet 1430\Omega}{V_{OUT} - V_{REF}} (\Omega) \qquad (1)$$

V_{REF} is the internal reference voltage (0.8V).

V_{OUT}	3.3V	3.0V	2.5V	1.8V	1.5V	1.2V	1.0V	0.8V
R_{SET} (E96)	453Ω	523Ω	665Ω	1130Ω	1620Ω	2870Ω	5620Ω	open



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Step 2 Setting the operating frequency (f_{SW})

The switching frequency must be selected according to the input voltage, output voltage and load current for the best performance in loop regulation and transient response.

Note: R_{RT} open (f_{SW} = 500 kHz) is only allowed under specific conditions (see table below)

OPERATING FREQUENCY [kHz]	R_{RT} [kΩ]	V_{IN} = 5V				V_{IN} = 3.3V	
		I_{OUT} = 0 to 3.5A		I_{OUT} > 3.5A		I_{OUT} = 0 to 4A	
		V_{OUT} RANGE [V]		V_{OUT} RANGE [V]		V_{OUT} RANGE [V]	
		MIN	MAX	MIN	MAX	MIN	MAX
500	open	0.8	1.4	0.8	1.0	0.8	2.2
550	3400	0.8	1.6	0.8	1.1	0.8	2.4
600	1800	0.8	1.8	0.8	1.2	0.8	2.5
650	1200	0.8	2.1	0.8	1.4	0.8	2.5
700	887	0.8	2.6	0.8	1.6	0.8	2.5
750	715	0.9	3.6	0.9	1.8	0.8	2.5
800	590	0.9	3.6	0.9	2.1	0.8	2.5
900	511	1.0	3.6	1.0	3.6	0.8	2.5
1000	348	1.2	3.6	1.2	3.6	0.8	2.5
1250	232	1.4	3.6	1.4	3.6	1.0	2.4
1500	174	1.7	3.6	1.7	3.6	1.1	2.3
1750	137	2.0	3.6	2.0	3.6	1.3	2.2
2000	113	2.3	3.4	2.3	3.3	1.5	2.2

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Step 3 Select input capacitor (C_{IN})

The energy at the input of the power module is stored in the input capacitor. A small input capacitor (100nF) is integrated inside the 1710x0302 MagI³C Power Module series, ensuring good EMI performance. Additional external input capacitance is required to the power module to provide cycle-by-cycle switch current and to support load transients. The external input capacitors must be placed directly at the VIN pin. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Input ripple current rating is dictated by the equation:

$$I_{C_{INRMS}} \approx I_{OUT} \bullet \sqrt{D \bullet (1 - D)} \quad (2) \quad \text{where} \quad D \approx \frac{V_{OUT}}{V_{IN}}$$

As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_{OUT}$.

Recommended minimum input capacitance is 47µF X7R or X5R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature deratings of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain minimum value of peak-to-peak input ripple voltage (ΔV_{IN}) then the following equation may be used:

$$C_{IN} \geq \frac{I_{OUT} \bullet D \bullet (1 - D)}{f_{SW_{CCM}} \bullet \Delta V_{IN}} \quad (3) \quad \text{where } D \approx \frac{V_{OUT}}{V_{IN}} \qquad CCM = \text{continuous conduction mode}$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines or the existing inductance of the input circuit.

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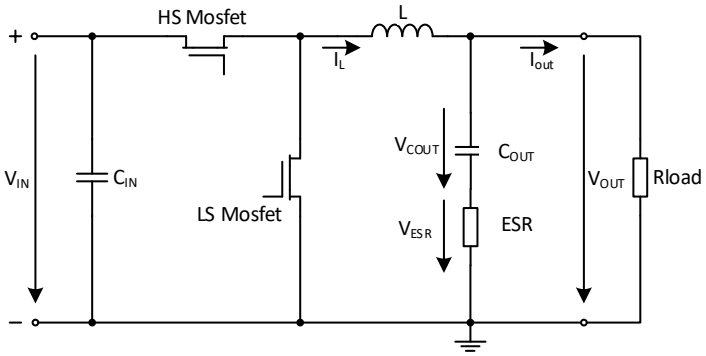
Step 4 Select output capacitor (C_{OUT})



None of the required output capacitors are integrated within the module. The output capacitor must meet the worst case RMS current rating of $0.5 * \Delta I_L$, as calculated in equation (4).

$$\Delta I_L = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{f_{SW} \bullet L \bullet V_{IN}} \quad (4)$$

Selection by output voltage ripple requirements

The capacitor should be selected in order to minimize the output voltage and provide a stable voltage at the output. Under steady state conditions, the voltage ripple observed at the output can be defined as:

$$V_{OUT\ ripple} = \Delta I_L \bullet ESR + \Delta I_L \bullet \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} \quad (5)$$

Very low ESR capacitors, like ceramic and polymer electrolytic, are recommended. If a low ESR capacitor is selected, equation (4) can be simplified and a first condition for the minimum capacitance value can be derived:

$$C_{OUT} \geq \frac{\Delta I_L}{8 \bullet V_{OUT\ ripple} \bullet f_{SW}} \quad (6)$$

Beyond that, additional capacitance will reduce output ripple as long as the ESR is low enough to permit it. Please consider the derating of the nominal capacitance value due to temperature, aging and applied DC voltage.

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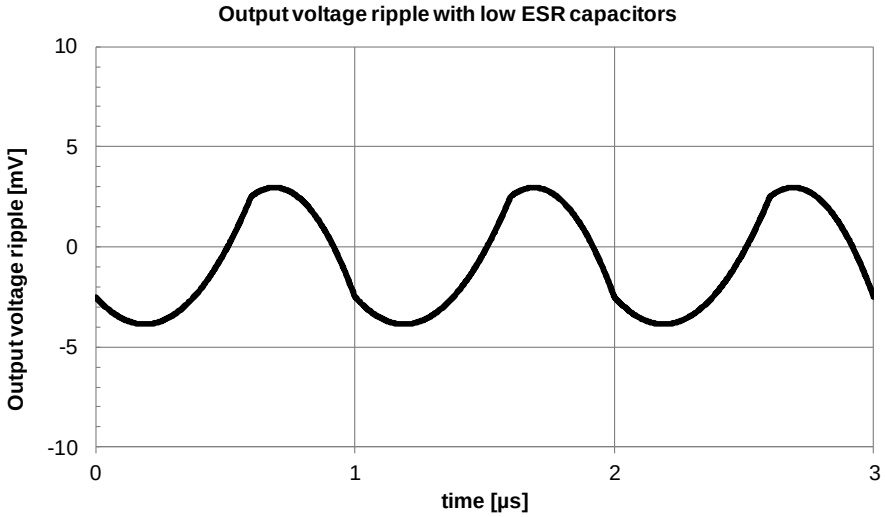
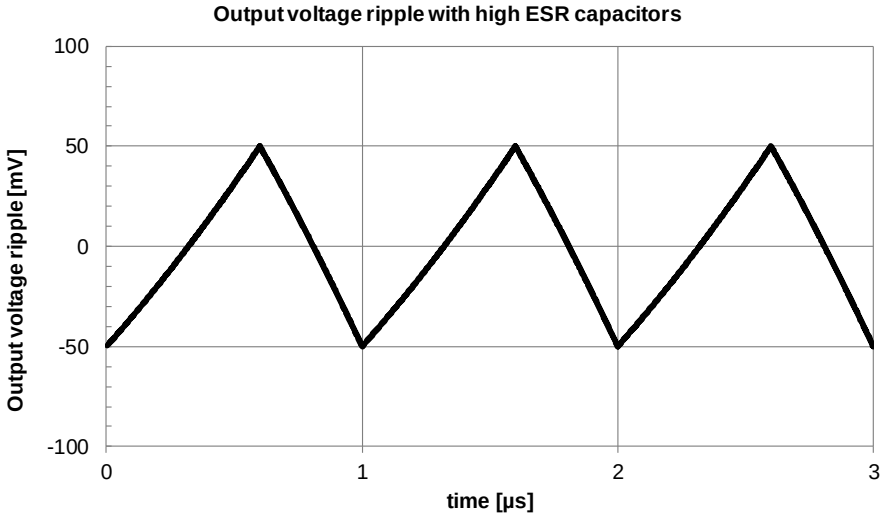
The use of very low ESR capacitors leads to an output voltage ripple as shown below:



When capacitors with slightly higher ESR are utilized, the dominant parameter which influences the output voltage ripple is just the ESR:

$$\mathrm{ESR} \leq \frac{\mathrm{V_{OUT\ ripple}}}{\Delta \mathrm{I_L}} \quad (7)$$

Consequently the shape of the output voltage ripple changes, as shown below:



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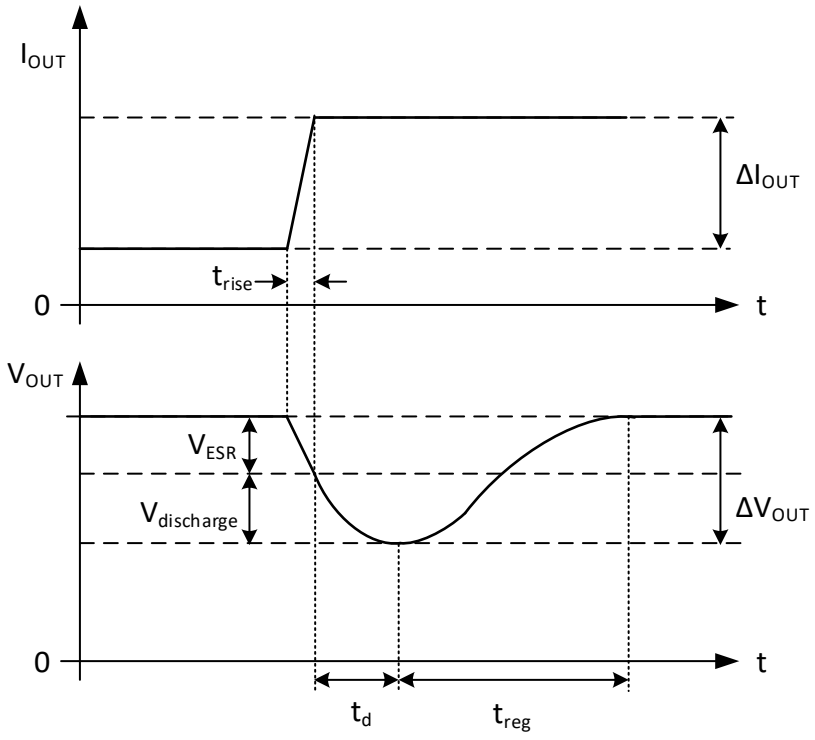
Selection by load step requirements

The output voltage is also affected by load transients (see picture below).

When the output current transitions from a low to a high value, the voltage at the output capacitor (V_{OUT}) drops. This involves two contributing factors. One is caused by the voltage drop across the ESR (V_{ESR}) and depends on the slope of the rising edge of the current step (t_{rise}). For low ESR values and small load currents, this is often negligible. It can be calculated as follows:

$$V_{ESR} = ESR \bullet \Delta I_{OUT} \quad (8)$$

Where ΔI_{OUT} is the load step, as shown in the picture below (simplified: no voltage ripple is shown).



The second contributing factor is the voltage drop due to discharge of the output capacitor, which can be estimated as:

$$V_{discharge} = \frac{\Delta I_{OUT} \bullet t_d}{2 \bullet C_{OUT}} \quad (9)$$

In a current mode architecture the t_d is strictly related to the bandwidth of the regulation loop and influenced by the C_{OUT} (increasing C_{OUT}, the t_d increases as well).

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In order to choose the value of the output capacitor, the following steps should be utilized:

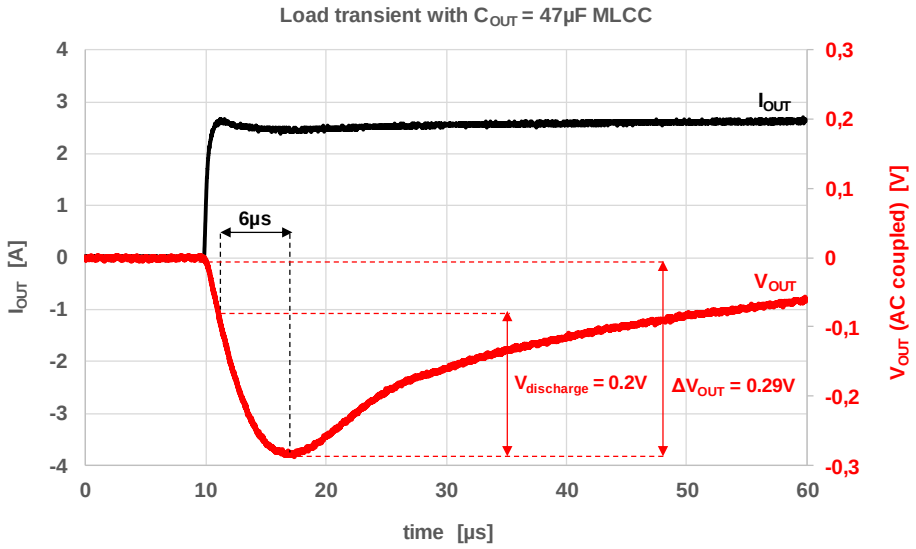
1. According to the operating conditions (V_{IN}, V_{OUT} and f_{SW}), select the minimum C_{OUT} recommended in table on page 35.
2. Measure t_d.
3. Calculate the appropriate value of C_{OUT} for the maximum voltage drop $V_{discharge}$ allowed at a defined load step, using the following equation (10), derived from equation (9):

$$C_{OUT} \geq \frac{\Delta I_{OUT} \bullet t_d}{2 \bullet V_{discharge}} \quad (10)$$

4. As above mentioned, changing C_{OUT} affects also t_d. Therefore a new measurement should be performed and, if necessary, step 2 and 3 repeated (it is an iterative process and few steps could be required).

Example: V_{IN} = 5V, V_{OUT} = 3.3V, ΔI_{OUT} = 2.5A, f_{sw} = 1.5MHz, ΔV_{OUT}<0.2V.

According to the table on page 35, an output MLCC of 47µF would be necessary. After mounting this capacitor, the load transient should be performed and the t_d measured (see picture below).



The ΔV_{OUT} = 0.29V and t_d= 6µs. It is important to remind that the ΔV_{OUT} includes also the voltage drop during t_{rise}, mainly due to the ESR (V_{ESR} = 90mV, see picture above). In order to achieve the desired maximum ΔV_{OUT}, the $V_{discharge}$ should be below 0.1V. Using the equation (9), the minimum required output capacitor is:

$$C_{OUT} \geq \frac{2.5A \bullet 6\mu s}{2 \bullet 0.1V} = 75\mu F$$

To achieve the calculated value of C_{OUT} an additional MLCC of 47µF is mounted in parallel (considering the lower effective capacitance due to DC biasing).

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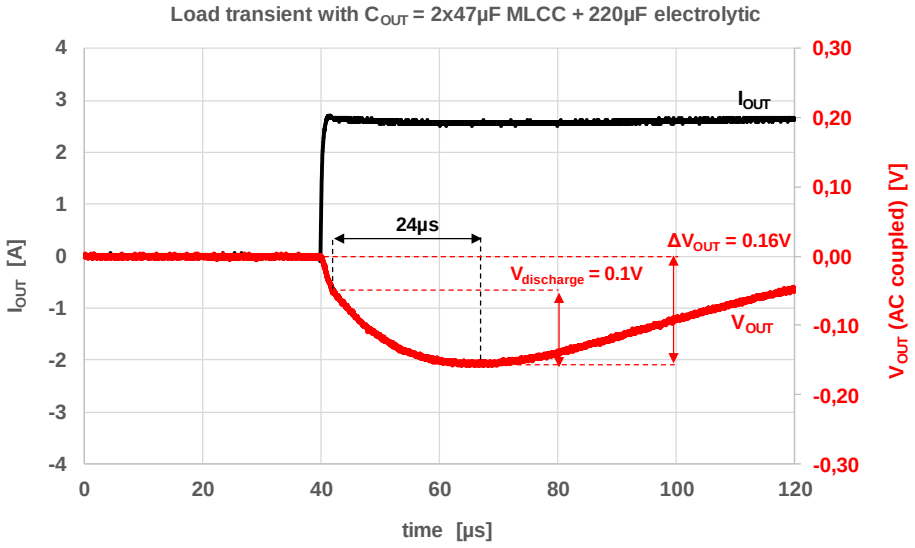
Nevertheless, as indicated in point 4, one or more measurements should be performed in order to find the most suitable value of C_{OUT}. After some iterations, the most suitable output capacitance is determined. Due to its high value, a combination of two MLCC (47µF each one) and an electrolytic capacitor (220µF) is implemented. The final result is shown in the picture below:



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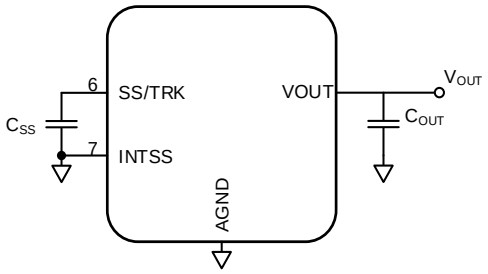
Step 5 Select soft-start capacitor (C_{SS})

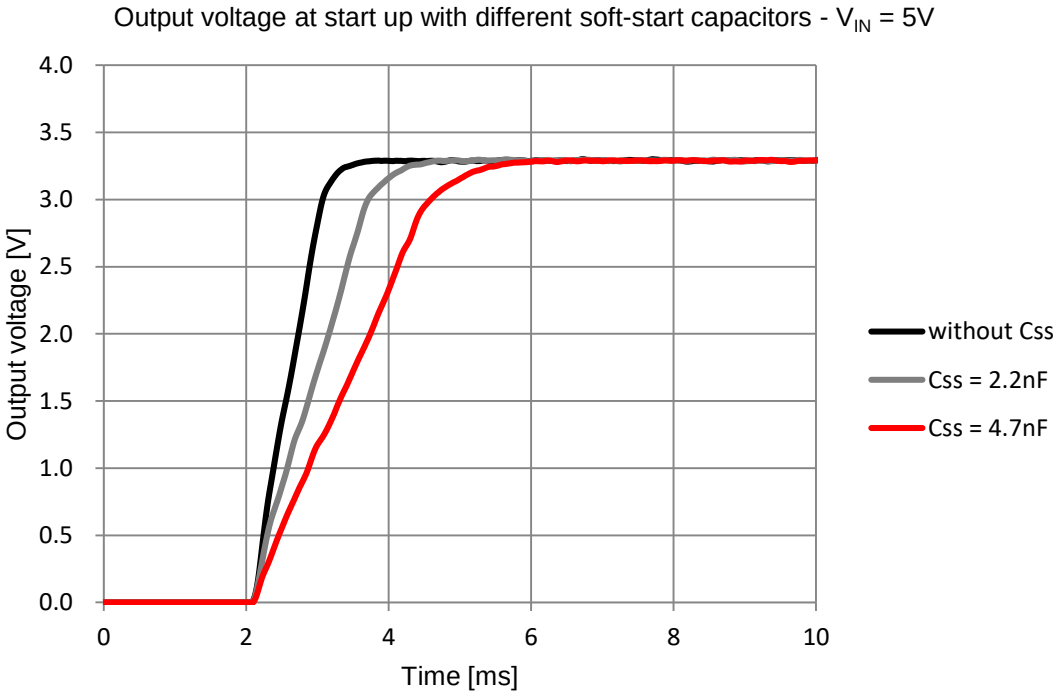
Connecting the INTSS pin to AGND and leaving SS/TRK pin open enables the internal soft-start capacitor with a soft-start interval of approximately 1 ms. Adding additional capacitance between the SS/TRK pin and AGND increases the soft-start time according to the table below. There is no maximum value limit for C_{SS}.



C_{SS} [nF]	Open	2.2	4.7	10	15	22	27
Soft-start [ms]	~1	~2	~3	~4	~6	~9	~10

The values in the table have been measured at room temperature under full load condition and gives an indication of the soft-start duration.

The diagram below illustrates how the slope of the output voltage changes according to the different soft-start settings. It is important to highlight that the implementation of the soft-start (also without the external C_{SS}, a default soft-start capacitor is internally present) prevents the output voltage from experiencing overshoots.



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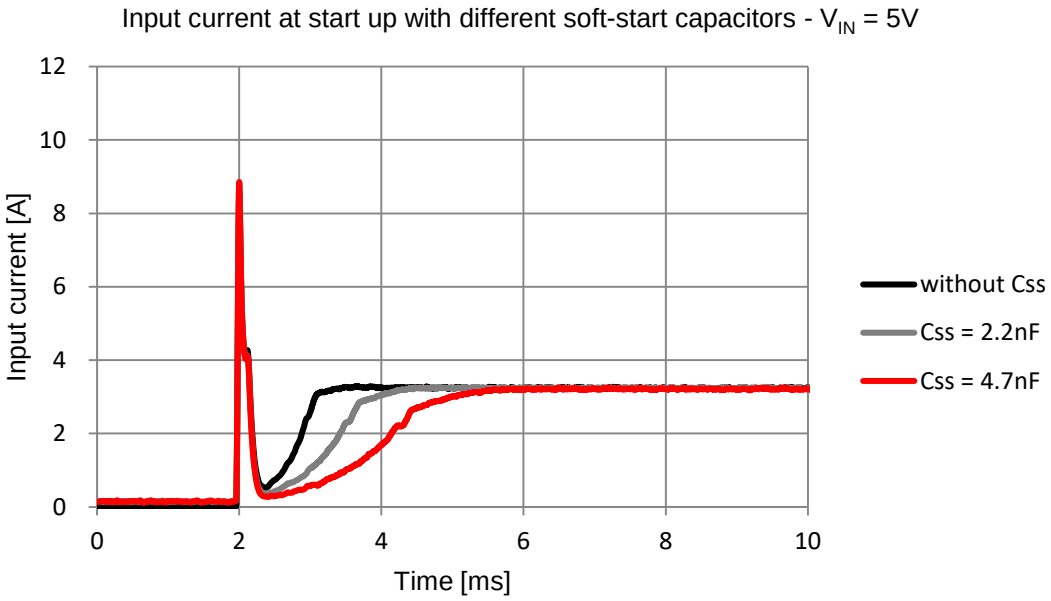
The curves below show a comparison among the input currents under three different soft-start conditions:

- Default soft-start (without any additional external capacitor)
- Soft-start with two different values of C_{SS}.

The first peak (same for any condition) is due to the initial charge of the capacitors at the input (C_{IN}). This current peak is not affected by the soft-start. Therefore it can´t be reduced by different soft-start capacitor values.
The right part of the diagram shows the smooth rise of the input current during the start-up. The different slope of the rising edge of the currents is defined by the different soft-start durations.



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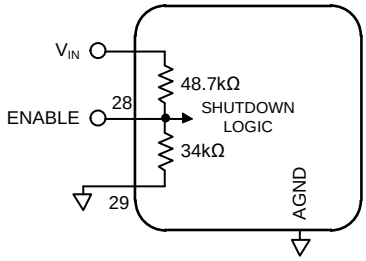
Step 6 Select undervoltage lockout divider

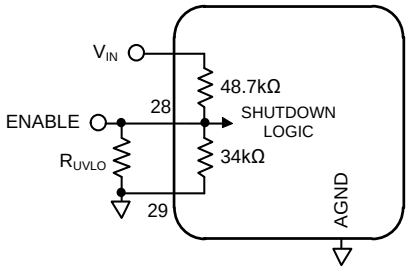
Pin 29 connected to analog ground

This connects the internal undervoltage lockout resistor divider. The enable rising threshold is typ. 1.25V. The enable falling threshold is at 1V max. Use at least 10% safety tolerance. For 3.3V input voltage use a rising threshold below 3V. This threshold is attainable by leaving pin 29 open. An external undervoltage lockout resistor will set the rising threshold below 3V.

$V_{IN(UVLO)}$ rising threshold typ. [V]	3.14V
Hysteresis [mV]	300



Pin 29 connected to AGND with additional resistor to adjust undervoltage lockout.



$V_{IN(UVLO)}$ rising threshold typ. [V]	3.25	3.5	3.75	4.0	4.25	4.5	4.75
R_{UVLO} [kΩ]	294	133	86.6	63.4	49.9	42.2	35.7
Hysteresis [mV]	325	335	345	355	365	375	385

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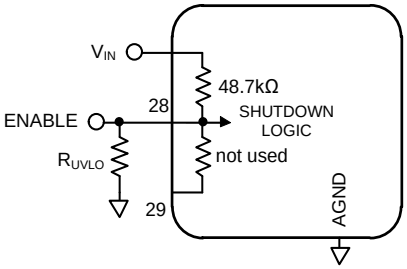
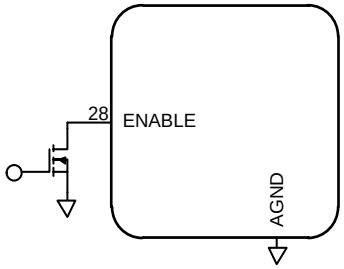
Pin 29 open with additional resistor to adjust undervoltage lockout for lower values.



$V_{IN(UVLO)}$ rising threshold typ. [V]	3.0	2.75	2.5	2.25
R_{UVLO} [kΩ]	34.0	39.7	47.5	60.4
Hysteresis [mV]	170	156	142	126

Step 7 Enable

The ENABLE pin provides electrical on/off control of the device. Once the ENABLE pin voltage exceeds the threshold voltage, the device starts operation. If the ENABLE pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low shutdown current state. Apply a voltage ≤ 1V to the enable pin to disable the device. Left open or set to ≥ 1.5V will enable the device. When manually disabling during lab tests, use short leads to connect to AGND of the module. If the logic driver is not close to the ENABLE pin of the module, use a transistor (as shown below) to prevent the noise from disturbing the proper ENABLE/DISABLE function.



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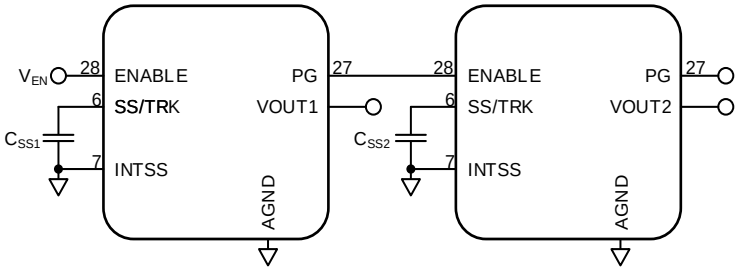
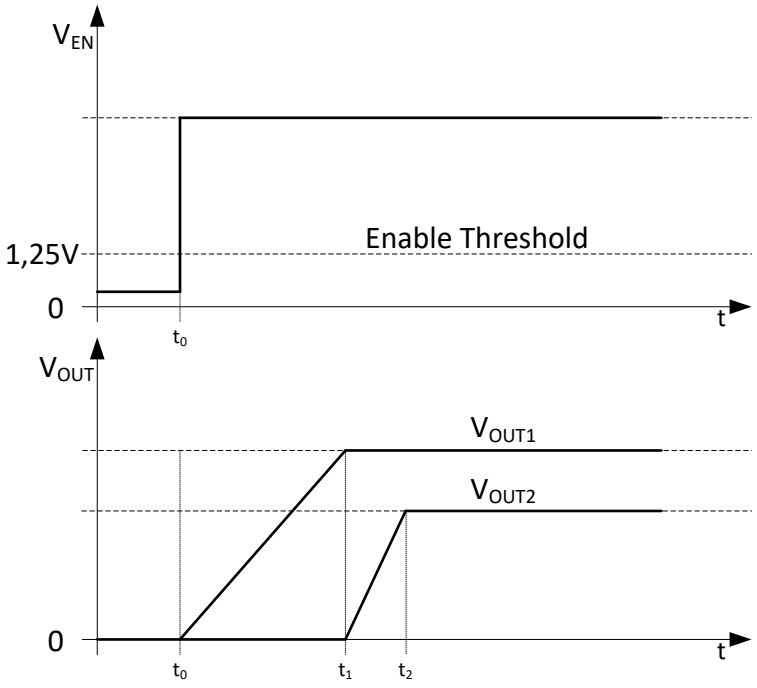
Step 8 Voltage sequencing & tracking

Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TRK, ENABLE and PG pins. The sequential voltage tracking is illustrated below using two devices. The PG pin of the first device is connected to the ENABLE pin of the second device which enables the second power supply once the primary supply reaches regulation. Both modules can apply different slopes of the output voltage during start by selecting the individual soft-start capacitors accordingly.





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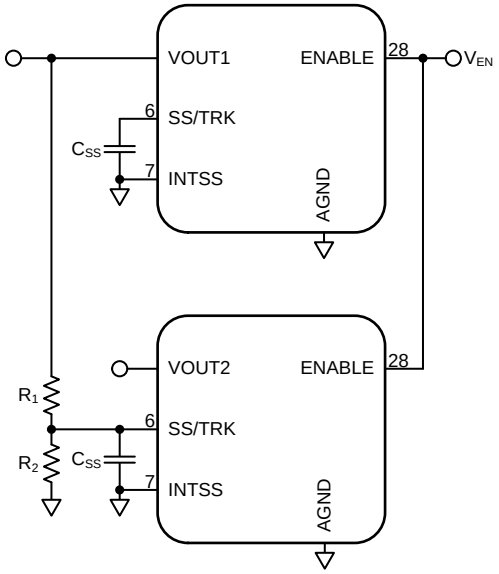
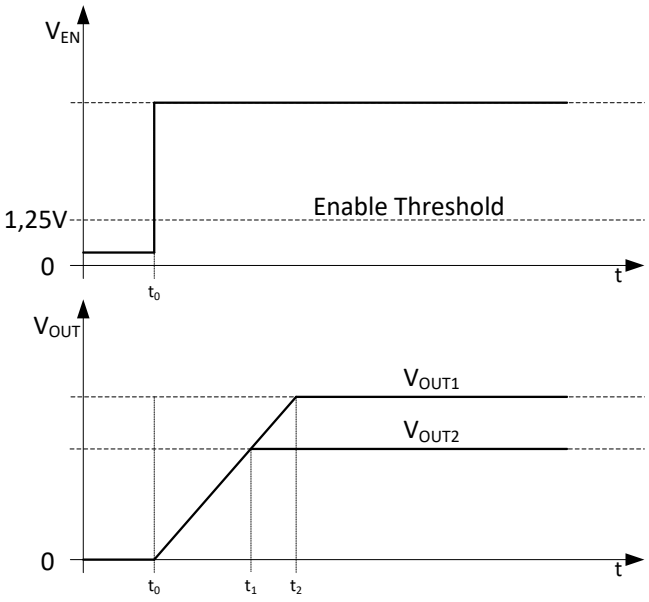
Simultaneous tracking

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R_1 and R_2 as shown below to the output of the power supply that needs to be tracked or to another voltage reference source.



$$R_1 = \frac{V_{OUT2} \bullet 12.6}{V_{REF}}\ (k\Omega) \qquad (10) \qquad\qquad R_2 = \frac{V_{REF} \bullet R_1}{V_{OUT2} - V_{REF}}\ (k\Omega) \qquad (11)$$



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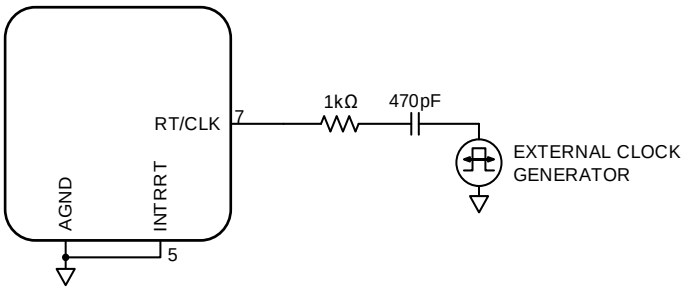
Step 9 Synchronizing with an external clock

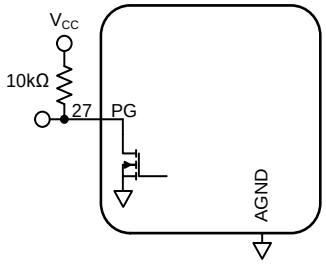
An internal phase locked loop (PLL) has been implemented to allow synchronization between 500 kHz and 2 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a minimum pulse width of 75 ns. The maximum clock pulse width must be calculated using Equation 9. The clock signal amplitude must transition lower than 0.4 V and higher than 2.2 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. For applications requiring both RT mode and CLK mode, configure the device as shown in the figure below. Before the external clock is present, the device works in RT mode and the switching frequency is set by the RT resistor (R_{RT}). When the external clock is present, the CLK mode overrides the RT mode. The device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. The device will lock to the external clock frequency approximately 15 µs after a valid clock signal is present. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to a lower frequency before returning to the switching frequency set by the RT resistor.

$$\text{Maximum clock pulse width} = \frac{0.75 \bullet \left(1 - \frac{V_{OUT}}{V_{INMIN}}\right)}{f_{SW}} \qquad (12)$$



Step 10 Power Good

The PG pin is an open drain output. Once the voltage on the SENSE+ pin is between 93% and 107% of the nominal value, the PG pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 6 V or less. The PG pin is in a defined state once V_{IN} is higher than 1.2 V, but with reduced current sinking capability. The PG pin achieves full current sinking capability once the V_{IN} pin is above 2.95V. The PG pin is pulled low when the voltage on SENSE+ is lower than 91% or higher than 109% of the set output voltage. Also, the PG pin is pulled low if the input UVLO or thermal shutdown is asserted, or if the ENABLE pin is pulled low.



V_{CC} = V_{IN} or other supply voltage below 6V

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PROTECTIVE FEATURES

Over Temperature Protection (OTP)

The junction temperature of the MagI³C Power Module should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal thermal shutdown circuit which activates at 175°C (typ) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_{OUT} to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures due to accidental device overheating. When the junction temperature falls below 160°C the SS pin is released, V_{OUT} rises smoothly, and normal operation resumes. Applications requiring maximum output current, especially those at high input voltages, may require additional derating at elevated temperatures.

Overcurrent Protection (OCP)

For protection against load faults, the MagI³C Power Module incorporates cycle-by-cycle current limiting (see I_{OCP} in “Electrical Specification” on page 7). During an overcurrent condition the output current is limited and the output voltage is reduced. As the output voltage drops more than 9% below the set point, the PG signal is pulled low. If the output voltage drops more than 25%, the switching frequency is reduced to reduce power dissipation within the device. When the overcurrent condition is removed, the output voltage returns to the nominal voltage.

Short Circuit Protection (SCP)

The short circuit protection is realized the cycle-by-cycle current limiting. The short circuit protection is continuous with a recovery at the following switching cycle if the short circuit condition is removed.

Output Overvoltage Protection (OVP)

The device incorporates an overvoltage protection to minimize output voltage overshoot when recovering from output fault conditions. When the output voltage reaches the upper trip point of 109% of the voltage programmed with the feedback resistor divider, the high-side MOSFET is disabled to prevent further output voltage rise caused by the module itself. When the output voltages reaches the lower trip point of 105% of the programmed output voltage, the high-side MOSFET will be turned on again at the next switching cycle.

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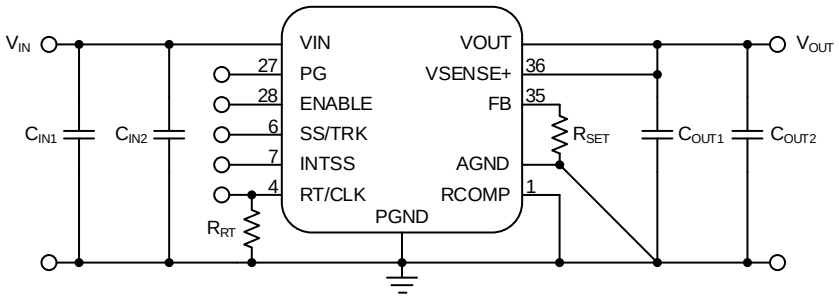
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

TYPICAL SCHEMATIC



INPUT	OUTPUT	C_{IN2}	C_{IN1}	R_{RT}	R_{SET}	C_{OUT1}	C_{OUT2}
5V	3.3V	220µF	47µF X5R	174kΩ	459Ω	47µF X5R	-
5V	2.5V	220µF	47µF X5R	174kΩ	673Ω	47µF X5R	47µF X5R
5V	1.8V	220µF	47µF X5R	348kΩ	1150Ω	47µF X5R	100µF
5V	1.5V	220µF	47µF X5R	348kΩ	1650Ω	47µF X5R	100µF
5V	1.2V	220µF	47µF X5R	715kΩ	2870Ω	47µF X5R	100µF
5V	1.0V	220µF	47µF X5R	715kΩ	5830Ω	47µF X5R	100µF
5V	0.8V	220µF	47µF X5R	1200kΩ	Open	47µF X5R	100µF
3.3V	1.8V	220µF	47µF X5R	348kΩ	1150Ω	47µF X5R	100µF
3.3V	1.5V	220µF	47µF X5R	348kΩ	1650Ω	47µF X5R	100µF
3.3V	1.2V	220µF	47µF X5R	715kΩ	2870Ω	47µF X5R	100µF
3.3V	1.0V	220µF	47µF X5R	715kΩ	5830Ω	47µF X5R	100µF
3.3V	0.8V	220µF	47µF X5R	1200kΩ	Open	47µF X5R	100µF

C_{IN2} and C_{OUT2} ≥ 100µF are polymer electrolytic types.

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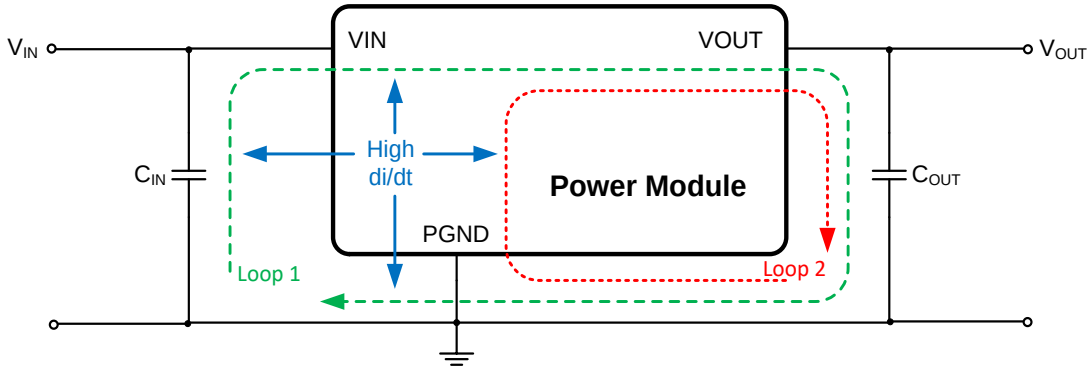
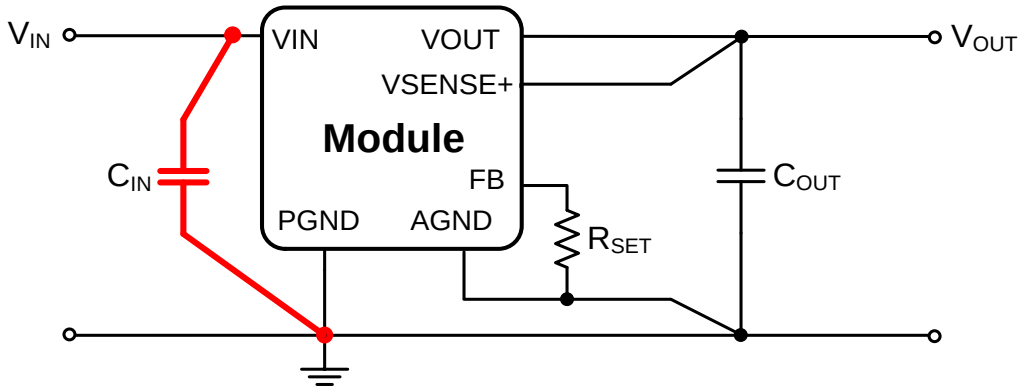
LAYOUT RECOMMENDATION

PCB layout is an important part of DC-DC converter design. Poor board layout can interfere with the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following five simple design rules.

1: Minimize area of switched current loops



Target is to identify the paths in the system which have discontinuous current flow. They are the most critical ones because they act as an antenna and cause observable high frequency noise (EMI). The easiest approach to find the critical paths is to draw the high current loops during both switching cycles and identify the sections which do not overlap. They are the ones where no continuous current flows and high di/dt is observed. Loop1 is the current path during the ON-time of the High-Side MOSFET. Loop2 is the current path during the OFF-time of the High-Side MOSFET.



Based on those considerations, the path of the input capacitor C_{IN} is the most critical one to generate high frequency noise on V_{IN}. Therefore place C_{IN} as close as possible to the MagI³C power module V_{IN} and PGND pins. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND pins.

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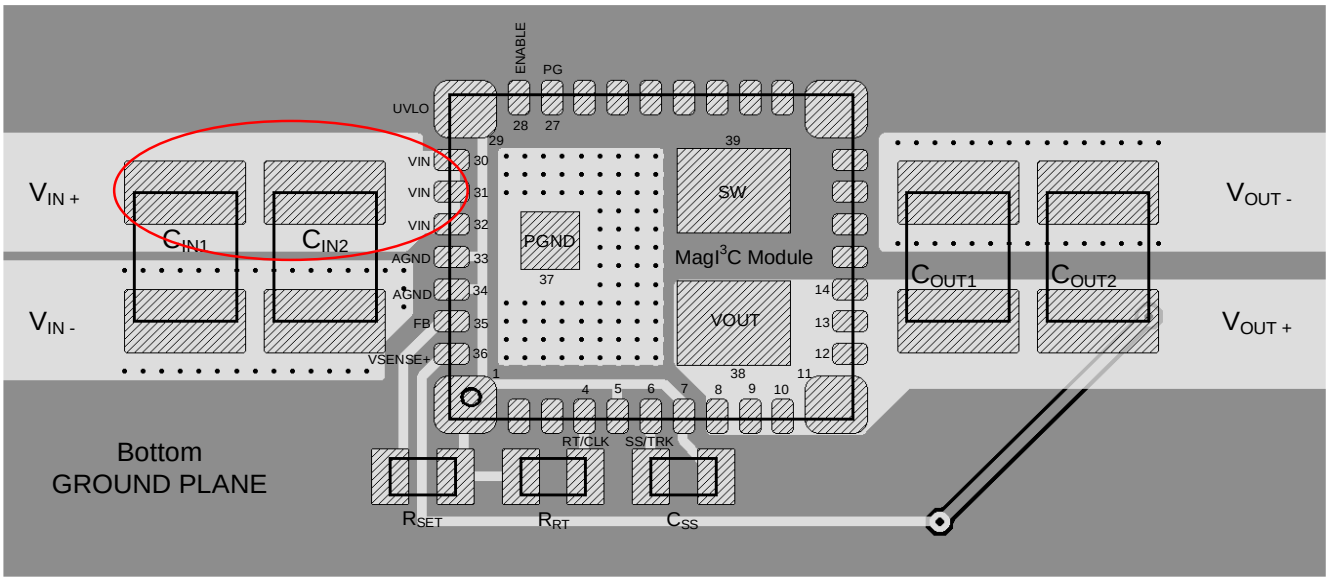
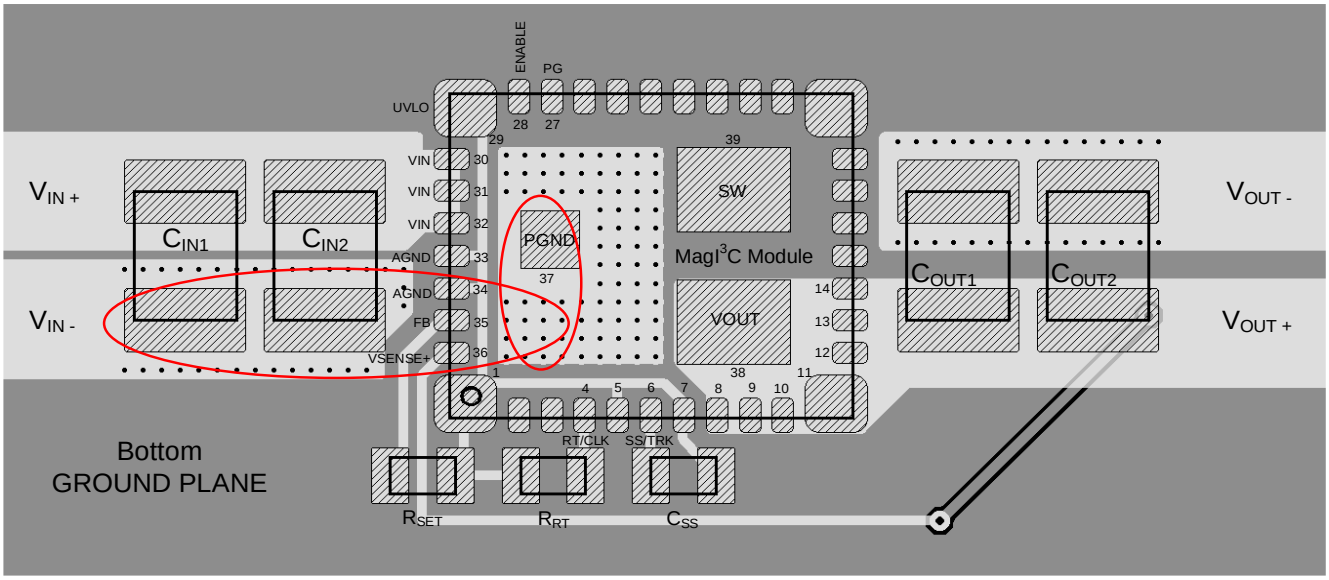
The placement of the input capacitors is highlighted in the following pictures of the evaluation board.

The positive terminal of CIN1 and CIN2 need to be very close to the V_{IN} pins of the power module.



PCB color coding: Top layer Bottom layer

The negative terminal of C_{IN1} and C_{IN2} need to be very close to the PGND pad of the power module. The ground path is passing through the vias at the C_{IN} terminals and thermal vias around the PGND pad.



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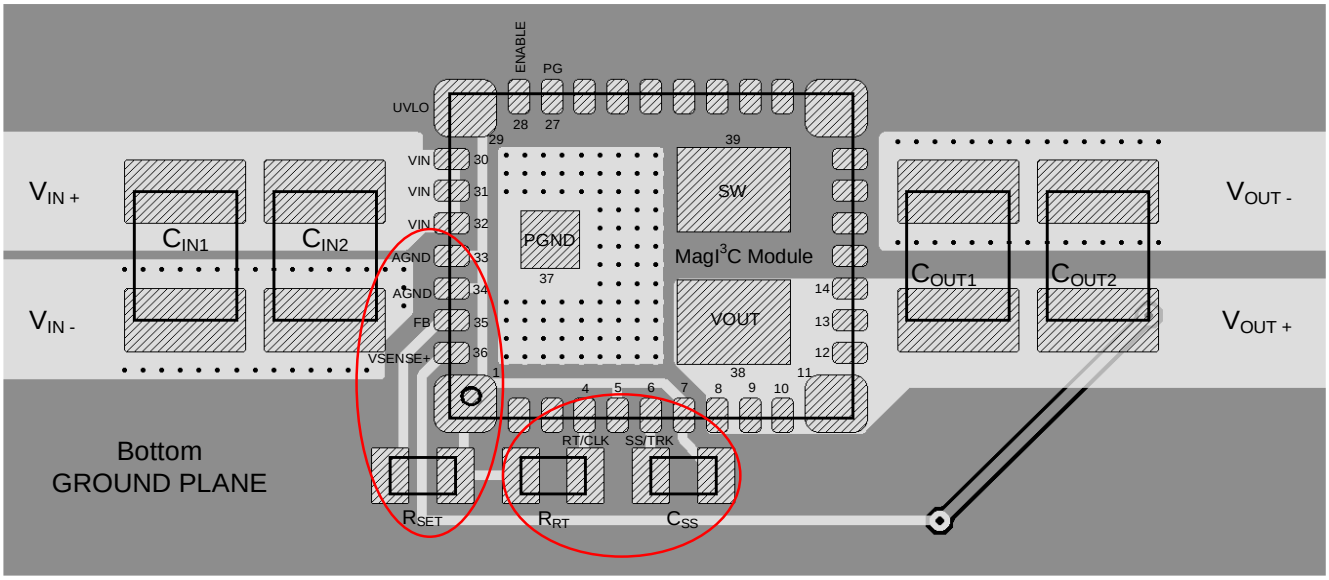
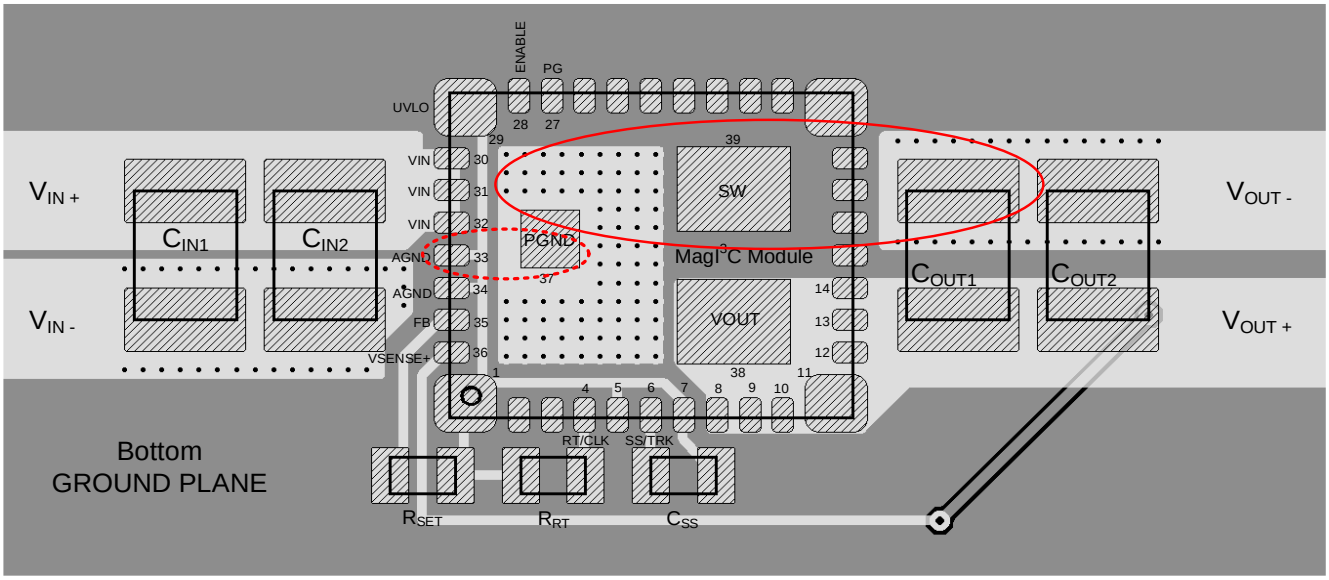
2: Analog Ground (AGND) connections

The ground connections for the clock setting resistor (R_{RT}), soft-start capacitor (SS/TRK), output voltage setting resistor (R_{SET}) and enable components should be routed to the AGND pins of the device. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Place R_{RT}, and C_{SS} close to their respective pins.



3: Analog Ground (AGND) to Power Ground (PGND) connections

The AGND is **internally connected** to PGND at a low noise node. The output ground current is flowing from the PGND pad through the ground plane through the ground terminal of the first output capacitor. Due to its very low ripple it will not inject noise in the ground plane.



Module Internal connection:

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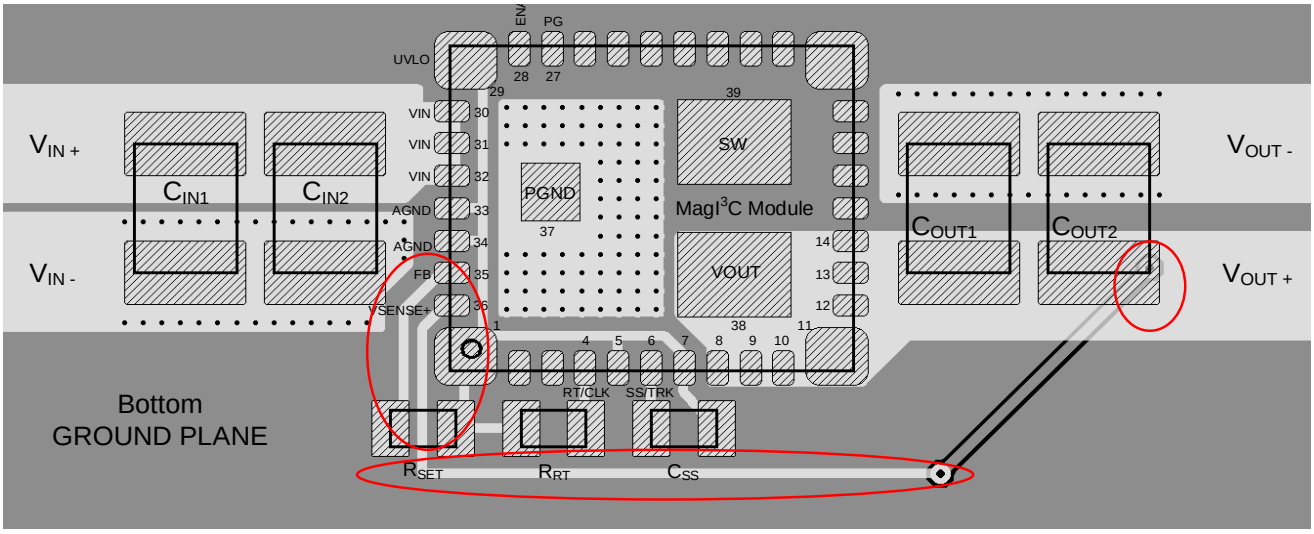
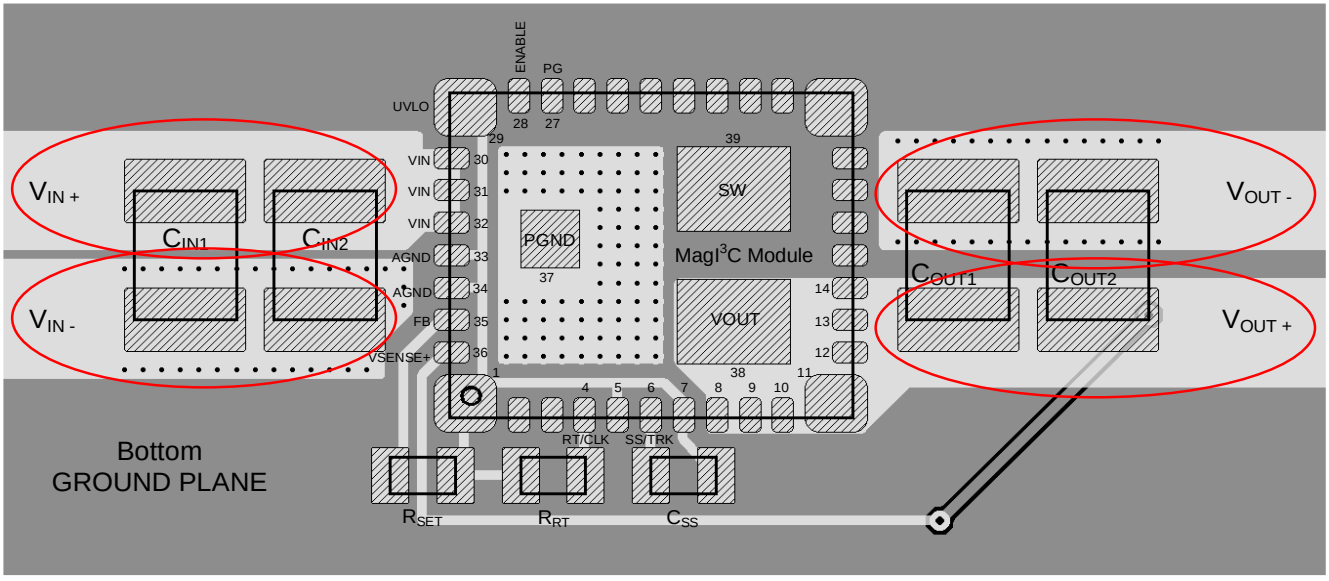
4: Feedback layout

The feedback resistor, R_{SET} should be located close to the FB pin. Since the FB node is high impedance, maintain the trace thickness small. The traces from R_{SET} should be routed away from the body of the MagI³C power module to minimize noise pickup. Connect the feedback trace at the positive terminal of the last output capacitor (C_{OUT2}). As this is the node of lowest noise.



5: Make input and output bus connections as wide as possible

This reduces any voltage drops on the input or output of the converter and maximizes efficiency.



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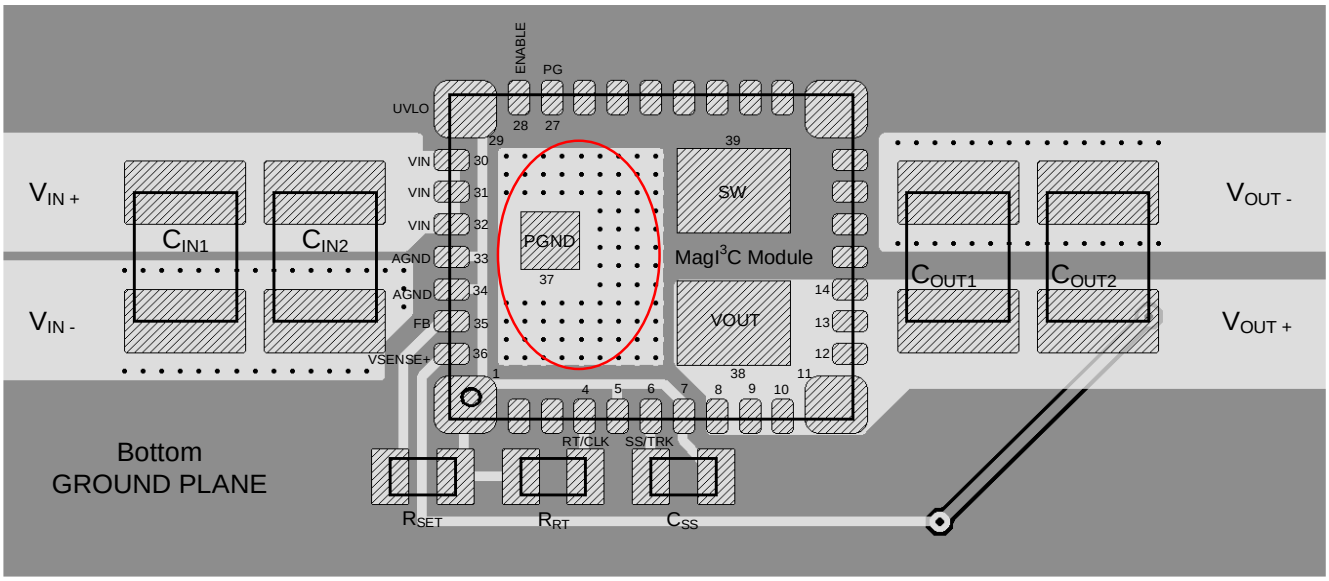
6: Provide adequate device heat-sinking

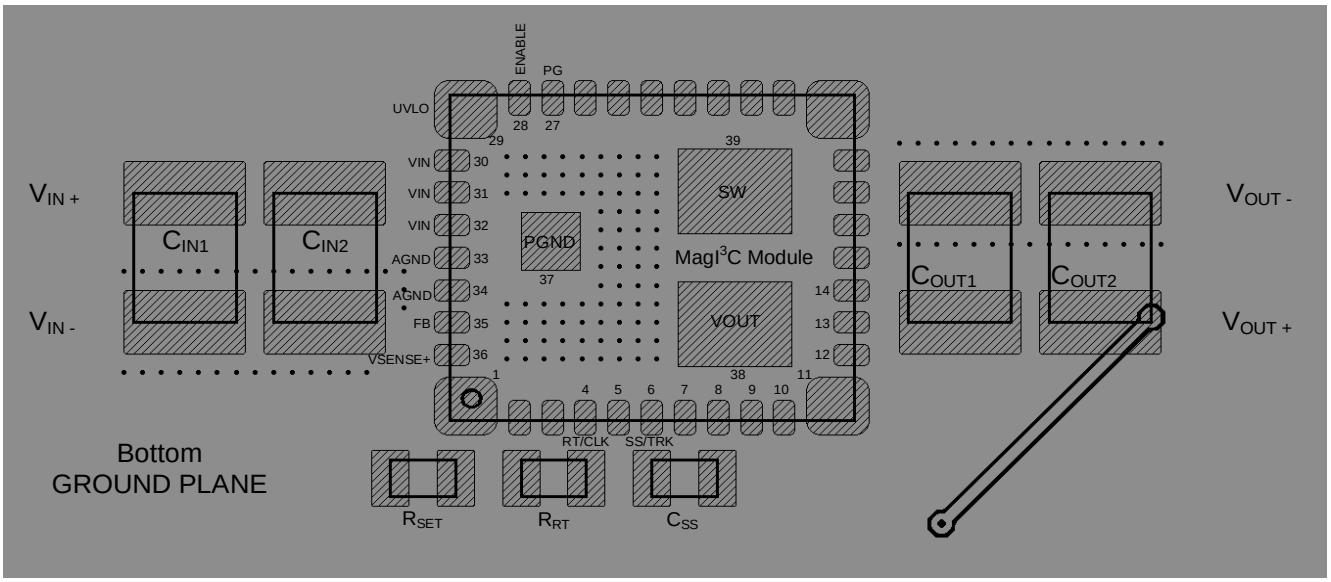
Place a dedicated PGND copper area beneath the MagI³C Power Module.

Use an array of heat-sinking vias to connect the PGND pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be used to make connection to inner layer heat-spreading ground planes. For best results use a via array as proposed in the picture above with via diameter of 200µm (hole: 100µm) thermal vias spaced 200µm. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.



6: Isolate high noise areas

Place a dedicated solid GND copper area beneath the MagI³C Power Module.



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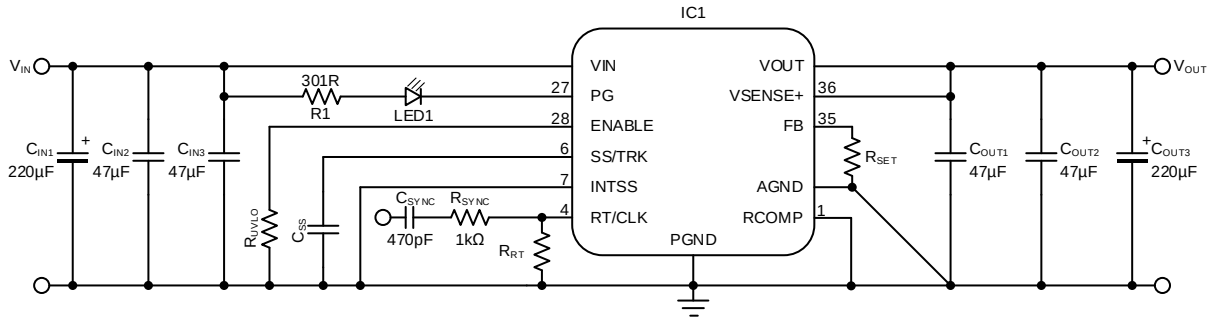
EVALUATION BOARD SCHEMATIC (178040302 v1.0)

The board schematic has been developed to be suitable for all conditions of input and output voltage, switching frequency, load current and to achieve optimum load transient response.

The two 47µF multi-layer ceramic capacitors (MLCCs) at the input handle the switching current ripple and support fast load transients preventing the voltage at the VIN pin from dropping, potentially below the UVLO. Two MLCCs in parallel helps reducing further the ESR. The additional 220µF aluminum electrolytic polymer capacitor is mounted as termination of the supply line and provides damping of possible oscillations due to the series resonance circuit represented by the inductance of the supply line and the input capacitance.
The output capacitors should provide a high value of capacitance as well as a low ESR, in order to reduce the output voltage ripple and improving load transient response. This is achieved in this evaluation board by combining two 47µF MLCCs with a 220µF aluminum electrolytic polymer capacitor. The use of two MLCCs in parallel leads to a further reduction of the ESR. Furthermore, the use of two parallel MLCCs at the input and at the output increases the reliability of the system.



Operational Requirements

At small V_{IN} to V_{OUT} ratio (high duty cycle) the input current will be in a similar range than the output current. Make sure that your supply for the module is capable of high currents (check current limit setting of your power supply). In case your module output voltage V_{OUT} is set to very low values (for example 0.8V) electronic loads might not be able to work correctly. Use discrete high power resistors instead as a load. Use thick and short leads to the input of the module and to the load. High currents result in additional voltage drops across the cables which decrease the voltage at the load. Measure the input and output voltage directly at the ceramic capacitors at the input and output (test points).

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Bill of Material

Designator	Description		Quantity	Order Code	Manufacturer
IC1	MagI³C Power Module		1	171040302	Würth Elektronik
C_{IN1},C_{OUT3}	Electrolytic polymer capacitor 220µF/10V		2	875105244013	Würth Elektronik
C_{IN2},C_{IN3},C_{OUT1},C_{OUT2}	Ceramic chip capacitor 47µF/10V X5R, 1210		4	885012109007	Würth Elektronik
C_{SYNC}	Ceramic chip capacitor 470pF/50V NP0/COG		1	885012007007	Würth Elektronik
LED1	LED red		1	150080SS75000	Würth Elektronik
C_{SS}, R_{UVLO}	Not mounted				
R_{SYNC}	1000Ω		1		
R1	301Ω		1		
R_{RT}	Set by jumper	1.2 MΩ for f_{SW} = 650kHz	1		
		715 kΩ for f_{SW} = 750kHz	1		
		348 kΩ for f_{SW} = 1MHz	1		
		232kΩ for f_{SW} = 1.25MHz	1		
		174kΩ for f_{SW} = 1.5MHz	1		
		113kΩ for f_{SW} = 2MHz	1		
R_{SET}	Set by jumper	5620Ω for V_{OUT} = 1.0V	1		
		2870Ω for V_{OUT} = 1.2V	1		
		1620Ω for V_{OUT} = 1.5V	1		
		1130Ω for V_{OUT} = 1.8V	1		
		665Ω for V_{OUT} = 2.5V	1		
		453Ω for V_{OUT} = 3.3V	1		

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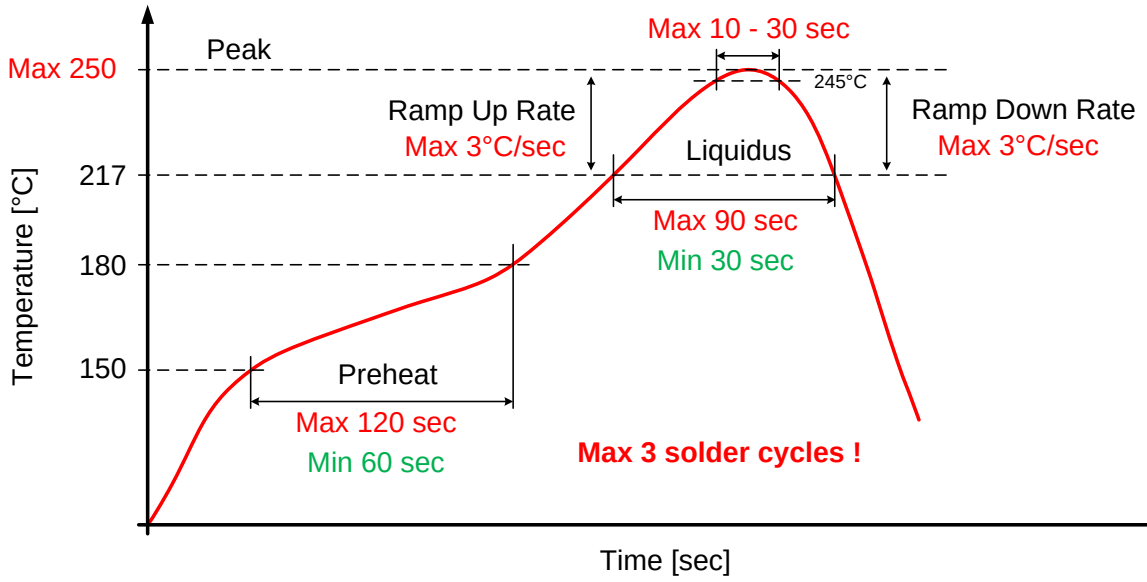
VDRM – Variable Step Down Regulator Module

HANDLING RECOMMENDATIONS

1. The power module is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033).
2. The parts are delivered in a sealed bag (Moisture Barrier Bags = MBB) and should be processed within one year.
3. When opening the moisture barrier bag check the Humidity Indicator Card (HIC) for color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card.
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033 recommendation.

SOLDER PROFILE

1. Only Pb-Free assembly is recommended according to JEDEC J-STD020.
2. Measure the peak reflow temperature of the MagI³C Power Module in the middle of the top view.
3. Ensure that the peak reflow temperature does not exceed 245°C ±5°C as per JEDEC J-STD020.
4. The reflow time period during peak temperature of 245°C ±5°C must not exceed 30 seconds.
5. Reflow time above liquidus (217°C) must not exceed 90 seconds.
6. Maximum ramp up is rate 3°C per second.
7. Maximum ramp down rate is 3°C per second.
8. Reflow time from room (25°C) to peak must not exceed 8 minutes as per JEDEC J-STD020.
9. **Maximum numbers of reflow cycles is three.**
10. **For minimum risk, solder the module in the last reflow cycle of the PCB production.**
11. For soldering process please consider lead material copper (Cu) and lead finish tin (Sn).
12. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
13. Below profile is valid for convection reflow only.
14. Other soldering methods (e.g.vapor phase) are not verified and have to be validated by the customer on his own risk.



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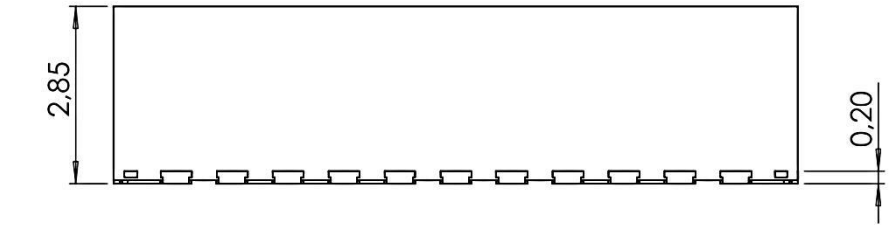
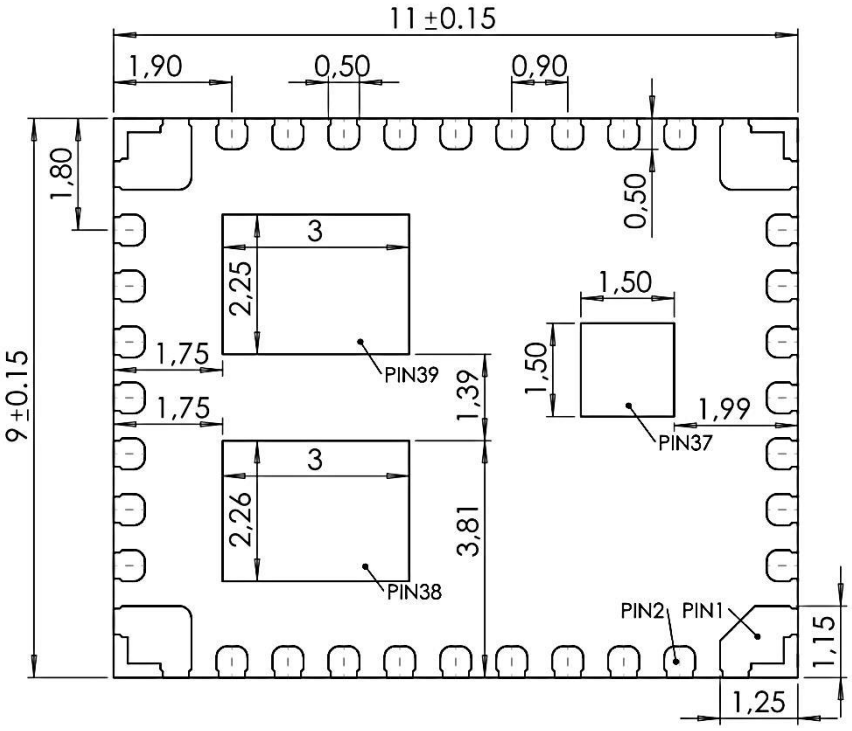
PHYSICAL DIMENSIONS





Bottom View

all dimensions in mm

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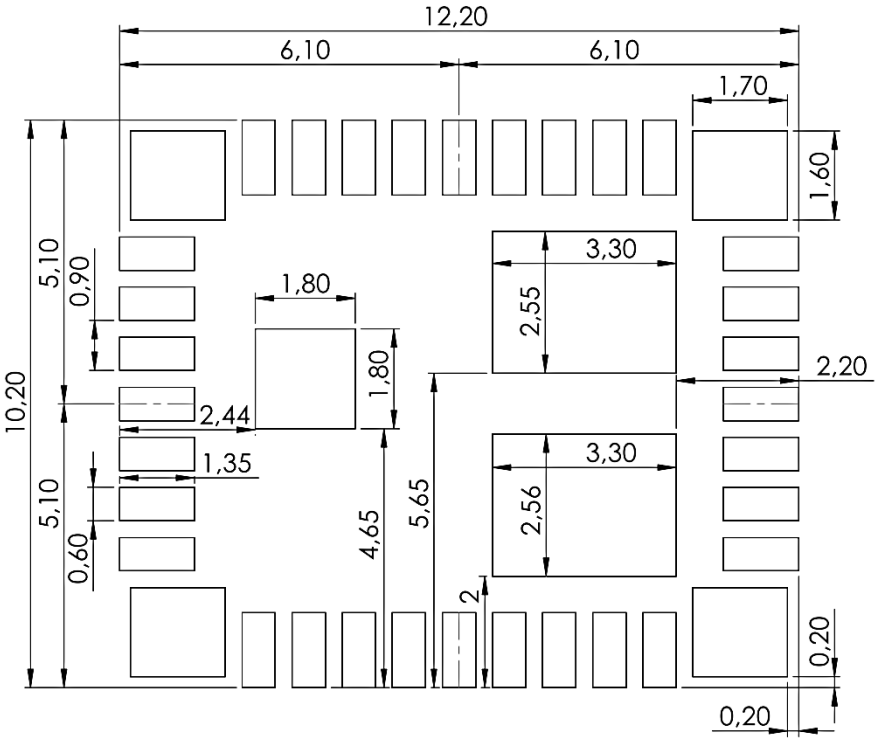
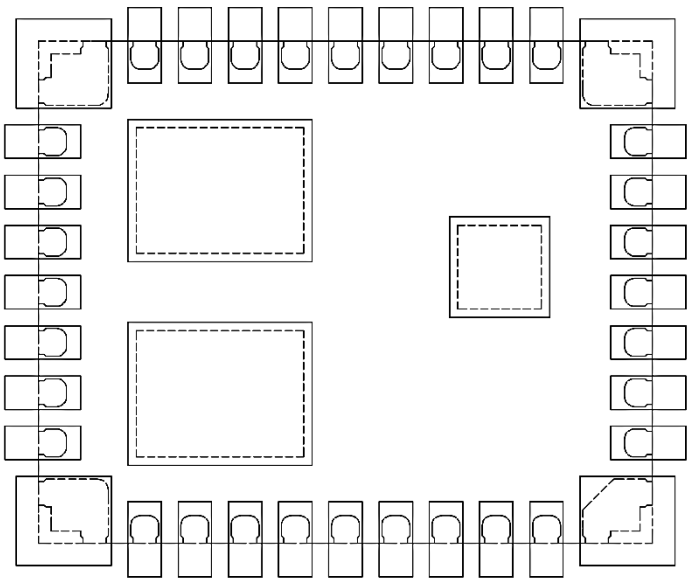
MagI³C Power Module
VDRM – Variable Step Down Regulator Module

EXAMPLE FOOTPRINT DESIGN



All dimensions in mm



Example footprint with pins

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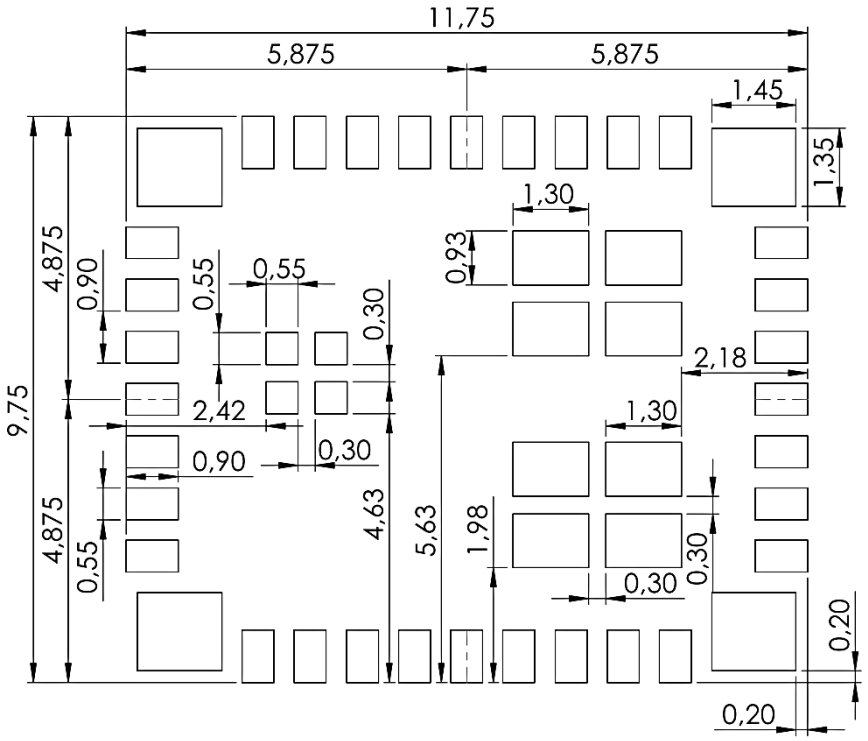
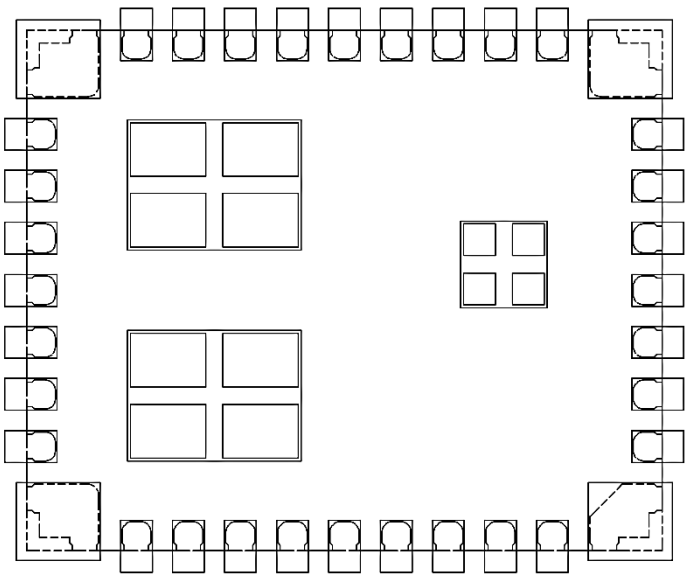
VDRM – Variable Step Down Regulator Module

EXAMPLE SOLDER PASTE STENCIL DESIGN



All dimensions in mm



Example solder paste stencil with pins
Stencil thickness 0.125mm

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DOCUMENT HISTORY

Revision	Date	Description	Comment
1.0	May 2016	Release of the final version	
1.1	July 2022	Minor formatting change	Added pin 1 to schematics on page 1, 18, 35 and 41. Adjusted equation for CIN, on page 21. Updated CAUTIONS AND WARNINGS and IMPORTANT NOTES

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MagI³C Power Module
VDRM – Variable Step Down Regulator Module

CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of MagI³C of Würth Elektronik eiSosGmbH & Co. KG:

General:

- This electronic component is designed and manufactured for use in general electronic equipment.
- Würth Elektronik must be asked for written approval (following the PPAP procedure) before incorporating thecomponents into any equipment in fields such as military, aerospace, aviation, nuclear control, submarine,transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical,public information network, etc. where higher safety and reliability are especially required and/or if there is thepossibility of direct damage or human injury.
- Electronic components that will be used in safety-critical or high-reliability applications, should be pre-evaluated bythe customer.
- The component is designed and manufactured to be used within the datasheet specified values. If the usage andoperation conditions specified in the datasheet are not met, the component may be damaged or dissolved.
- Do not drop or impact the components as material of the body, pins or termination may flake apart.
- Würth Elektronik products are qualified according to international standards, which are listed in each productreliability report. Würth Elektronik does not warrant any customer qualified product characteristics beyond WürthElektronik's specifications, for its validity and sustainability over time.
- All technical specifications for standard products also apply to customer specific products.
- Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory andsafety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KGcomponents in its applications, notwithstanding any applications-related information or support that may beprovided by Würth Elektronik eiSos GmbH & Co. KG. Customer represents and agrees that it has all thenecessary expertise to create and implement safeguards which anticipate dangerous consequences of failures,monitor failures and their consequences lessen the likelihood of failures that might cause harm and takeappropriate remedial actions. Customer will fully indemnify Würth Elektronik eiSos and its representatives againstany damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications.

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MagI³C Power Module
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Product specific:

Soldering:

- The solder profile must comply with the technical product specifications. All other profiles will void the warranty
- All other soldering methods are at the customer's own risk.
- Cleaning and Washing:
- Residual washing varnish agent that is used during the production to clean the application might change thecharacteristics of the body, pins or termination. The washing varnish agent may have a negative effect on the longterm function of the component
- Using a brush during the cleaning process may break the component. Therefore, we do not recommend using abrush during the PCB cleaning process.

Potting and Coating:

- If the component is potted in the customer application, the potting material might shrink or expand during and afterhardening. Shrinking could lead to an incomplete seal, allowing contaminants into the component. Expansion coulddamage the components or parts of it. We recommend a manual inspection after potting to avoid these effects.
- Conformal coating may affect the product performance.
- Storage Conditions:
- A storage of Würth Elektronik products for longer than 12 months is not recommended. Within other effects, theterminals may suffer degradation, resulting in bad solderability. Therefore, all products shall be used within theperiod of 12 months based on the day of shipment.
- Do not expose the components to direct sunlight.
- The storage conditions in the original packaging are defined according to DIN EN 61760-2.
- For a moisture sensitive component, the storage condition in the original packaging is defined according toIPC/JEDEC-J-STD-033. It is also recommended to return the component to the original moisture proof bag andreseal the moisture proof bag again
- ESD prevention methods need to be followed for manual handling and processing by machinery.
- The storage conditions stated in the original packaging apply to the storage time and not to the transportation timeof the components.

Packaging:

- The packaging specifications apply only to purchase orders comprising whole packaging units. If the orderedquantity exceeds or is lower than the specified packaging unit, packaging in accordance with the packagingspecifications cannot be ensured.

Handling:

- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void thewarranty and also the conformance to regulatory requirements.
- The edge castellation is designed and made for prototyping, i.e. hand soldering purposes, only.
- The applicable country regulations and specific environmental regulations must be observed.
- Do not disassemble the component. Evidence of tampering will void the warranty.
- The temperature rise of the component must be taken into consideration. The operating temperature is comprisedof ambient temperature and temperature rise of the component. The operating temperature of the component shallnot exceed the maximum temperature specified.
- Direct mechanical impact to the component must be prevented as the material of the body, pins or terminationcould flake or, in the worst case, could break. As these devices are sensitive to electrostatic discharge, proper ICHandling Procedures must be followed.These cautions and warnings comply with the state of the scientific and technical knowledge and are believed to beaccurate and reliable. However, no responsibility is assumed for inaccuracies or incompleteness.

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IMPORTANT NOTES

General Customer Responsibility

Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

Customer Responsibility Related to Specific, in Particular Safety-Relevant, Applications

It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

Best Care and Attention

Any product-specific notes, warnings and cautions must be strictly observed. Any disregard will result in the loss of warranty.

Customer Support for Product Specifications

Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

Product R&D

Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

Product Life Cycle

Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

Property Rights

All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

General Terms and Conditions

Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.

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