



**THE DATASHEET OF  
RMWV3216AGBG-5S2#AC0**



# RMWV3216A Series

32Mb Advanced LPSRAM (2M word × 16bit)

R10DS0259EJ0101

Rev.1.01

2020.02.20

## Description

The RMWV3216A Series is a family of 32-Mbit static RAMs organized 2,097,152-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMWV3216A Series has realized higher density, higher performance and low power consumption. The RMWV3216A Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 48-ball fine pitch ball grid array.

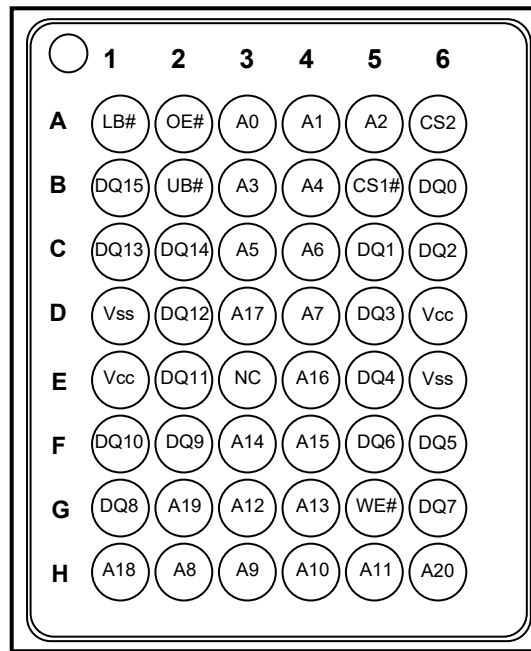
## Features

- Single 3V supply: 2.7V to 3.6V
- Access time: 55ns (max.)
- Current consumption:
  - Standby: 1.0μA (typ.)
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Battery backup operation

## Part Name Information

Part Name	Access time	Temperature Range	Package
RMWV3216AGBG-5S2	55 ns	-40 ~ +85°C	48-ball FBGA with 0.75mm ball pitch

Pin Arrangement

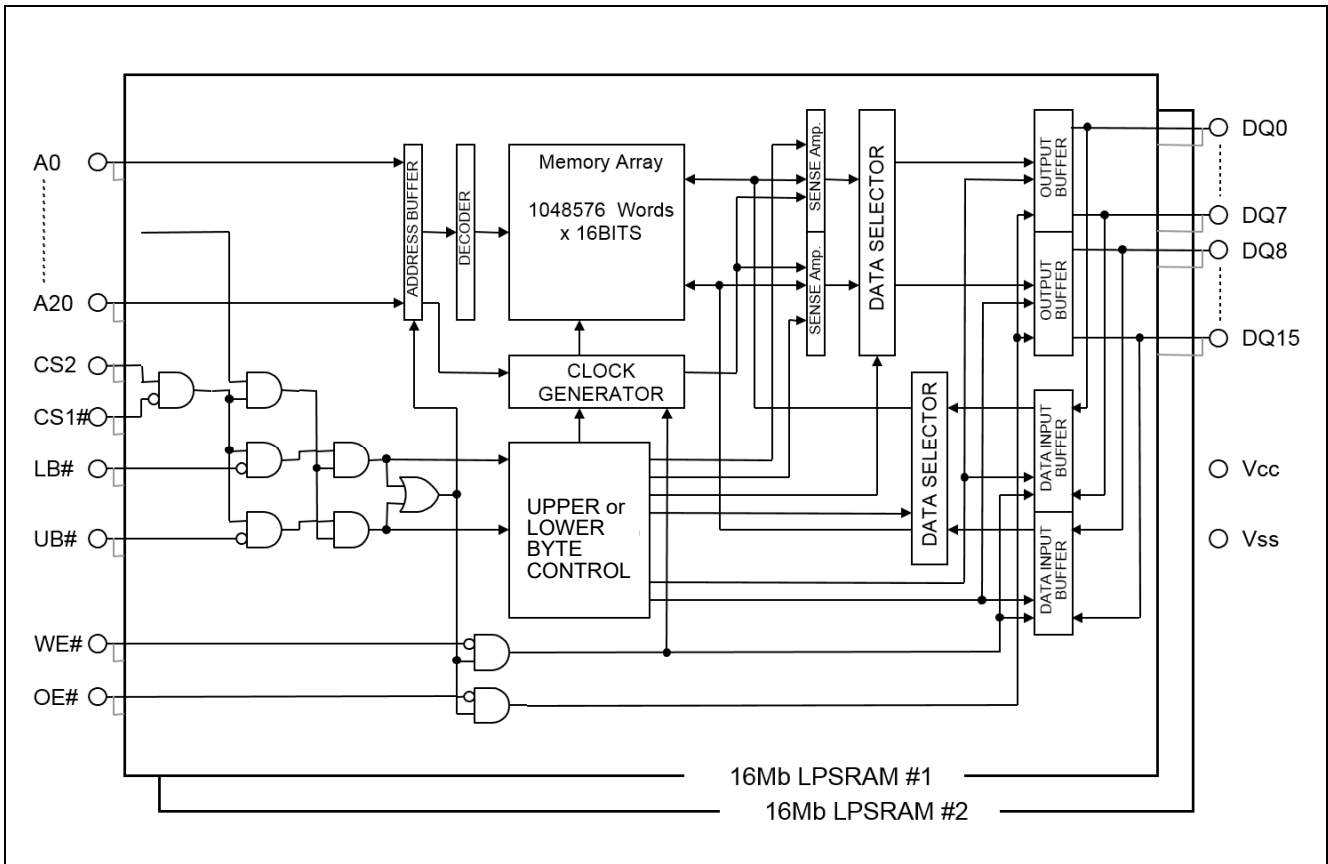


48-ball FBGA (TOP VIEW)

Pin Description

Pin name	Function
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground
A0 to A20	Address input
DQ0 to DQ15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
NC	No connection

Block Diagram



Operation Table

CS1#	CS2	WE#	OE#	UB#	LB#	DQ0~7	DQ8~15	Operation
H	X	X	X	X	X	High-Z	High-Z	Stand-by
X	L	X	X	X	X	High-Z	High-Z	Stand-by
X	X	X	X	H	H	High-Z	High-Z	Stand-by
L	H	H	L	L	L	Dout	Dout	Read read
L	H	H	L	H	L	Dout	High-Z	Read in lower byte
L	H	H	L	L	H	High-Z	Dout	Read in upper byte
L	H	L	X	L	L	Din	Din	Write
L	H	L	X	H	L	Din	High-Z	Write in lower byte
L	H	L	X	L	H	High-Z	Din	Write in upper byte
L	H	H	H	X	X	High-Z	High-Z	Output disable

Note 1. H: V<sub>IH</sub> L: V<sub>IL</sub> X: V<sub>IH</sub> or V<sub>IL</sub>

## Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5 to +4.6	V
Terminal voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub>	-0.5 <sup>2</sup> to V <sub>CC</sub> +0.3 <sup>3</sup>	V
Power dissipation	P <sub>T</sub>	0.7	W
Operation temperature	T <sub>opr</sub>	-40 to +85	°C
Storage temperature range	T <sub>stg</sub>	-65 to +150	°C
Storage temperature range under bias	T <sub>bias</sub>	-40 to +85	°C

Note 2. -2.0V for pulse ≤ 30ns (full width at half maximum)

3. Maximum voltage is +4.6V.

## DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V	
	V <sub>SS</sub>	0	0	0	V	
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> +0.3	V	
Input low voltage	V <sub>IL</sub>	-0.3	—	0.6	V	4
Ambient temperature range	T <sub>a</sub>	-40	—	+85	°C	

Note 4. -2.0V for pulse ≤ 30ns (full width at half maximum)

## DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	I <sub>LI</sub>	—	—	1	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	—	—	1	μA	CS1# = V <sub>IH</sub> or CS2 = V <sub>IL</sub> or OE# = V <sub>IH</sub> or WE# = V <sub>IL</sub> or LB# = UB# = V <sub>IH</sub> , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Average operating current	I <sub>CC1</sub>	—	25 <sup>5</sup>	30	mA	Cycle = 55ns, duty = 100%, I <sub>I/O</sub> = 0mA, CS1# = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>	
	I <sub>CC2</sub>	—	2 <sup>5</sup>	4	mA	Cycle = 1μs, duty = 100%, I <sub>I/O</sub> = 0mA, CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V, V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V, V <sub>IL</sub> ≤ 0.2V	
Standby current	I <sub>SB</sub>	—	—	0.3	mA	CS2 = V <sub>IL</sub> , Others = V <sub>SS</sub> to V <sub>CC</sub>	
Standby current	I <sub>SB1</sub>	—	1.0 <sup>5</sup>	6	μA	~+25°C	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub> , (1) CS2 ≤ 0.2V or (2) CS1# ≥ V <sub>CC</sub> -0.2V, CS2 ≥ V <sub>CC</sub> -0.2V or (3) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V
		—	1.6 <sup>6</sup>	12	μA	~+40°C	
		—	5 <sup>7</sup>	24	μA	~+70°C	
		—	10 <sup>8</sup>	32	μA	~+85°C	
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1mA	
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2mA	

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=25°C), and not 100% tested.

6. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=40°C), and not 100% tested.

7. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=70°C), and not 100% tested.

8. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=85°C), and not 100% tested.

## Capacitance

(T<sub>a</sub> =25°C, f =1MHz)

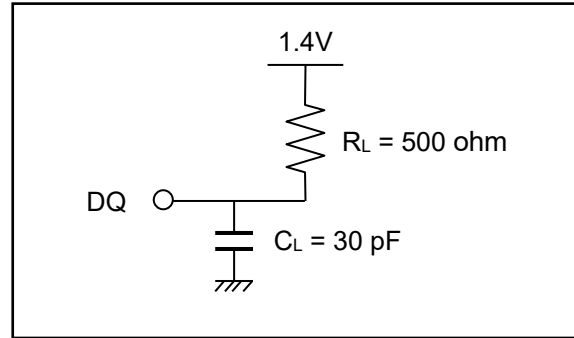
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C <sub>in</sub>	—	—	10	pF	V <sub>in</sub> =0V	9
Input / output capacitance	C <sub>I/O</sub>	—	—	10	pF	V <sub>I/O</sub> =0V	9

Note 9. This parameter is sampled and not 100% tested.

## AC Characteristics

Test Conditions ( $V_{CC} = 2.7V \sim 3.6V$ ,  $T_a = -40 \sim +85^{\circ}C$ )

- Input pulse levels:  
 $V_{IL} = 0.4V$ ,  $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



## Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	$t_{RC}$	55		ns	
Address access time	$t_{AA}$	—	55	ns	
Chip select access time	$t_{ACS1}$	—	45	ns	
	$t_{ACS2}$	—	45	ns	
Output enable to output valid	$t_{OE}$	—	22	ns	
Output hold from address change	$t_{OH}$	10	—	ns	
LB#, UB# access time	$t_{BA}$	—	45	ns	
Chip select to output in low-Z	$t_{CLZ1}$	10	—	ns	10,11
	$t_{CLZ2}$	10	—	ns	10,11
LB#, UB# enable to low-Z	$t_{BLZ}$	5	—	ns	10,11
Output enable to output in low-Z	$t_{OLZ}$	5	—	ns	10,11
Chip deselect to output in high-Z	$t_{CHZ1}$	0	18	ns	10,11,12
	$t_{CHZ2}$	0	18	ns	10,11,12
LB#, UB# disable to high-Z	$t_{BHZ}$	0	18	ns	10,11,12
Output disable to output in high-Z	$t_{OHZ}$	0	18	ns	10,11,12

Note 10. This parameter is sampled and not 100% tested.

- At any given temperature and voltage condition,  $t_{CHZ1}$  max is less than  $t_{CLZ1}$  min,  $t_{CHZ2}$  max is less than  $t_{CLZ2}$  min,  $t_{BHZ}$  max is less than  $t_{BLZ}$  min, and  $t_{OHZ}$  max is less than  $t_{OLZ}$  min, for any device.
- $t_{CHZ1}$ ,  $t_{CHZ2}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	$t_{WC}$	55	—	ns	
Address valid to write end	$t_{AW}$	35	—	ns	
Chip select to write end	$t_{CW}$	35	—	ns	
Write pulse width	$t_{WP}$	35	—	ns	13
LB#,UB# valid to write end	$t_{BW}$	35	—	ns	
Address setup time to write start	$t_{AS}$	0	—	ns	
Write recovery time from write end	$t_{WR}$	0	—	ns	
Data to write time overlap	$t_{DW}$	25	—	ns	
Data hold from write end	$t_{DH}$	0	—	ns	
Output enable from write end	$t_{OW}$	5	—	ns	13
Output disable to output in high-Z	$t_{OHZ}$	0	18	ns	14,15
Write to output in high-Z	$t_{WHZ}$	0	18	ns	14,15

Note 13.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

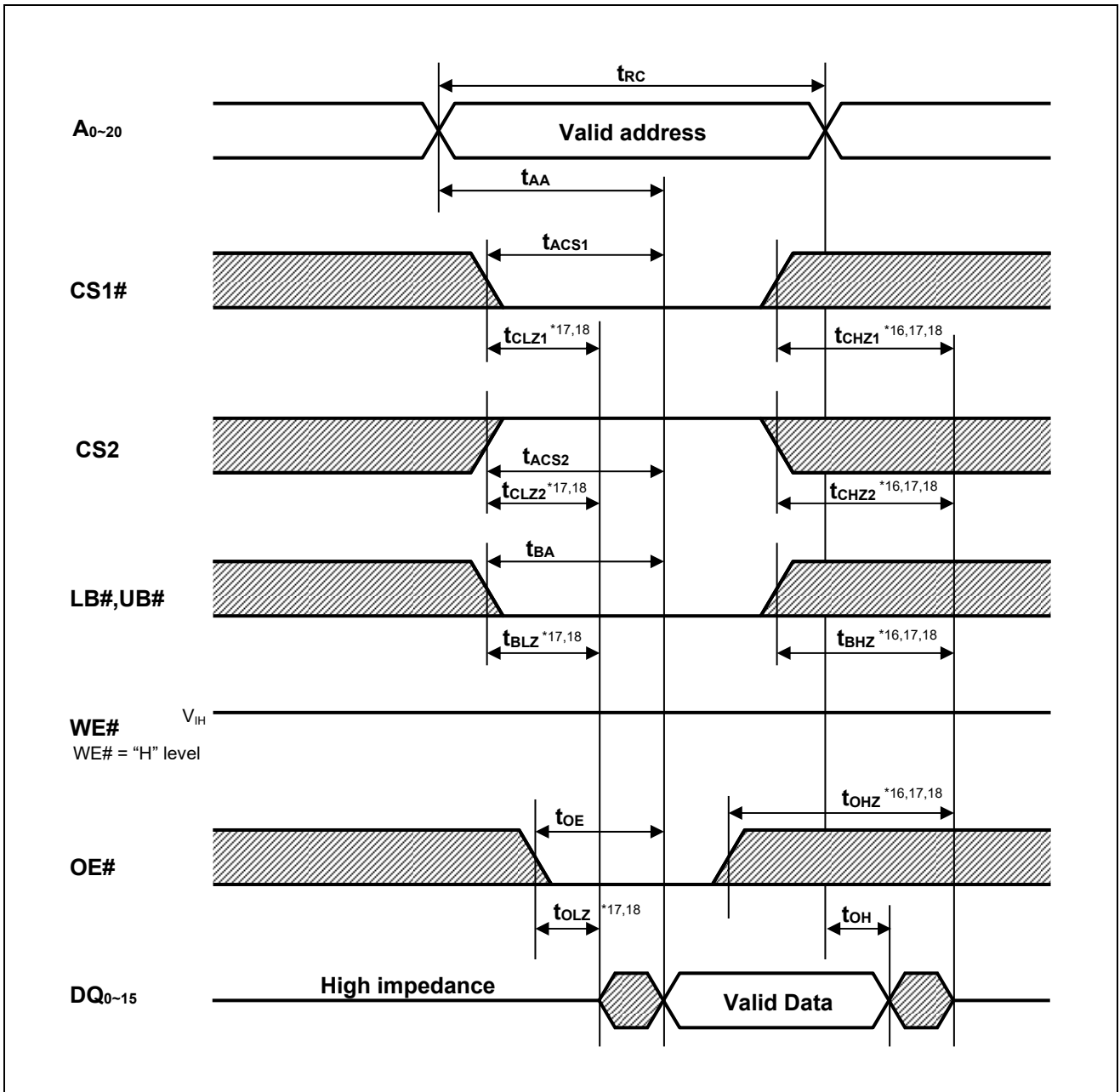
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

14. This parameter is sampled and not 100% tested.

15.  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

## Timing Waveforms

### Read Cycle

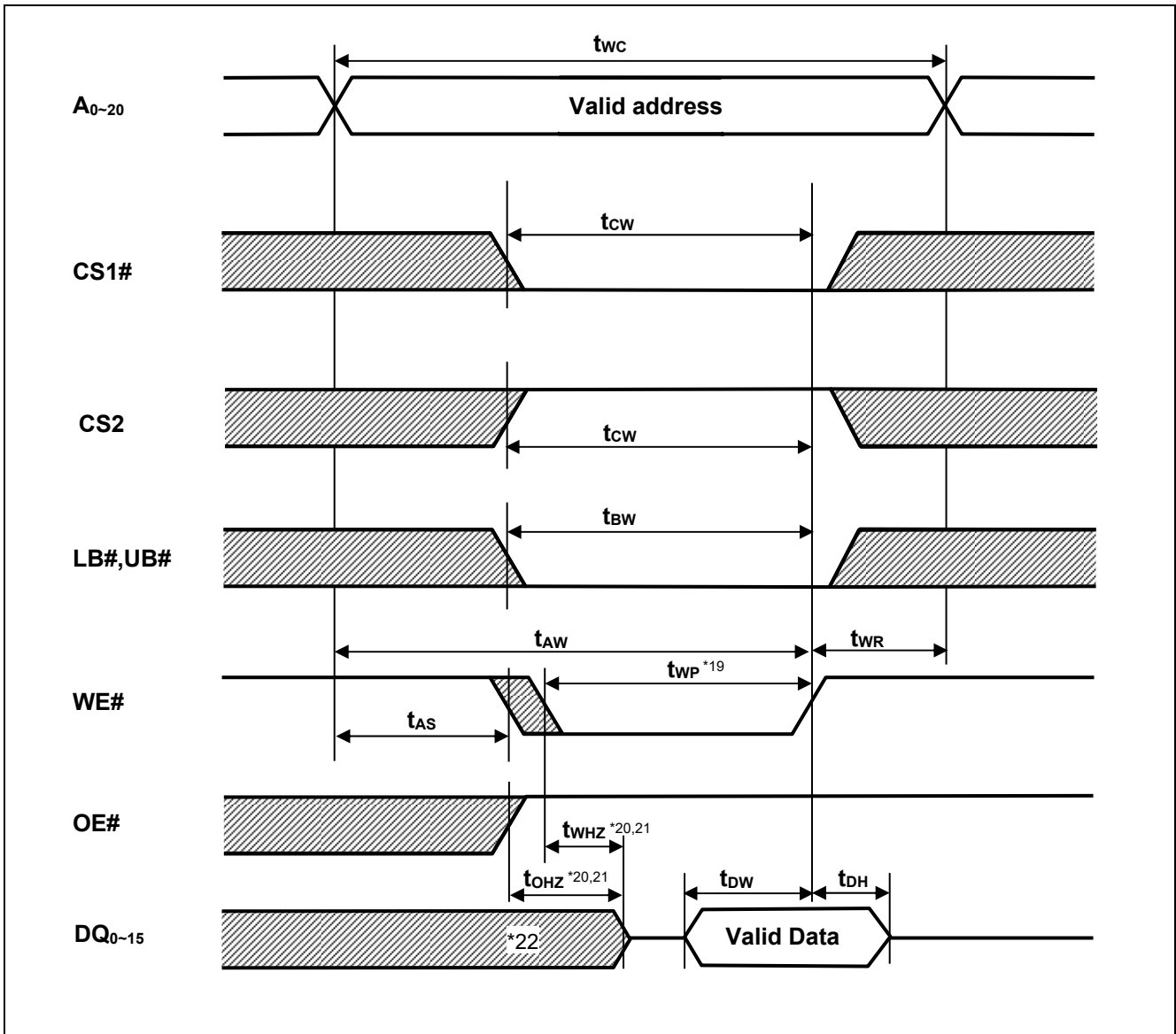


Note 16.  $t_{CHZ1}$ ,  $t_{CHZ2}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

17. This parameter is sampled and not 100% tested.

18. At any given temperature and voltage condition,  $t_{CHZ1}$  max is less than  $t_{CLZ1}$  min,  $t_{CHZ2}$  max is less than  $t_{CLZ2}$  min,  $t_{BHZ}$  max is less than  $t_{BLZ}$  min, and  $t_{OHZ}$  max is less than  $t_{OLZ}$  min, for any device.

Write Cycle (1) (WE# CLOCK, OE#="H" while writing)



Note 19.  $t_{wp}$  is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

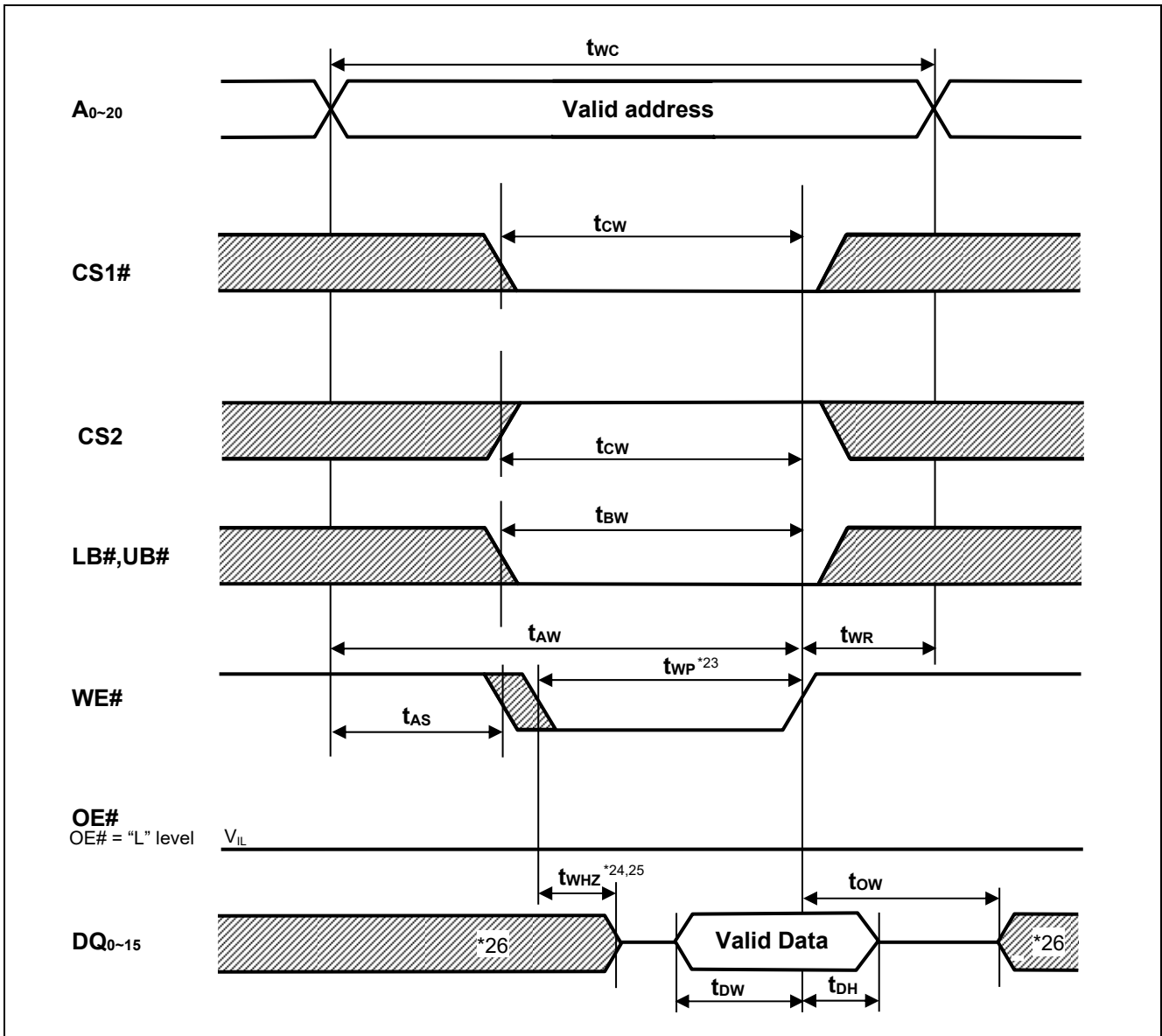
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

20.  $t_{ohz}$  and  $t_{whz}$  are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

21. This parameter is sampled and not 100% tested.

22. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (2) (WE# CLOCK, OE# Low Fixed)



Note 23.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

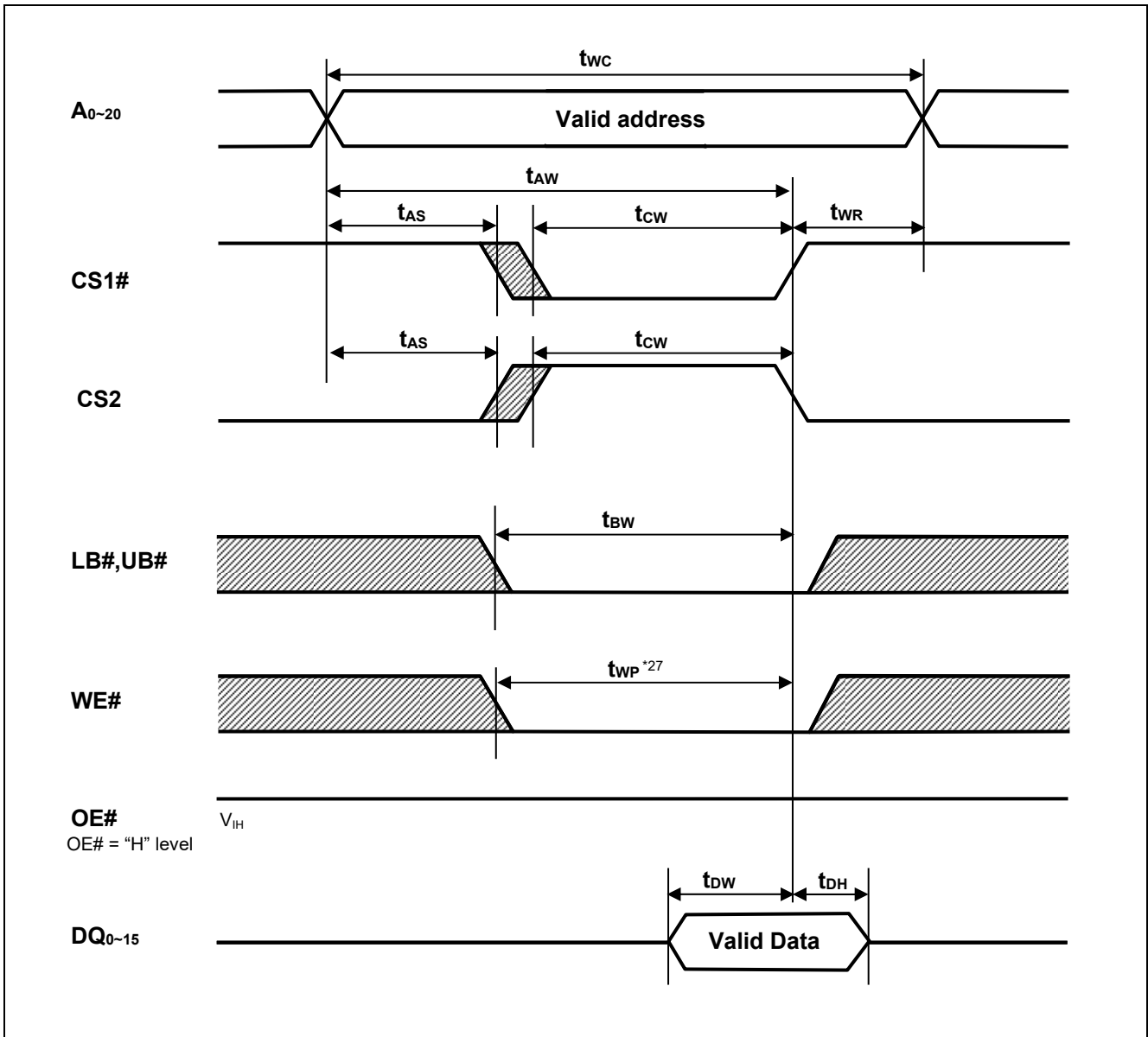
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

24.  $t_{WHZ}$  is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

25. This parameter is sampled and not 100% tested.

26. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (3) (CS1#, CS2 CLOCK)



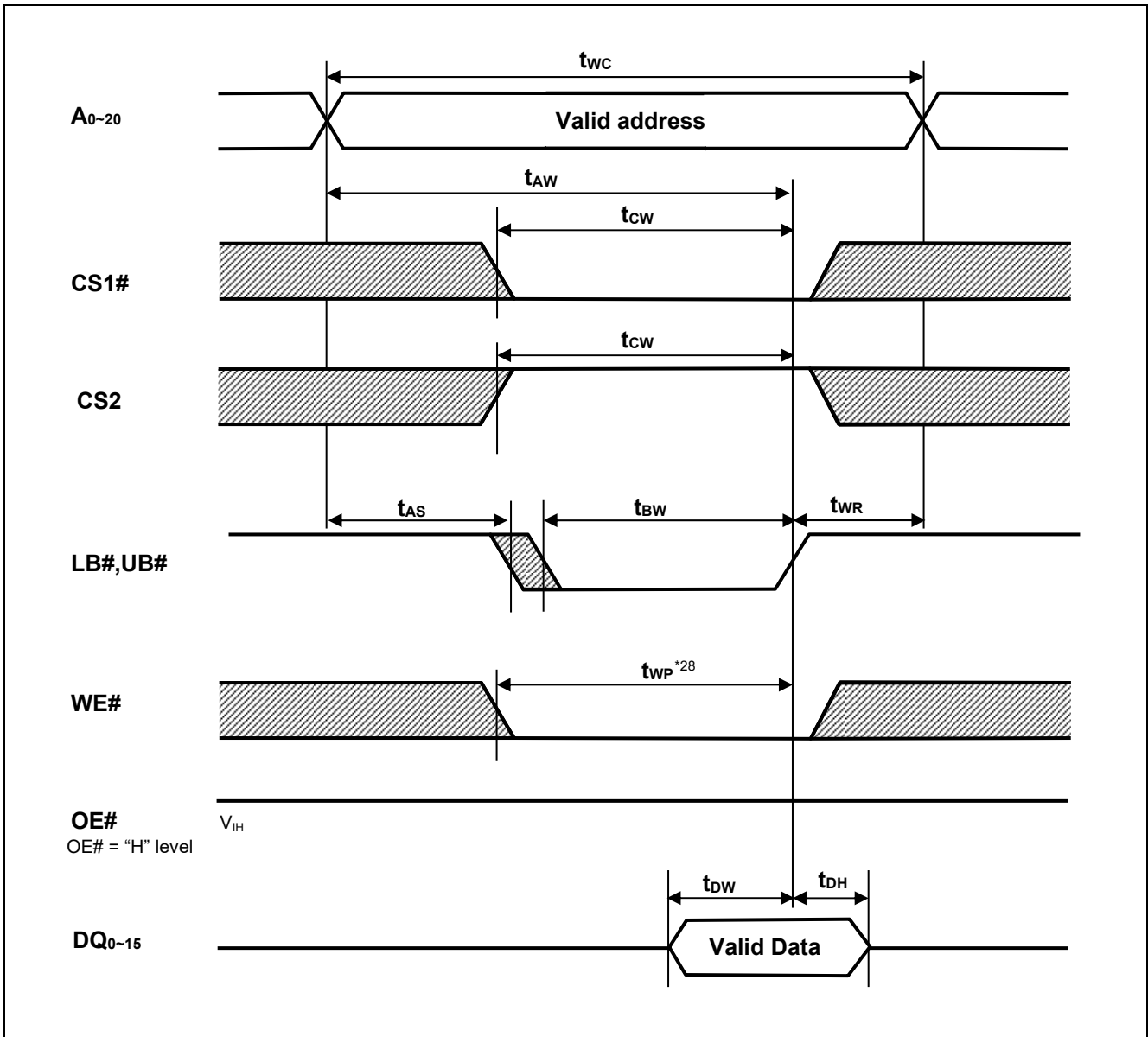
Note 27.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4) (LB#, UB# CLOCK)



Note 28.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

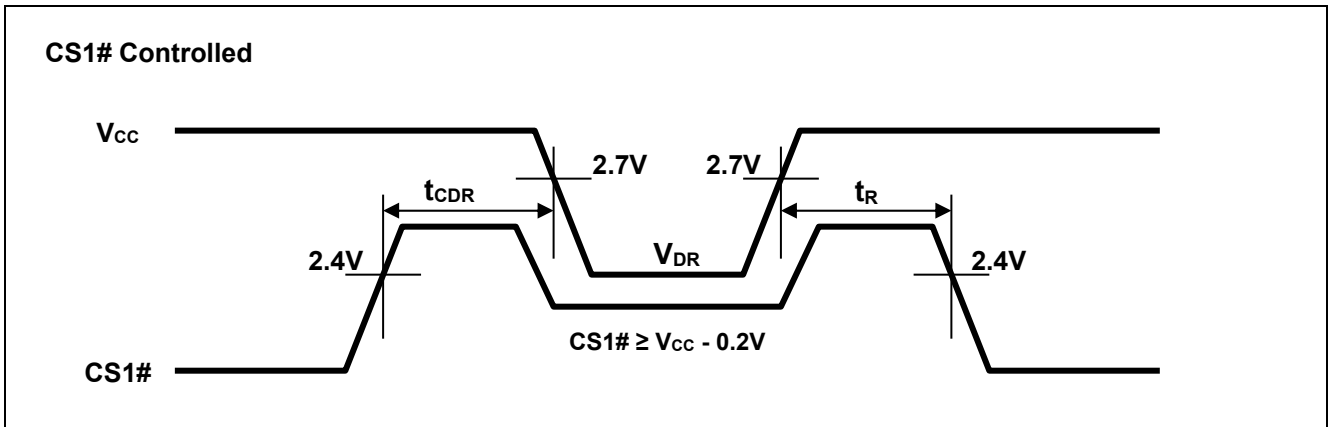
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Low V<sub>CC</sub> Data Retention Characteristics

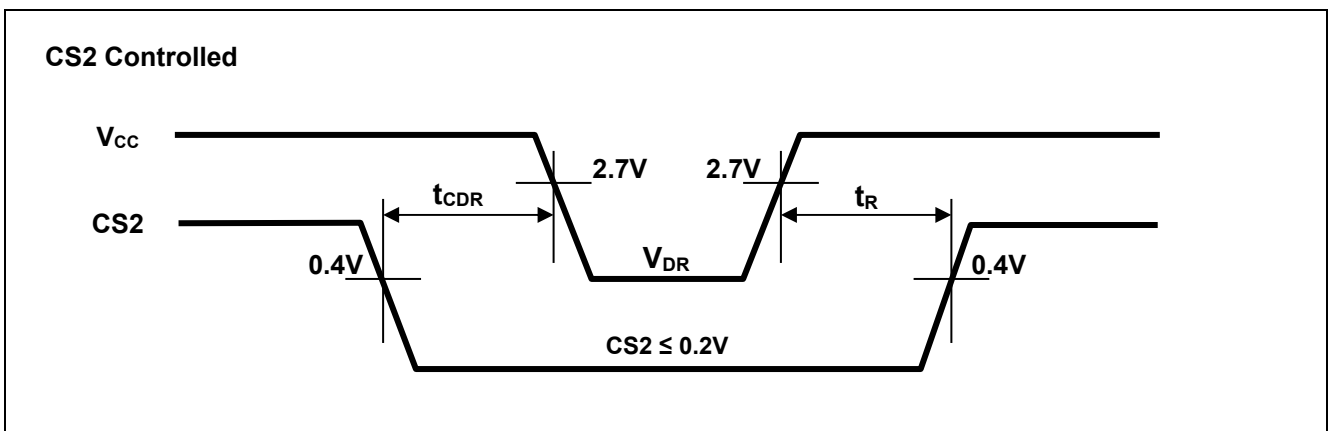
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions <sup>*29</sup>	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	1.5	—	3.6	V	Vin ≥ 0V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V <sub>CC</sub> -0.2V, CS2 ≥ V <sub>CC</sub> -0.2V or (3) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V	
Data retention current	I <sub>CCDR</sub>	—	1.0 <sup>*30</sup>	6	μA	~+25°C	V <sub>CC</sub> = 3.0V, Vin ≥ 0V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V <sub>CC</sub> -0.2V, CS2 ≥ V <sub>CC</sub> -0.2V or (3) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V
		—	1.6 <sup>*31</sup>	12	μA	~+40°C	
		—	5 <sup>*32</sup>	24	μA	~+70°C	
		—	10 <sup>*33</sup>	32	μA	~+85°C	
Chip deselect time to data retention	t <sub>CDR</sub>	0	—	—	ns	See retention waveform.	
Operation recovery time	t <sub>R</sub>	5	—	—	ms		

- Note 29. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and DQ buffer.  
 If CS2 controls data retention mode, Vin levels (address, WE#, CS1#, OE#, LB#, UB#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V<sub>CC</sub>-0.2V or CS2 ≤ 0.2V.  
 The other inputs levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high-impedance state.
30. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25°C), and not 100% tested.
31. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40°C), and not 100% tested.
32. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=70°C), and not 100% tested.
33. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=85°C), and not 100% tested.

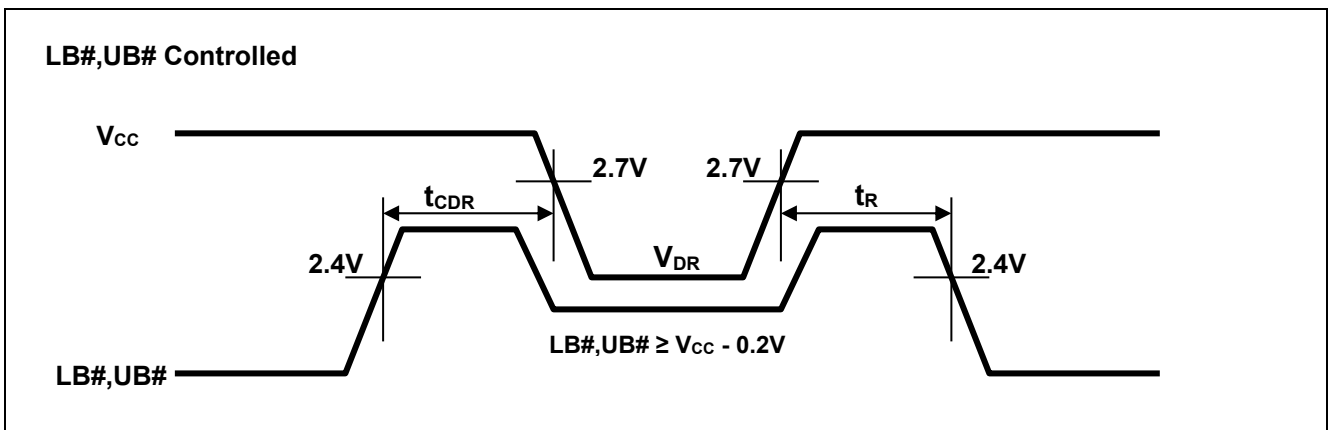
Low Vcc Data Retention Timing Waveforms (CS1# controlled)



Low Vcc Data Retention Timing Waveforms (CS2 controlled)



Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled)



Revision History	RMWV3216A Series Data Sheet
------------------	-----------------------------

Rev.	Date	Description	
		Page	Summary
1.00	2016.01.06	—	First Edition issued
1.01	2020.02.20	Last page	Updated the Notice to the latest version

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information



For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View RMWV3216AGBG-5S2#AC0 on WIN SOURCE](#)
-  [Renesas Electronics America Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management