THE DATASHEET OF

MC33XS2410ELR2

MC33XS2410

Quad 100 mΩ / dual 50 mΩ, 3.0 V to 60 V high-side switch

Rev. 7 — 31 October 2022 Product data sheet

1 General description

The MC33XS2410 is a four channel self-protected high-side switch. Featuring advanced digital monitoring and control function, the device is operational from 3.0 V to 60 V. As a result of high-level integration, the embedded 12-bit analog-to-digital converter enables a drastically simplified hardware design and MCU software control. The device is controlled by SPI port for configuration, monitoring and diagnostics of the outputs. Whenever communication with the MCU is lost, the device enters a safe operation mode, but remains operational, controllable and protected.

This product has been qualified to the appropriate Automotive Electronics Council (AEC) standard Q100 and is suitable for use in automotive applications.

2 Features and benefits

- Four fully protected 100 mΩ / dual 50 mΩ (at 25 °C) high-side switches
- Active current limitation is 5 A
- Configurable parallel mode to double current capability
- 16-bit SPI port communication 3.3 V / 5.0 V compatible with daisy chain capability
- Outputs controllable via SPI-bus or direct inputs
- Diagnostic status reported via SPI-bus
- Watchdog for invalid commands or inactive SPI, with programmable timeout
- Programmable interrupt generator that reports to $\overline{\text{FAULT}}$ pin or SPI-bus
- Four independent PWM modules programmable from 0.5 Hz to 2.0 kHz with internal or external clock
- Protection for battery transient overvoltage and reversed polarity battery connection
- Configurable safe mode
- Standby mode with very low power consumption
- Digital PI PWM closed loop current regulation
- External FAULTB pin for warning or IRQ reporting
- 10 mA open load detection in ON state
- Latch off with configurable auto retry
- Configurable severe short-circuit and overload protection
- Programmable active current limit threshold to minimize short-circuit effect
- 12 bits ADC:
  - Current from 5.0 mA to 5.0 A with ± 6 % above 1 A
  - Voltage from 0.5 V to 65 V with ± 6.5 % above 5.0 V
  - Temperature warning for each channel and central die monitoring
- Qualified in accordance with AEC Q100 grade 1
- Electrical transient disturbance immunity according of ISO 7637-2 and ISO 16750-2

3 Applications

- 12 V automotive, truck, and off-highway equipment
- 12 V and 24 V systems as well as industrial applications up to 60 V
- LED modules
- Solenoids valve and solenoid valve proportional with PI regulation
- DC motor up to 20 W with PWM control
- Incandescent bulbs up to 21 W
- ECU module with large input bypass capacitor, 470 µF and above

4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PWR}	Power supply voltage	operating [1]	3.0	14 / 28	60[2]	V
I_{OUT_4DC}	Nominal load current	4 outputs active [3]	—	1.8	—	A
I_{OUT_2DC}	Parallel mode load	2 outputs active [3]	—	3.6	—	A
T_J	Junction temperature	—	–40	—	+150	°C
I_{VDD_STB}	Stand-by current (Disable mode)	Tj ≤ 85 °C	—	—	1	µA
F_{SPI}	SPI frequency	— [4]	—	—	10	MHz

[1] When V_{PWR} < 4.0 V, full device operation is guaranteed if V_{DD} ≥ 4.0 V.
[2] Device is designed to operate with 12 V and 24 V bus/truck mission profiles. Maximum continuous voltage depends on application mission profile.
[3] PCB JEDEC 2s2p, T_{amb} ≤ 85 °C, $R_{th(j-a)}$ = 24 °C/W (see thermal characteristics).
[4] Maximum SPI frequency can be reduced depending on output buffer configuration.

5 Ordering information

Table 2. Ordering information

Part number [1]	Package		
	Name	Description	Version
MC33XS2410EL	HTSSOP28	Plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad	SOT1172-4

[1] To order parts in tape and reel, add the R2 suffix to the part number.

6 Block diagram

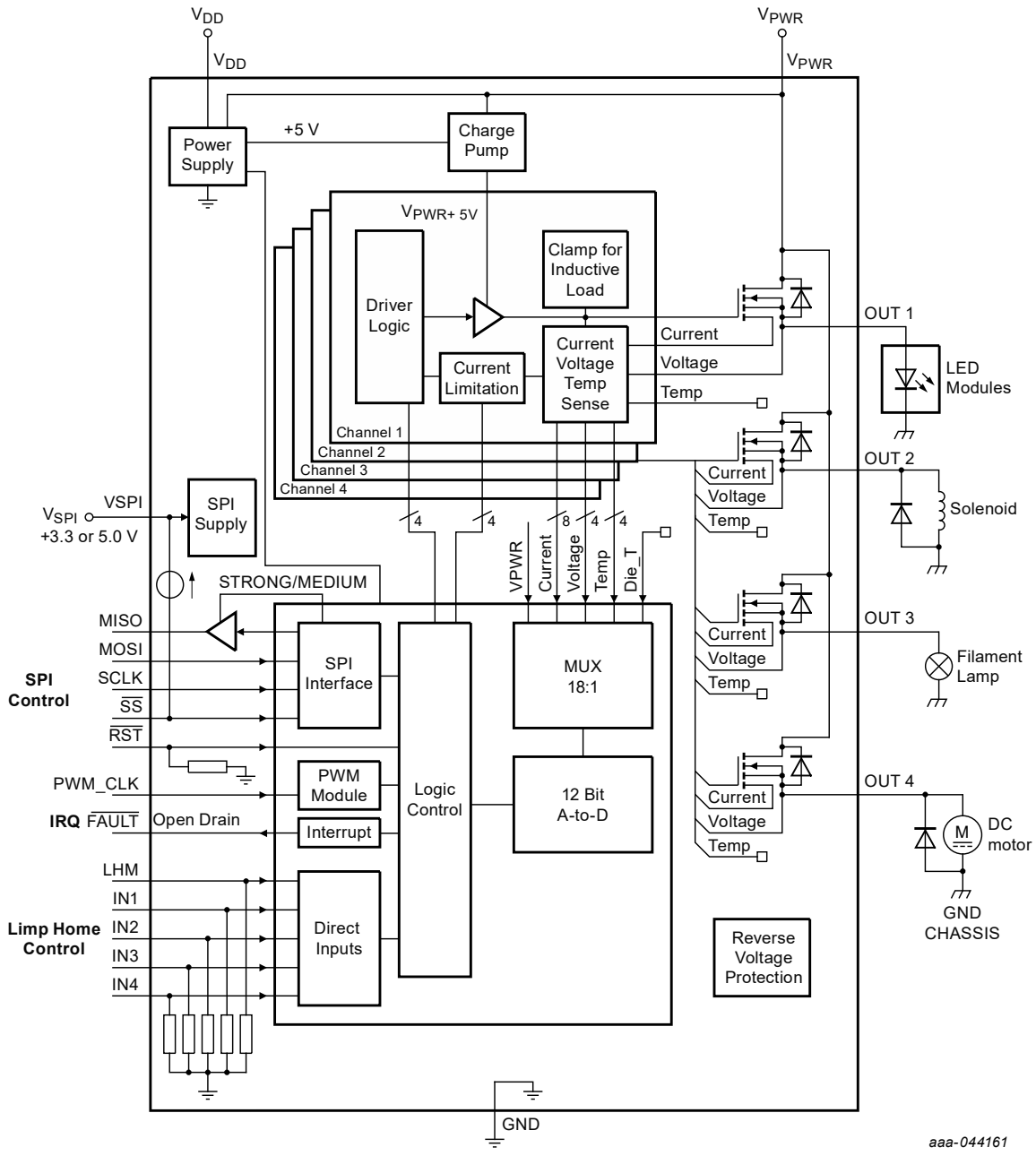


Figure 1. Block diagram

7 Pinning information

7.1 Pinning

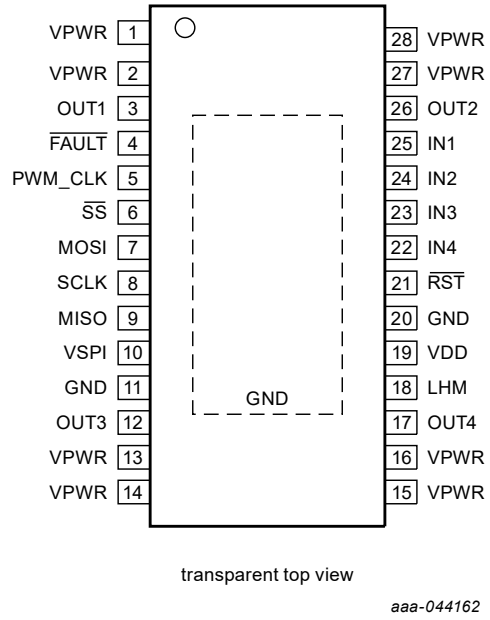


Figure 2. Pin configuration for HTSSOP28

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
Supplies			
VPWR	1, 2, 13, 14, 15, 16, 27, 28	Power	Power switch supply
VDD	19	Power	Logic supply voltage
VSPI	10	Power	Supply voltage for SPI
GND	11, 20	Power	Device ground
Digital			
$\overline{RST}$	21	Input	Reset input; pulldown resistor
$\overline{FAULT}$	4	Output	Interrupt output; open-drain output
PWM_CLK	5	Input	PWM module clock; internal pulldown current source
Serial peripheral interface			
SCLK	8	Input	SPI clock; internal pulldown current source
$\overline{SS}$	6	Input	SPI client select; pullup current source
MOSI	7	Input	SPI data input; pulldown current source
MISO	9	Output	SPI data output; high-Z when inactive

Table 3. Pin description...*continued*

Symbol	Pin	Type	Description
Direct input pins			
LHM	18	Input	Limp home mode; active direct input
IN1	25	Input	Direct input 1; pulldown resistor
IN2	24	Input	Direct input 2; pulldown resistor
IN3	23	Input	Direct input 3; pulldown resistor
IN4	22	Input	Direct input 4; pulldown resistor
Output switches			
OUT1	3	Power	Output 1, connected to load (NMOS source)
OUT2	26	Power	Output 2, connected to load (NMOS source)
OUT3	12	Power	Output 3, connected to load (NMOS source)
OUT4	17	Power	Output 4, connected to load (NMOS source)
Center pad			
—	GND	—	Center pad [1]

[1] For enhanced thermal and electrical performance, the exposed center pad of the HTSSOP28 package should be soldered to board ground (and not to any other voltage level).

8 Functional description

8.1 Power supplies

The device is supplied by three sources: VPWR, VDD and VSPI.

- VPWR pins are the power supply for high side switch (HSS) and carry high current. They are connected to each drain of power NMOS.
- VDD pin is the power terminal to supply the internal circuits. If VDD voltage is lower than V_{DD_UV} (3.95 V typ.), the device internal supply automatically switches to VPWR.
- VSPI supply line is used by the SPI port and has been designed for 3.3 V and 5.0 V logic level.

8.2 Operational mode

The MC33XS2410 has the following operation modes:

- Reset mode
- Disable mode
- Normal mode
- Safe mode

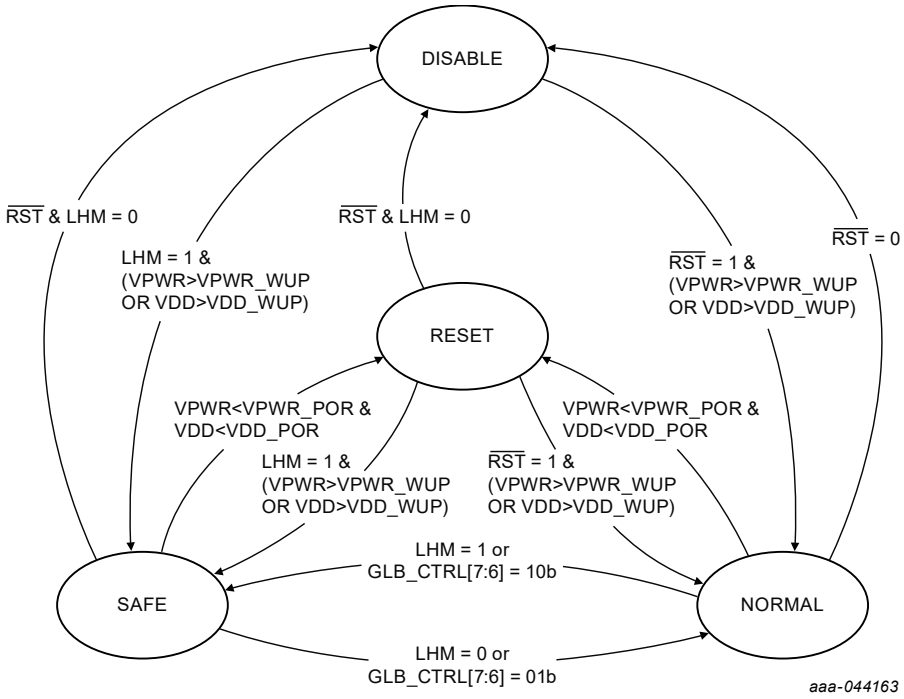


Figure 3. MC33XS2410 state machine

8.2.1 Reset mode

The reset mode is applied if VDD and VPWR are lower than their respective power-on reset values (VPWR_POR and VDD_POR). When the device is entering reset mode, all logic is reset, as well as SPI registers. Power NMOS is turned off and remains off state to protect the device. The device remains protected against overvoltage by active voltage clamp circuit (see Section 8.14.1 "Active voltage clamp").

8.2.2 Disable mode

When entering disable mode, all outputs are turned off after $T_{FAST\_TOFF\_D}$ (see Table 56) and the current consumption is reduced to the very minimum (see parameter in Table 45). The device remains protected against overvoltage by active voltage clamp circuit. The disable mode is applied if $\overline{RST}$ and LHM pins are pulled LOW, all registers configuration are reset to default values.

8.2.3 Normal mode

The device wakes up and transits to normal mode if $\overline{RST}$ pin goes from LOW to HIGH and VPWR > VPWR_WUP. After a T_{WAKE_UP} time, all functions are fully operational and the device is controlled by SPI port unless Safe mode is enabled. For details, see Figure 3.

8.2.4 Safe mode

The device provides a safe mode via limp home mode LHM pin and INx input pin. In this mode all outputs OUTx are directly controlled by INx input logic signal. The ON_OFFx bits in OUT1-4_CTRL register programmed by SPI are therefore bypassed. During

safe mode all control register configurations are not reset and kept in memory. SPI communication is available for read access (diagnostics and ADC register are available).

The device switches to safe mode in the following case:

- If LHM pin is pulled to HIGH logic level
- If GLB_CTRL[7:6] bits are set to b10 by SPI command
- If the watchdog timeout flag and transition in safe mode is enabled by bit WDT_REG[6]
- If an overload protection (OLP) is detected and transition in safe mode is enabled by bit OLP_CTRL[7]
- If a low-voltage condition (V_{SPI_LV}) is detected on VSPI supply pin

8.3 Power stages

Each HSS can be switched on via SPI or via direct input INx pin, when available. Output power stage is fully floating and can swing from Vpwr + 0.3 V to -35 V versus GND or Vpwr - 60 V (voltage is limited above that range). For details, see Section 8.14 "Protection".

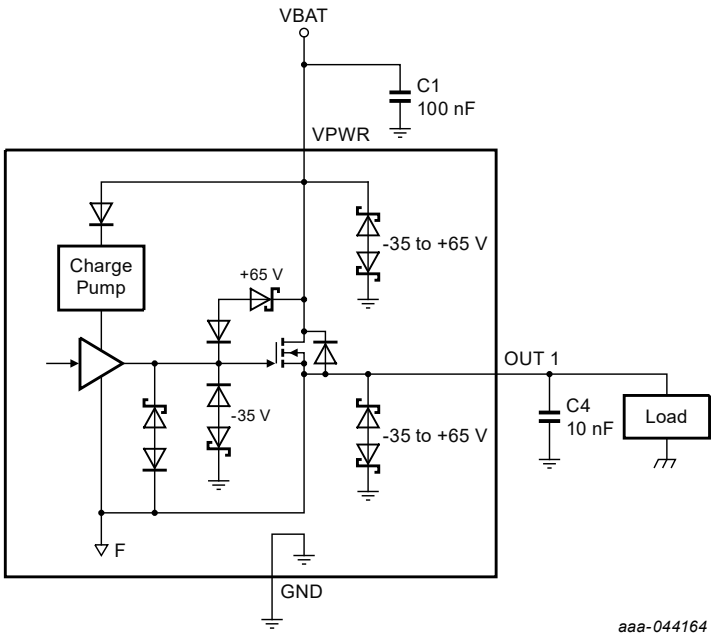


Figure 4. Simplified power stage

8.3.1 Resistive load switch

A typical switching characteristic on resistive load is depicted in Figure 5. The risetime (SR_R) and fall time (SR_F) are adjustable in OUT1-4_CTRL register in order to minimize EMI. Parameters are defined in Table 46.

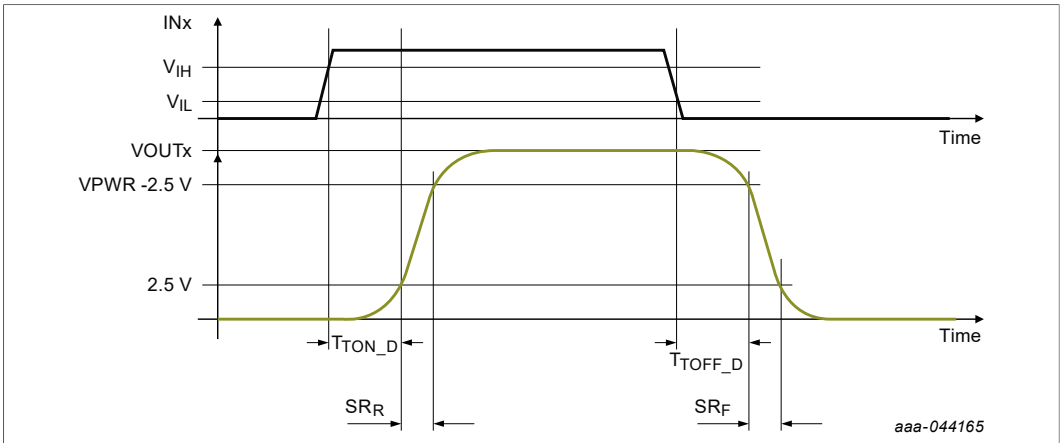


Figure 5. Resistive load switching timing

8.3.2 Minimum ON and OFF time

Open load in ON state and short to Vbat in OFF state features are respectively related to the ON and OFF state duration to provide their diagnostic.

Therefore, the minimum and maximum duty cycle can be limited depending on the PWM frequency used during operation.

To get these 2 diagnostics operational, the combination duty cycle (δ) / PWM frequency (F_{PWM}) should respect the following conditions:

- Minimum duty cycle to get Open load in ON state operational: $\delta_{MIN(\%)} = (T_{ON\_MIN} \times F_{PWM})$
- Maximum duty cycle to get short to Vbat in OFF state operational: $\delta_{MAX(\%)} = 1 - (T_{OFF\_MIN} \times F_{PWM})$

For more details about open load configuration in ON state, see Section 8.13.3 "Open load in ON state". For more details about short to Vbat in OFF state, see Section 8.13.1 "Short to VBAT in OFF state".

8.3.3 Parallel mode

The outputs can be parallelized two by two (OUT1/2 and OUT3/4) to divide the output Rdson by 2 and drive higher currents. When one pair is set up in parallel mode, outputs must be connected together with a short and low impedance track (see Section 9.1 "Circuit loops and tracks"). The current is split between the two power switches, the current limitation value is doubled and each current sense sees half of the total current.

If GLB_CTRL[4] bit is set to 1, OUT1 and OUT2 are in parallel. All control bits are managed by OUT1 control bits while OUT2 control bits have no use. The IN2 direct input is OR logic with IN1 and directed to OUT1 ON/OFF Logic Control.

If GLB_CTRL[3] bit is set to 1, OUT3 and OUT4 are in parallel. All control bits are managed by OUT3 control bits while OUT4 control bits have no use. The IN4 direct input is OR logic with IN3 and directed to OUT3 ON/OFF Logic Control.

8.4 16-bit SPI interface

The SPI is used for communication with a controller and provides control and diagnostic functions. The device is configured as an SPI client.

The serial peripheral interface (SPI) is a full duplex synchronous serial client interface, which uses four lines: MISO, MOSI, SCLK and $\overline{SS}$. Data is transferred by the lines MOSI and MISO at the rate given by SCLK. The falling edge of $\overline{SS}$ indicates the beginning of an access.

Data is sampled on the MOSI line at the falling edge of SCLK and shifted out on the MISO line at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{SS}$. In idle state, before and after the transfer, the base value of the clock SCLK is 0. A modulo 8 counter ensures that data is taken only when multiple of 8 bits have been transferred. The interface provides daisy chain capability.

8.4.1 SPI communication protocol

Due to the SPI full duplex feature when a “Frame” is received by the device on MOSI line, simultaneously a “Frame” is transmitted on MISO line by the device. The MOSI line represents the frame sent from the MCU and MISO line is the answer provided by the device. The relationship between MOSI and MISO content during SPI communication is shown in Figure 6. The “Previous Response” means that the “Frame” sent back depends on the command frame sent from the MCU before.

After a Write command the content of the next MISO frame reported by the device depends on the address selected by the READBACK register. After the reset by default, the register selected by READBACK is the global status register (GLB_STA). The last written register can also be selected to be reported on the N+1 frame with Bit 6 = 1 on the READBACK register.

After a Read command the content of the next MISO frame reported by the device depends on the address selected in the Read command.

The device reads MOSI data on clock SCLK falling edge and shift out MISO data on the clock SCLK rising edge. So data is valid for reading by MCU on SCLK falling edge. For full timing details, see Table 57 and Figure 26.

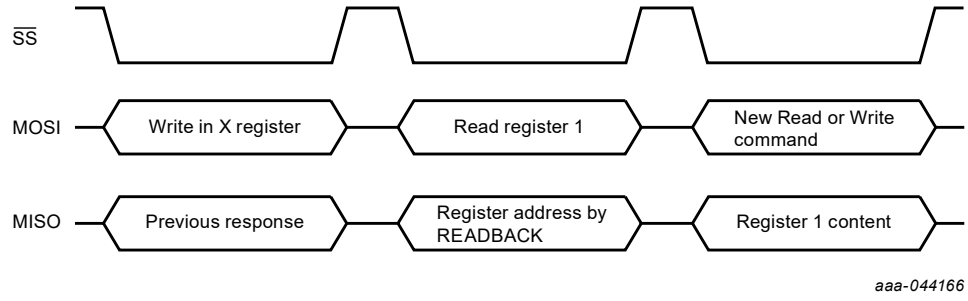


Figure 6. SPI communication protocol

8.4.2 SPI MOSI frame data IN

The SPI communication uses 2x8-bit words; see Figure 7 and Figure 8. In MISO frame, the most significant byte contents two control bits (Read/Write and Toggle) plus 6 bits of address. During a Write command (bit 15 = 1), the less significant byte contains 8 bits of data. During a Read command only bit 7 is used to select between Diagnostic or Control register.

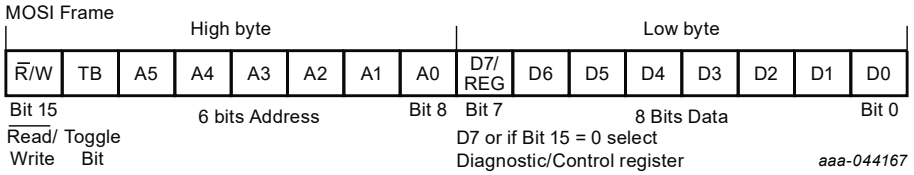


Figure 7. SPI MOSI 16-bit words

Bit 15: R/W: Read/Write bit

0 = Read Diagnostic register or Control register (see bit 7)
1 = Write Control register

Bit 14: TB: Toggle bit

0 = Toggle bit to 0: TB = 0
1 = Toggle bit to 1: TB = 1

The 6 least significant bits in the high byte contains the address.

Bit 13-8: A5 to A0: Address to Read or Write

During a Write command (bit 15 = 1) the 8 bits of the low byte content the data.

Bit 7-0: D7 to D0: Data to Write

During a Read command (bit 15 = 0) the bit 7 selects the Diagnostic or Control register and bits 6-0 are not used.

Bit 7: D7/REG: Select Diagnostic or Control registers in read operation (bit 15 = 0)

0 = Select Diagnostic register
1 = Select Control register

8.4.3 SPI MISO frame data OUT

The 2 most significant bits (15-14) of the high byte are used to provide device status.

Bit 15-14: ST1-ST0: Status bits
00 = Nothing to report
01 = Warning event: WARN (maskable interrupt)
10 = Interrupt Request: IRQ (priority over WARN, maskable interrupt)
11 = Invalid SPI Communication: ISPI (high priority non-maskable interrupt)

The 6 least significant bits of the high byte content the highest significant bits data.

Bit 13-8: D13 to D8: Data read

The 8 bits of the low byte content the least significant bits data.

Bit 7-0: D7 to D0: Data read

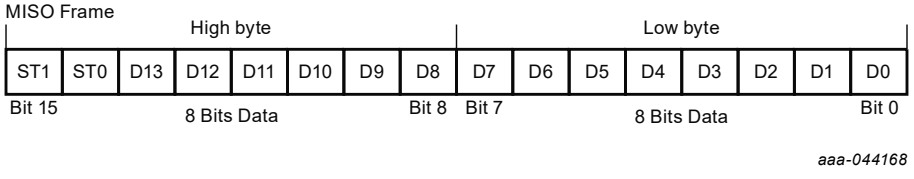


Figure 8. SPI MISO 16-bit words

8.4.4 SPI daisy chain configuration

Devices can be daisy chained by connecting the MISO of the first client to the MOSI of the next client and so on; see Figure 9.

All devices have their $\overline{SS}$ inputs connected to the same controller chip select so that they can be selected together. When n devices are daisy chained, then n SPI 16-bit word cycles must be executed to program all devices. This 16-bit shift register is a 2 byte shift register, therefore devices with modulo 8-bit can share the same daisy chain.

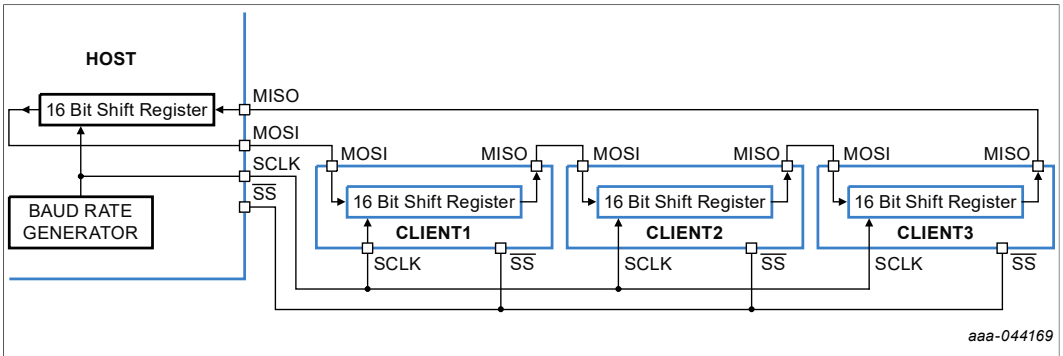


Figure 9. Daisy chain connection example of three clients

8.4.5 SPI communication error

In order to detect some SPI communication error the following functions are available:

- SPI watchdog timer to detect a breakdown
- Check a modulo 8-bit error in frame
- Invalid address in MOSI frame
- Toggle bit error to improve the safety frame protocol

8.4.5.1 SPI watchdog timer

Watchdog purpose is to ensure that both device and MCU are active to continue operation. The SPI watchdog detects if there is a breakdown in the SPI communication with the controller. A timer is activated and is reset when a valid SPI communication is received. If no valid SPI communications are received within the specified period, the watchdog raises a flag to the logic. Two different timeout periods are available: the watchdog warning period and watchdog timeout period as depicted in Figure 10. Both watchdog periods are configurable from 2.0 ms to 256 ms (see Table 5).

When no valid SPI communication is received within the watchdog warning period, the bit ISR_WARN[7] in interrupt service routine is set to 1 by WD_WF flag.

When no valid SPI communication is received within the watchdog timeout period, the bit ISR_IRQ[7] in interrupt service routine is set to 1 by WD_TOF flag and if the bit WDT_REG[6] = 1, the device transits in safe mode.

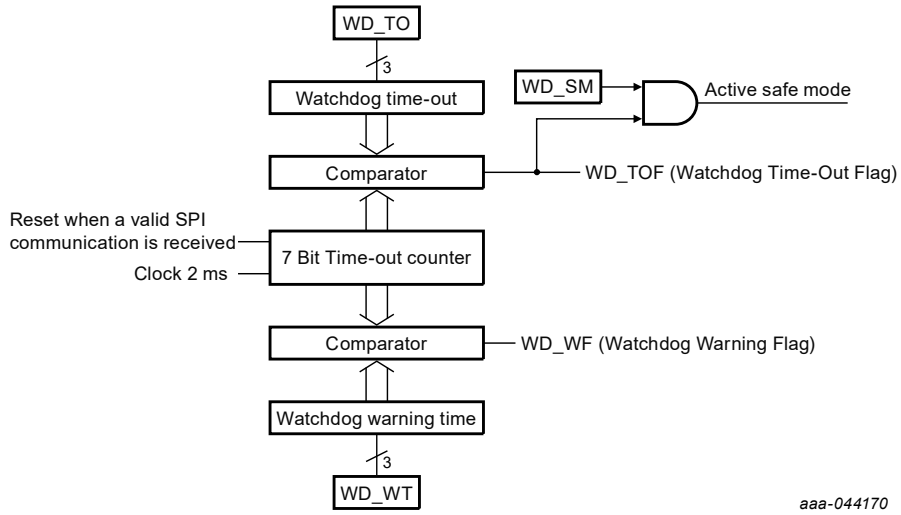


Figure 10. Watchdog logic circuit

Table 4. Watchdog timer - control register (address 14h) bit description

Address	Register	Bit	Description
14h	WDT_REG	7	Unused
		6	Transit in safe mode when watchdog timeout flag 0 = transit in safe mode is disabled 1 = transit in safe mode is enabled (reset value)
		5 to 3	Watchdog timeout period (see Table 5)
		2 to 0	Watchdog warning period (see Table 5)

Table 5. Watchdog period

Period			
Value	**Time**	**Value**	**Time**
000b	2 ms	100b	32 ms
001b	4 ms	101b	64 ms
010b	8 ms	110b	128 ms [1]
011b	16 ms	111b	256 ms [2]

[1] Reset value of watchdog warning period
[2] Reset value of watchdog timeout period

8.4.5.2 Wrong number of bits

This function monitors the number of bit that must be transmitted in a communication frame. If the number of clock pulses within $\overline{SS}$ signal low state, not 0 or a multiple of 8, then the SPI frame is ignored and an invalid SPI communication ISPI code is generated. With this non-maskable ISPI code interrupt on the next SPI frame, MISO data reports an invalid SPI communication code.

8.4.5.3 Invalid address

This function checks if each MOSI frame has a valid address. If the read or write address A0 to A5 in MOSI frame points to an unmapped address this wrong address is considered invalid and the SPI command is ignored. An invalid SPI communication ISPI code is generated. With this non-maskable ISPI code interrupt, MISO data reports an invalid SPI communication code in the next SPI frame.

8.4.5.4 Toggle bit error

This feature improves safety of the system using SPI communication. When enabled, the TB bit (bit 14 in MOSI frame) must be toggled in each MOSI frame otherwise a SPI toggle bit error is detected and the SPI frame is ignored. So the SPI Toggle Bit Error (ISR_IRQ[4]) is set to 1 in interrupt service routine. Depending on EN_IRQ_SPI[4] and EN_IRQ_PIN[4] bits an interrupt could be generated.

After the reset, by default the TB bit is 0. To avoid toggle bit error, once the feature is enabled, the first SPI command must be toggled with TB bit to 1.

8.5 Interrupt control logic

An interrupt can be generated to notify the controller that an event has occurred. This notification can be reported by the $\overline{\text{FAULT}}$ pin and or by SPI using ST1-ST0 bits status in each MISO frame. The $\overline{\text{FAULT}}$ open-drain output enables an immediate reporting and an interrupt sets pin $\overline{\text{FAULT}}$ = LOW. The SPI enables distinction between a warning event, an interrupt request or an invalid SPI communication error depending on ST1-ST0 bits status.

8.5.1 Mask of interrupt register

Four registers configure which faults generate an interrupt as depicted in Table 6.

There are two sets of maskable interrupts: Warning even (WARN) and Interrupt Request (IRQ). Both the WARN and IRQ flags can be reported to SPI MISO bits status (see Section 8.4.3 "SPI MISO frame data OUT") and/or external /$\overline{\text{FAULT}}$ pin. In case both information are raised together, IRQ has priority over WARN.

Table 6. Mask of interrupt - control register (addresses 10h to 13h) bit description

Address	Register	Bit	Description
10h	EN_IRQ_SPI		SPI IRQ interrupt request; for each bit: 0 = IRQ not active (reset value) 1 = IRQ active
		7	Charge pump fault
		6	Unused
		5	Watchdog timeout
		4	SPI toggle bit error
		3	The device transits to safe mode [1]
		2	overtemperature [2]
		1	Current limit N retry reached or severe short-circuit [2]
		0	Overload condition [2]

Table 6. Mask of interrupt - control register (addresses 10h to 13h) bit description*...continued*

Address	Register	Bit	Description
11h	EN_IRQ_PIN		$\overline{\text{FAULT}}$ pin IRQ interrupt request; for each bit: 0 = IRQ not active (reset value) 1 = IRQ active
		7	Charge pump fault
		6	Unused
		5	Watchdog timeout
		4	SPI toggle bit error
		3	The device transits to safe mode [1]
		2	Overtemperature [2]
		1	Current limit N retry reached or severe short-circuit [2]
		0	Overload condition [2]
12h	EN_WARN_SPI		SPI WARN interrupt request; for each bit: 0 = WARN not active (reset value) 1 = WARN active
		7	Watchdog warning
		6	Overtemperature warning[2]
		5	Overcurrent warning [2]
		4	undercurrent warning [2]
		3	Overvoltage warning [2]
		2	Undervoltage warning [2]
		1	VDD undervoltage [2]
		0	VPWR undervoltage [2]
13h	EN_WARN_PIN		$\overline{\text{FAULT}}$ pin WARN interrupt request; for each bit: 0 = WARN not active (reset value) 1 = WARN active
		7	Watchdog warning
		6	Overtemperature warning [2]
		5	Overcurrent warning [2]
		4	Undercurrent warning [2]
		3	Overvoltage warning [2]
		2	Undervoltage warning [2]
		1	VDD undervoltage warning [2]
		0	VPWR undervoltage warning [2]

[1] Except when set by SPI command
[2] At least one output reaches or exceeds the threshold

8.5.2 Interrupt service routines ISR

Two registers indicate when an interrupt occurs. The ISR_IRQ register is dedicated for IRQ type interrupt event and ISR_WARN register is dedicated for WARN type warning event; see Table 7.

Each bit in the ISR_IRQ and ISR_WARN registers is latched when a fault is generated. Each register ISR_IRQ and ISR_WARN is cleared by reading it.

Table 7. Interrupt service routine - diagnostics register (addresses 06h 07h) bit description

Address	Register	Bit	Description
06h	ISR_IRQ		ISR_IRQ interrupt status; for each bit: 0 = no interruption request (reset value) 1 = interruption is requested
		13 to 8	Unused
		7	Charge pump fault
		6	Unused
		5	Watchdog timeout
		4	SPI toggle bit error
		3	The device transits to safe mode
		2	Overtemperature
		1	Current limit N retry reached or severe short-circuit
		0	Overload condition
07h	ISR_WARN		ISR_WARN interrupt status; for each bit: 0 = no interruption request (reset value) 1 = interruption is requested
		13 to 8	Unused
		7	Watchdog warning
		6	Overtemperature warning
		5	Overcurrent warning
		4	Undercurrent warning
		3	Overvoltage warning
		2	Undervoltage warning
		1	VDD undervoltage
		0	VPWR undervoltage

8.6 Control register

The following table provides an overview of all user accessible control registers and available addressing space. All registers enable digital control of the device by SPI command. Control registers are 8-bits write and also read in order to check the content, if necessary. The default value is loaded during power-on reset.

Table 8. Control: 8-bits Read/Write registers

Register [1]	Symbol	Description	Reset value	Reference
00h	GLB_CTRL	Global controls register	20h	Section 8.6.1
01h	READBACK	Select which register is read back	00h	Section 8.6.2
02h	OUT1-4_CTRL	Output control register, slew rate and turn ON/OFF control	00h	Section 8.6.3
03h	IN_CTRL1	Direct input control logic setup 1	00h	Section 8.6.4
04h	IN_CTRL2	Direct input control logic setup 2	00h	Section 8.6.4
05h	PWM_CTRL1	PWM module control register	00h	Section 8.7
06h	PWM_CTRL2	PWM module phase shift control	00h	Section 8.7
07h	PWM_CTRL3	PWM module control register	00h	Section 8.7
08h	PWM_FREQ1	PWM frequency setting output 1	00h	Section 8.7
09h	PWM_FREQ2	PWM frequency setting output 2	00h	Section 8.7
0Ah	PWM_FREQ3	PWM frequency setting output 3	00h	Section 8.7
0Bh	PWM_FREQ4	PWM frequency setting output 4	00h	Section 8.7
0Ch	PWM_DC1	PWM duty cycle control output 1	00h	Section 8.7
0Dh	PWM_DC2	PWM duty cycle control output 2	00h	Section 8.7
0Eh	PWM_DC3	PWM duty cycle control output 3	00h	Section 8.7
0Fh	PWM_DC4	PWM duty cycle control output 4	00h	Section 8.7
10h	EN_IRQ_SPI	IRQ type interrupt request by SPI	00h	Section 8.5.1
11h	EN_IRQ_PIN	IRQ type interrupt request by pin	00h	Section 8.5.1
12h	EN_WARN_SPI	Warning type interrupt request by SPI	00h	Section 8.5.1
13h	EN_WARN_PIN	Warning type interrupt request by FAULT pin	00h	Section 8.5.1
14h	WDT_REG	Watchdog timer	7Eh	Section 8.4.5.1
15h	M_SETUP	Measurement setup: current range and timing	00h	Section 8.12.1
16h	C_CTRL	Synchronous current mode and on-demand C and V	00h	Section 8.12.1
17h	WC_CTRL	Warning current control	00h	Section 8.12.2
18h	OCW_OUT1	Overcurrent warning threshold output 1	FFh	Section 8.12.2
19h	UCW_OUT1	Undercurrent warning threshold output 1	00h	Section 8.12.2
1Ah	OCW_OUT2	Overcurrent warning threshold output 2	FFh	Section 8.12.2
1Bh	UCW_OUT2	Undercurrent warning threshold output 2	00h	Section 8.12.2
1Ch	OCW_OUT3	Overcurrent warning threshold output 3	FFh	Section 8.12.2
1Dh	UCW_OUT3	Undercurrent warning threshold output 3	00h	Section 8.12.2
1Eh	OCW_OUT4	Overcurrent warning threshold output 4	FFh	Section 8.12.2
1Fh	UCW_OUT4	Undercurrent warning threshold output 4	00h	Section 8.12.2
20h	WV_CTRL	Warning voltage control	00h	Section 8.12.4
21h	OVW_OUT1	Overvoltage warning threshold output 1	00h	Section 8.12.4
22h	UVW_OUT1	Undervoltage warning threshold output 1	00h	Section 8.12.4
23h	OVW_OUT2	Overvoltage warning threshold output 2	00h	Section 8.12.4

Table 8. Control: 8-bits Read/Write registers...*continued*

Register [1]	Symbol	Description	Reset value	Reference
24h	UVW_OUT2	Undervoltage Warning threshold output 2	00h	Section 8.12.4
25h	OVW_OUT3	Overvoltage warning threshold output 3	00h	Section 8.12.4
26h	UVW_OUT3	Undervoltage warning threshold output 3	00h	Section 8.12.4
27h	OVW_OUT4	Overvoltage warning threshold output 4	00h	Section 8.12.4
28h	UVW_OUT4	Undervoltage warning threshold output 4	00h	Section 8.12.4
29h	TEMP_WT	Common temperature warning threshold	A5h	Section 8.12.6
2Ah	ΔV_STVB	Voltage offset short to VBAT in OFF state	04h	Section 8.13.1
2Bh	BT_STVB	Blanking delay short to VBAT in OFF state	70h	Section 8.13.1
2Ch	OPD_CTRL1	Open load detection control in ON state output 1 and 2 and clear OUT1_LF and OUT2_LF bits	24h	Section 8.13.3
2Dh	OPD_CTRL2	Open load detection control in ON state output 3 and 4 and clear OUT3_LF and OUT4_LF bits	24h	Section 8.13.3
2Eh	I_OLD1	Open load threshold in ON state output 1	03h	Section 8.13.3
2Fh	I_OLD2	Open load threshold in ON state output 2	03h	Section 8.13.3
30h	I_OLD3	Open load threshold in ON state output 3	03h	Section 8.13.3
31h	I_OLD4	Open load threshold in ON state output 4	03h	Section 8.13.3
32h	ACL_CTRL1	Active current limit control 1	6Dh	Section 8.14.5
33h	ACL_CTRL2	Active current limit control 2	2Dh	Section 8.14.5
34h	SSC_CTRL	Severe short-circuit control	00h	Section 8.14.6
35h	OLP_CTRL	Overload protection control	18h	Section 8.14.7
36h	OCL_OUT1	Overload current level threshold output 1	CCh	Section 8.14.7
37h	OCL_OUT2	Overload current level threshold output 2	CCh	Section 8.14.7
38h	OCL_OUT3	Overload current level threshold output 3	CCh	Section 8.14.7
39h	OCL_OUT4	Overload current level threshold output 4	CCh	Section 8.14.7
3Ah	PI_CTRL1	Proportional-integral regulation compensation setup	00h	Section 8.8
3Bh	PI_CTRL2	Dither PI setup	00h	Section 8.8
3Ch	I_SET1	Current set-point output 1	00h	Section 8.8
3Dh	I_SET2	Current set-point output 2	00h	Section 8.8
3Eh	I_SET3	Current set-point output 3	00h	Section 8.8
3Fh	I_SET4	Current set-point output 4	00h	Section 8.8

[1] To address control register bit 7 (D7/REG) = 1 in 16-bits MOSI frame.

8.6.1 Global control

The global control register GLB_CTRL is used to:

- Transit in normal or safe mode
- Configure output in parallel
- Optimize EMI by selecting the MISO output buffer impedance
- Change the oscillator spread spectrum
- Configure the direct inputs logic level.

Transit mode: Writing in bits GLB_CTRL[7:6] enables transition from normal to safe mode or vice versa. The bit values are not retained and are cleared once transition is done.

Reset: Writing 11b in bits GLB_CTRL[7:6] executes a complete reset of the device.

Drive strength: The bit GLB_CTRL[5] configures the MISO output buffer impedance between MEDIUM and STRONG strength in order to optimize EMI.

Parallel mode: The bits GLB_CTRL[4:3] configure independently the OUT1 + OUT2 and OUT3 + OUT4 in parallel; for details see Section 8.3.3 "Parallel mode".

Oscillator modulation frequency: The bits GLB_CTRL[2:1] help improve EMI by spreading the 42 MHz oscillator's frequency.

Direct input logic level: The bit GLB_CTRL[0] help change the input logic level for LHM, IN1, IN2, IN3 and IN4 pins.

Table 9. Global control - control register (address 00h) bit description

Address	Register	Bit	Description
00h	GLB_CTRL	7 to 6	transit mode and reset 00 = no transition asked (reset value) 01 = transit to normal mode 10 = transit to safe mode 11 = reset
		5	drive strength (MISO) 0 = STRONG configuration (50 Ω) 1 = MEDIUM configuration (200 Ω) (reset value)
		4	parallel mode for OUT1 and OUT2 0 = OUT1-2 are independent (reset value) 1 = OUT1-2 are in parallel
		3	parallel mode for OUT3 and OUT4 0 = OUT3-4 are independent (reset value) 1 = OUT3-4 are in parallel
		2	oscillator modulation frequency; F_MOD 0 = disable (reset value) 1 = enable
		1	frequency modulation band; F_DEV 0 = F1_DEV selected (reset value) 1 = F2_DEV selected
		0	direct input logic level 0 = AUTOMOTIVE input level (reset value) 1 = CMOS input logic level

8.6.2 Readback

After a Write command, the content of the next MISO frame reported by the device depends on the address selected by the READBACK register. On first SPI communication after reset, the first register selected by READBACK and sent on the MISO line is the Global Status GLB_STA (00h); for details see Section 8.4.1 "SPI communication protocol". This is also possible to read the last written register by enabling the automatic mode with bit READBACK[6] = 1. In that case, each MISO frame will report the content of the register configured in the previous SPI access.

Table 10. Readback - control register (address 01h) bit description

Address	Register	Bit	Description
01h	READBACK	7	Select Diagnostic or Control register 0 = Diagnostics bank register [1] 1 = Control bank register
		6	Automatic 0 = No action (Default) 1 = Select automatically last written register (Control)
		5 to 0	Select register address [2]

[1] By default, select diagnostics bank register
[2] By default, the 5 bits = 0000b and select GLB_STA register

8.6.3 Output control

Outputs are controlled by OUT1-4_CTRL (02h) register that enables turn-on, turn-off and selects the switching slew rate for each output.

Slew rate: The bits OUT1-4_CTRL[7:4] configure the power NMOS switching slew rate. Defined slew rates minimize EMI during PWM operation but increase the switching losses and limit the frequency operation.

Table 11. Output control - control register (address 02h) bit description

Address	Register	Bit	Description
02h	OUT1-4_CTRL		Output slew rate control for T_SRx bit 0 = slow slew rate (reset value) 1 = fast slew rate
		7	T_SR4 output 4
		6	T_SR3 output 3
		5	T_SR2 output 2 [1]
		4	T_SR1 output 1
			Output ON / OFF control for ON_OFFx bit 0 = OUTx is OFF (reset value) 1 = OUTx is ON [2]
		3	ON_OFF4 output 4 [1]
		2	ON_OFF3 output 3
		1	ON_OFF2 output 2 [1]
		0	ON_OFF1 output 1

[1] This bit is non-active when this output is configured in parallel mode.
[2] Unless latch-off by OUTx_LF logic signal

8.6.4 Direct input control

The device can be controlled by direct input in the following case:

- In safe mode
- In normal mode if enabled by bits IN_CTRL1[3:0]

Direct inputs are used to directly turn-on or turn-off the outputs. PWM signal can be applied within the limits of minimum on-time and off-time to guarantee diagnostic feature; for details see Section 8.3.2 "Minimum ON and OFF time".

Two registers IN_CTRL1 and IN_CTRL2 configure the direct input:

Deglitch time: By default INx input is provided with a deglitch time of 200 µs typ. ($T_{IN\_DGL\_DI}$). This deglitch time can be disabled with IN_CTRL[7:4] bits

Input control: Bits IN_CTRL1[3:0] control the output by applying direct input logic signal to INx pins.

OR logic with SPI control: Bits IN_CTRL2[7:4] enable an OR logic with internal INTx logic signal from ON / OFF SPI control or PWM module; see Figure 11.

Active logic level: Bits IN_CTRL2[3:0] configure the input logic as active high or low.

Note that GLB_CTRL[0] enables to change the input logic level: see Section 8.6.1 "Global control".

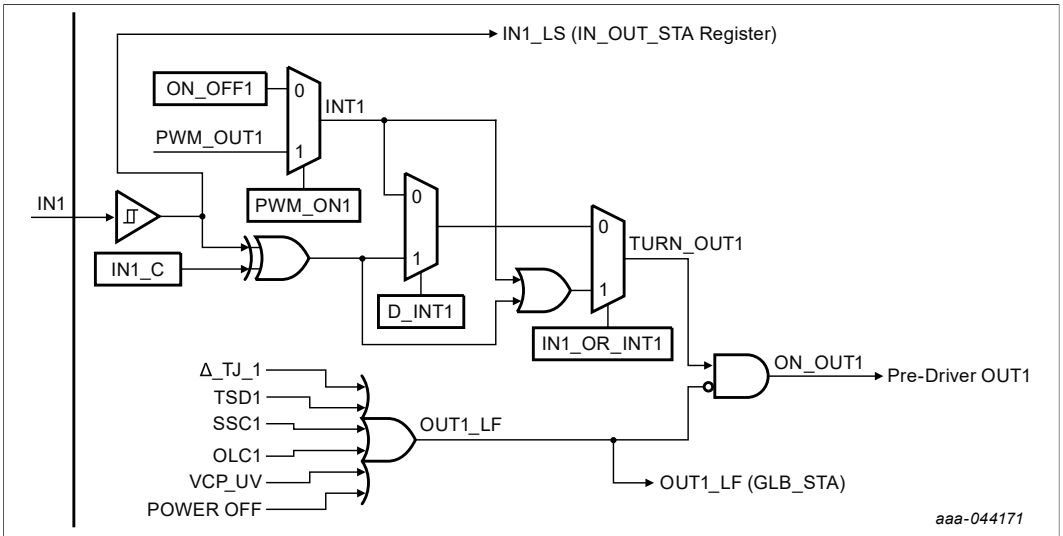


Figure 11. Simplified ON/OFF logic control (output 1)

Table 12. Direct input control - control register (address 03h, 04h) bit description

Address	Register	Bit	Description
03h	IN_CTRL1		Disable deglitch time 0 = enable (reset value) 1 = disable
		7	DDT_IN4 output 4 [1]
		6	DDT_IN3 output 3
		5	DDT_IN2 output 2 [1]
		4	DDT_IN1 output 1
			Output is controlled by 0 = OUTx is controlled by SPI (reset value) 1 = OUTx is controlled by INx input
		3	D_IN4 output 4 [1]
		2	D_IN3 output 3
		1	D_IN2 output 2 [1]
		0	D_IN1 output 1
04h	IN_CTRL2		OR Logic with internal INTx logic signal 0 = OR logic is disabled (reset value) 1 = INx input logic is OR logic with INTx
		7	IN4_OR_INT4 output 4 [1]
		6	IN3_OR_INT3 output 3
		5	IN2_OR_INT2 output 2 [1]
		4	IN1_OR_INT1 output 1
			Active logic level: INx_C bit 0 = INx input logic is not invert (reset value) 1 = INx input logic is complemented
		3	IN4_C output 4 [1]
		2	IN3_C output 3
		1	IN2_C output 2 [1]
		0	IN1_C output 1

[1] This bit is non-active when the output is configured in parallel mode.

8.7 Pulse-width Modulation module (PWM)

The device integrates a PWM module with an 8-bit duty cycle capability per output. Reference frequency signal for PWM module can be either internal or external. When all outputs have same frequency they can be phase shifted by 0°, 90°, 180° or 270°. The internal clock drive loads at different frequencies typically from 0.5 Hz up to 2.048 kHz.

PWM clock reference: The internal reference clock has an accuracy of ± 5 % over temperature and voltage operating range. When the bit PWM_CTRL1[7] is set high, the external clock source is selected and a clock signal (512 kHz typ.) should be applied to the PWM_CLK input. A clock fail circuit is monitoring the PWM_CLK clock and detects if the signal is toggled within T_{OUT} timeout (100 µs typ.). If a clock fail is detected the

device clears the PWM_CTRL1[7] bit and transits to internal PWM_CLK clock signal. By reading the PWM_CTRL1[7] bit the MCU can check if the external clock failed.

PWM synchronization: To start the PWM operation at a known point in time the bit PWM_CTRL1[6] shall be set high. Once PWM_CTRL1[6] is set high all PWM 8 bits counter reset when $\overline{SS}$ transits from 0 to 1 at the end of the 16-bit SPI frame. The PWM_CTRL1[6] bit value is not retained and always reads 0.

PWM output polarity: For each PWM output the polarity can be selected by PWM_POL_x bits in PWM_CTRL1 register.

PWM frequency: For the four outputs the PWM_FREQx registers enable to configure the frequency typically from 0.5 Hz to 2.048 kHz. The 2 most significant bits (7-6) select the factor for division by 1, 4, 16, or 64. The 6 least significant bits (5-0) select the frequency step by step; see Table 13.

When one of the I_SETx registers is enabled (≠ 00h) the PWMx module is rerouting to clock the PI loop module.

PWM phase shift: PWM_CTRL2 register configures the phase shift by adding a delay of 0, 1/4, 1/2 or 3/4 of PWM period before turning ON PWM output signal. This contributes to improve EMI by shifting the output turn ON and spreading the inrush current.

PWM duty cycle: Duty cycle is defined by δ = (n+1) / 256 where n is a decimal number from 0 to 255 configured by PWM_DCx registers. Thus the duty cycle is adjustable from 0.39 % to 100 %. It is important to note that the on-time (T_{ON}) is defined by: T_{ON} = (δ / F_{PWM}) where δ is the duty cycle and F_{PWM} the PWM frequency. To guarantee diagnostic feature, T_{ON} and also T_{OFF} which is the off-time must be within the limits; for details see Section 8.3.2 "Minimum ON and OFF time".

PWM control: PWM_CTRL3 register allows each PWM channel to be turned ON or OFF. Note that PWM operation gets the priority against ON_OFFx bits from OUT1-4_CTRL.

Table 13. PWM module control - control register (address 05h to 07h) bit description

Address	Register	Bit	Description
05h	PWM_CTRL1	7	Select PWM clock signal source 0 = internal clock signal (reset value) 1 = external clock input PWM_CLK pin
		6	PWM synchronization 0 = no action (reset value) 1 = reset PWM 8 bits counter
			PWM output polarity 0 = Signal is non-inverted (reset value) 1 = Signal is inverted
		5	PWM_POL_4 output 4 [1]
		4	PWM_POL_3 output 3
		3	PWM_POL_2 output 2 [1]
		2	PWM_POL_1 output 1
		1	unused
		0	unused

Table 13. PWM module control - control register (address 05h to 07h) bit description*...continued*

Address	Register	Bit	Description
06h	PWM_CTRL2		PWM Phase shift control 00 = 0° (reset value) 01 = 90° 10 = 180° 11 = 270°
		7 to 6	PHA_4 output 4 [1]
		5 to 4	PHA_3 output 3
		3 to 2	PHA_2 output 2 [1]
		1 to 0	PHA_1 output 1
07h	PWM_CTRL3		enable PWM output 0 = disable (reset value) 1 = enable
		7	PWM_ON4 output 4 [1]
		6	PWM_ON3 output 3
		5	PWM_ON2 output 2 [1]
		4	PWM_ON1 output 1
		3 to 0	unused
08h to 0Bh	PWM_FREQx	7 to 6	PWM Frequency range and step 00 = 0.5 Hz steps from 0.5 Hz to 32 Hz 01 = 2 Hz steps from 2 Hz to 128 Hz 10 = 8 Hz steps from 8 Hz to 512 Hz 11 = 32 Hz steps from 32 Hz to 2048 Hz
		5 to 0	Frequency = (code + 1) x steps Example to get 100 Hz in range 2 Hz to 128 Hz: code = ((100/2) - 1) = 49
0Ch to 0Fh	PWM_DCx	7 to 0	Internal PWM duty cycle for specified x output: 00h (reset value) = 0.39 % to FFh = 100 % Example to get δ = 25 % code = (0.25 x 256) - 1 = 63

[1] This bit is non-active when the output is configured in parallel mode.

8.8 PI PWM closed loop current regulation

The device integrates a digital proportional-integral controller (PI controller) to regulate a constant current for Proportional Solenoid Valve (PSV) with 12-bits PWM resolution per output. For each output the desired set-point is programmable by 8-bits register up to 3.2 A. In parallel mode, the regulated current is multiplied by 2 compared to the current set point. Reference frequency signal for PWM module can be either internal or external signal. Each output can be phase shifted 0, 90, 180 or 270 ° from the internal PWM signal. To control the closed loop regulation the duty cycle and feedback current can be monitored; see Table 17.

Regulated current: For each output the current set point is programmable by I_SETx register by step of 12.5 mA. The feedback current is sampling a Ton/2. When the I_SETx is cleared the closed loop regulation is disabled.

Loop stability: PI_CTRL1 register configures the loop regulation criteria and select the appropriate proportional gain KP factor and integral gain KI factor.

Dither signal: PI_CTRL2 register allows the user to program a dither signal. The Amplitude D_AMP of each step is 4 bits programmable where LSB ≈ 4.88 mA (= 5.0 A / 1023). The time N_PI_PWM of each step is 4 bits programmable PI_PWM_F clock count. So the dither period = (8 * N_PI_PWM) / PI output frequency.

Table 14. PI module setting - control register (address 3Ah to 3Fh) bit description

Address	Register	Bit	Description
3Ah	PI_CTRL1	7 to 4	proportional gain KP factor; see Table 15
		3 to 0	integral gain KI factor, see Table 16
3Bh	PI_CTRL2	7 to 4	setup the dither amplitude: D_AMP 0000b = disable (reset value) 0001b = 1 x 4.88 mA D_AMP = code x 4.88 mA
		3 to 0	setup the dither N_PI_PWM time 0000b = disable (reset value) 0001b = 1x PWM Div by 2^{10} N_PI_PWM = code x PWM Div by 2^{10}
3Ch to 3Fh	I_SETx	7 to 0	current set-point for output x (OUT1 to OUT4) 00h = disable 08h = 100 mA (reset value) I_SET1 = code x 12.5 mA (LSB)

Table 15. Proportional gain KP factor

KP factor							
Value	Gain	Value	Gain	Value	Gain	Value	Gain
0000b [1]	0.13 A^{-1}	0100b	1.07 A^{-1}	1000b	2.27 A^{-1}	1100b	4.28 A^{-1}
0001b	0.27 A^{-1}	0101b	1.34 A^{-1}	1001b	2.67 A^{-1}	1101b	4.87 A^{-1}
0010b	0.53 A^{-1}	0110b	1.51 A^{-1}	1010b	3.21 A^{-1}	1110b	5.34 A^{-1}
0011b	0.80 A^{-1}	0111b	1.87 A^{-1}	1011b	3.74 A^{-1}	1111b	5.90 A^{-1}

[1] Reset value

Table 16. Integral gain KP factor

KI factor							
Value	Gain	Value	Gain	Value	Gain	Value	Gain
0000b [1]	0.03 $A^{-1}s^{-1}$	0100b	0.15 $A^{-1}s^{-1}$	1000b	0.33 $A^{-1}s^{-1}$	1100b	0.77 $A^{-1}s^{-1}$
0001b	0.08 $A^{-1}s^{-1}$	0101b	0.17 $A^{-1}s^{-1}$	1001b	0.45 $A^{-1}s^{-1}$	1101b	0.88 $A^{-1}s^{-1}$
0010b	0.11 $A^{-1}s^{-1}$	0110b	0.22 $A^{-1}s^{-1}$	1010b	0.56 $A^{-1}s^{-1}$	1110b	0.98 $A^{-1}s^{-1}$
0011b	0.13 $A^{-1}s^{-1}$	0111b	0.27 $A^{-1}s^{-1}$	1011b	0.67 $A^{-1}s^{-1}$	1111b	1.09 $A^{-1}s^{-1}$

[1] Reset value

Table 17. PI module measurement – diagnostic register (address 18h to 23h) bit description

Address	Register	Bit	Description
27h to 2Ah	PI_DCx		PI PWM duty cycle value OUT1 to OUT4
		9 to 0	000h = 0 % 3FFh = 100 %
2Bh to 2Eh	FB_IOUTx		Feedback current measure at Ton/2 OUT1 to OUT4
		9 to 0	000h = 0 A 3FFh = 5.0 A

8.9 Diagnostic register

The diagnostic registers enable to readout the device state and to provide detailed information on each output, supply and direct input. Diagnostic registers can be obtained by reading data from the relevant 14-bit read-only registers; see Table 18. Whatever the register read the 2 most significant bits (15-14) of the high byte are used to provide device status; see Section 8.4.3 "SPI MISO frame data OUT".

Table 18. Diagnostic: 14-bits Read only register

Register [1]	Symbol	Description	Reference
00h	GLB_STA	Global status	Section 8.10.1
01h	IN_OUT_STA	Direct input and output logic state reporting	Section 8.10.2
02h	OUT1_STA	Bits status of OUT1	Section 8.10.3
03h	OUT2_STA	Bits status of OUT2	Section 8.10.3
04h	OUT3_STA	Bits status of OUT3	Section 8.10.3
05h	OUT4_STA	Bits status of OUT4	Section 8.10.3
06h	ISR_IRQ	ISR_IRQ interrupt status	Section 8.5.2
07h	ISR_WARN	ISR_WARN interrupt status	Section 8.5.2
08h	OD_IOUT1	On-demand output 1 current (ODCM)	Section 8.12.1
09h	OD_IOUT2	On-demand output 2 current (ODCM)	Section 8.12.1
0Ah	OD_IOUT3	On-demand output 3 current (ODCM)	Section 8.12.1
0Bh	OD_IOUT4	On-demand output 4 current (ODCM)	Section 8.12.1
0Ch	IOUT1	Current monitoring output 1 (CMM)	Section 8.12.1
0Dh	IOUT2	Current monitoring output 2 (CMM)	Section 8.12.1
0Eh	IOUT3	Current monitoring output 3 (CMM)	Section 8.12.1
0Fh	IOUT4	Current monitoring output 4 (CMM)	Section 8.12.1
10h	INI_IOUT1	Initial output 1 current (SCM)	Section 8.12.1
11h	INI_IOUT2	Initial output 2 current (SCM)	Section 8.12.1
12h	INI_IOUT3	Initial output 3 current (SCM)	Section 8.12.1
13h	INI_IOUT4	Initial output 4 current (SCM)	Section 8.12.1
14h	FIN_IOUT1	Final output 1 current (SCM)	Section 8.12.1
15h	FIN_IOUT2	Final output 2 current (SCM)	Section 8.12.1

Table 18. Diagnostic: 14-bits Read only register*...continued*

Register [1]	Symbol	Description	Reference
16h	FIN_IOUT3	Final output 3 current (SCM)	Section 8.12.1
17h	FIN_IOUT4	Final output 4 current (SCM)	Section 8.12.1
18h	VOUT1_ON	Continuous conversion mode voltage output 1 (CMM)	Section 8.12.3
19h	VOUT2_ON	Continuous conversion mode voltage output 2 (CMM)	Section 8.12.3
1Ah	VOUT3_ON	Continuous conversion mode voltage output 3 (CMM)	Section 8.12.3
1Bh	VOUT4_ON	Continuous conversion mode voltage output 4 (CMM)	Section 8.12.3
1Ch	OD_VOUT1	On-demand voltage output 1	Section 8.12.3
1Dh	OD_VOUT2	On-demand voltage output 2	Section 8.12.3
1Eh	OD_VOUT3	On-demand voltage output 3	Section 8.12.3
1Fh	OD_VOUT4	On-demand voltage output 4	Section 8.12.3
20h	VOUT1	Voltage monitoring output 1	Section 8.12.3
21h	VOUT2	Voltage monitoring output 2	Section 8.12.3
22h	VOUT3	Voltage monitoring output 3	Section 8.12.3
23h	VOUT4	Voltage monitoring output 4	Section 8.12.3
25h	VPWR_M	VPWR voltage monitoring	Section 8.12.5
26h	TS_0_TEMP	Central die temperature	Section 8.12.6
27h	PI_DC1	PI PWM duty cycle output 1	Section 8.8
28h	PI_DC2	PI PWM duty cycle output 2	Section 8.8
29h	PI_DC3	PI PWM duty cycle output 3	Section 8.8
2Ah	PI_DC4	PI PWM duty cycle output 4	Section 8.8
2Bh	FB_IOUT1	Feedback current at Ton/2 for OUT1	Section 8.8
2Ch	FB_IOUT2	Feedback current at Ton/2 for OUT2	Section 8.8
2Dh	FB_IOUT3	Feedback current at Ton/2 for OUT3	Section 8.8
2Eh	FB_IOUT4	Feedback current at Ton/2 for OUT4	Section 8.8
2Fh	TS_1_Temp	Channel 1 temperature	Section 8.12.6
30h	TS_2_Temp	Channel 2 temperature	Section 8.12.6
31h	TS_3_Temp	Channel 3 temperature	Section 8.12.6
32h	TS_4_Temp	Channel 4 temperature	Section 8.12.6
33h to 39h	Reserved	Reserved	

[1] To address diagnostic register bit 7 (D7/REG) = 0 in 16-bits MOSI frame.

8.10 Device status

The first eight registers (from 00h to 07h) provide all device status which includes global status, direct input, output state and interruption.

8.10.1 Global status

The global status register provides a one glance failure overview. Bits reporting an event like supply voltage supervision (bits 11 to 8) or output warning (bits 7 to 4) are latched in GLB_STA register and are cleared by reading them. When latched bit is read 1, this means an event occurs at least once since last global status readout.

When a fault condition like warning event or latch-off output is indicated by one of GLB_STA[7:0] bits, the fault detail can be obtained in corresponding OUTx_STA register.

Table 19. Global status - diagnostic register (address 00h) bit description

Address	Register	Bit	Description
00h	GLB_STA	13 to 12	Mode of operation 00 = normal mode [1] 01 = unused 10 = safe mode 11 = unused
		11	charge pump fault
		10	VPWR low-voltage [1]
		9	VPWR undervoltage [1]
		8	VDD undervoltage [1]
		7	OUT4_W output 4 warning event occurs [1]
		6	OUT3_W output 3 warning event occurs [1]
		5	OUT2_W output 2 warning event occurs [1]
		4	OUT1_W output 1 warning event occurs [1]
		3	OUT4_LF output 4 in latch-off state
		2	OUT3_LF output 3 in latch-off state
		1	OUT2_LF output 2 in latch-off state
		0	OUT1_LF output 1 in latch-off state

[1] Bit latches and clears when register is read.

8.10.2 Direct input and output logic state

The IN_OUT_STA register reports the logic state for direct input pins IN1 to IN4 and output OUT1 to OUT4.

This register shows each of the power NMOS outputs as a logic signal and consequently changes the OUTx pin to the OFF state as a logic input. To select the logic level threshold; see Section 8.12.4 "Output voltage programmable warning threshold".

Table 20. Input and output logic state - diagnostic register (address 01h) bit description

Address	Register	Bit	Description
01h	IN_OUT_STA	13 to 9	Unused
		8	Test mode activated
		7	OUT4_LS output 4 logic state
		6	OUT3_LS output 3 logic state
		5	OUT2_LS output 2 logic state
		4	OUT1_LS output 1 logic state
		3	IN4_LS direct input IN4 logic state
		2	IN3_LS direct input IN3 logic state
		1	IN2_LS direct input IN2 logic state
		0	IN1_LS direct input IN1 logic state

8.10.3 Outputs status

The four OUTx_STA registers provide details concerning each fault condition detected. All bits are latched and are cleared by reading them.

Table 21. Output status - diagnostic register (address 02h to 05h) bit description

Address	Register	Bit	Description
02h to 05h	OUTx_STA	13	TSDx Thermal shutdown[1][2]
		12	NCRx: Number of current limit retries exceed ACL circuit[1][2]
		11	SSCx: Severe short-circuit[1][2]
		10	OLCx: overload condition[1][2]
		9	ACLx: Active current limit[1][2]
		8	OTWx: Overtemperature warning[1][2]
		7	OCWx: Overcurrent warning[1][2]
		6	UCWx: Undercurrent warning[1][2]
		5	OVWx: Overvoltage warning[1][2]
		4	UVWx: Undervoltage warning[1][2]
		3	SVFx: Short to VBAT in OFF state[1][2]
		2	OLOx: Open load in ON state[1][2]
		1, 0	Unused[1][2]

[1] By default, bit is clear
[2] Bit latches and clears when register is read.

8.11 12-bits ADC

The Analog-to-Digital Converter is a 12-bit converter which is multiplexing the following signals:

- Eight current senses from 0 A to 5.0 A for OUT1 to OUT4
- Five voltage senses from 3.0 V to 65 V for OUT1 to OUT4 and VPWR

- Five thermal sensor signal from −40 °C to 215 °C one for the central die and one for each power NMOS

The ADC state machine runs following two modes; the cycle conversion mode and interrupt conversion mode. By default, the ADC is operated in cycle conversion mode and continuously running to convert all 18 analog inputs. In normal or safe mode the ADC is running and refreshing register content, regardless of the output state. A complete cycle time to refresh all registers is performed in about 80 µs. An average of N sample methods is recommended to get rid of the noise.

8.11.1 Output current measurement

The device has automatic current sense to provide enhanced accuracy over 3 decades. The low range from 5.0 mA provides the best accuracy, for instance for LED module or open load detection. The high range up to 5.0 A[1] is intended for current exceeding the low range like overload protection (OLP) circuits.

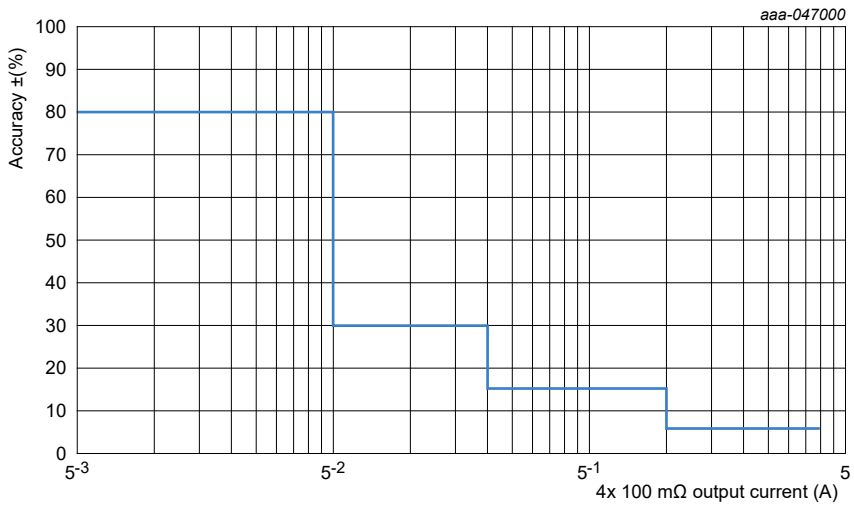


Figure 12. ADC current measurement accuracy (T_J = –40 °C to 150 °C)

8.11.2 Output voltage measurement

The ADC voltage measurement can be performed from 0.5 V to 65 V for the outputs (OUTx) and from 3.0 V to 65 V for monitoring VPWR supply pins.

1 The ADC accuracy is tested in production up to 4.0A output current.

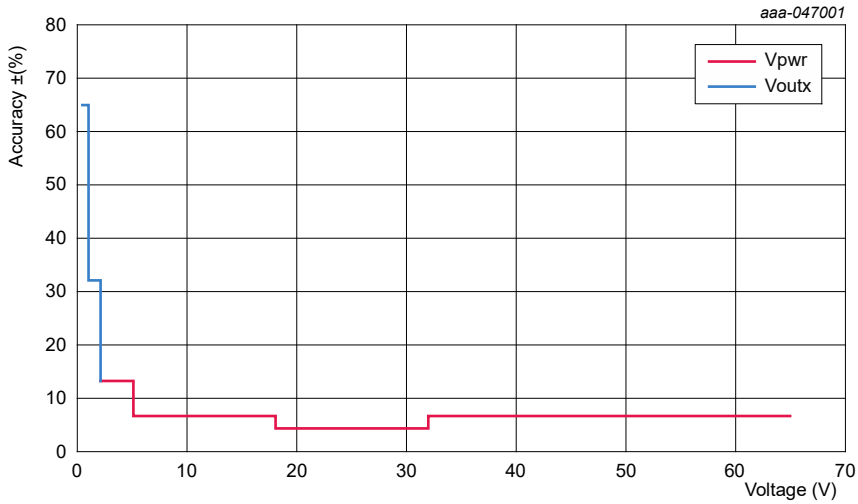


Figure 13. ADC voltage measurement accuracy (T_J = – 40 °C to 150 °C)

8.12 Monitoring and programmable warning threshold

The four outputs are provided with specific circuitry to monitor current, voltage and power NMOS temperature. Combined registers allow for the configuration of various types of warning thresholds to detect many events that may occur and report them with interrupt control logic circuit.

8.12.1 Output current monitoring

Two registers (M_SETUP and C_CTRL) enable configuring the current range and three different modes of conversion per output; see Figure 14.

On-demand conversion (ODC): Requests ADC conversion to refresh OD_IOUTx and OD_VOUTx registers. By SPI command, when one of the ODCVx bit in C_CTRL register is set high a fast conversion is requested. This bit is automatically cleared when the conversion is done. Thus by reading, the MCU can check the OD_IOUTx and OD_VOUTx registers validity.

Continuous measurement mode (CMM): When one output is in on-state, the current and voltage are continuously monitored every 1.0 ms to 8.0 ms and refreshed in registers IOUTx and VOUTx_ON. In M_SETUP register, the first measurement delay (FMD) enables mask turn on load behavior like inrush current from 1.0 ms to 64 ms. After that a periodic measurement time (PMT) can be selected from 1.0 ms to 8.0 ms. CMM conversion is disabled when device operates in PI Loop Current regulation.

Synchronized current mode (SCM): When enabled this function provides an initial (INI_IOUTx) and final (FIN_IOUTx) synchronized current. Just after the turn-on when the output voltage reaches VBAT – 2.0 V typ. (Δ_{V_COMP}) plus and delay of 50 µs typ. (T_{D_INI}), the initial current is triggered. The final current is sampled just before the turn-off.

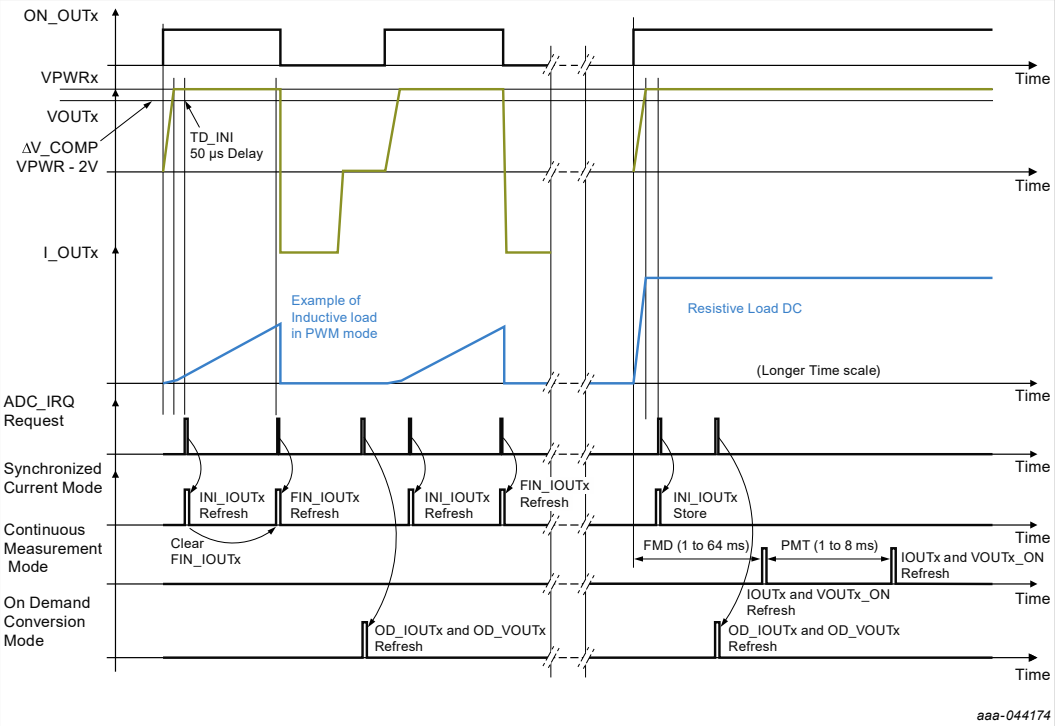


Figure 14. Simplified output current measurement logic diagram

Table 22. Measurement and conversion mode - control register (address 15h, 16h) bit description

Address	Register	Bit	Description
15h	M_SETUP	7 to 4	Unused
		3,2	Select the first measurement delay: FMD; see Table 23.
		1,0	Select the periodic measurement time: PMT; see Table 24.
16h	C_CTRL		Synchronous current mode: I_SCM 0 = disable (reset value) 1 = enable
		7	I_SCM4 for output 4
		6	I_SCM3 for output 3
		5	I_SCM2 for output 2
		4	I_SCM1 for output 1
			On-demand conversion: ODCVx 0 = conversion done (reset value) 1 = Trig one conversion (current + voltage)
		3	ODCV4 for output 4
		2	ODCV3 for output 3
		1	ODCV2 for output 2
		0	ODCV1 for output 1

Table 23. First measurement delay in CMM

FMD Time			
Value	**Time**	**Value**	**Time**
00b [1]	1.0 ms	10b	16 ms
01b	8.0 ms	11b	64 ms

[1] Reset value

Table 24. Periodic measurement time in CMM

PMT Time			
Value	**Time**	**Value**	**Time**
00b [1]	1.0 ms	10b	4.0 ms
01b	2.0 ms	11b	8.0 ms

[1] Reset value

Table 25. Output current measurement – diagnostic register (address 08h to 17h) bit description

Address	Register	Bit	Description
08h to 0Bh	OD_IOUTx		ODC: On-demand output current OUT1 to OUT4
		12 to 0	Value = code x (1/1023) A (LSB =0.98 mA) h03FF = 1.0 A h13FB = 5.0 A
0Ch to 0Fh	IOUTx		CCM: Continuous current monitoring OUT1 to OUT4
		12 to 0	h0000 = 0 A h13FB = 5.0 A
10h to 13h	INI_IOUTx		SCM: Initial current OUT1 to OUT4
		12 to 0	h0000 = 0 A h13FB = 5.0 A
14h to 17h	FNI_IOUTx		SCM: Final current OUT1 to OUT4
		12 to 0	h0000 = 0 A h13FB = 5.0 A

8.12.2 Output current programmable warning threshold

This function provides undercurrent and overcurrent warning logic signals to the interrupt service routing when an output exceeds the programmable thresholds.

Warning current control: WC_CTRL register specifies if the overcurrent and undercurrent warnings are compared with the initial output current register (INI_IOUTx) or the continuous output current monitoring (IOUTx).

Overcurrent warning: Depending on WC_CTRL configuration when the comparison is equal or above the selected overcurrent warning threshold (OCW_OUTx), the warning bit (OCWx) is set to 1 in OUTx_STA and interrupt can be generated.

Undercurrent warning: Depending on WC_CTRL configuration when the comparison is equal or below the selected undercurrent warning threshold (UCW_OUTx), the warning bit (UCWx) is set to 1 in OUTx_STA and interrupt can be generated.

Table 26. Warning current control and threshold - control register (address 17h to 1Fh) bit description

Address	Register	Bit	Description
17h	WC_CTRL	7 to 6	Warning current output 4
			00b = disable (reset value) 01 = comparison is done with INI_IOUT4 10 = comparison is done with IOUT4 11 = comparison is done with INI_IOUT4 and IOUT4
		5 to 4	Warning current output 3
			00b = disable (reset value) 01 = comparison is done with INI_IOUT3 10 = comparison is done with IOUT3 11 = comparison is done with INI_IOUT3 and IOUT3
		3 to 2	Warning current output 2
			00b = disable (reset value) 01 = comparison is done with INI_IOUT2 10 = comparison is done with IOUT2 11 = comparison is done with INI_IOUT2 and IOUT2
		1 to 0	Warning current output 1
			00b = disable (reset value) 01 = comparison is done with INI_IOUT1 10 = comparison is done with IOUT1 11 = comparison is done with INI_IOUT1 and IOUT1
18h, 1Ah, 1Ch, 1Eh	OCW_OUTx		Overcurrent warning threshold OUT1 to OUT4
		7 to 0	00h = disable (reset value) Threshold = code x (5/255) LSB = 19.6 mA FFh = 5.0 A
19h, 1Bh, 1Dh, 1Fh	UCW_OUTx		Undercurrent warning threshold OUT1 to OUT4
		7 to 0	00h = disable (reset value) Threshold = code x (1/255) LSB = 3.9 mA FFh = 1.0 A

8.12.3 Output voltage monitoring

Three different modes of voltage conversion per output are available; see Figure 15.

Output voltage monitoring (OVM): The VOUTx register is refreshed all the time by the ADC cycle conversion even in ON or OFF state.

Continuous measurement mode (CMM): When one output is ON state, this function is refreshing both I_OUTx and V_OUTx_ON registers as depicted in Section 8.12.1 "Output current monitoring". The first measurement delay (FMD) and periodic measurement time (PMT) are selectable in by M_SETUP register.

On-demand conversion (ODC): This function refreshes both OD_IOUTx and OD_VOUTx registers as depicted in Section 8.12.1 "Output current monitoring".

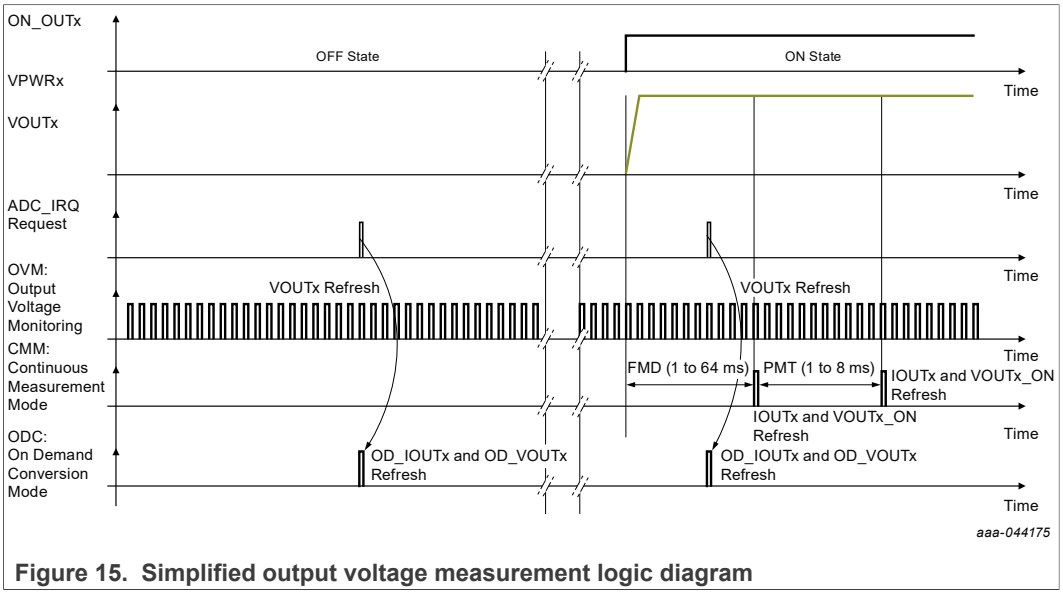


Figure 15. Simplified output voltage measurement logic diagram

Table 27. Output voltage measurement – diagnostic register (address 18h to 23h) bit description

Address	Register	Bit	Description
18h to 1Bh	VOUTx_ON		CMM: Continuous conversion mode in ON state OUT1 to OUT4
		9 to 0	000h = 0 V 3FFh = 65 V [1]
1Ch to 1Fh	OD_VOUTx		ODC: On-demand output voltage OUT1 to OUT4
		9 to 0	000h = 0 V 3FFh = 65 V [1]
20h to 23h	VOUTx		OVM: Output voltage monitoring OUT1 to OUT4
		9 to 0	000h = 0 V 3FFh = 65 V [1]

[1] LSB = 63.4 mV

8.12.4 Output voltage programmable warning threshold

This function provides undervoltage and overvoltage warning logic signals to the interrupt service routing when an output exceeds the programmable thresholds. This feature allows converting the NMOS Output into a digital input with configurable comparator thresholds. (This can be done when comparing Output in Off state to VOUTx register.)

Warning voltage control: WV_CTRL register allows selecting if the overvoltage and undervoltage warnings are done with the output voltage on state (VOUTx_ON), the continuous output voltage monitoring (VOUTx) or the output voltage on-demand (OD_VOUTx).

Overvoltage warning: Depending on WV_CTRL configuration when the comparison is equal or above the selected overvoltage warning threshold (OVW_OUTx) the warning bit (OVWx) in OUTx_STA register is set to 1 and interrupt can be generated.

Undervoltage warning: Depending on WV_CTRL configuration when the comparison is equal or below the selected undervoltage warning threshold (UVW_OUTx) the warning bit (UVWx) in OUTx_STA register is set to 1 and interrupt can be generated.

Output logic state: When the overvoltage circuit set the bit OVWx high, the bit OUTx_LS in IN_OUT_STA register is set to 1. When the undervoltage circuit set the bit UVWx high, the bit in OUTx_LS in IN_OUT_STA register is set to 0. This feature reports the output logic state where thresholds are configurable by OVW_OUTx and UVW_OUTx registers. Following wrong configuration if OVWx and UVWx flags are high at the same time, the OUTx_LS bit is set to 0.

Table 28. Warning voltage control and threshold - control register (address 20h to 28h) bit description

Address	Register	Bit	Description
20h	WV_CTRL	7 to 6	Warning voltage output 4
			00b = disable (reset value) 01 = comparison is done with VOUT4_ON 10 = comparison is done with VOUT4 11 = comparison is done with OD_VOUT4
		5 to 4	Warning voltage output 3
			00b = disable (reset value) 01 = comparison is done with VOUT3_ON 10 = comparison is done with VOUT3 11 = comparison is done with OD_VOUT3
		3 to 2	Warning voltage output 2
			00b = disable (reset value) 01 = comparison is done with VOUT2_ON 10 = comparison is done with VOUT2 11 = comparison is done with OD_VOUT2
		1 to 0	Warning voltage output 1
			00b = disable (reset value) 01 = comparison is done with VOUT1_ON 10 = comparison is done with VOUT1 11 = comparison is done with OD_VOUT1
21h, 23h, 25h, 27h	OVW_OUTx		Overvoltage warning threshold OUT1 to OUT4
		7 to 0	00h = disable (reset value) FFh = 65 V [1]
22h, 24h, 26h, 28h	UVW_OUTx		Undercurrent warning threshold OUT1 to OUT4
		7 to 0	00h = disable (reset value) FFh = 65 V [1]

[1] LSB = 255 mV

8.12.5 Voltage supply monitoring

VPWR voltage value is available by reading VPWR_M register. This register is updated by the ADC cycle conversion.

Table 29. Supply voltage measurement – diagnostic register (address 25h) bit description

Address	Register	Bit	Description
25h	VPWR_M		VPWR voltage monitoring
		9 to 0	000h = 0 V 3FFh = 65 V [1]

[1] LSB = 63.4 mV

8.12.6 Temperature monitoring and programmable warning threshold

The central die temperature is available by reading the TS_0_TEMP register. A thermal sensor is also available on outputs. It gives information for each power stage junction temperature through TS_1_TEMP to TS_4_TEMP registers.

Overtemperature warning: When one power NMOS thermal sensor is above the temperature warning threshold configured by TEMP_WT register the warning bit (OTWx) in OUTx_STA register is set to 1 and interrupt can be generated.

Table 30. Temperature warning threshold - control register (address 29h) bit description

Address	Register	Bit	Description
29h	TEMP_WT		Die temperature warning threshold
		7 to 0	Temperature warning threshold = Code – 40 [1] A5h = 125 °C (reset value) FFh = 215 °C

[1] LSB = 1 °C

Table 31. Thermal sensor – diagnostic register (address 26h) bit description

Address	Register	Bit	Description
26h	TS_0_TEMP		Central die temperature
		9 to 0	Temperature = Code x 0.25 – 40 [1] 105h = 25 °C 3FFh = 215 °C
2Fh to 32h	TS_x_TEMP		OUT1 to OUT4 junction temperature
		9 to 0	Temperature = Code x 0.25 – 40 [1] 105h = 25 °C 3FFh = 215 °C

[1] LSB = 0.25 °C

8.13 Load diagnostics

The device provides dedicated function for diagnostic issues like short-circuit to VBAT in off-state, short-circuit to GND in on-state and open load detection in on-state.

8.13.1 Short to VBAT in OFF state

Continuous sensing of the output voltage can diagnose an output short to VBAT in OFF state. To properly detect this event, it is necessary to define the characteristics of this condition. Depending on type of load connected, for all outputs the detection threshold must be selected as well as the appropriate blanking delay, see Figure 16.

The detection is activated automatically and once an output turns OFF, after a blanking delay (ΔT_STVB) if the output voltage is higher than offset voltage (VPWR – ΔV_STVB), a short-circuit to VBAT (= VPWR) is detected. Consequently, for each output a bit SVFx in register OUTx_STA is set to 1 and latched to indicate that event has occurred.

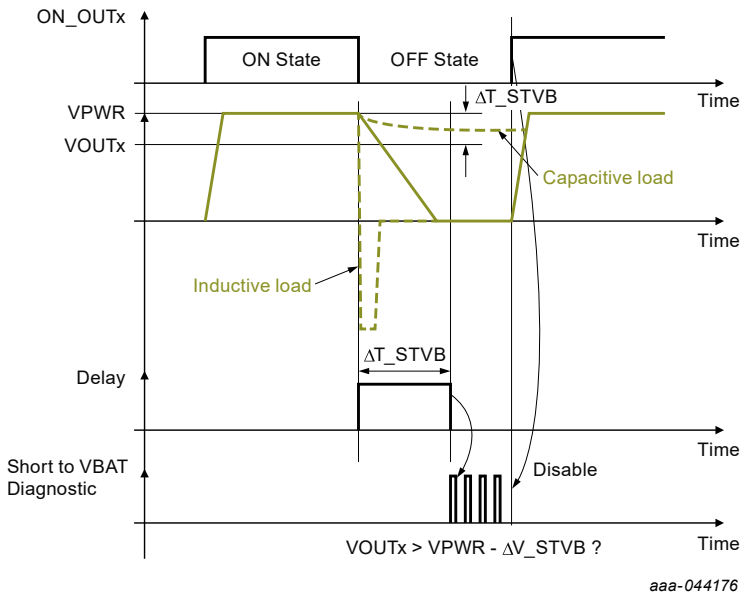


Figure 16. Short to VBAT in OFF state detection

Table 32. Short to VBAT in OFF state - control register (address 2Ah, 2Bh) bit description

Address	Register	Bit	Description
2Ah	ΔV_STVB	7 to 0	Offset voltage to diagnose a short to VBAT in OFF state
			Threshold = code x 0.255 V 04h = 1.0 V (reset value) FFh = 65 V
2Bh	ΔT_STVB	7 to 4	Blanking delay; see Table 33
		3 to 0	Unused

Table 33. ΔT_STVB blanking delay

Period							
Value	Time	Value	Time	Value	Time	Value	Time
0000b	0.1 ms	0100b	0.3 ms	1000b	3.2 ms	1100b	51.2 ms
0001b	0.15 ms	0101b	0.4 ms	1001b	6.4 ms	1101b	102.4 ms
0010b	0.20 ms	0110b	0.8 ms	1010b	12.8 ms	1110b	unused
0011b	0.25 ms	0111b [1]	1.6 ms	1011b	25.6 ms	1111b	unused

[1] Reset value

8.13.2 Short to GND in ON state

A short-circuit to ground in the ON state is diagnosed by reading the OUTx_STA registers content. Bits [13:10] in OUTx_STA registers allows distinguishing the type of short-circuit to GND or overload which has occurred: see Section 8.10.3 "Outputs status".

- One thermal shutdown event has occurred
- The number of ACL (active current limit) retry has exceeded
- An overload condition has occurred
- A severe short-circuit (SSC) has been detected

8.13.3 Open load in ON state

Continuously sensing of the output current allows for the diagnosis of an open load condition during an ON state. To properly detect this event, it is necessary to precisely define the characteristics of this condition. Depending on type of load connected, for each output the detection threshold must be selected as well as the appropriate delay, see Figure 17.

The detection is activated automatically once an output turns ON and reaches VPWR - 2.0 V. After a selected delay (T_OLDx) if the output current is lower than the chosen threshold (I_OLDx), an open load condition is detected. Consequently, for each output a bit OLOx in associated register OUTx_STA is set to 1 and latched to indicate that event has occurred.

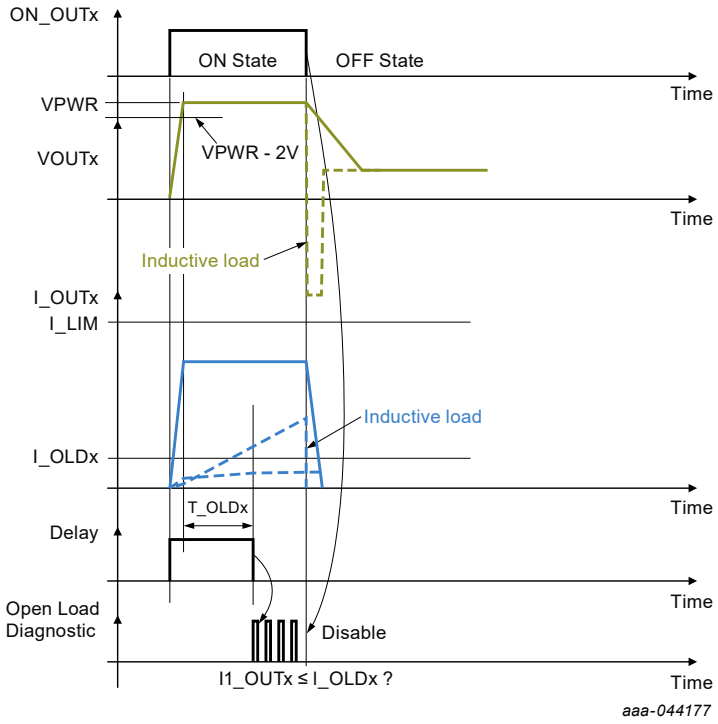


Figure 17. Open load detection in ON state

Table 34. Open Load Detection - control register (address 2Ch to 31h) bit description

Address	Register	Bit	Description
2Ch	OPD_CTRL1	7 to 5	T_OLD1 time for output 1; see Table 35
		4 to 2	T_OLD2 time for output 2; see Table 35
		1	0 = No action default 1 = Clear OUT2_LF bit in GLB_STA [1]
		0	0 = No action default 1 = Clear OUT1_LF bit in GLB_STA [1]
2Dh	OPD_CTRL2	7 to 5	T_OLD3 time for output 3; see Table 35
		4 to 2	T_OLD4 time for output 4; see Table 35
		1	0 = No action default 1 = Clear OUT4_LF bit in GLB_STA [1]
		0	0 = No action default 1 = Clear OUT3_LF bit in GLB_STA [1]
2Eh to 31h	I_OLD1 to I_OLD4	7 to 0	open load current detection threshold = code x 4.0 mA 00h = disable 03h = 12 mA (reset value) FFh = 1.0 A

[1] When OUTx_LF bit clear is set to 1, its value is not retained and is cleared when action is complete. When performing this action, the OPD_CTRLx[2 to 7] configuration bits are unchanged.

Table 35. Delay to Open Load in ON State (T_OLDx)

T_OLDx Time			
Value	**Time**	**Value**	**Time**
000b	50 µs	100b	300 µs
001b [1]	100 µs	101b	400 µs
010b	150 µs	110b	800 µs
011b	200 µs	111b	1600 µs

[1] Reset value

8.13.4 Open load in OFF state

During the OFF state, an open load can be diagnosed by using on-demand conversion mode (ODC) with programmable voltage warning thresholds in addition to an external passive system that could force a residual voltage to a floating output.

8.14 Protection

A set of protection against overvoltage and overcurrent stress is included in the device. Several voltage clamps systems are protecting supply pin against ISO pulses and power output against inductive load. Smart current limit and programmable overcurrent functions have been designed to protect loads, wire harness and device itself.

Voltage protection:

- Positive and negative clamping structures for each output limits the VPWR to OUTx and OUTx to GND in case of inductive switching.
- One central clamp against overvoltage transient on VPWR versus GND
- A reverse VBAT polarity circuit

Current protection:

- An active current limiting (ACL)
- A severe short-circuit (SSC)
- An over load protection (OLP)
- A thermal shutdown per output

8.14.1 Active voltage clamp

For any mode of operation, the device remains protected against overvoltage between VPWR to GND and between VPWR to OUTx by voltage clamp circuits.

A positive clamp inductive switching (P_CIS) circuit limits to +63.5 V typ. (VP_CIS) the voltage from VPWR to OUTx. These circuits protect each output against undervoltage caused by inductive impedance; see Table 47.

A negative clamp inductive switching (N_CIS) circuit limits to −37.5 V typ. (VN_CIS) the voltage from OUTx to GND. These circuits protect each output against undervoltage caused by inductive impedance; see Table 47.

A positive central clamp (P_CC) senses the voltage from VPWR to GND and activates four switches in order to clamp VPWR to GND at +63.5 V typ. (VP_CC). The VP_CC voltage threshold clamp can be achieved only if an external load with sufficient low impedance allows to conduct enough current to create a supply voltage drop according to supply impedance losses.

8.14.2 Reverse battery

In case the application is not protected against reverse battery condition, the current can circulate in reverse through the connected loads.

To prevent the device from thermal overheating because of its intrinsic body diode, the four power outputs are turned ON when GND terminal is 4.0 V higher than VPWR terminal; see Table 47.

8.14.3 Output latch-off overview

The faults listed latches off an output. Depending on the configuration, the output does not allow turn on until the latch is cleared or the fault disappears.

- Thermal shutdown: TSDx
- Delta temperature triggered by ACL protection: Δ_TJ
- Severe short-circuit: SSCx
- Overload condition: OLCx
- Charge pump undervoltage: VCP_UV
- VBAT undervoltage VPWR_UV

8.14.4 Thermal protection

A thermal sensor is monitoring each power NMOS. When one of the sensors exceeds the overtemperature threshold 175 °C (T_{SD}) this NMOS is turned off. The device returns to “normal state” by temperature reducing below the threshold hysteresis (T_{SD_H}).

If the thermal shutdown retry mode is disabled by ACL_CTRL2[7] bit = 1, the device returns to “normal state” by a 10 second timeout. The fault is reported in OUTx_STA and an interrupt can be generated.

In addition the current limit threshold (ACL) is reduced to I_{LIMx_R} in order to minimize fast repetitive thermal shutdown cycles and returned to normal level I_{LIMx_N} when the temperature reduces below 150 °C (T_{SD_R}).

8.14.5 Active current limit (ACL)

In case of excessive load or short-circuit, the ACL circuit limits the power NMOS current to I_{LIMx} by increasing its resistance. The device has one current limit threshold I_{LIM1_N} for each output

To minimize the power dissipation, the current limit threshold is VDS (VOUT – VPWR) dependent. When V_{DS} is above 32 V and up to 42 V the current limitation threshold is decreasing linearly; see Figure 18.

When one ACL is activated, the power NMOS temperature is rising rapidly. In order to minimize the device stress during this activation, the delta junction temperature increase is limited +60 °C (Δ_{TJ}). If it is exceeded, the NMOS is fast turned off until its temperature is decreased by 30 °C (Δ_{TJH}). Depending on configuration if the fault condition remains the device retries N times; see Figure 19. When the number of retries is exceeded, the output is latched off, the fault is reported in OUTx_STA and an interrupt can be generated. If the ACL remains inactivated longer than 5.0 s the count retry CRx is cleared. It is possible to clear the counter retry CRx by an action on registers OPD_CTRLx and then re-arm the output right after SPI command is sent (see Table 34).

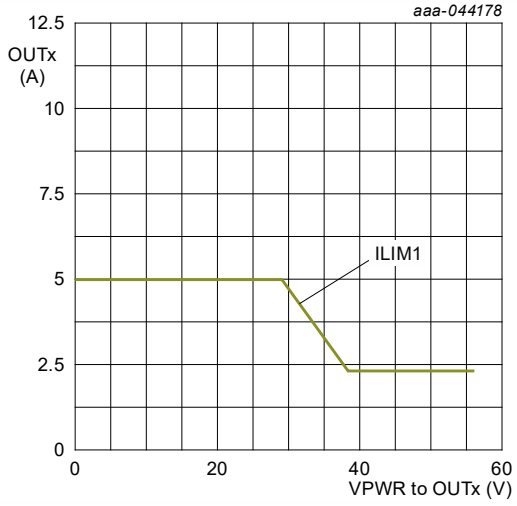


Figure 18. Typical current limitation

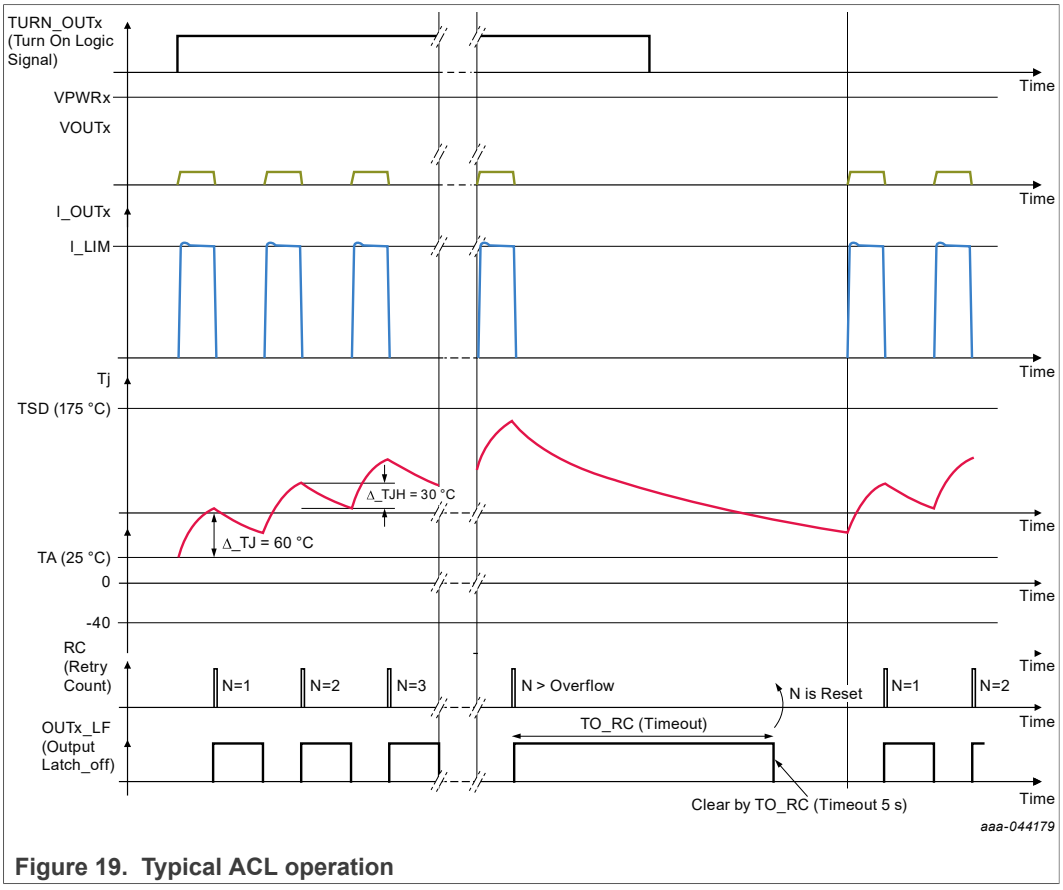


Figure 19. Typical ACL operation

Table 36. Open Load Detection - control register (address 32h to 33h) bit description

Address	Register	Bit	Description
32h	ACL_CTRL1	7 to 6	Current Limit threshold level: I_LIM 00 = Unused 01 = I_Lim1 (reset) 10 = Unused 11 = Unused
		5 to 3	Number of retry count: NRC4; see Table 37
		2 to 0	Number of retry count: NRC3; see Table 37
33h	ACL_CTRL2	7	Disable thermal shutdown retry mode (for all output) 0 = thermal shutdown retry (reset value) 1 = thermal shutdown once
		6	Unused
		5 to 3	Number of retry count: NRC2; see Table 37
		2 to 0	Number of retry count: NRC1; see Table 37

Table 37. Number of retry count

NCRx			
Value	N retry	Value	N retry
000b	0	100b	10
001b	1	101b [1]	15
010b	3	110b	20
011b	5	111b	30

[1] Reset value

8.14.6 Severe short-circuit (SSC)

The SSC function enables to detect a severe short-circuit when turning on the power NMOS or in steady state. When enabled, this function is able to distinguish a real short-circuit from a capacitive load. For example, the device can turn on a charge with a bypass capacitor of 470 µF with I_LIM = 5.0 A without triggering the SSC protection.

When a severe short-circuit condition is detected the output is fast turned off, the condition is reported in OUTx_STA and an interrupt can be generated.

Two types of SSC can be configured and both are based on 1.0 V delta output voltage monitoring. After 5.0 s delay the SSC condition is cleared and the device retries. As for the ACL function, this is also possible to clear the OUTx_LF fault with an action on registers OPD_CTRLx and then re-arm the output right after SPI command is sent (see Table 34.

Severe short-circuit on delay:

If one ACL is activated and the output voltage did not increase more than 1.0 V ($\Delta_{\_VOUTx}$) after a delay of 200 µs (T_{C_VOUT}) a severe short-circuit is detected; see Figure 20.

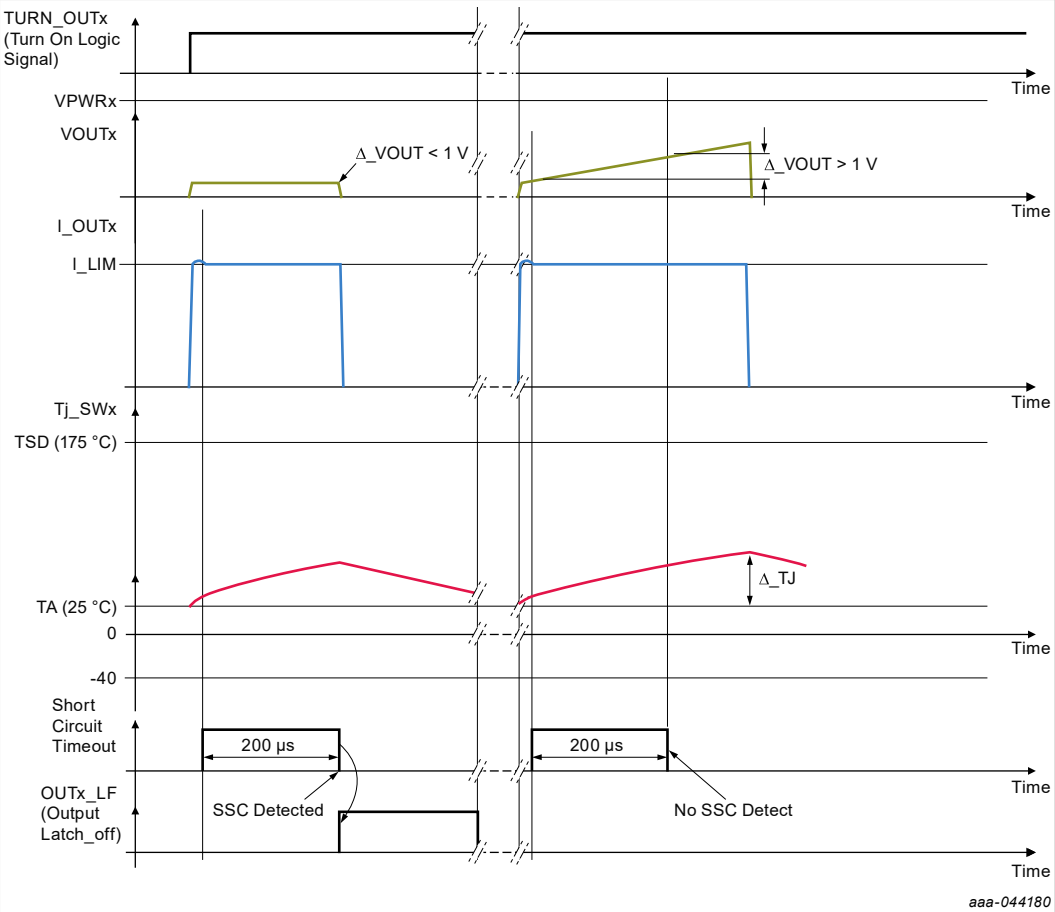


Figure 20. Severe short-circuit on delay

Severe short circuit on ACL count retry:

After 3 retries triggered by the ACL circuit, if the output voltage did not increase more than 1.0 V (Δ_{VOUTx}), a severe short-circuit on retry is detected; see Figure 21.

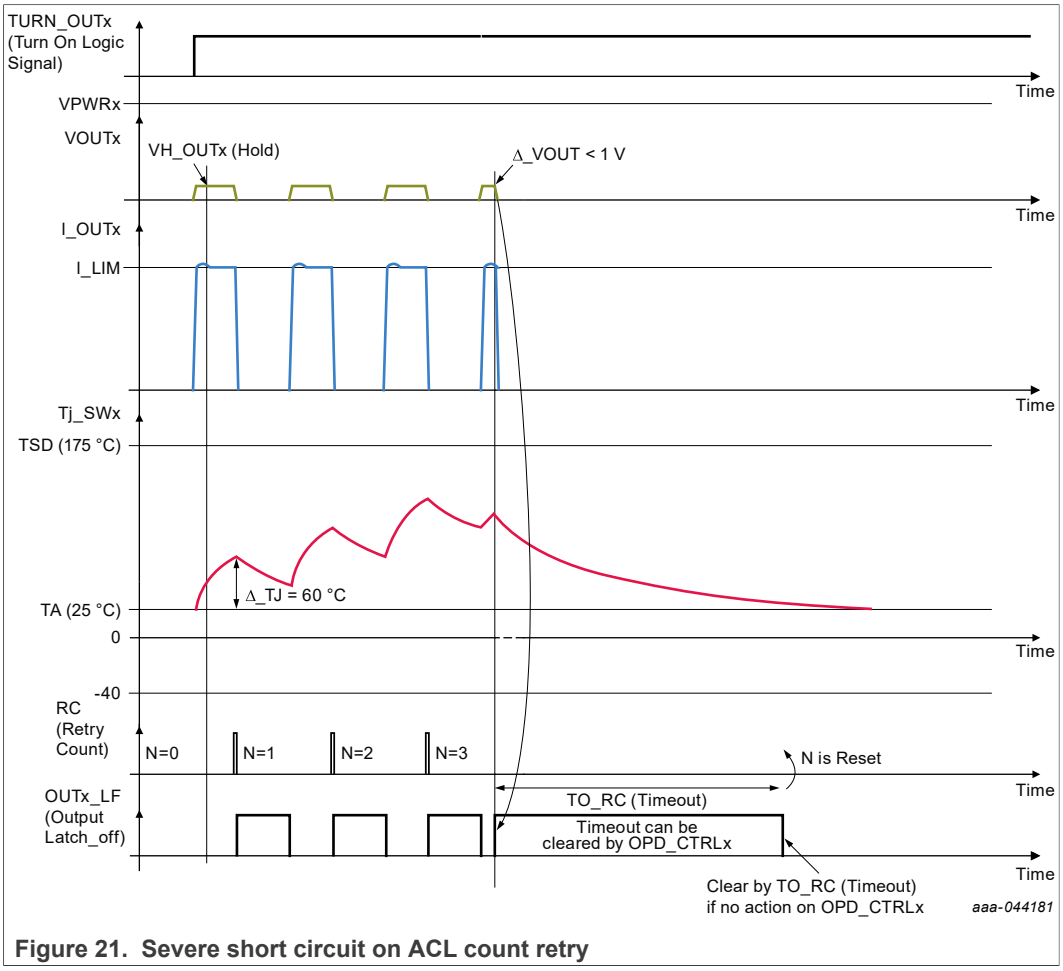


Figure 21. Severe short circuit on ACL count retry

Table 38. Severe short-circuit - control register (address 34h) bit description

Address	Register	Bit	Description
34h	SSC_CTRL		Enable severe short circuit on delay 0 = SSC_Dx on delay is enabled (reset value) 1 = SSC_Dx on delay is disabled
		7	SSC_D4
		6	SSC_D3
		5	SSC_D2
		4	SSC_D41
			Enable severe short circuit on 3 + 1 ACL count retry 0 = SSC_Rx on retry is enabled (reset value) 1 = SSC_Rx on retry is disabled
		3	SSC_R4
		2	SSC_R3
		1	SSC_R2
		0	SSC_R1

8.14.7 Overload protection (OLP)

The device is protected against overload and this condition is detected when an output is above a current level longer than a timeout period. Each enabled output current is continuously monitored by ADC in CCM. When an NMOS current exceeds the programmable (OCL_OUTx) threshold longer than (T_OC) period, an overload condition is detected. After a 10 ms (± 10 %) deglitch time the fault is valid and reports in OUTx_STA, also an interrupt can be generated. Depending on configuration, the output can be fast turned off or the device can transit in safe mode.

Table 39. Over load protection - control register (address 35h) bit description

Address	Register	Bit	Description
35h	OLP_CTRL	7	Transit is safe mode 1 = enable 0 = disable (reset value)
		6	Disable latches off activation 1 = disable 0 = enable (reset value)
		5 to 3	Overcurrent timeout period: T_OC see Table 40
		2 to 0	unused

Table 40. Overcurrent timeout period

T_OC			
Value	**Time**	**Value**	**Time**
000b	125 ms	100b	2 s
001b	250 ms	101b	4 s
010b	500 ms	110b	8 s
011b [1]	1 s	111b	16 s

[1] Reset value

Table 41. Overcurrent level - control register (address 36h to 39h) bit description

Address	Register	Bit	Description
36h to 39h	OCL_OUTx		Overcurrent level for OUT1 to OUT4
		7 to 0	Overcurrent level threshold = code × (5/255) A 00h = disable CCh = 4.0 A (reset value) FFh = 5.0 A

9 Application design-in information

9.1 Circuit loops and tracks

In parallel mode in order to keep good current measurement accuracy the current path must be balanced between the two connected outputs. Ideally a copper track must connect both outputs directly together and the load is connected in the middle of this track.

9.2 Decoupling capacitors

Decoupling capacitors should be fitted directly on. Low ESR multi-layer ceramic capacitor type X7R is recommended. To achieve full performance a 10 nF shall bypass each power output, placed as close as possible to the connector. VPWR, VDD and VSPI pin must be decoupled by at least 100 nF as close as possible to the pin. Finally, VBAT line on ECU module shall be decoupled by at least a 100 µF electrolytic capacitor per MC33XS2410 to compensate the inductance supply line. See Section 15 "Application information" for application examples and components details.

9.3 PCB design

To prevent overheating it is important to ensure the average junction temperature (T_j) is less than 150 °C. PCB layout shall be designed to minimize the junction to ambient thermal resistance ($R_{th(j-a)}$). The HTSSOP-28 package has good thermal resistance from junction to case bottom ($R_{th(j-cb)}$). To optimize heat transfer through the PCB, the exposed pad is designed to be soldered to the ground plane. This ground should be connected to internal layer and bottom copper ground pad with thermal via placed directly under the package. Add as many thermal vias as possible to optimize the thermal conductivity of the board. Thermal vias should either be plated shut or plugged and capped on both sides to prevent solder voids. Recommended PCB layout is depicted in Figure 22 and Figure 23.

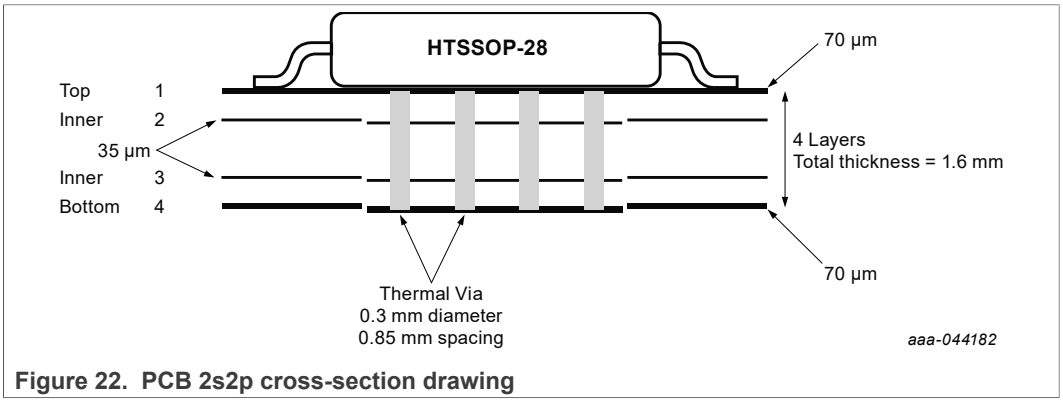


Figure 22. PCB 2s2p cross-section drawing

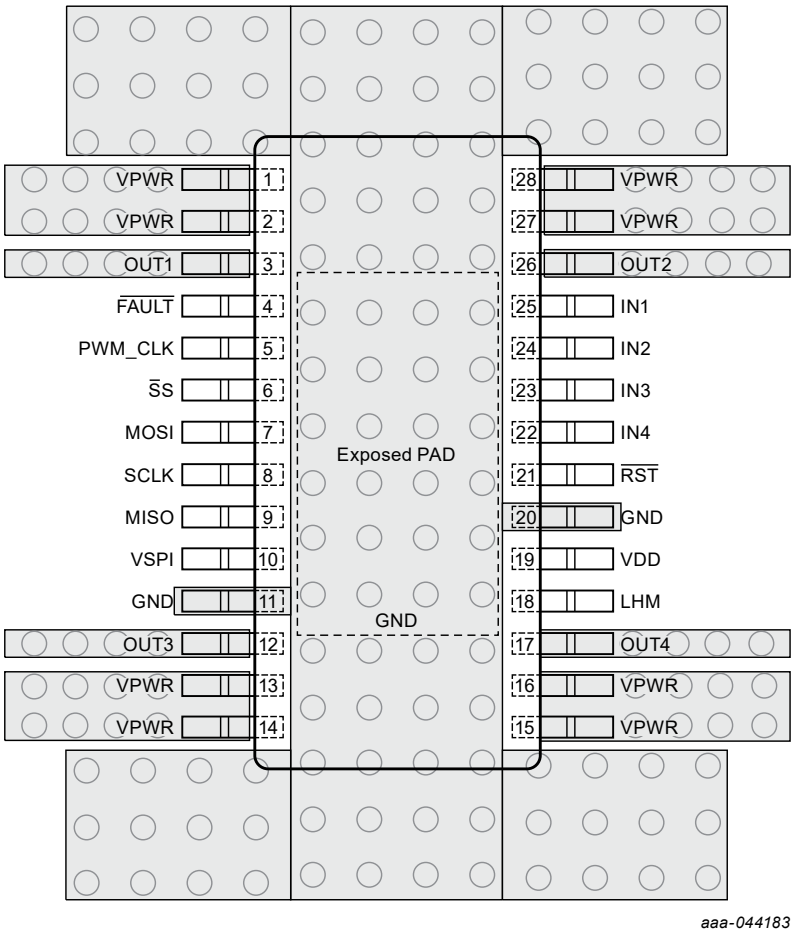


Figure 23. PCB 2s2p Recommended thermal pad and via layout

9.4 Thermal considerations

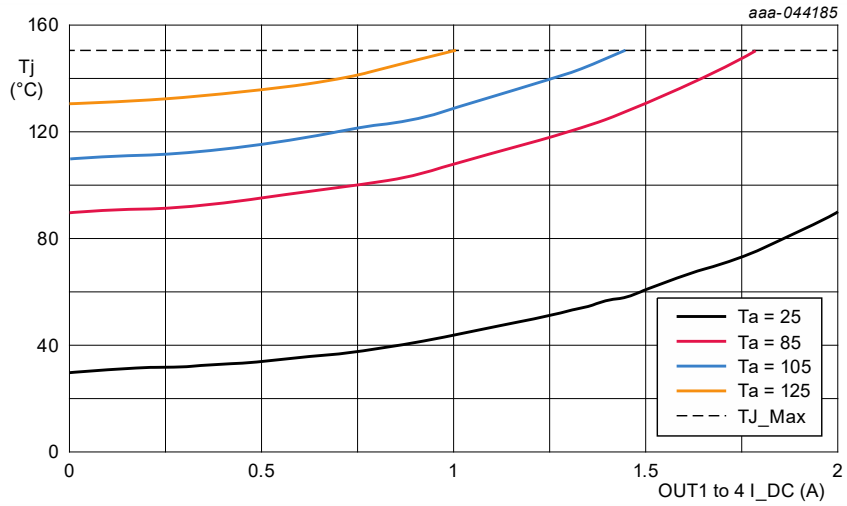
Since the MC33XS2410 device integrates four power NMOS, thermal considerations should be taken into account to prevent overheating, which can cause the device to go into thermal shutdown.

Nevertheless in order to ensure the long-term reliability of the device and operating conditions, junction temperature (T_j) should be calculated to ensure that is below the continuous junction temperature limit (150 °C).

The T_j of the device depends on the ambient temperature (T_{amb}), device's total power dissipation (P_{tot}), and thermal resistance ($R_{th(j-a)}$).

The device junction temperature can be calculated by using the following equation:

$$T_j = T_{amb} + R_{th(j-a)} \times P_{tot}$$



$R_{th(j-a)}$ = 24 °C/W, 4 channels ON state DC operation, V_{DD} = 5.0 V, V_{PWR} = 28 V

Figure 24. Typical T_J variation versus output current [A]

9.5 Output ON resistance

The ON state resistance R_{on} depends mainly on junction temperature (T_j). Figure 25 shows the variation across the whole T_j range.

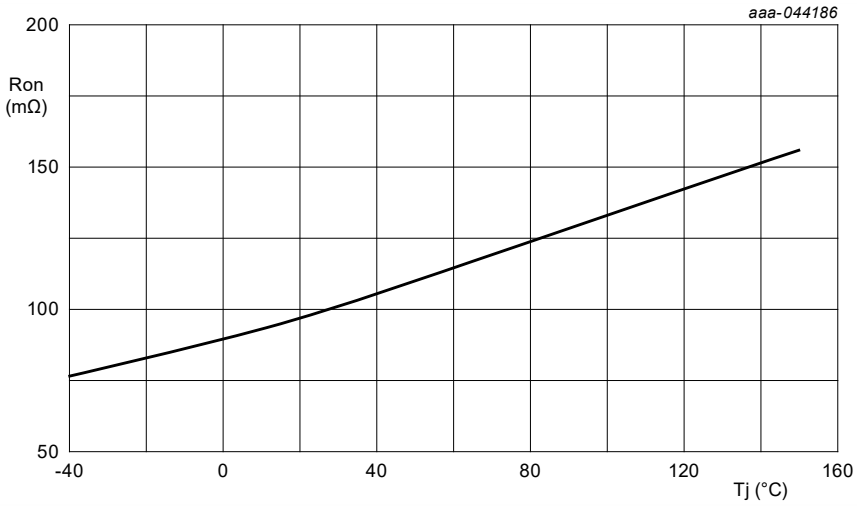


Figure 25. Typical R_{on} variation versus junction temperature (T_j)

10 Limiting values

Exceeding the limits of one or more values in reference may cause permanent damage to the device. Exposure to limiting values for extended periods may affect device reliability.

Table 42. Limiting values

Symbol	Parameter	Conditions	Min.	Max.	Unit
P_{tot_DC}	Total DC power dissipation	T_{amb} ≤ 85 °C	—	2.5	W
		T_{amb} ≤ 105 °C	—	1.8	
		T_{amb} ≤ 125 °C		1	
T_J	Junction temperature	continuous	−40	+150	°C
		transient [1]	−40	+195	°C
T_{STG}	Storage temperature		−55	+150	°C
Supplies					
VMR_V_{PWRx}	Power supply voltage		−35	60	V
VMR_V_{DD}	Device supply voltage		−0.3	6.5	V
VMR_V_{SPI}	SPI supply voltage		−0.3	6.5	V
SPI and Digital pins					
V_{DIG}	Digital voltage	pins MISO, MOSI, SCLK, $\overline{SS}$, PWM_CLK	−0.3	VSPI + 0.3	V
		pin $\overline{RST}$	−0.3	6.5	
I_{DIG}	Digital current	pins MISO, MOSI, SCLK, $\overline{SS}$, PWM_CLK,	—	1.0	mA
Logic output open-drain					
V_{DIG_OD}	Digital voltage	pin $\overline{FAULT}$	−35 or (VPWR − 60 V)	60	V
I_{DIG_OD}	Digital current	pin $\overline{FAULT}$ input sink current [2] [3]	—	1.0	mA
Limp Home Control Input					
V_{DIG_LH}	Digital high voltage	pins LHM, IN1, IN2, IN3 and IN4	–35 or (VPWR – 60 V)	60	V
Power output					
V_{OUT}	Output switches	pins OUT1, OUT2, OUT3 and OUT4	–35 V or (VPWR – 60 V)	VPWR + 0.3 V	V
I_{OUT}	Output current	pins OUT1, OUT2, OUT3 and OUT4 [4] [5]	−5.0	Internally limited	A
E_{CIS_S}	Single pulse energy	pins OUT1, OUT2, OUT3 and OUT4 [6]		30	mJ

Table 42. Limiting values...*continued*

Symbol	Parameter	Conditions	Min.	Max.	Unit
Electrostatic discharge voltages					
V_{ESD}	Electrostatic discharge voltage	CDM corner pins	–750	750	V
		other pins	–500	500	V
		HBM: all pins	–2.0	2.0	kV
		ESD Voltage at system level on global pins (VPWRx, OUTx, LHM, INx, $\overline{FAULT}$)	-8.0	8.0	kV

[1] Limited to 10 hours life time
[2] Reverse current is blocking internally
[3] Can support an inductive load at least up to 100 µH
[4] Positive V_{PWR} supply as defined in recommended operating conditions
[5] Transient of negative V_{PWR} supply ≤ 10 ms
[6] I_L = 5 A ± 20 % turn OFF current, T_J = 150 °C initial, V_{PWR} = 32 V

11 Recommended operating conditions

Table 43. Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supplies						
VO_V_{PWR}	Power supply voltage	operating [1]	3.0	28	60	V
VO_V_{DD}	Device supply voltage		4.5	5.0	5.5	V
VO_V_{SPI}	SPI supply voltage		3.3	5.0	5.5	V
General						
T_{amb}	Ambient temperature		−40	25	+125	°C
Direct input pins						
f_{PWM}	Switching frequency	on pins IN1, IN2, IN3 and IN4	—	400	2000	Hz

[1] When V_{PWR} < 3.95 V (typ.), the operating is guaranteed if V_{DD} ≥ 3.95 V (typ).

12 Thermal characteristics

Table 44. Thermal characteristics

Symbol	Parameter	Conditions	Typ.	Unit
$R_{th(j-a)}$	Thermal resistance from junction to ambient	[1]	24	°C/W
$R_{th(j-cb)}$	Thermal resistance from junction to case bottom (package exposed pad)		2	°C/W

[1] Thermal Resistance Junction-to-Ambient is specified value is according to JEDEC standard JESD51-2, JESD51-5 and JESD51-7 on FR4 2s2p board. Board 76.2 x 114.3 mm, 1.6 mm thickness with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer at the exposed pad of the package.

13 Static characteristics

Table 45. Supplies static characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Standby currents (disable mode)						
I_{VDD_STB}	V_{DD} standby current	T_j ≤ 85 °C	—	—	1.0	µA
I_{VSPI_STB}	V_{SPI} standby current	T_j ≤ 85 °C	—	—	1.0	µA
I_{VPWR_STB}	V_{PWR} standby current	V_{PWR} = 28 V, V_{OUT} = GND [1] T_j = 25 °C	—	—	2.0	µA
		T_j = 85 °C	—	—	4.0	µA
		T_j = 150 °C	—	—	40	µA
Operating currents ($\overline{RST}$ pin or LHM = HIGH)						
I_{VDD_OPR}	V_{DD} operating current		—	7.0	10	mA
$I_{VPWR\_OPR\_DC}$	V_{PWR} operating current	Channels OFF state, VPWR = 32 V	—	4.0	6	mA
$I_{VPWR\_OPR\_ON}$	V_{PWR} operating current	No load, 4 channel PWM operation at 2.0 kHz, 50 % duty cycle	—	5.5	8	mA
Supply: pins VPWR, VDD and VSPI						
VPWR low-voltage						
V_{PWR_LV}	Low-voltage detection		3.8	3.95	4.1	V
$V_{PWR\_LV\_HYS}$	Low-voltage hysteresis	[2]	200	300	400	mV
VPWR undervoltage						
V_{PWR_UV}	Undervoltage detection		2.7	2.85	3.0	V
$V_{PWR\_UV\_HYS}$	Undervoltage hysteresis	[2]	200	250	300	mV
VDD undervoltage						
V_{DD_UV}	Undervoltage detection		3.8	3.95	4.1	V
$V_{DD\_UV\_HYS}$	Undervoltage hysteresis	[2]	200	300	400	mV
VPWR and VDD wake up and power-on reset						
V_{DD_WUP}, V_{PWR_WUP}	VDD, VPWR wake-up		3.2	—	4.1	V
V_{DD_POR}, V_{PWR_POR}	VDD, VPWR power-on reset		2.6	—	3.3	V
VSPI low-voltage						
V_{SPI_LV}	Low-voltage detection		2.5	2.6	2.7	V
$V_{SPI\_LV\_HYS}$	Low-voltage hysteresis	[2]	200	275	350	mV

[1] 50 ms after all channels have been switched OFF.
[2] Rising slop.

Table 46. High-side switches static characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power stage						
R_{on_25}	ON state resistance	V_{PWR} to OUTx pin at T_j = 25 °C	—	100	—	mΩ
R_{on_150}	ON state resistance	V_{PWR} to OUTx pin at T_j = 150 °C	—	—	200	mΩ
R_{on_DER}	ON state resistance increases with temperature		—	0.45	—	mΩ/ °C
ΔR_{on_150}	ON state resistance difference between two outputs in parallel mode	V_{PWR} to OUTx pin at T_j = 150 °C	−5.0	—	5.0	mΩ
I_{OUT_4DC}	DC Output current per channel	4 channels ON state (4 x 100 mΩ) [1]	—	1.8	[2]	A
I_{OUT_1DC}	DC Output current per channel	1 channels ON state (1 x 100 mΩ) [1]	—	3.6	[2]	A
I_{OUT_2DC}	DC Output current per channel	2 channels ON state in parallel mode (2 x 50 mΩ) [1]	—	3.6	[2]	A
Output leakage currents (Output in OFF state)						
$I_{LKG\_OUT\_0}$	OUTx leakage current	V_{PWR} = 32 V, V_{OUT} = GND [3] T_j = 25 °C	—	—	0.5	µA
		T_j = 85 °C	—	—	2	µA
		T_j = 150 °C	—	—	10	µA
$I_{LKG\_OUT\_32}$	OUTx leakage current	V_{PWR} = V_{OUT} = 32 V [3]	—	—	—	—
		T_j = 85 °C	—	—	300	µA
		T_j = 150 °C	—	—	300	µA
$I_{LKG\_OUT\_60}$	OUTx leakage current	V_{PWR} = V_{OUT} = 60 V [3]	—			
		T_j = 85 °C	—	—	600	µA
		T_j = 150 °C	—	—	600	µA
Output sense resistance to GND						
R_{S_OUT}	OUTx output resistive network voltage sense	OUTx to GND [4]	100	220	300	kΩ

[1] Based on T_{amb} = 85 °C and JEDEC 2s2p PCB
[2] Maximum current is limited by active current limiting circuit
[3] 50 ms after channel or all channels have been turned OFF, current leak out from OUTx pins.
[4] Guaranteed by design

Table 47. Protection circuits characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to + 150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Overvoltage protection						
V_{P_CC}	Positive central clamp voltage	V_{PWR} to GND	60	63.5	67	V
V_{N_RB}	Reverse current turn ON voltage	V_{PWR} to GND	–4.0	—	—	V
V_{P_CIS}	Positive clamping structure for clamped inductive switching (CIS)	V_{PWR} to V_{OUTx} pin	60	63.5	67	V
V_{N_CIS}	Negative clamping structure for CIS	V_{OUTx} pin to GND	−40	−37.5	−35	V
Overtemperature protection						
T_{SD}	Overtemperature shutdown threshold		165	175	185	°C
T_{SD_H}	Overtemperature hysteresis		15	20	25	°C
T_{SD_R}	Overtemperature reset		130	140	150	°C
Overcurrent protection: active current limit (ACL)						
I_{LIM1_N}	Normal limit 1 current	ACL_CTRL1[7-6] = 01 [1]	4.0	5.0	6.0	A
I_{LIM1_R}	Reduce limit 1 current	ACL_CTRL1[7-6]=01 [2]	1.6	2.3	3.0	A
$\Delta_{\_TJ}$	Delta junction temperature		40	60	80	°C
$\Delta_{\_TJH}$	Delta junction temperature hysteresis		20	30	40	°C
T_{O_RC}	Time-out to reset retry count register RCx		4.5	5.0	5.5	s
Overcurrent protection: severe short-circuit (SSC)						
T_{C_VOUT}	Comparison delay		160	200	240	µs
Δ_{VOUTx}	Delta voltage comparison		0.8	1.0	1.2	V
T_{O_SSC}	Time-out to reset severe short bits flag SSCx_F		4.5	5.0	5.5	s
Overcurrent protection: overload protection (OLP)						
I_{R_OLP}	OLP range current		—	4.0	5.0	A

[1] V_{PWR} to V_{OUTx} pin < 32 V
[2] V_{PWR} to V_{OUTx} pin > 42 V

Table 48. Output current measurement characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to + 150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{O_MR}	Output current measurement range		5.0	—	5000	mA
Current measurement accuracy; T_J = −40 °C to 150 °C						
E_{IO_T1}	ADC error output current measurement	I_{OUT} = 5.0 mA	−80	—	80	%
		I_{OUT} = 50 mA	−30	—	30	%
		I_{OUT} = 200 mA	−15	—	15	%
		I_{OUT} = 1.0 A	−6	—	6	%
		I_{OUT} = 4.0 A	−6	—	6	%
Synchronized Current mode: (SCM)						
Δ_{V_COMP}	Comparator threshold from VBAT	[1]	1.4	2.0	2.6	V
$\Delta_{V\_COMP\_H}$	Comparator detection hysteresis from VBAT		300	—	600	mV
T_{D_INI}	Delay from Δ_{V_COMP} to capture INI_IOUTx current		40	50	60	µs

[1] When VPWR is 3 V to 5.0 V ΔV_COMP can be reduced to 1.5 V typ.

Table 49. Short to VBAT in OFF state: ΔV_STVB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ΔV_STVB_A	ΔV_STVB accuracy over range		–5.0	—	+5.0	%
ΔV_STVB_O	ΔV_STVB offset		–0.5	—	+0.5	V
ΔT_STVB	Blanking Delay ΔT_STVB time accuracy		–10	—	10	%

Table 50. Output voltage measurement characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{O_MR}	Output voltage measurement range		0	—	65	V
Output voltage measurement accuracy; 1 LSB ≈ 63.5 mV, T_J = −40 °C to 150 °C						
E_{VO_T1}	ADC error output voltage measurement	VOUT = 500 mV	—	—	± 65	%
		VOUT = 1.0 V	—	—	± 32	%
		VOUT = 2.0 V	—	—	± 13	%
		VOUT = 5.0 V	—	—	± 6.5	%

Table 50. Output voltage measurement characteristics...*continued*

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		VOUT = 18 V	—	—	± 4	%
		VOUT = 32 V	—	—	± 6.5	%
		VOUT = 65 V	—	—	± 6.5	%

Table 51. Supply voltage measurement characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{S_MR}	Supply voltage measurement range	V_{PWR}	3.0	—	65	V
Supply voltage measurement accuracy VPWR, 1 LBS ≈ 63.5 mV, T_J = −40 °C to 150 °C						
E_{VS_T1}	ADC error voltage measurement	V_{PWR} = 3.0 V [1]	—	—	± 13	%
		V_{PWR} = 5.0 V	—	—	± 6.5	%
		V_{PWR} = 18 V	—	—	± 4	%
		V_{PWR} = 32 V	—	—	± 6.5	%
		V_{PWR} = 65 V	—	—	± 6.5	

[1] Only apply for V_{PWR}

Table 52. Supply voltage measurement characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Temperature measurement; TS_0, TS_1, TS_2, TS_3 and TS_4; 1 LBS ≈ 0.23 °C						
T_{S_MR}	Temperature measurement range		−40	—	200	°C
E_{TS}	ADC error temperature measurement		—	—	± 7	°C

Table 53. Control circuits characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to +150 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Digital control input: pin $\overline{RST}$						
V_{IH_R}	HIGH-level input voltage		2.1	—	—	V
V_{IL_R}	LOW-level input voltage		—	—	0.9	V

Table 53. Control circuits characteristics...*continued*

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to +150 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{PD}	Input pulldown resistor	V_{RST} > 0.9 V	150	250	350	kΩ
C_{IN}	input capacitance	[1]	—	—	10	pF
$T_{IN\_FT\_RST}$	Deglitching filter time		10	—	20	µs
Interrupt output: pin $\overline{FAULT}$						
V_{OL_OD}	LOW-level output voltage	I_L = 1.0 mA	—	—	0.9	V
I_{L_OD}	Output leakage current	V_L = 0 V to 60 V	−10	—	10	µA
C_{out}	Output capacitance	[1]	—	—	10	pF
IMR_$\overline{FAULT}$	Open drain input sink current	Reverse current blocking by back to back open drain MOSFET.	—	—	1	mA
Digital input PWM clock reference: pin PWM_CLK						
V_{IH}	HIGH-level input voltage		0.7V_{SPI}	—	—	V
V_{IL}	LOW-level input voltage		—	—	0.3V_{SPI}	V
V_{HYS}	Input hysteresis voltage		0.1V_{SPI}	—	—	V
I_{WPD}	Weak pulldown current	V_{SPI} = 3.0 V to 5.5 V	12	—	60	µA
C_{IN}	Input capacitance	[1]	—	—	10	pF
Direct input control inputs: pins LHM, IN1, IN2, IN3 and IN4						
V_{IH_DI}	HIGH-level input voltage	GLB_CTRL[0] = 0 “AUTOMOTIVE level”	3.8	—	—	V
		GLB_CTRL[0] = 1 “CMOS level”	0.7V_{SPI}	—	—	V
V_{IL_DI}	LOW-level input voltage	GLB_CTRL[0] = 0 “AUTOMOTIVE level”	—	—	2.2	V
		GLB_CTRL[0] = 1 “CMOS level”		—	0.3V_{SPI}	V
V_{HYS_DI}	input hysteresis voltage	GLB_CTRL[0] = 0 “AUTOMOTIVE level”	400	—	—	mV
		GLB_CTRL[0] = 1 “CMOS level"	0.1V_{SPI}	—	—	V
R_{PD_DI}	input pulldown resistor		150	250	350	kΩ
C_{IN}	input capacitance	[1]	—	—	12	pF
$T_{IN\_DGL\_DI}$	deglitching filter time	IN_CTRL1[4..7] = 0	150	—	250	µs
		IN_CTRL1[4..7] = 1 [2]	—	—	—	µs

[1] Not tested in production; guaranteed by design and characterization.
[2] Not applicable for LHM input

Table 54. SPI static characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Serial peripheral interface inputs; pins MOSI, SCLK and $\overline{SS}$						
V_{IH}	HIGH-level input voltage		$0.7V_{SPI}$	—	—	V
V_{IL}	LOW-level input voltage		—	—	$0.3V_{SPI}$	V
V_{HYS}	Input hysteresis voltage		$0.1V_{SPI}$	—	—	V
I_{WPU}	Weak pullup current	pin $\overline{SS}$ only	12	—	60	µA
I_{WPD}	Weak pulldown current		12	—	60	µA
C_{IN}	Input capacitance		—	—	10	pF
Serial peripheral interface output; pins MISO						
R_{OH_M}	HIGH-level output impedance - Medium configuration	GLB_CTRL[5] = 1 MEDIUM configuration	80	200	410	Ω
R_{OH_S}	HIGH-level output impedance - Strong configuration	GLB_CTRL[5] = 0 STRONG configuration	20	50	108	Ω
I_{OZ}	OFF-state output current		−1.0	—	1.0	µA

14 Dynamic characteristics

14.1 General timing characteristics

Table 55. General dynamic characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to + 150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Oscillator clock reference						
$F_{\_OSC}$	Internal oscillator		40.13	42.24	44.35	MHz
F_{1_DEV}	Band 1 frequency modulation versus $F_{\_OSC}$	GLB_CTRL[1] = 0	0.735	1.05	1.365	MHz
F_{2_DEV}	Band 2 frequency modulation versus $F_{\_OSC}$	GLB_CTRL[1] = 1	1.47	2.1	2.73	MHz
$F_{\_MOD}$	Oscillator modulation frequency	GLB_CTRL[2] = 1 (enable)	140	200	260	kHz
Digital input PWM clock reference: pin PWM_CLK						
F_{PWM}	PWM clock frequency		50	—	512[1]	kHz
T_{OUT}	PWM clock timeout		80	100	120	µs
Device wake-up time						
T_{WAKE_UP}	Wake-up time	from RST or LHM pins transit LOW to HIGH	—	—	10	ms

[1] There is no PWM_CLK fail detection for high limit. 512 kHz corresponds to 2 kHz PWM frequency on power output.

14.2 High-side switches timing

Table 56. High-side switches dynamic characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to + 150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Output switch timing						
SR_R, SR_F	Rising and falling slew rate	fast slew rate mode OUT1-4_CTRL[4..7] = 1 [1]	1.5	3.0	4.5	V/µs
		slow slew rate mode OUT1-4_CTRL[4..7] = 0 [1]	0.25	0.5	0.75	V/µs
T_{TON_D}	Turn-on delay	fast slew rate mode OUT1-4_CTRL[4..7] = 1 [2]	16	—	28	µs
		slow slew rate mode OUT1-4_CTRL[4..7] = 0 [2]	29	—	58	µs
T_{TOFF_D}	Turn-off delay	fast slew rate mode OUT1-4_CTRL[4..7] = 1 [3]	16	—	28	µs
		slow slew rate mode OUT1-4_CTRL[4..7] = 0 [3]	29	—	58	µs
$T_{FAST\_TOFF\_D}$	Fast turn-off delay	from OUTx_LF signal to VOUT< VPWR/2 [4]	—	—	6.0	µs

Table 56. High-side switches dynamic characteristics...*continued*

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, T_J = −40 °C to + 150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Output turn ON and OFF time						
T_{ON_MIN}	Minimum ON time	from V_{PWR} – 2.5 V to internal logic signal turn off [5]	—	—	100	µs
T_{OFF_MIN}	Minimum OFF time	from V_{PWR} – 2.5 V to internal logic signal turn on	—	—	100	µs

[1] V_{OUT} from 2.5 V to V_{PWR} – 2.5 V, V_{PWR} = 7.0 V to 60 V, I_{OUT} = 1.4 A in steady state on resistive load
[2] From input INx to V_{OUTx} at 2.5 V, Load = 20 Ω, V_{PWR} = 28 V
[3] From input INx to V_{OUTx} at V_{PWR} – 2.5 V, Load = 20 Ω, V_{PWR} = 28 V
[4] Load = 20 Ω, VPWR = 28 V
[5] Iout > 50 mA

14.3 SPI-bus timing characteristics

Table 57. SPI-bus dynamic characteristics

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, V_{SPI} = 3.0 V to 5.5 V, T_J = −40 °C to + 150 °C; unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to VIL and VIH (see Figure 26).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI timing Input (, SCLK, MOSI)						
$F_{\_SPI\_S}$	SPI frequency STRONG conf.	[1] [2]	0	—	10	MHz
$F_{\_SPI\_M}$	SPI frequency MEDIUM conf.	[1] [2]	0	—	4	MHz
T_{SCLK}	SCLK period	[2] [3]	100	—	∞	ns
T_{LEAD}	Enable lead time	[2] [3]	100	—	—	ns
T_{LAG}	Enable lag time	[2] [3]	10	—	—	ns
T_{W_SS}	$\overline{SS}$ pulse width	[2] [3]	300	—	—	ns
T_{WH}	Clock SCLK high	[2] [3]	45	$T_{SCLK}/2$	—	ns
T_{WL}	Clock SCLK low	[2] [3]	45	$T_{SCLK}/2$	—	ns
T_{SU}	Data MOSI setup time	[2] [3]	8	—	—	ns
T_H	MOSI hold time	[2] [3]	8	—	—	ns
SPI timing output (MISO)						
T_{A_S}	Time to MISO data active	[1] [2] STRONG configuration V_SPI = 5 V ± 10 %	—	—	45	ns
T_{DIS_S}	MISO disable time	[1] [2] STRONG configuration V_SPI = 5 V ± 10 %	—	—	45	ns
T_{VSCLK_S}	Data valid after SCLK edge	[1] [2] STRONG configuration V_SPI = 5 V ± 10 %	—	—	35	ns
T_{R_S}	MISO risetime	[1] [2] STRONG configuration V_SPI = 5 V ± 10 % V_SPI = 3.3 V ± 10 %	 5 6	 — —	 16 27	ns

Table 57. SPI-bus dynamic characteristics...*continued*

Typical values are given at T_{amb} = 25 °C, V_{DD} = 5.0 V, V_{PWR} = 28 V; limit values are given at V_{DD} = 4.5 V to 5.5 V, V_{PWR} = 3.0 V to 60 V, V_{SPI} = 3.0 V to 5.5 V, T_J = −40 °C to + 150 °C; unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to VIL and VIH (see Figure 26).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{F_S}	MISO fall time	STRONG configuration [1] [2]				ns
		V_SPI = 5 V ± 10 %	5	—	16	
		V_SPI = 3.3 V ± 10 %	6	—	27	
T_{A_M}	Time to MISO data active	MEDIUM configuration [1] [2]				ns
		V_SPI = 5 V ± 10 %	—	—	65	
T_{DIS_M}	MISO disable time	MEDIUM configuration [1] [2]				ns
		V_SPI = 5 V ± 10 %	—	—	65	
T_{VSCLK_M}	Data valid after SCLK edge	MEDIUM configuration [1] [2]				ns
		V_SPI = 5 V ± 10 %	—	—	100	
T_{R_M}	MISO risetime	MEDIUM configuration [1] [2]				
		V_SPI = 5 V ± 10 %	18	—	60	ns
		V_SPI = 3.3 V ± 10 %	24	—	86	
T_{F_M}	MISO fall time	MEDIUM configuration [1] [2]				ns
		V_SPI = 5 V ± 10 %	18	—	60	
		V_SPI = 3.3 V ± 10 %	24	—	86	

[1] C_L = 50 pF
[2] Guaranteed by design
[3] Delay, rise and fall are measured to 20 % or 80 % of the respective signal

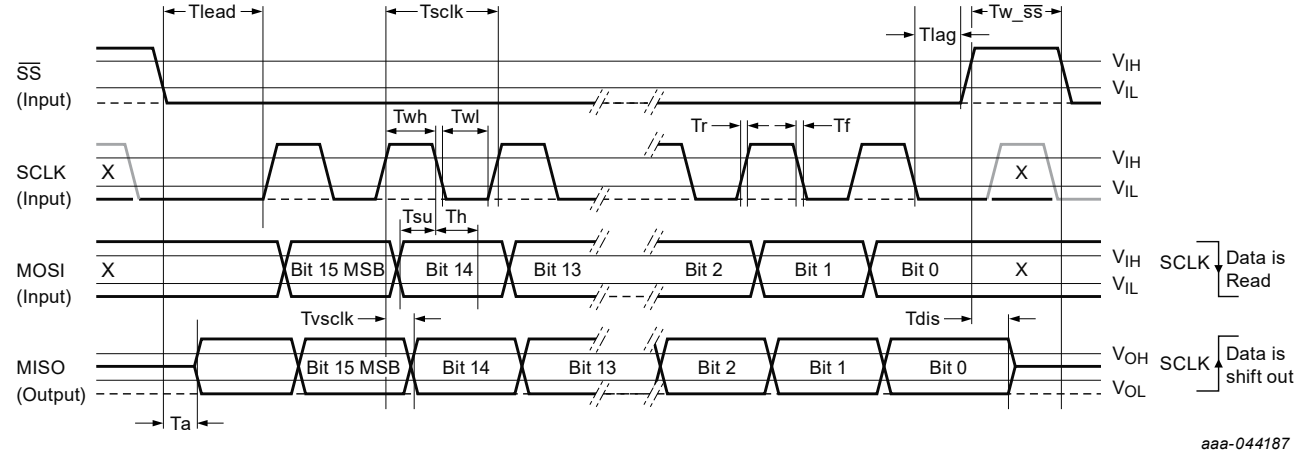
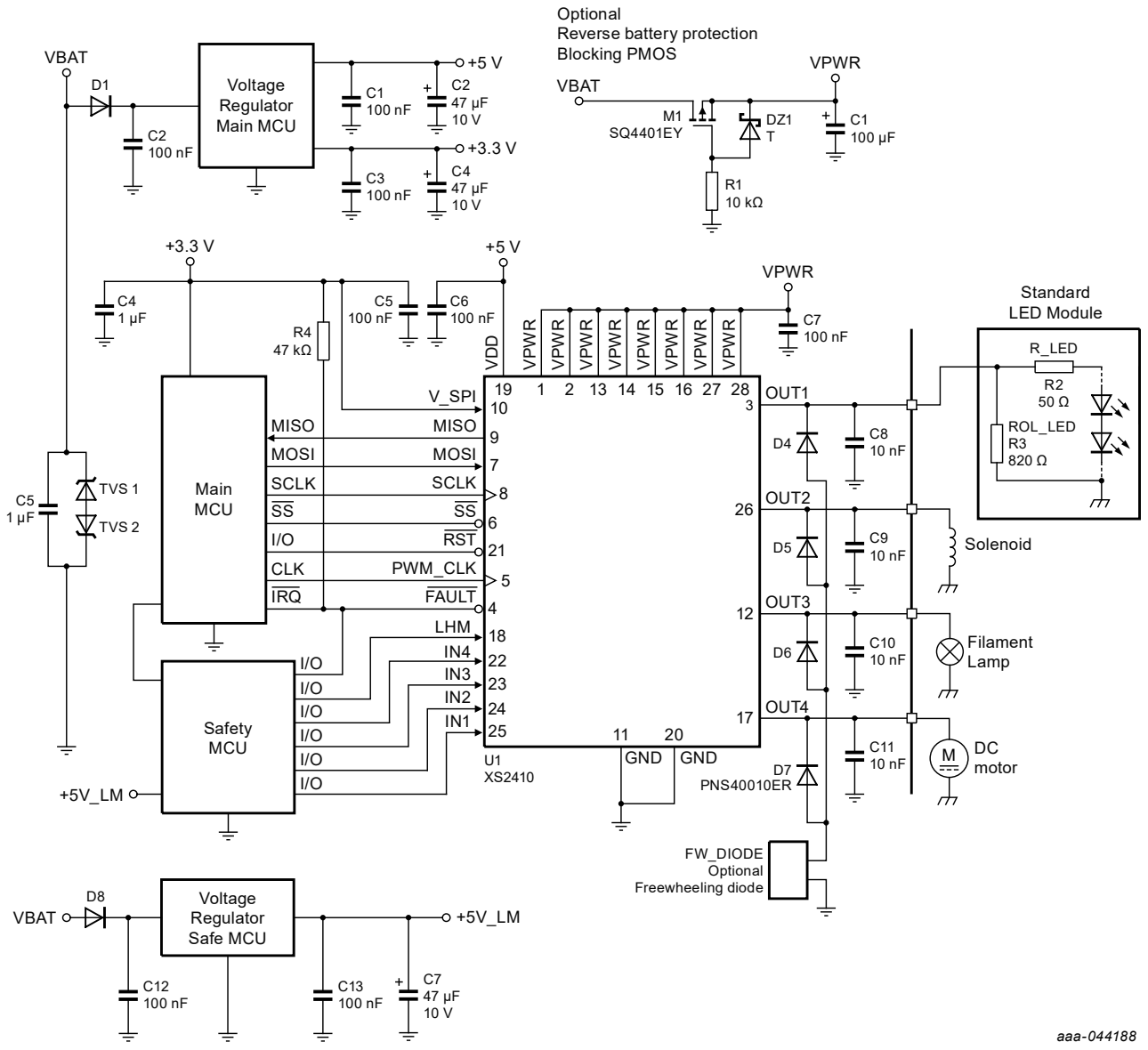


Figure 26. SPI timing diagram

15 Application information

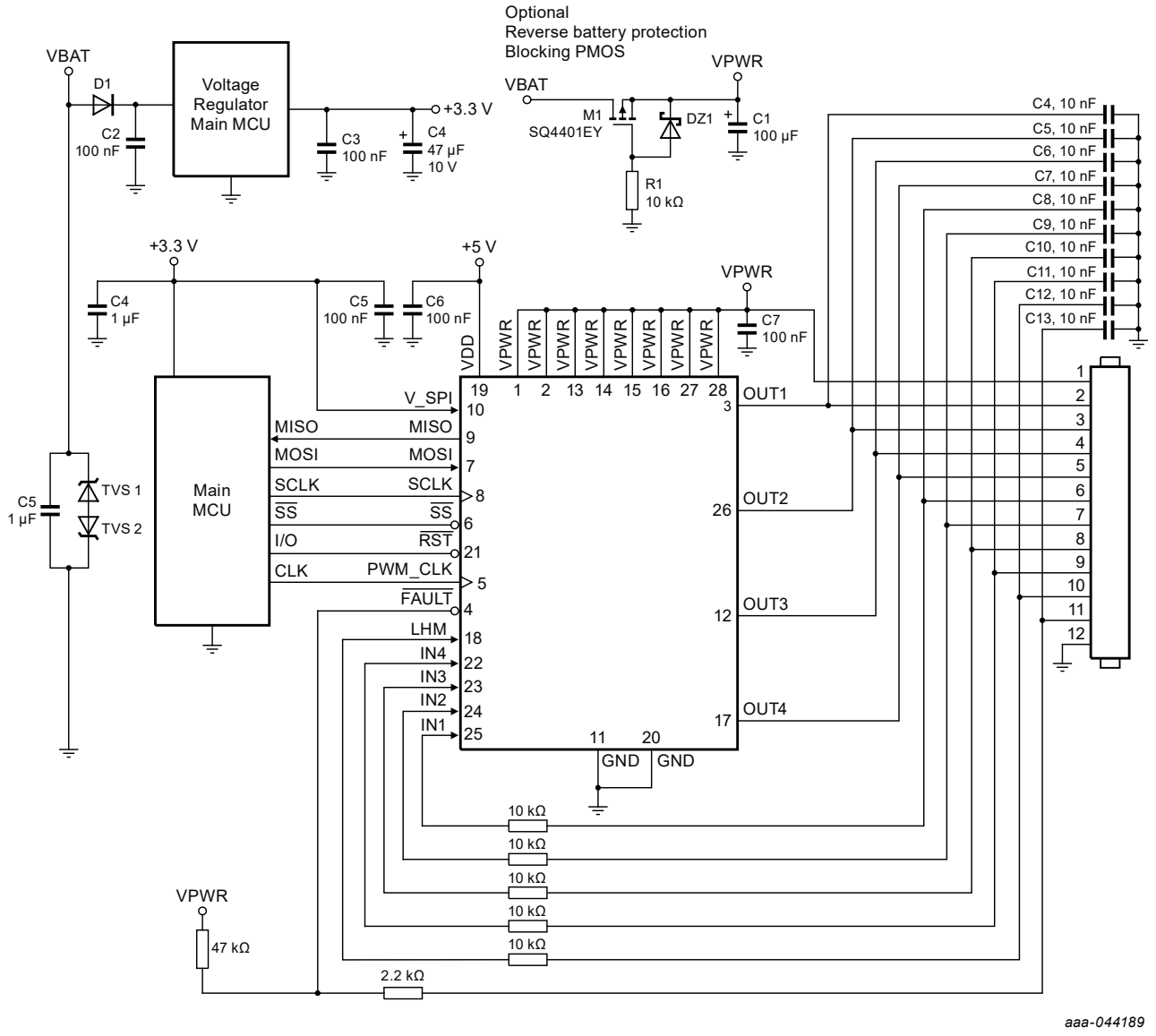


(1) C7 (VPWR): 100 nF X7R 100 V

(2) C6 (VDD), C5(V_SPI): 100 nF X7R 25 V

(3) C4 to C13 (connector): 10 nF X7R 100 V

Figure 27. Application circuit example with local safety MCU



(1) C7 (VPWR): 100 nF X7R 100 V

(2) C6 (VDD), C5(V_SPI): 100 nF X7R 25 V

(3) C4 to C13 (connector): 10 nF X7R 100 V

(4) TVS1 and TVS2 (VPWR): 60 V and 35 V unidirectional zener diodes

Figure 28. Application circuit example with external direct input control

16 Test information

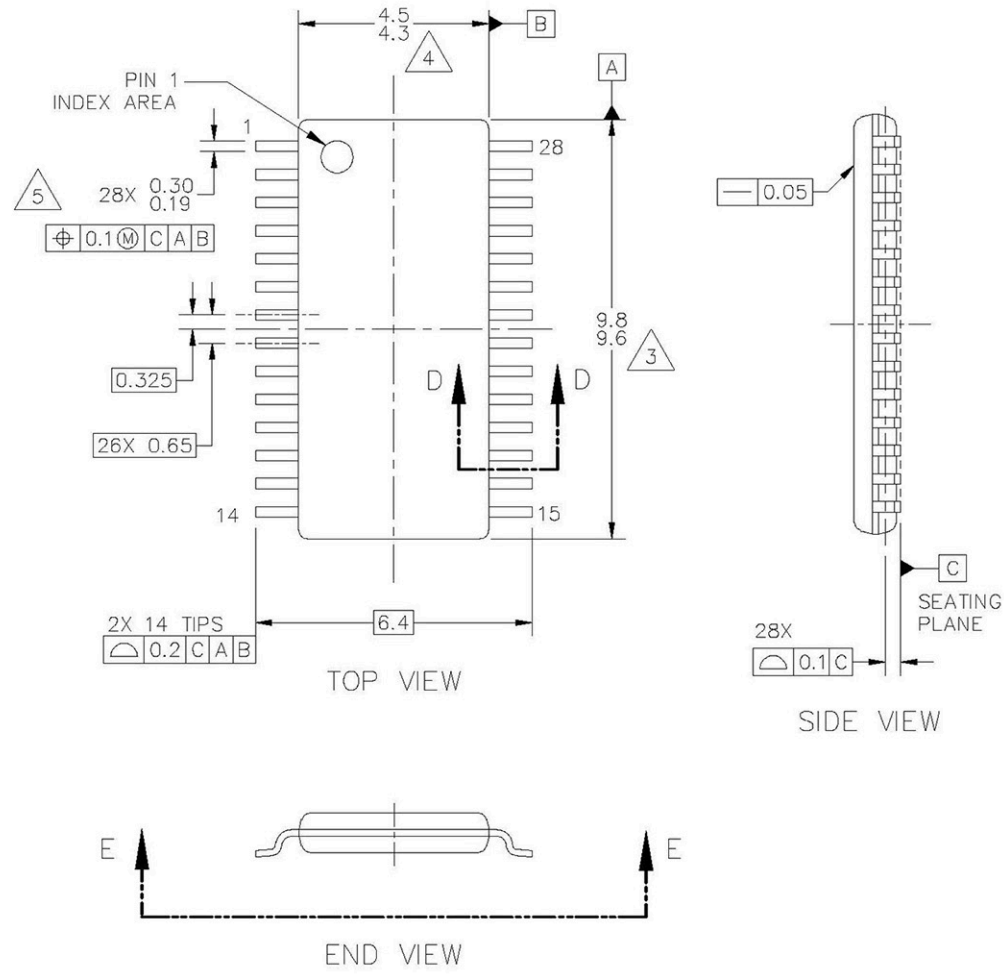
16.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - Failure mechanism based stress test qualification for integrated circuits, and is suitable for use in automotive applications.

17 Package outline

HTSSOP28: plastic thermal enhanced thin shrink small outline package; 28 leads;

Body width 4.4 mm; lead pitch 0.65 mm; exposed die pad



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	STANDARD: NON JEDEC	
	SOT1172-4	10 MAY 2017

Figure 29. Package outline SOT1172-4 (HTSSOP28)

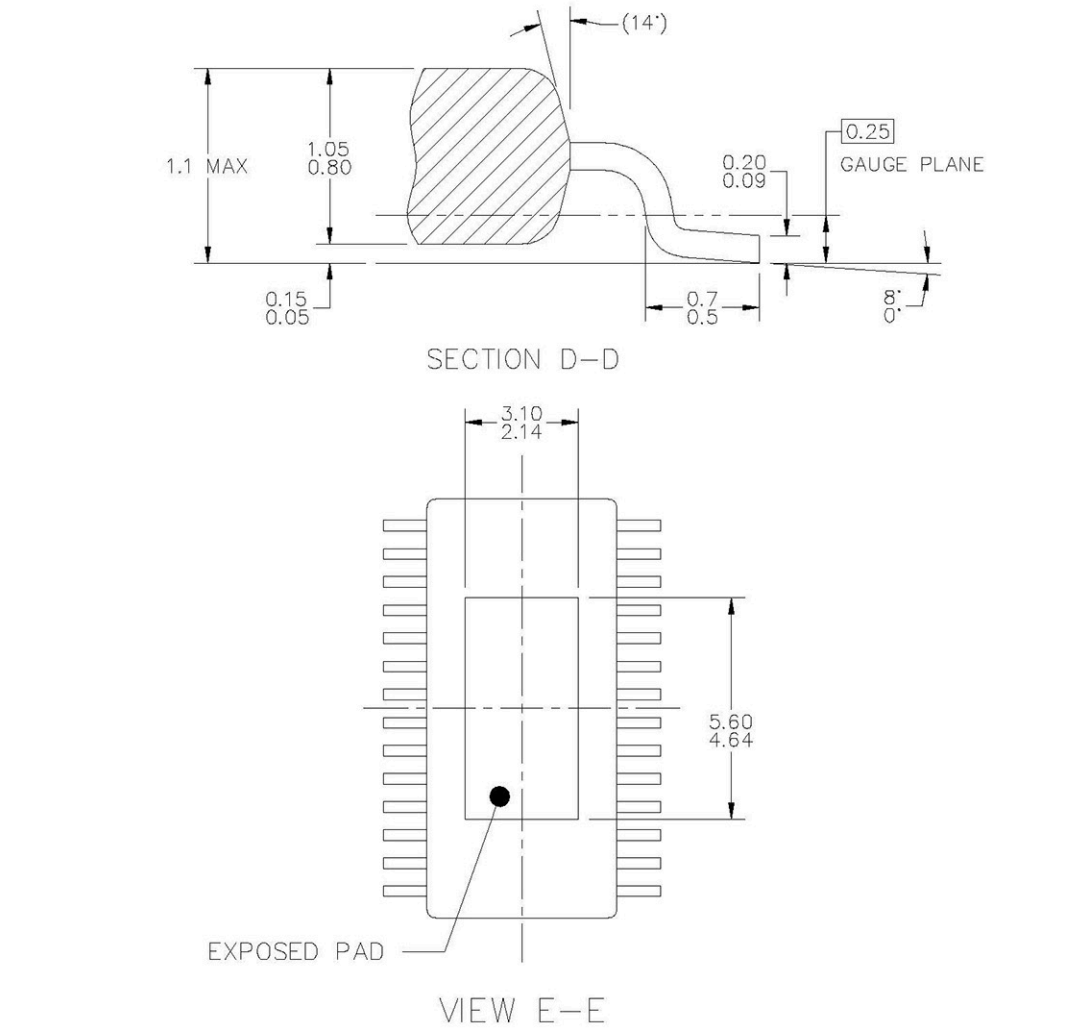

Figure 30. Package outline detail SOT1172-4 (HTSSOP28)

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 PER END.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR MOLD PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSIONS. DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.38.

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Figure 31. Package outline notes SOT1172-4 (HTSSOP28)

18 Handling information

All input and output pins are protected against Electrostatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in JESD625-A or equivalent standards.

19 Soldering of SMD packages

For in-depth account of soldering ICs, see application note AN10365 “Surface mount reflow soldering description.”

20 Soldering PCB footprints

Footprint information for reflow soldering of HTSSOP28 package.

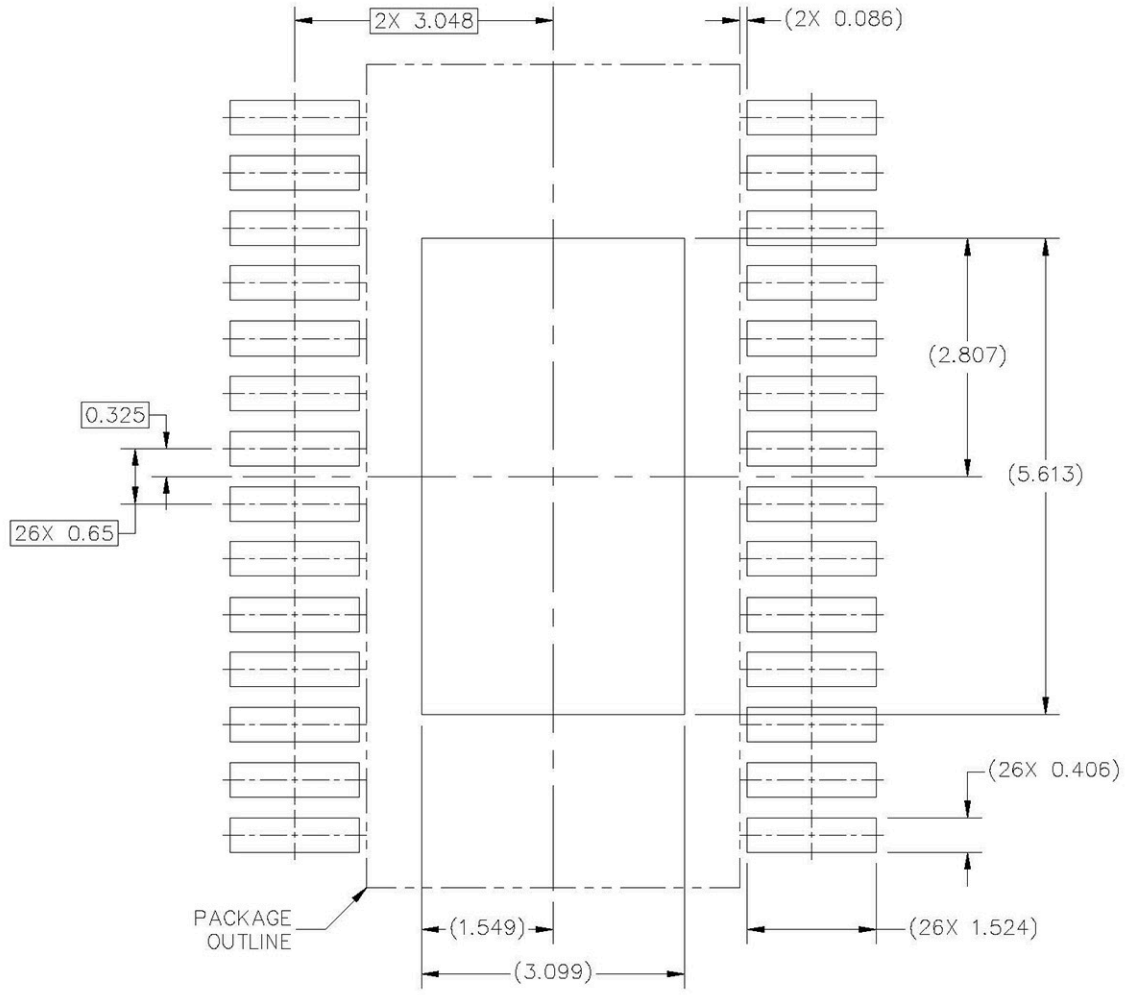

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Figure 32. PCB footprint for SOT1172-4 (HTSSOP28)

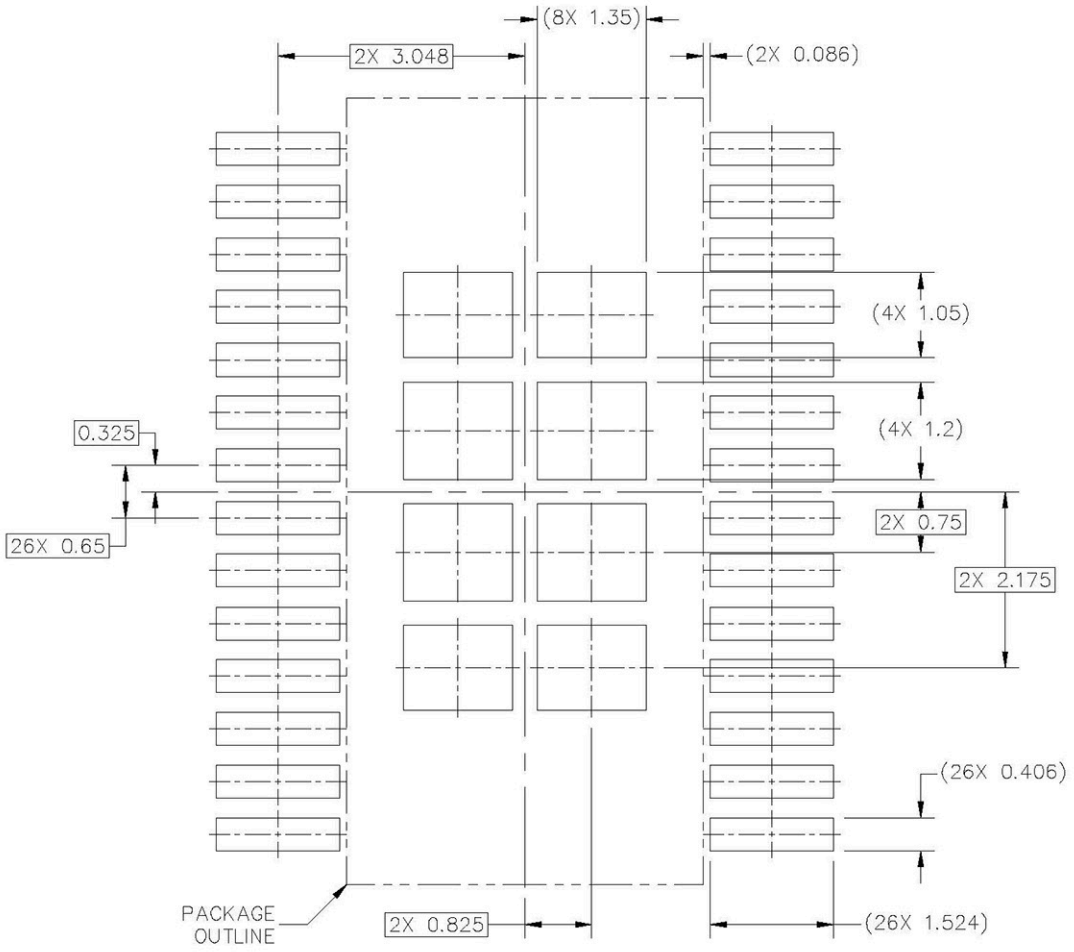

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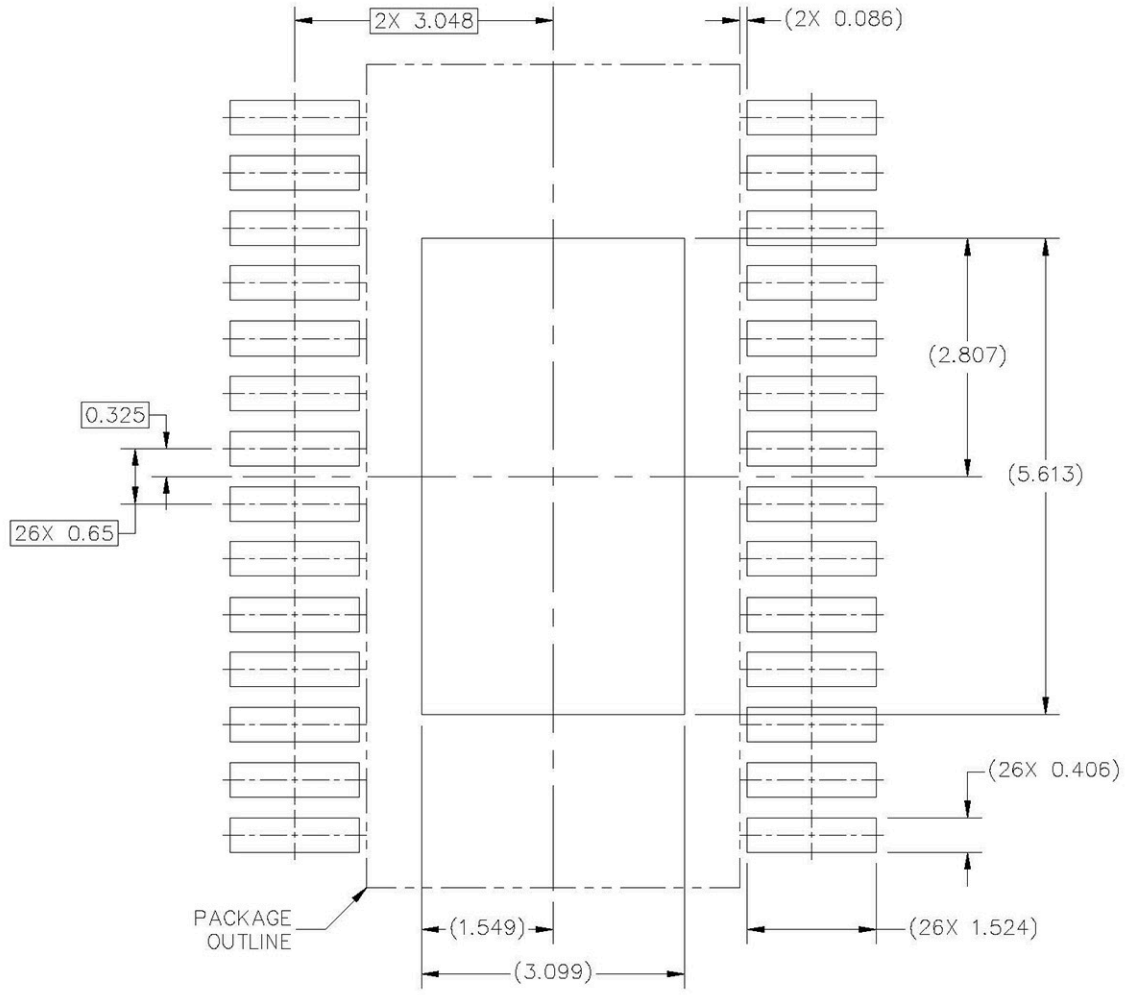
Figure 33. PCB design guidelines - solder paste stencil



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	STANDARD: NON JEDEC	
	SOT1172-4	10 MAY 2017

Figure 34. PCB design guidelines - I/O pads and solderable area

21 Abbreviations

Table 58. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
b	Binary Symbol
ECU	Electronic Control Unit: is embedded system that controls one or more of the electrical system or subsystems in a transport vehicle
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
h	Hexadecimal Symbol
I/O	Input / Output
LSB	Least Significant Bit
MSB	Most Significant Bit
NMOS	Negative-channel Metal-Oxide Semiconductor
SPI	Serial Peripheral Interface
VBAT	Battery voltage = VPWR
PCB	Printed-circuit Board
PWM	Pulse-width Modulation

22 Revision history

Table 59. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MC33XS2410 v.7	20221031	Product	—	MC33XS2410 v.6.1
Modifications	• Document status changed from objective to product			
MC33XS2410 v.6.1	20220923	Objective	—	MC33XS2410 v.6
Modifications	• Section 15: Corrected Figure 27 and Figure 28: TVS2 flipped			
MC33XS2410 v.6	20220909	Objective	—	MC33XS2410 v.5
Modifications	• Section 4: Corrected I_{VDD_STB} "Conditions" entry from 25 ℃ to Tj ≤ 85 ℃ • Section 13: Corrected I_{VPWR_STB} "Conditions" entry from V_{PWR} = 60 V, V_{OUT} = GND to V_{PWR} = 28 V, V_{OUT} = GND			
MC33XS2410 v.5	20220826	Objective	—	MC33XS2410 v.4

Table 59. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications	• Table 1: Removed second row. • Section 8.1 Corrected (4.0 V typ.) to (3.95 V typ.) in second bullet. • Section 8.3 Corrected second sentence to "Output power stage is fully floating and can swing from Vpwr + 0.3 V to -35 V versus GND or Vpwr-60 V. (voltage is limited above that range)." • Section 8.14.1: Corrected values in the following sentences: – A positive clamp inductive switching (P_CIS) circuit limits to +63.5 V typ. (VP_CIS) the voltage from VPWR to OUTx. – A negative clamp inductive switching (N_CIS) circuit limits to −37.55 V typ. (VN_CIS) the voltage from OUTx to GND. – A positive central clamp (P_CC) senses the voltage from VPWR to GND and activates four switches in order to clamp VPWR to GND at +63.5 V typ. (VP_CC). • Section 8.14.2: Corrected second sentence to read: "To prevent the device from thermal overheating because of its intrinsic body diode, the four power outputs are turned ON when GND terminal is 4.0 V higher than VPWR terminal; see Table 47." • Section 10: Corrected Min value for Symbol "V_{ESD}", Conditions, "ESD Voltage at system level on global pins (VPWRx, OUTx, LHM, INx, $\overline{FAULT}$)", from -8 to 8.0. • Section 13: – Table 45 – I_{VPWR_STB} "Conditions"entry corrected from <tbd>: VPWR = 60 V, VOUT = GND – $I_{VPWR\_OPR\_DC}$ "Conditions"entry corrected from <tbd>: Channels OFF state, VPWR = 32 V; Max. entry corrected from <tbd>: 6 – $I_{VPWR\_OPR\_ON}$: Max. entry corrected from <tbd>: 8 – $V_{SPI\_LV\_HYS}$: Typ. entry corrected from 250: 275 – Table 46 – $I_{LKG\_OUT\_0}$: Conditions corrected to: V_{PWR} = 32 V, V_{OUT} = GND T_j = 25 °C – $I_{LKG\_OUT\_32}$: Corrected T_j = 85 °C Max. from 10: 300, T_j = 150 °C Max. from 20: 300 – $I_{LKG\_OUT\_60}$: Corrected T_j = 85 °C Max. value from 20: 600; T_j = 150 °C Max value from 40: 600 – R_{S_OUT}: Inserted footnote – Table 47 – V_{N_RB}: Corrected Min. (-3.0), Typ. (-2.0), Max. (-1.0) values: -4, —, — – Table 48 – Δ_{V_COMP}: Added footnote in Conditions – Table 53 – R_{PD}: Corrected Conditions V_{PWR} > 0.9 V: V_{RST} > 0.9 V – Table 54 – : Removed I_{OL} and I_{OH} entries • Section 14.1 – Table 55 – F_{1_DEV}: Corrected Min. —, Max. —, Unit kHz: 0.735, 1.365, MHz – F_{2_DEV}: Corrected Min. —, Max. —: 1.47, 2.73 – $F_{\_MOD}$: Corrected Min. —, Max. —: 140, 260 – T_{WAKE_UP}: Corrected Max. 1.0: 10 – Table 56 – T_{TON_D}: Removed Typ. values – T_{TOFF_D}: Removed Typ. values – $T_{FAST\_TOFF\_D}$: Added Conditions footnote			
MC33XS2410 v.4	20220705	Objective	—	MC33XS2410 v.3

Table 59. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications	• Table 34: updated description for OPD_CTRL2 register – Bit 1: replaced "1 = Clear OUT3_LF bit in GLB_STA" by "1 = Clear OUT4_LF bit in GLB_STA" – Bit 0: replaced "1 = Clear OUT4_LF bit in GLB_STA by "1 = Clear OUT3_LF bit in GLB_STA" • Table 36: updated description for ACL_CTRL1 register (replaced "01 = U_Lim1 (reset)" by "01 = I_Lim1 (reset)") • Table 48: updated values for ADC error output current measurement parameter • Table 57: added note "Guaranteed by design" • Table 45: updated values for VDD, VPWR power-on reset (replaced 3.0 by 2.6) and Low-voltage hysteresis (replaced 300 by 350) • Table 47: updated values for I_{LIM1_R} • Table 56: added values for Turn-on delay and Turn-off delay • Table 57: added values for MISO risetime and MISO fall time (strong and medium configurations)			
MC33XS2410 v.3	20211112	Objective	—	MC33XS2410 v.2
MC33XS2410 v.2	20190911	Objective	—	XS2410 v.1
Modifications	• Revised content to conform with latest silicon.			
XS2410 v.1	20170707	Product preview	—	—

23 Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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