



**THE DATASHEET OF  
RMLV0408EGSA-4S2#KA1**



# RMLV0408E Series

4Mb Advanced LPSRAM (512-kword × 8-bit)

R10DS0206EJ0300  
Rev.3.00  
2021.8.18

## Description

The RMLV0408E Series is a family of 4-Mbit static RAMs organized 524,288-word × 8-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0408E Series has realized higher density, higher performance and low power consumption. The RMLV0408E Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 32-pin SOP, 32-pin TSOP (II) or 32-pin sTSOP.

## Features

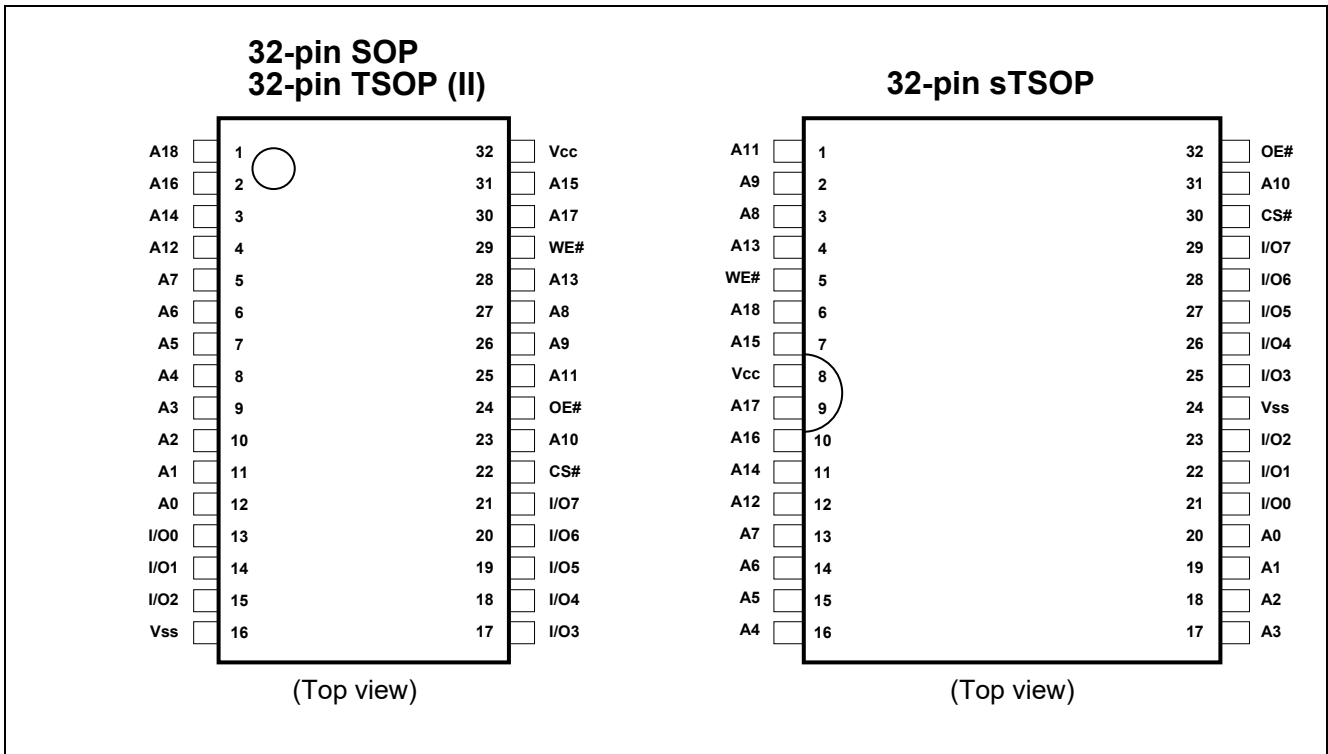
- Single 3V supply: 2.7V to 3.6V
- Access time: 45ns (max.)
- Current consumption:
  - Standby: 0.3μA (typ.)
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Battery backup operation

## Orderable part number information

Orderable part number	Access time	Temperature range	Package	Shipping container
RMLV0408EGSA-4S2#AA*	45 ns	-40 ~ +85°C	8mm×13.4mm 32-pin plastic sTSOP	Tray
RMLV0408EGSA-4S2#KA*				Embossed tape
RMLV0408EGSB-4S2#AA*			400-mil 32pin plastic TSOP (II)	Tray
RMLV0408EGSB-4S2#HA*				Embossed tape
RMLV0408EGSP-4S2#CA*			525-mil 32-pin plastic SOP	Tube
RMLV0408EGSP-4S2#HA*				Embossed tape

Note 1. \* = Revision code for Assembly site change, etc. (\* = 0, 1, etc.)

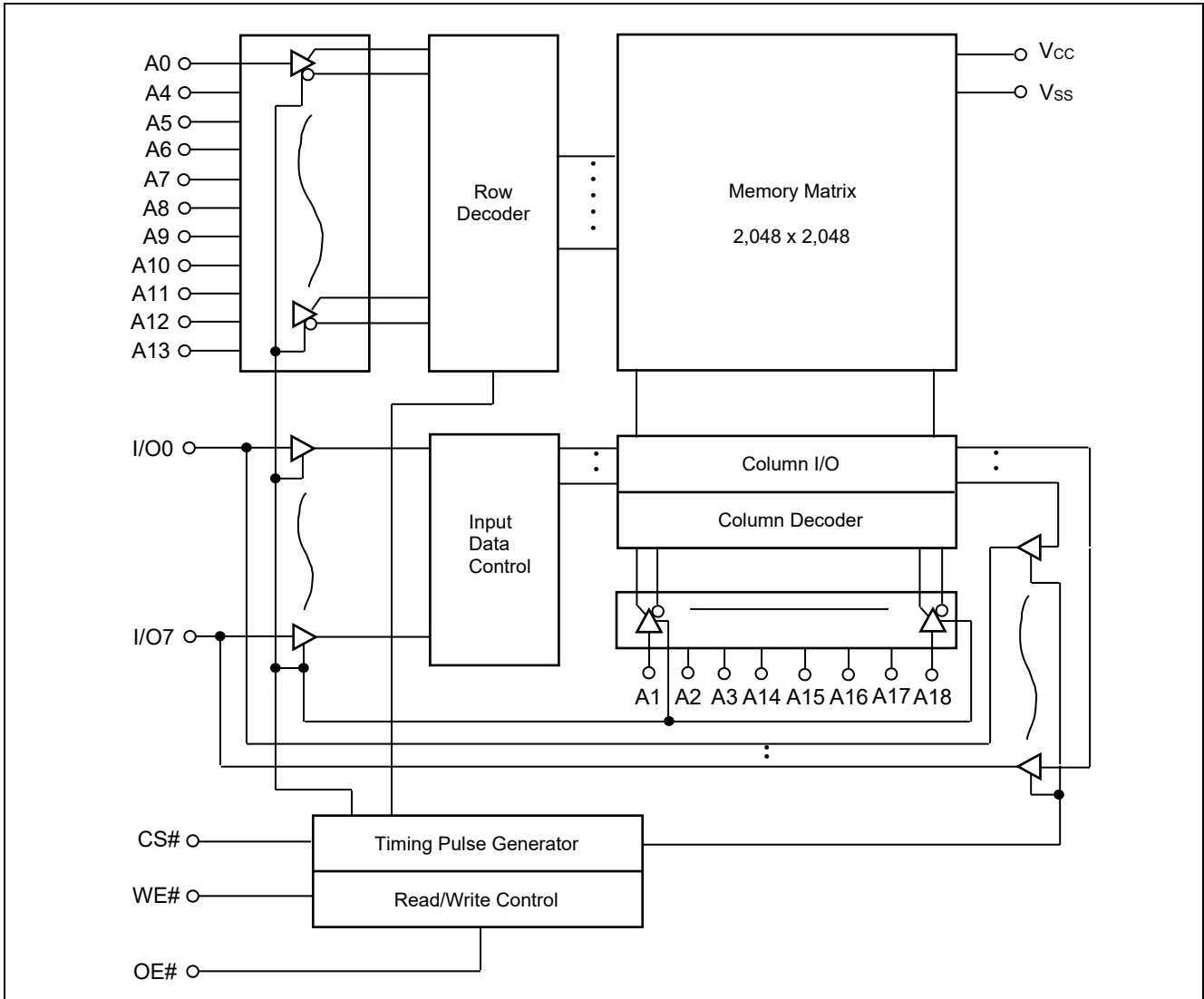
## Pin Arrangement



## Pin Description

Pin name	Function
Vcc	Power supply
Vss	Ground
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS#	Chip select
WE#	Write enable
OE#	Output enable

### Block Diagram



### Operation Table

CS#	WE#	OE#	I/O0 to I/O7	Operation
H	X	X	High-Z	Standby
L	H	L	Dout	Read
L	L	X	Din	Write
L	H	H	High-Z	Output disable

Note 2. H:  $V_{IH}$  L:  $V_{IL}$  X:  $V_{IH}$  or  $V_{IL}$

### Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 <sup>3</sup> to $V_{CC}+0.3$ <sup>4</sup>	V
Power dissipation	$P_T$	0.7	W
Operation temperature	$T_{opr}$	-40 to +85	°C
Storage temperature range	$T_{stg}$	-65 to +150	°C
Storage temperature range under bias	$T_{bias}$	-40 to +85	°C

Note 3. -3.0V for pulse  $\leq 30$ ns (full width at half maximum)

4. Maximum voltage is +4.6V.

## DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V	
	V <sub>SS</sub>	0	0	0	V	
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> +0.3	V	
Input low voltage	V <sub>IL</sub>	-0.3	—	0.6	V	5
Ambient temperature range	T <sub>a</sub>	-40	—	+85	°C	

Note 5. -3.0V for pulse ≤ 30ns (full width at half maximum)

## DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	I <sub>LI</sub>	—	—	1	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	—	—	1	μA	CS# = V <sub>IH</sub> or OE# = V <sub>IH</sub> or WE# = V <sub>IL</sub> , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Operating current	I <sub>CC</sub>	—	—	10	mA	CS# = V <sub>IL</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	
Average operating current	I <sub>CC1</sub>	—	—	20	mA	Cycle = 55ns, duty = 100%, I <sub>I/O</sub> = 0mA, CS# = V <sub>IL</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>	
		—	—	25	mA	Cycle = 45ns, duty = 100%, I <sub>I/O</sub> = 0mA, CS# = V <sub>IL</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>	
	I <sub>CC2</sub>	—	—	2.5	mA	Cycle = 1μs, duty = 100%, I <sub>I/O</sub> = 0mA, CS# ≤ 0.2V, V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V, V <sub>IL</sub> ≤ 0.2V	
Standby current	I <sub>SB</sub>	—	0.1*6	0.3	mA	CS# = V <sub>IH</sub> , Others = V <sub>SS</sub> to V <sub>CC</sub>	
Standby current	I <sub>SB1</sub>	—	0.3*6	2	μA	~+25°C	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub> , CS# ≥ V <sub>CC</sub> -0.2V
		—	—	3	μA	~+40°C	
		—	—	5	μA	~+70°C	
		—	—	7	μA	~+85°C	
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1mA	
	V <sub>OH2</sub>	V <sub>CC</sub> -0.2	—	—	V	I <sub>OH</sub> = -0.1mA	
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1mA	
	V <sub>OL2</sub>	—	—	0.2	V	I <sub>OL</sub> = 0.1mA	

Note 6. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=25°C), and not 100% tested.

## Capacitance

(V<sub>CC</sub> = 2.7V ~ 3.6V, f = 1MHz, T<sub>a</sub> = -40 ~ +85°C)

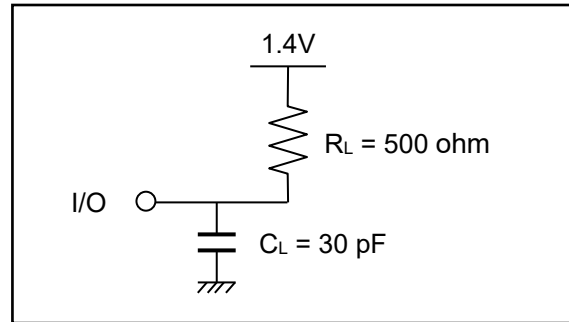
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C <sub>in</sub>	—	—	8	pF	V <sub>in</sub> = 0V	7
Input / output capacitance	C <sub>I/O</sub>	—	—	10	pF	V <sub>I/O</sub> = 0V	7

Note 7. This parameter is sampled and not 100% tested.

## AC Characteristics

Test Conditions ( $V_{CC} = 2.7V \sim 3.6V$ ,  $T_a = -40 \sim +85^{\circ}C$ )

- Input pulse levels:  $V_{IL} = 0.4V$ ,  $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



### Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	$t_{RC}$	45	—	ns	
Address access time	$t_{AA}$	—	45	ns	
Chip select access time	$t_{ACS}$	—	45	ns	
Output enable to output valid	$t_{OE}$	—	22	ns	
Output hold from address change	$t_{OH}$	10	—	ns	
Chip select to output in low-Z	$t_{CLZ}$	10	—	ns	8,9
Output enable to output in low-Z	$t_{OLZ}$	5	—	ns	8,9
Chip deselect to output in high-Z	$t_{CHZ}$	0	18	ns	8,9,10
Output disable to output in high-Z	$t_{OHZ}$	0	18	ns	8,9,10

### Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	$t_{WC}$	45	—	ns	
Address valid to write end	$t_{AW}$	35	—	ns	
Chip select to write end	$t_{CW}$	35	—	ns	
Write pulse width	$t_{WP}$	35	—	ns	11
Address setup time to write start	$t_{AS}$	0	—	ns	
Write recovery time from write end	$t_{WR}$	0	—	ns	
Data to write time overlap	$t_{DW}$	25	—	ns	
Data hold from write end	$t_{DH}$	0	—	ns	
Output enable from write end	$t_{OW}$	5	—	ns	8
Output disable to output in high-Z	$t_{OHZ}$	0	18	ns	8,10
Write to output in high-Z	$t_{WHZ}$	0	18	ns	8,10

Note 8. This parameter is sampled and not 100% tested.

9. At any given temperature and voltage condition,  $t_{CHZ}$  max is less than  $t_{CLZ}$  min, and  $t_{OHZ}$  max is less than  $t_{OLZ}$  min, for any device.

10.  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

11.  $t_{WP}$  is the interval between write start and write end.

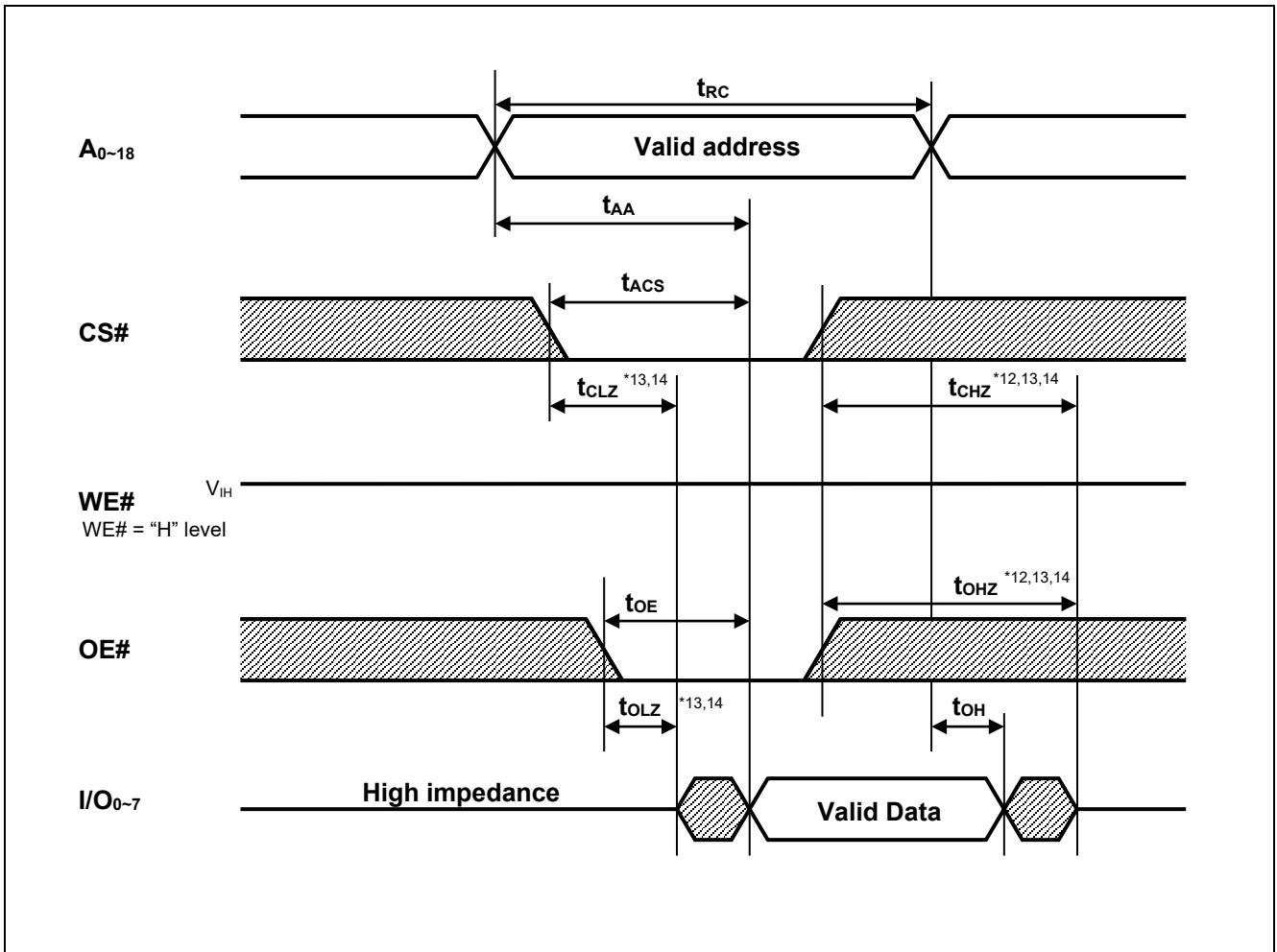
A write starts when both of CS# and WE# become active

A write is performed during the overlap of a low CS#, a low WE#

A write ends when any of CS#, WE# becomes inactive.

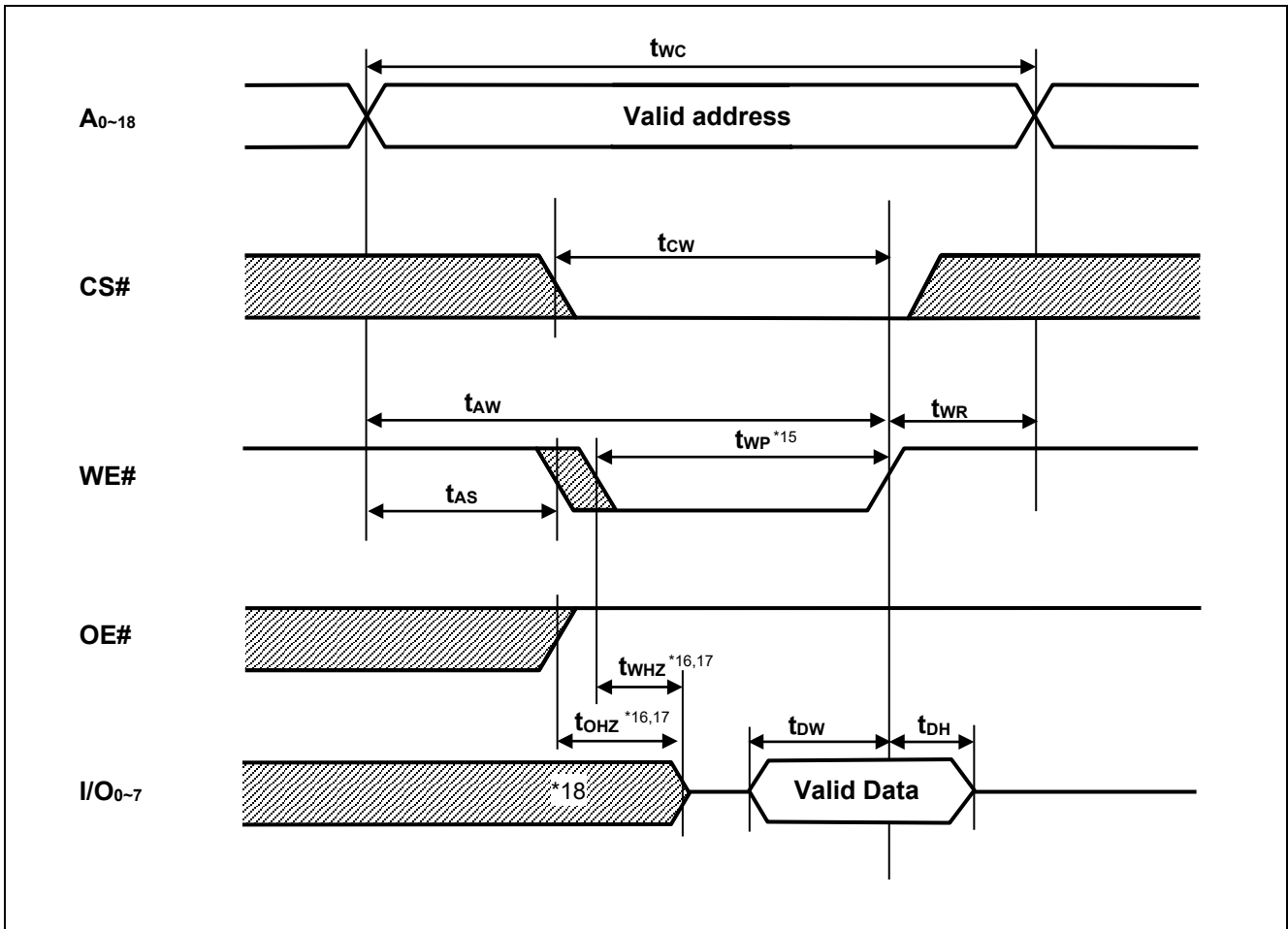
## Timing Waveforms

### Read Cycle



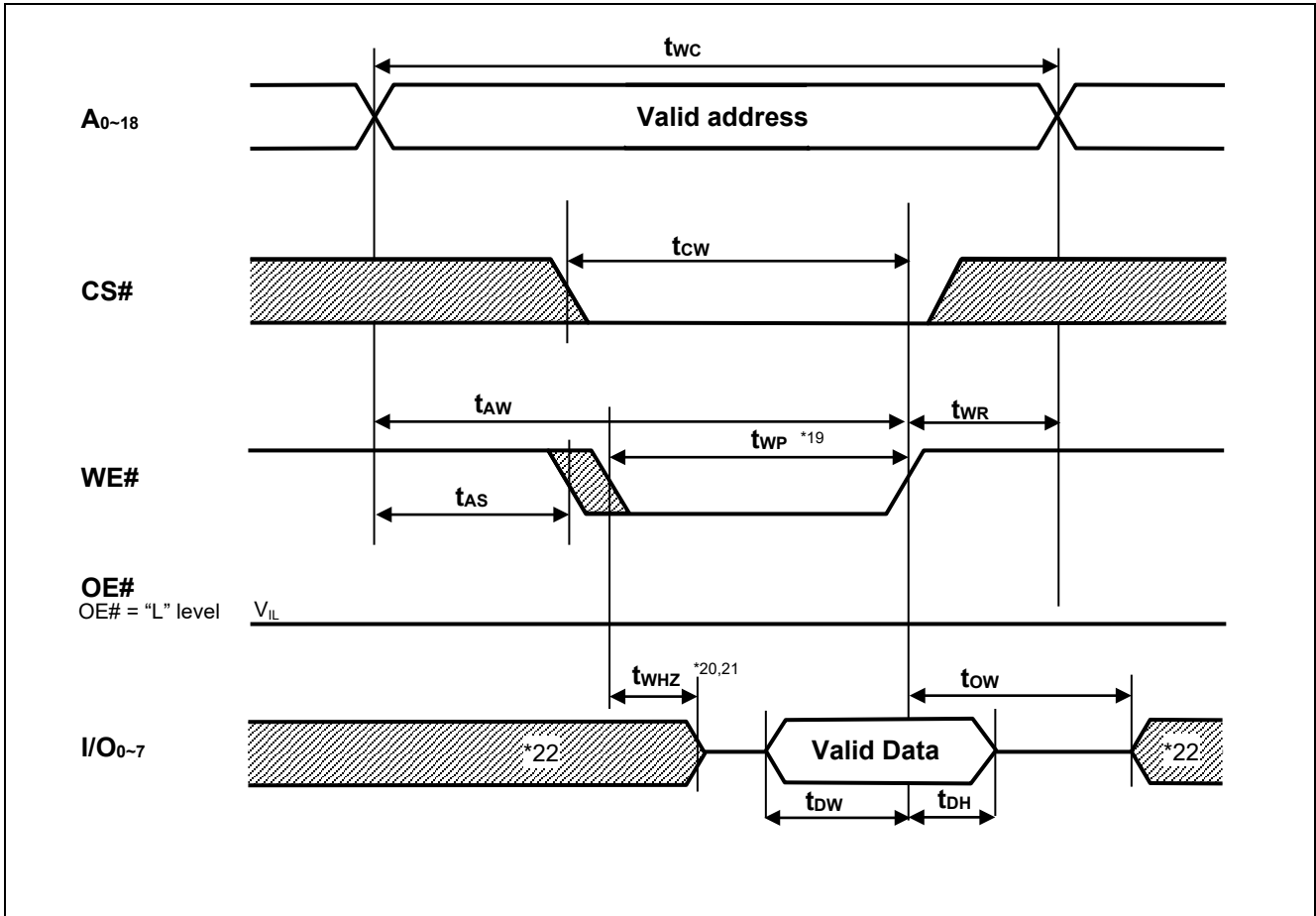
- Note 12.  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.
13. This parameter is sampled and not 100% tested.
14. At any given temperature and voltage condition,  $t_{CHZ}$  max is less than  $t_{CLZ}$  min, and  $t_{OHZ}$  max is less than  $t_{OLZ}$  min, for any device.

Write Cycle (1) (WE# CLOCK, OE#="H" while writing)



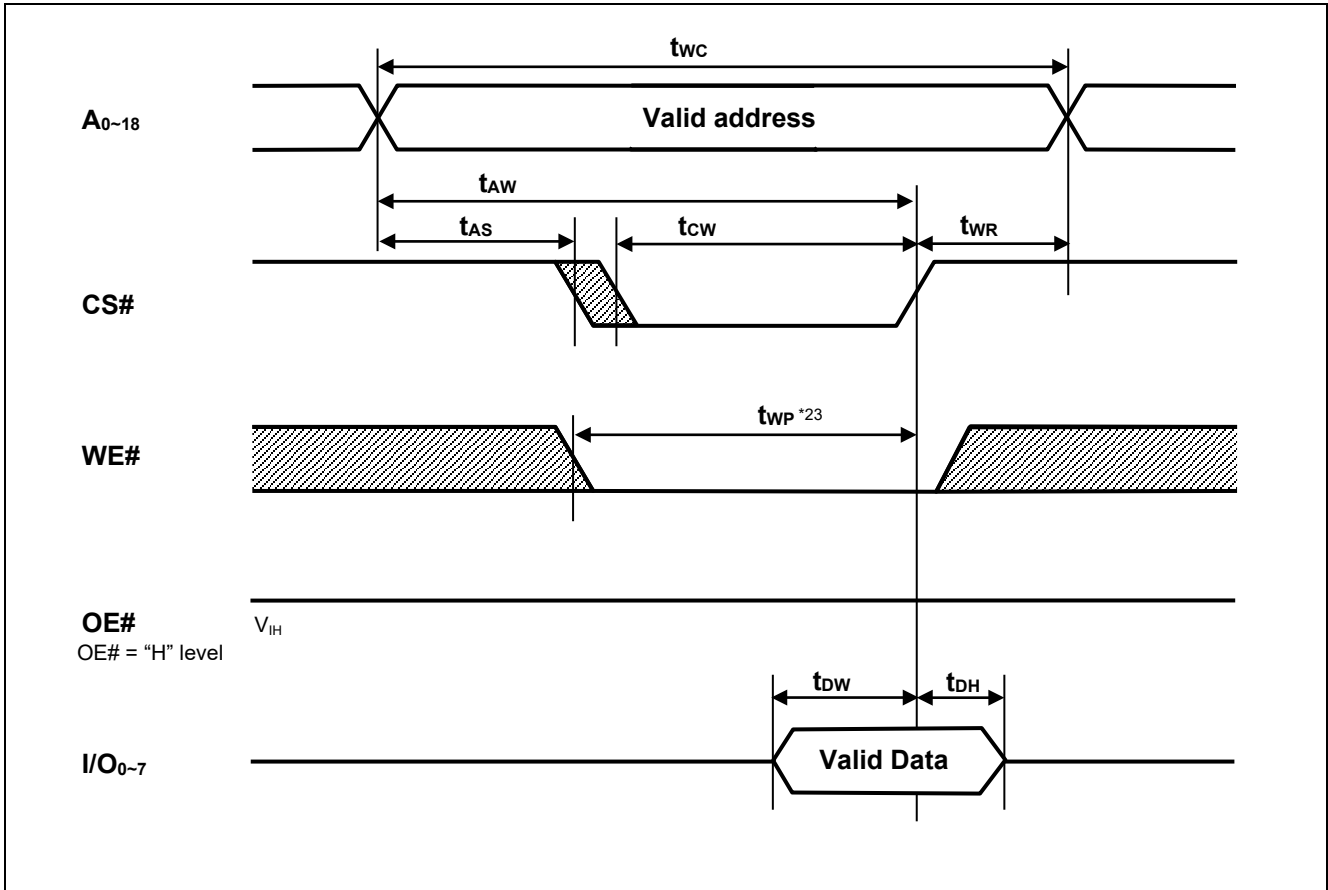
- Note 15.  $t_{wp}$  is the interval between write start and write end.  
 A write starts when both of CS# and WE# become active.  
 A write is performed during the overlap of a low CS# and a low WE#.  
 A write ends when any of CS# or WE# becomes inactive.
16.  $t_{ohz}$  and  $t_{whz}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.
17. This parameter is sampled and not 100% tested.
18. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.

Write Cycle (2) (WE# CLOCK, OE# Low Fixed)



- Note 19.  $t_{WP}$  is the interval between write start and write end.  
 A write starts when both of CS# and WE# become active.  
 A write is performed during the overlap of a low CS# and a low WE#.  
 A write ends when any of CS# or WE# becomes inactive.
20.  $t_{WHZ}$  is defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.
21. This parameter is sampled and not 100% tested.
22. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.

Write Cycle (3) (CS# CLOCK)



Note 23.  $t_{WP}$  is the interval between write start and write end.  
 A write starts when both of CS# and WE# become active.  
 A write is performed during the overlap of a low CS# and a low WE#.  
 A write ends when any of CS# or WE# becomes inactive.

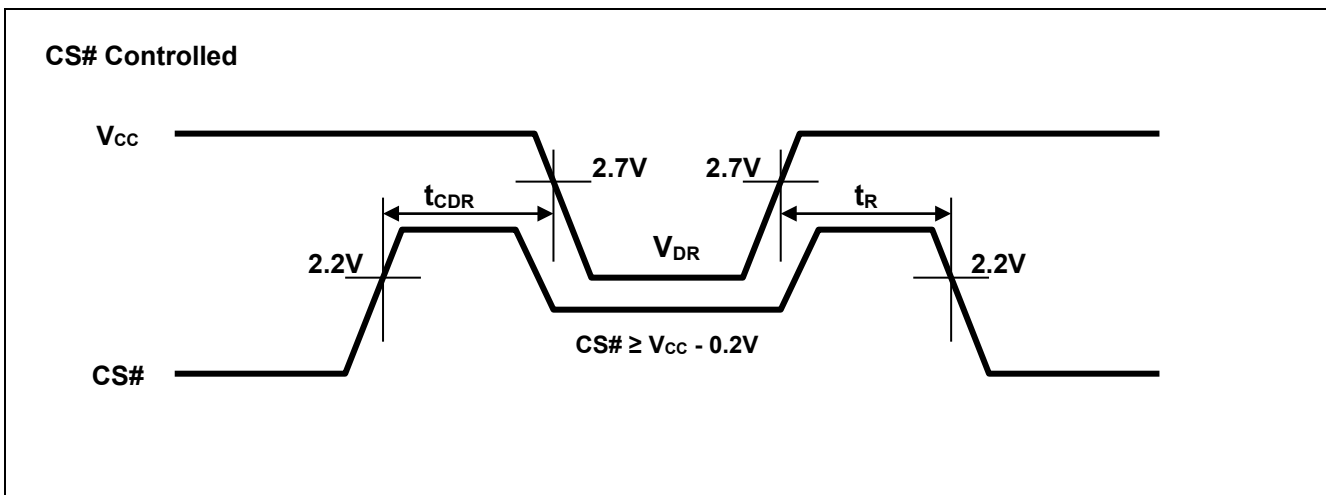
Low V<sub>CC</sub> Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions <sup>*25</sup>	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	1.5	—	—	V	V <sub>in</sub> ≥ 0V, CS# ≥ V <sub>CC</sub> -0.2V	
Data retention current	I <sub>CCDR</sub>	—	0.3 <sup>*24</sup>	2	μA	~+25°C	V <sub>CC</sub> =3.0V, V <sub>in</sub> ≥ 0V, CS# ≥ V <sub>CC</sub> -0.2V
		—	—	3	μA	~+40°C	
		—	—	5	μA	~+70°C	
		—	—	7	μA	~+85°C	
Chip deselect time to data retention	t <sub>CDR</sub>	0	—	—	ns	See retention waveform.	
Operation recovery time	t <sub>R</sub>	5	—	—	ms		

Note 24. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=25°C), and not 100% tested.

25. CS# controls address buffer, WE# buffer, OE# buffer, and I/O buffer. If CS# controls data retention mode, V<sub>in</sub> levels (address, WE#, OE#, I/O) can be in the high-impedance state.

Low V<sub>CC</sub> Data Retention Timing Waveforms (CS# controlled)



Revision History	RMLV0408E Series Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2014.2.27	—	First edition issued
2.00	2016.1.12	1	Changed section from “Part Name Information” to “Orderable part number information”
2.01	2020.2.20	Last page	Updated the Notice to the latest version
3.00	2021.8.18	1,4,10	Changed the typical value of $I_{SB1}$ and $I_{CCDR}$ from $0.4\mu A$ to $0.3\mu A$ . Revised orderable part number information

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information



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