THE DATASHEET OF

1337AGDCGI8

win-source.net 0086-755-83957316

REAL-TIME CLOCK WITH I^{2}C SERIAL INTERFACE IDT1337AG

General Description

The IDT1337AG device is a low-power serial real-time clock (RTC) device with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I^{2}C bus. The device provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

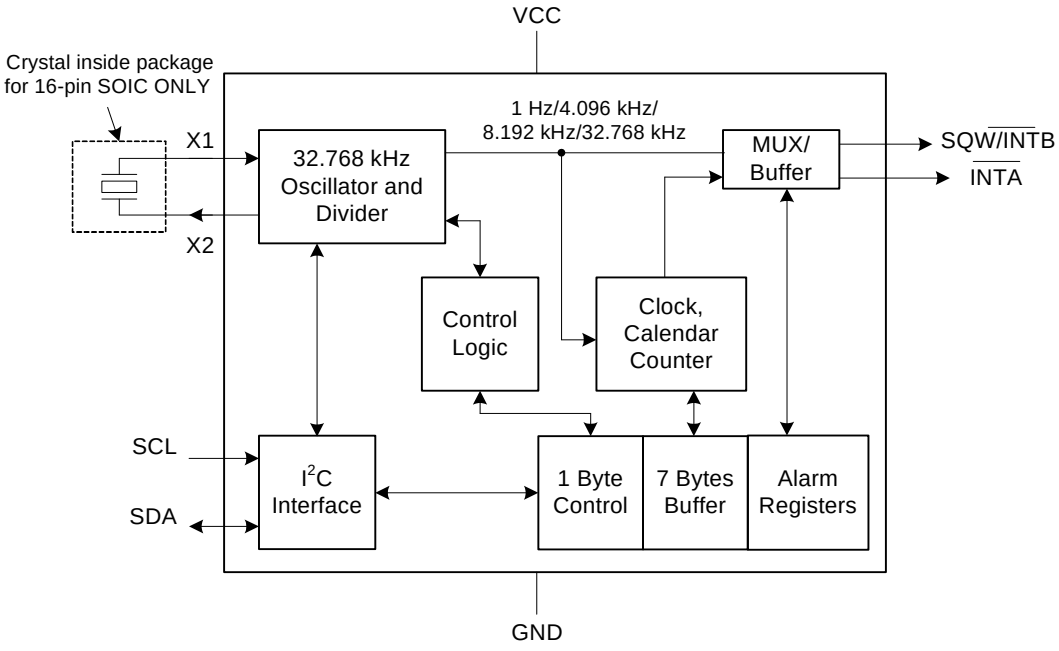
Applications

- Telecommunication (Routers, Switches, Servers)
- Handhelds (GPS, POS terminals, MP3 players)
- Set-Top Box, Digital Recording,
- Office (Fax/Printers, Copiers)
- Medical (Glucometer, Medicine Dispensers)
- Other (Thermostats, Vending Machines, Modems, Utility Meters, Digital Photo Frame devices)

Features

- Real-Time Clock (RTC) counts seconds, minutes, hours, day, date, month, and year with leap-year compensation valid up to 2100
- Packaged in 8-pin MSOP, 8-pin SOIC, or 16-pin SOIC (surface-mount package with an integrated crystal)
- I^{2}C serial interface (Normal and Fast modes)
- Two time-of-day alarms
- Oscillator stop flag
- Programmable square-wave output defaults to 32kHz on power-up
- Operating voltage of 1.8 to 5.5V
- Industrial temperature range (-40 to +85°C)

Block Diagram



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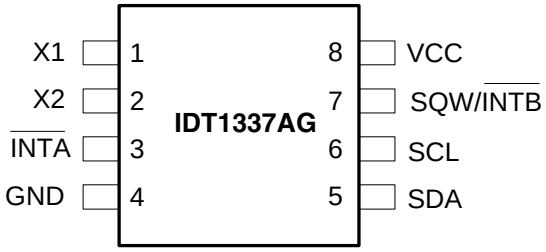
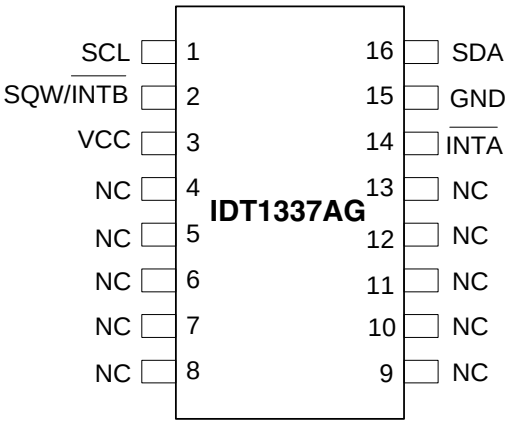
Pin Assignment (8-pin MSOP/SOIC)



Pin Assignment (16-pin SOIC)



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Pin Descriptions

Pin Number		Pin Name	Pin Description/Function
MSOP	SOIC		
1	—	X1	Connections for standard 32.768 kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 7 pF. An external 32.768 kHz oscillator can also drive the IDT1337AG. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left floating.
2	—	X2	
3	14	$\overline{\text{INTA}}$	Interrupt output. When enabled, $\overline{\text{INTA}}$ is asserted low when the time/day/date matches the values set in the alarm registers. This pin is an open-drain output and requires an external pull-up resistor (10 kΩ typical).
4	15	GND	Connect to ground. DC power is provided to the device on these pins.
5	16	SDA	Serial data input/output. SDA is the input/output pin for the I^{2}C serial interface. The SDA pin is an open-drain output and requires an external pull-up resistor (2 kΩ typical).
6	1	SCL	Serial clock input. SCL is used to synchronize data movement on the serial interface. The SCL pin is an open-drain output and requires an external pull-up resistor (2 kΩ typical).
7	2	SQW/$\overline{\text{INTB}}$	Square-Wave/Interrupt output. Programmable square-wave or interrupt output signal. The SQW/$\overline{\text{INT}}$ pin is an open-drain output and requires an external pull-up resistor (10 kΩ typical). This pin can also function as an additional interrupt pin under certain conditions (see page 6 for details).
8	3	VCC	Primary power supply. DC power is applied to this pin.
—	4 - 13	NC	No connect. These pins are unused and must be connected to ground.

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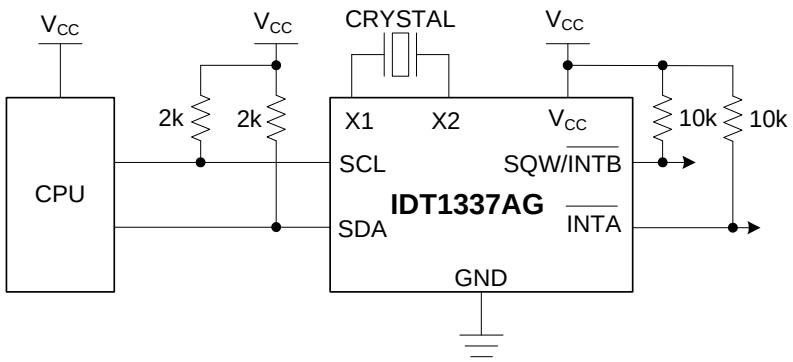
Typical Operating Circuit



Detailed Description

Communications to and from the IDT1337AG occur serially over an I2C bus. The IDT1337AG operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible through the I2C interface whenever VCC is between 5.5 V and 1.8 V. I2C operation is not guaranteed when VCC is below 1.8 V. The IDT1337AG maintains the time and date when VCC is as low as 1.3 V.

The following sections discuss in detail the Oscillator block, Clock/Calendar Register Block and Serial I2C block.

Oscillator Block

Selection of the right crystal, correct load capacitance and careful PCB layout are important for a stable crystal oscillator. Due to the optimization for the lowest possible current in the design for these oscillators, losses caused by parasitic currents can have a significant impact on the overall oscillator performance. Extra care needs to be taken to maintain a certain quality and cleanliness of the PCB.

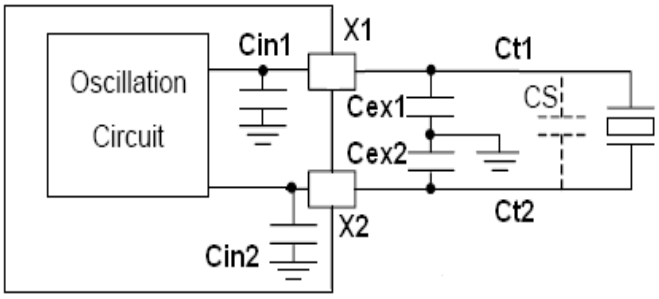
Crystal Selection

The key parameters when selecting a 32 kHz crystal to work with IDT1337AG RTC are:

- Recommended Load Capacitance
- Crystal Effective Series Resistance (ESR)
- Frequency Tolerance

Effective Load Capacitance

Please see diagram below for effective load capacitance calculation. The effective load capacitance (CL) should match the recommended load capacitance of the crystal in order for the crystal to oscillate at its specified parallel resonant frequency with 0ppm frequency error.



$$CL = CS + ((CX1 * CX2) / (CX1+CX2))$$
$$CX1 = (Cin1+Cex1+Ct1)$$
$$CX2 = (Cin2+Cex2+Ct2)$$

In the above figure, X1 and X2 are the crystal pins of our device. Cin1 and Cin2 are the internal capacitors which include the X1 and X2 pin capacitance. Cex1 and Cex2 are the external capacitors that are needed to tune the crystal frequency. Ct1 and Ct2 are the PCB trace capacitances between the crystal and the device pins. CS is the shunt capacitance of the crystal (as specified in the crystal manufacturer's datasheet or measured using a network analyzer).

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Note: IDT1337AGCSRI integrates a standard 32.768 kHz crystal in the package and contributes an additional frequency error of 10ppm at nominal V_{CC} (+3.3 V) and T_A=+25°C.

ESR (Effective Series Resistance)

Choose the crystal with lower ESR. A low ESR helps the crystal to start up and stabilize to the correct output frequency faster compared to high ESR crystals.

Frequency Tolerance

The frequency tolerance for 32 kHz crystals should be specified at nominal temperature (+25°C) on the crystal manufacturer datasheet. The crystals used with IDT1337AG typically have a frequency tolerance of +/-20ppm at +25°C.

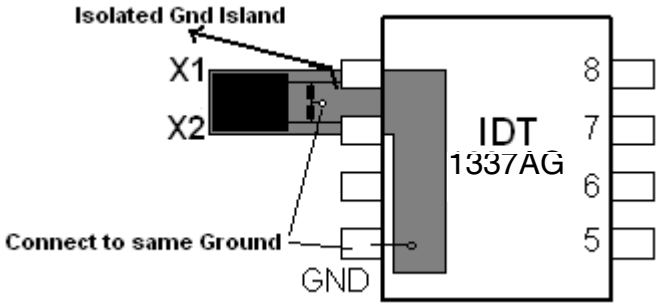
Specifications for a typical 32 kHz crystal used with our device are shown in the table below.

Parameter	Symbol	Min	Typ	Max	Units
Nominal Freq.	f_O		32.768		kHz
Series Resistance	ESR			80	kΩ
Load Capacitance	C_L		7		pF

PCB Design Consideration

- Signal traces between IDT device pins and the crystal must be kept as short as possible. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI. Note that the trace capacitances play a role in the effective crystal load capacitance calculation.
- Data lines and frequently switching signal lines should be routed as far away from the crystal connections as possible. Crosstalk from these signals may disturb the oscillator signal.
- Reduce the parasitic capacitance between X1 and X2 signals by routing them as far apart as possible.
- The oscillation loop current flows between the crystal and the load capacitors. This signal path (crystal to CL1 to CL2 to crystal) should be kept as short as possible and ideally be symmetric. The ground connections for both capacitors should be as close together as possible. Never route the ground connection between the capacitors all around the crystal, because this long ground trace is sensitive to crosstalk and EMI.
- To reduce the radiation / coupling from oscillator circuit, an isolated ground island on the GND layer could be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections for the load capacitors and the oscillator should be connected to this island.

PCB Layout



PCB Assembly, Soldering and Cleaning

Board-assembly production process and assembly quality can affect the performance of the 32kHz oscillator. Depending on the flux material used, the soldering process can leave critical residues on the PCB surface. High humidity and fast temperature cycles that cause humidity condensation on the printed circuit board can create process residuals. These process residuals cause the insulation of the sensitive oscillator signal lines towards each other and neighboring signals on the PCB to decrease. High humidity can lead to moisture condensation on the surface of the PCB and, together with process residuals, reduce the surface resistivity of the board. Flux residuals on the board can cause leakage current paths, especially in humid environments. Thorough PCB cleaning is therefore highly recommended in order to achieve maximum performance by removing flux residuals from the board after assembly. In general, reduction of losses in the oscillator circuit leads to better safety margin and reliability.

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Address Map

Table 2 (Timekeeper Registers) shows the address map for the IDT1337AG registers. During a multibyte access, when the address pointer reaches the end of the register space (0Fh), it wraps around to location 00h. On an I^{2}C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 1. Timekeeper Registers

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range
00h	0	10 seconds			Seconds				Seconds	00 - 59
01h	0	10 minutes			Minutes				Minutes	00 - 59
02h	0	12/$\overline{24}$	$\overline{AM}$/PM 10 hour	10 hour	Hour				Hours	1 - 12 + AM/PM 00 - 23
03h	0	0	0	0	0	Day			Day	1 - 7
04h	0	0	10 date		Date				Date	01 - 31
05h	Century	0	0	10 month	Month				Month/Century	01 - 12 + Century
06h	10 year				Year				Year	00 - 99
07h	A1M1	10 seconds			Seconds				Alarm 1 Seconds	00 - 59
08h	A1M2	10 minutes			Minutes				Alarm 1 Minutes	00 - 59
09h	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 10 hour	10 hour	Hour				Alarm 1 Hours	1 - 12 + AM/PM 00 - 23
0Ah	A1M4	DY/$\overline{DT}$	10 date		Day,				Alarm 1 Day	1 - 7
					Date				Alarm 1 Date	1 - 31
0Bh	A2M2	10 minutes			Minutes				Alarm 2 Minutes	00 - 59
0Ch	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 10 hour	10 hour	Hour				Alarm 2 Hours	1 - 12 + AM/PM 00 - 23
0Dh	A2M4	DY/$\overline{DT}$	10 date		Day,				Alarm 2 Day	1 - 7
					Date				Alarm 2 Date	1 - 31
0Eh	$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE	Control	
0Fh	OSF	0	0	0	0	0	A2F	A1F	Status	

Note: Unless otherwise specified, the state of the registers are not defined when power is first applied or when VCC falls below the V_{CCT} min

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Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers are illustrated in Table 1. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enable, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

The IDT1337AG can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{\text{AM}}$/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). All hours values, including the alarms, must be reinitialized whenever the 12/$\overline{\text{24}}$-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99–00.

Alarms

The IDT1337AG contains two time of day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the INTCN bits of the Control Register) to operate in two different modes—each alarm can drive its own separate interrupt output or both alarms can drive a common interrupt output. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 1). When all of the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h–06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 (Alarm Mask Bits table) shows the possible settings. Configurations not listed in the table result in illogical operation

The DY/$\overline{\text{DT}}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/$\overline{\text{DT}}$ is written to a logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{\text{DT}}$ is written to a logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding Alarm Flag (‘A1F’ or ‘A2F’) bit is set to logic 1. If the corresponding Alarm Interrupt Enable (‘A1IE’ or ‘A2IE’) is also set to logic 1, the alarm condition activates one of the interrupt output ($\overline{\text{INTA}}$ or SQW/$\overline{\text{INTB}}$) signals. The match is tested on the once-per-second update of the time and date registers.

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Table 2. Alarm Mask Bits

DY/$\overline{DT}$	Alarm 1 Register Mask Bits (Bit 7)				Alarm Rate
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second.
X	1	1	1	0	Alarm when seconds match.
X	1	1	0	0	Alarm when minutes and seconds match.
X	1	0	0	0	Alarm when hours, minutes, and seconds match.
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match.
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match.
DY/$\overline{DT}$	Alarm 2 Register Mask Bits (Bit 7)				Alarm Rate
	A2M4	A2M3	A2M2		
X	1	1	1		Alarm once per minute (00 seconds of every minute).
X	1	1	0		Alarm when minutes match.
X	1	0	0		Alarm when hours and minutes match.
0	0	0	0		Alarm when date, hours, and minutes match.
1	0	0	0		Alarm when day, hours, and minutes match.

Special-Purpose Registers

The IDT1337AG has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

Control Register (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{EOSC}$	0	0	RS2	RS1	INTCN	A2IE	A1IE

Bit 7: Enable Oscillator ($\overline{EOSC}$). This active-low bit when set to logic 0 starts the oscillator. When this bit is set to a logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. Table 3 shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32 kHz) when power is first applied.

Table 3. SQW/$\overline{INT}$ Output

INTCN	RS2	RS1	SQW/$\overline{INTB}$ Output	A2IE
0	0	0	1 Hz	X
0	0	1	4.096 kHz	X
0	1	0	8.192 kHz	X
0	1	1	32.768 kHz	X
1	X	X	$\overline{A2F}$	1

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Bit 2: Interrupt Control (INTCN). This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 registers activate the $\overline{\text{INTA}}$ pin (provided that the alarm is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/$\overline{\text{INTB}}$ pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{\text{INTB}}$ pin.This bit is set to logic 0 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to a logic 1, this bit permits the Alarm 2 Flag (A2F) bit in the status register to assert $\overline{\text{INTA}}$ (when INTCN = 0) or to assert SQW/$\overline{\text{INTB}}$ (when INTCN = 1). When the A2IE bit is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the Alarm 1 Flag (A1F) bit in the status register to assert $\overline{\text{INTA}}$. When the A1IE bit is set to logic 0, the A1F bit does not initiate the $\overline{\text{INTA}}$ signal. The A1IE bit is disabled (logic 0) when power is first applied.

Table 4. Alarm/Interrupt Table

Bit 2	Bit 1	Bit 0				
INTCN	**A2IE**	**A1IE**	**Alarm 1**	**Alarm 2**	**$\overline{\text{INTA}}$**	**$\overline{\text{INTB}}$/SQW**
0	0	0	None	None	Hi	SQW
0	0	1	INTA	None	Alarm 1	SQW
0	1	0	None	INTA	Alarm 2	SQW
0	1	1	INTA	INTA	Alarm 1 or Alarm 2	SQW
1	0	0	None	None	Hi	Hi
1	0	1	INTA	None	Alarm 1	Hi
1	1	0	None	INTB	Hi	Alarm 2
1	1	1	INTA	INTB	Alarm 1	Alarm 2

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Status Register (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and calendar data. This bit is set to logic 1 anytime the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on VCC is insufficient to support oscillation.
3) The $\overline{\text{EOSC}}$ bit is turned off.
4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to a logic 0.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. This flag can be used to generate an interrupt on either $\overline{\text{INTA}}$ or SQW/$\overline{\text{INTB}}$ depending on the status of the INTCN bit in the control register. If the INTCN bit is set to logic 0 and A2F is at logic 1 (and A2IE bit is also logic 1), the $\overline{\text{INTA}}$ pin goes low. If the INTCN bit is set to logic 1 and A2F is logic 1 (and A2IE bit is also logic 1), the SQW/$\overline{\text{INTB}}$ pin goes low. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the Alarm 1 Flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is also a logic 1, the $\overline{\text{INTA}}$ pin goes low. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

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I2C Serial Data Bus

The IDT1337AG supports the I2C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The IDT1337AG operates as a slave on the I2C bus. Within the bus specifications, a standard mode (100 kHz maximum clock rate) and a fast mode (400 kHz maximum clock rate) are defined. The IDT1337AG works in both modes. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see the “Data Transfer on I2C Serial Bus” figure):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

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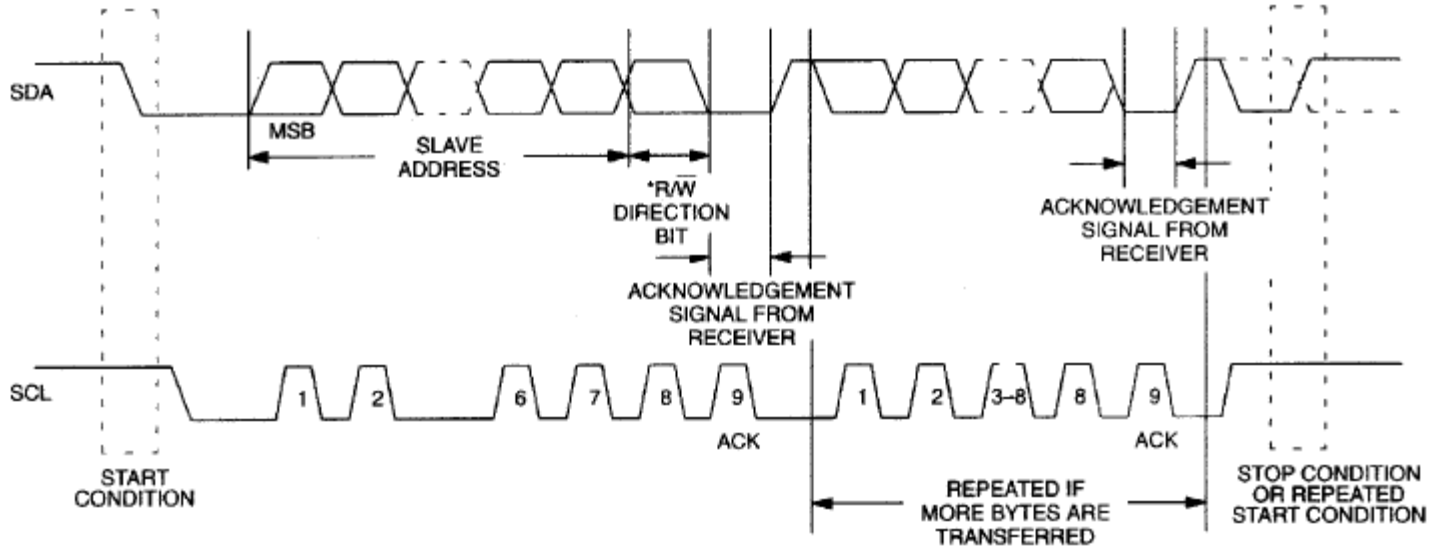
Data Transfer on I2C Serial Bus



Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The IDT1337AG can operate in the following two modes:

1) **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see the “Data Write–Slave Receiver Mode” figure). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit IDT1337AG address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 0 for a write. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the IDT1337AG acknowledges the slave address + write bit, the master transmits a register address to the IDT1337AG. This sets the register pointer on the IDT1337AG. The master may then transmit zero or more bytes of data, with the IDT1337AG acknowledging each byte received. The address pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2) **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the IDT1337AG while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (see the “Data Read–Slave Transmitter Mode” figure). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit IDT1337AG address, which is 1101000, followed by the direction bit (R/$\overline{W}$), which is 1 for a read. After receiving and decoding the slave address byte the slave outputs an acknowledge on the SDA line. The IDT1337AG then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The IDT1337AG must receive a “not acknowledge” to end a read.

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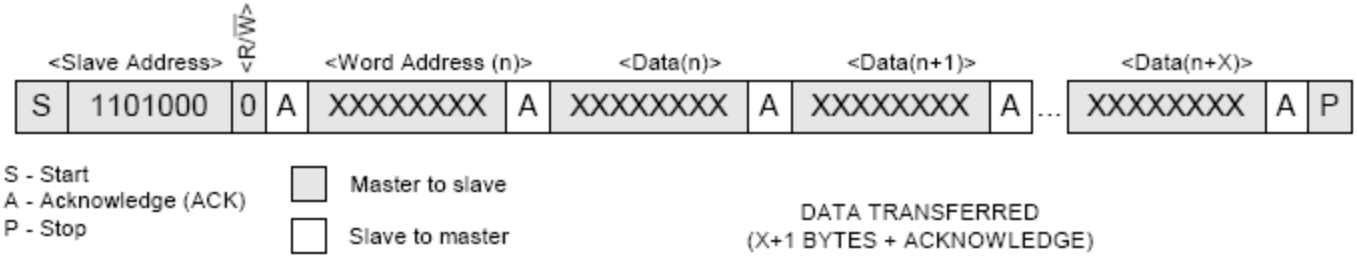
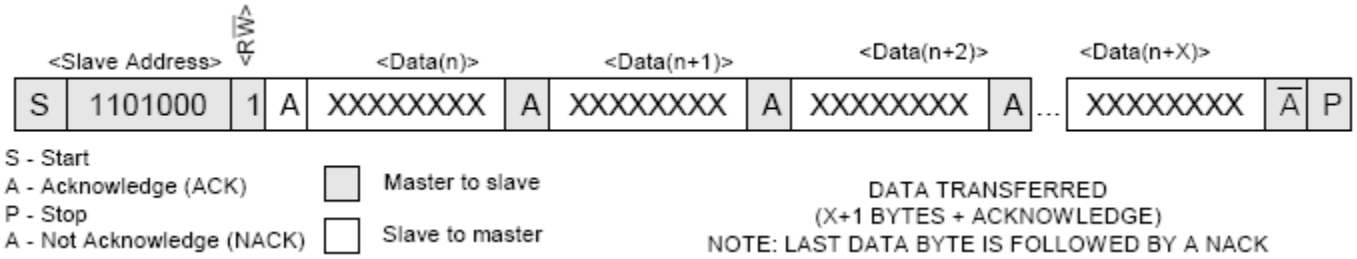
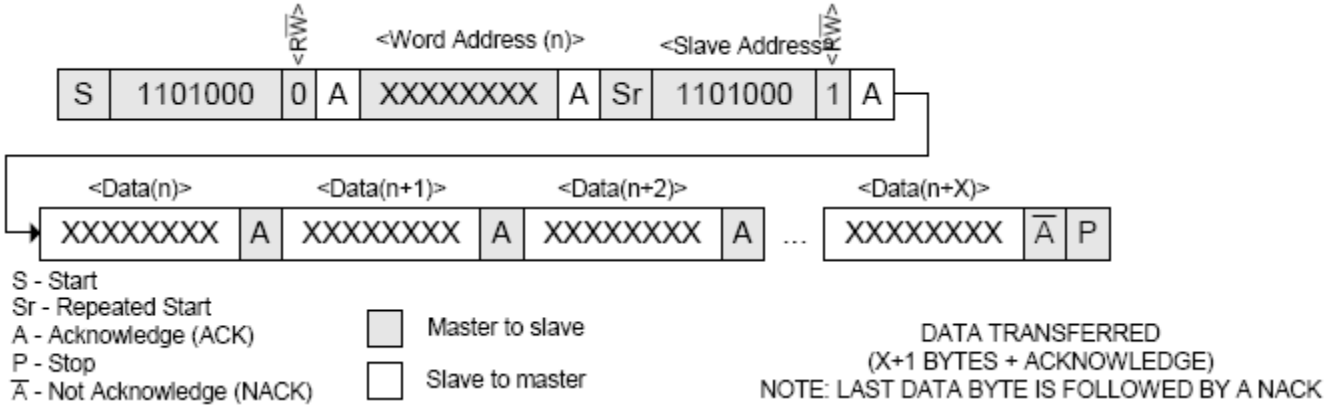
Data Write – Slave Receiver Mode



Data Read (from current Pointer location) – Slave Transmitter Mode



Data Read (Write Pointer, then Read) – Slave Receive and Transmit



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Handling, PCB Layout, and Assembly

The IDT1337AG package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning equipment should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All NC (no connect) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT1337AG. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Voltage Range (on any pin relative to ground)	-0.3 V to +6.0 V
Storage Temperature	-55 to +125°C
Soldering Temperature	260°C
Ambient Operating Temperature (industrial)	-40 to +85°C

Recommended DC Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
VCC Supply Voltage	V_{CC}	Full operation	1.8	3.3	5.5	V
	V_{CCT}	Timekeeping	1.3		1.8	V
Ambient Operating Temperature (industrial)	T_A		-40		+85	°C
Logic 1	V_{IH}	SCL, SDA	0.8VCC		VCC + 0.3	V
		$\overline{INTA}$, SQW/$\overline{INTB}$			5.5	
Logic 0	V_{IL}		-0.3		+0.3VCC	V

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DC Electrical Characteristics

Unless stated otherwise, **VCC = 1.8 V to 5.5 V**, Ambient Temp. -40 to +85°C, Note 1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Leakage	I_{LI}	Note 2	-1		+1	µA
I/O Leakage	I_{LO}	Note 3	-1		+1	µA
Logic 0 Output VOL = 0.4 V	I_{OL}	Note 3			3	mA
Active Supply Current	I_{CCA}	Note 4		5	150	µA
Standby Current	I_{CCS}	Notes 5, 6			1.5	µA

DC Electrical Characteristics

Unless stated otherwise, **VCC = 1.3 V to 1.8 V**, Ambient Temp. -40 to +85°C (industrial), Note 1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Timekeeper Current (Oscillator Enabled)	I_{CCTOSC}	Notes 5, 7, 8, 9		725	900	nA
Data-Retention Current (Oscillator Disabled)	I_{CCTDDR}	Notes 5, 9			300	nA

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AC Electrical Characteristics

Unless stated otherwise, **VCC = 1.8 V to 5.5 V**, Ambient Temp. -40 to +85°C, Note 1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SCL Clock Frequency	f_{SCL}	Fast Mode	100		400	kHz
		Standard Mode	0		100	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode	1.3			µs
		Standard Mode	4.7			
Hold Time (Repeated) START Condition, Note 10	$t_{HD:STA}$	Fast Mode	0.6			µs
		Standard Mode	4.0			
Low Period of SCL Clock	t_{LOW}	Fast Mode	1.3			µs
		Standard Mode	4.7			
High Period of SCL Clock	t_{HIGH}	Fast Mode	0.6			µs
		Standard Mode	4.0			
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode	0.6			µs
		Standard Mode	4.7			
Data Hold Time, Notes 11, 12	$t_{HD:DAT}$	Fast Mode	0		0.9	µs
		Standard Mode	0			
Data Setup Time, Note 13	$t_{SU:DAT}$	Fast Mode	100			ns
		Standard Mode	250			
Rise Time of Both SDA and SCL Signals, Note 14	t_R	Fast Mode	$20 + 0.1C_B$		300	ns
		Standard Mode			1000	
Fall Time of Both SDA and SCL Signals, Note 14	t_F	Fast Mode	$20 + 0.1C_B$		300	ns
		Standard Mode			300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast Mode	0.6			µs
		Standard Mode	4.0			
Capacitive Load for Each Bus Line, Note 14	C_B				400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	Note 15			10	pF
32.768 kHz Clock Accuracy with External Crystal		T_A=25°C V_{CC}=3.3 V			±10	ppm
32.768 kHz Clock Accuracy with Internal Crystal		T_A=25°C V_{CC}=3.3 V (crystal accuracy ±20ppm)			±30	ppm

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Note 1: Limits at -40°C are guaranteed by design and are not production tested.

Note 2: SCL only.

Note 3: SDA, $\overline{INTA}$, and SQW/$\overline{INTB}$.

Note 4: I_{CCA}—SCL clocking at maximum frequency = 400 kHz, VIL = 0.0V, VIH = VCC.

Note 5: Specified with the I^{2}C bus inactive, VIL = 0.0V, VIH = VCC.

Note 6: SQW enabled.

Note 7: Specified with the SQW function disabled by setting INTCN = 1.

Note 8: Using recommended crystal on X1 and X2.

Note 9: The device is fully accessible when 1.8 ≤ VCC ≤ 5.5 V. Time and date are maintained when 1.3 V ≤ VCC ≤ 1.8 V.

Note 10: After this period, the first clock pulse is generated.

Note 11: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 12: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 13: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns before the SCL line is released.

Note 14: C_B—total capacitance of one bus line in pF.

Note 15: Guaranteed by design. Not production tested.

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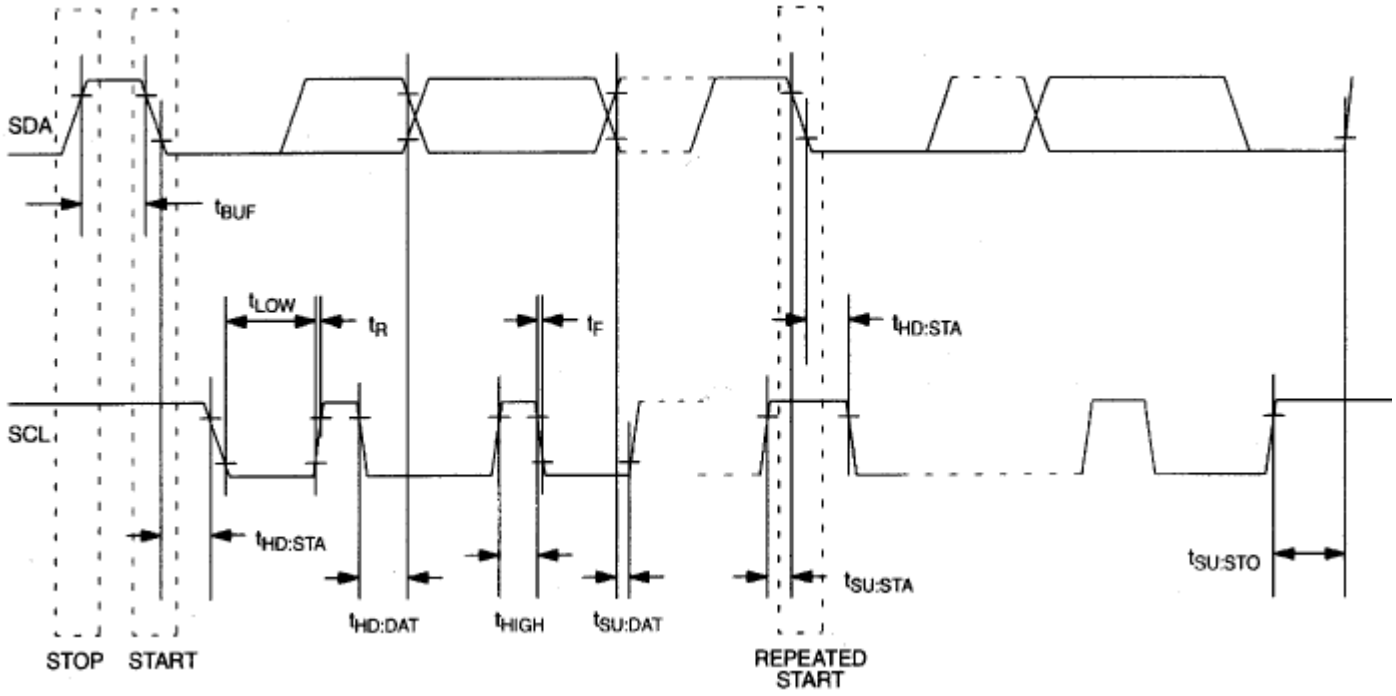
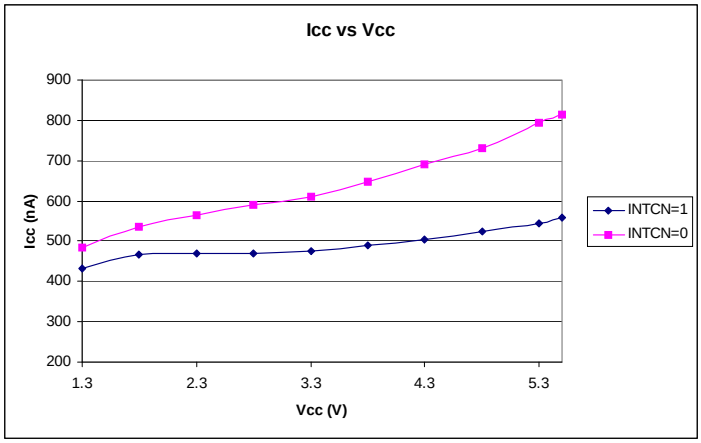
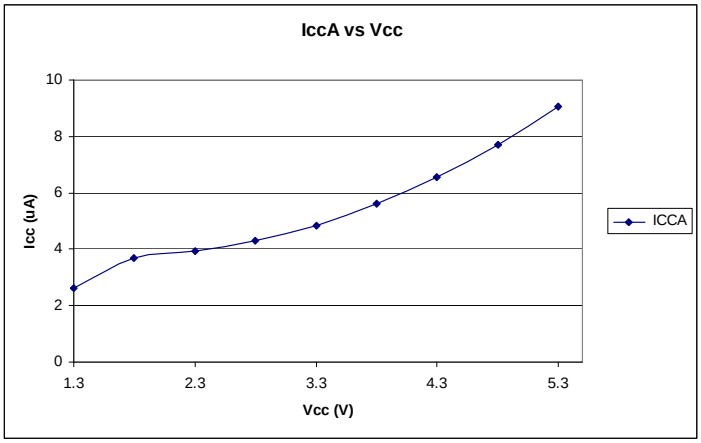
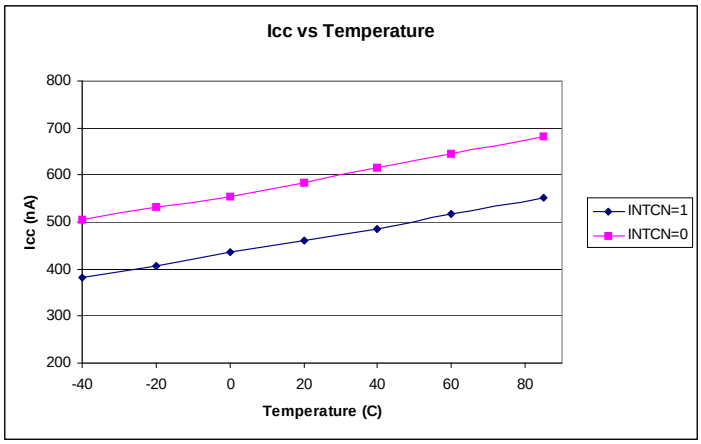
Timing Diagram

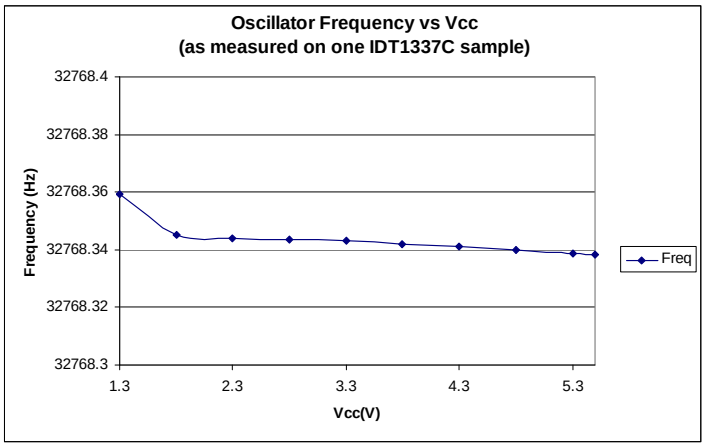


Typical Operating Characteristics









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Thermal Characteristics for 8SOIC

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Thermal Characteristics for 8MSOP

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		95		°C/W
Thermal Resistance Junction to Case	θ_{JC}			48		°C/W

Thermal Characteristics for 16SOIC

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

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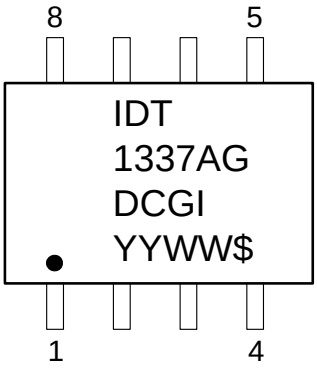
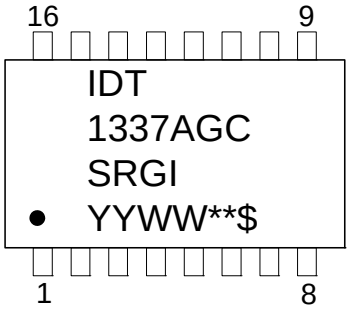
Marking Diagram (8 MSOP)

Marking Diagram (8 SOIC)



Marking Diagram (16 SOIC)



Notes:

1. # = product stepping.
2. $ = mark code.
3. ** = sequential lot code.
4. YYWW is the last two digits of the year and week that the part was assembled.
5. “XXX” = traceability (lot code).
6. “G” denotes RoHS compliant package.
7. “I” denotes industrial grade.
8. Bottom marking: country of origin if not USA.

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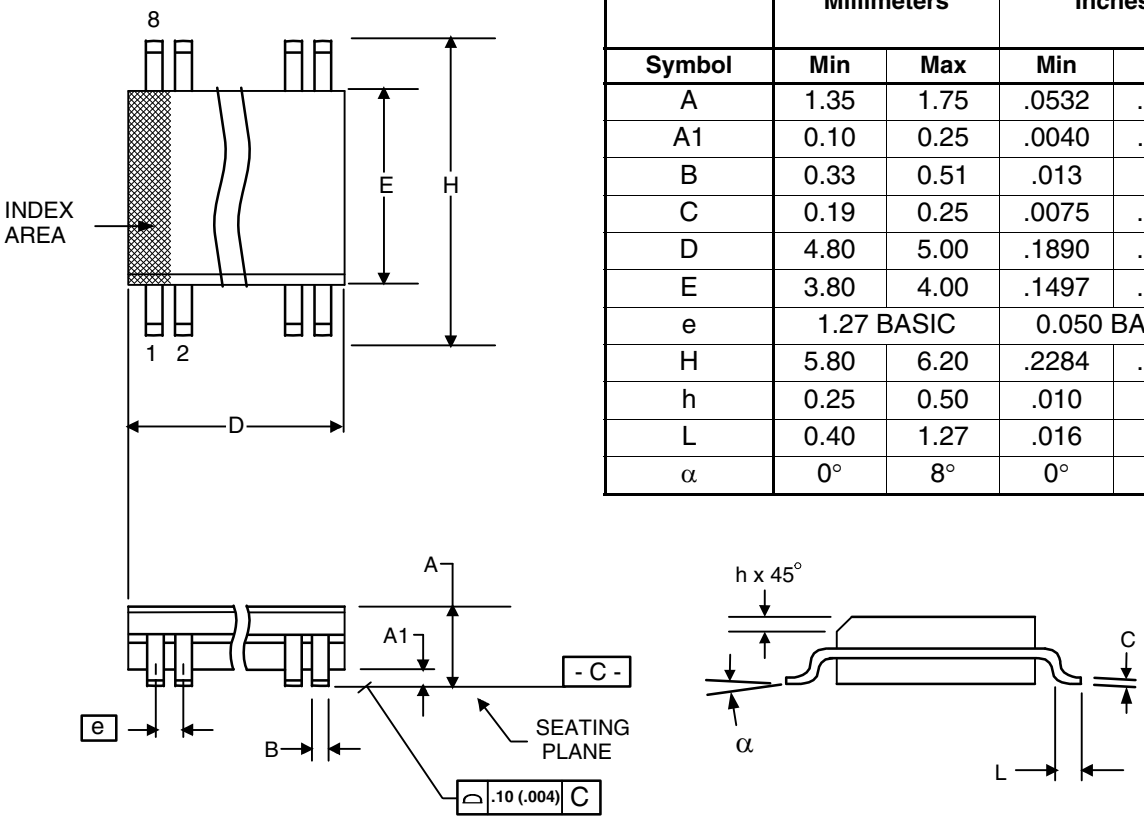
Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

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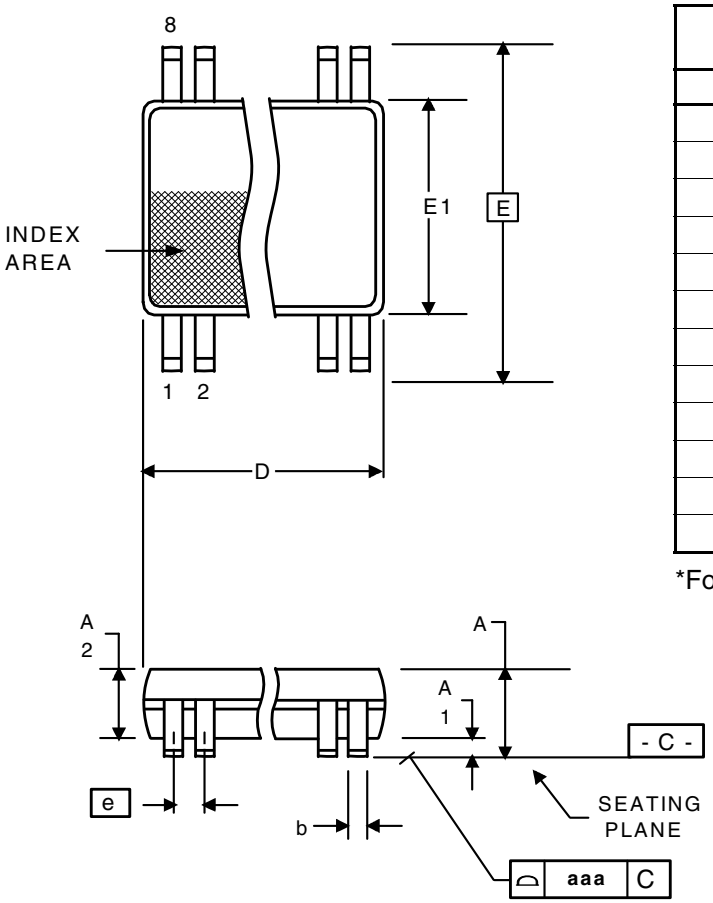
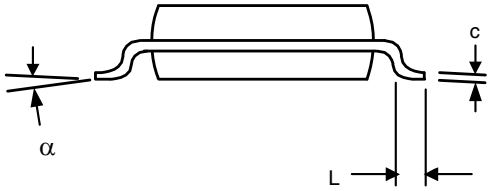
Package Outline and Package Dimensions (8-pin MSOP, 3.00 mm Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.10	--	0.043
A1	0	0.15	0	0.006
A2	0.79	0.97	0.031	0.038
b	0.22	0.38	0.008	0.015
C	0.08	0.23	0.003	0.009
D	3.00 BASIC		0.118 BASIC	
E	4.90 BASIC		0.193 BASIC	
E1	3.00 BASIC		0.118 BASIC	
e	0.65 Basic		0.0256 Basic	
L	0.40	0.80	0.016	0.032
α	0°	8°	0°	8°
aaa	-	0.10	-	0.004

*For reference only. Controlling dimensions in mm.



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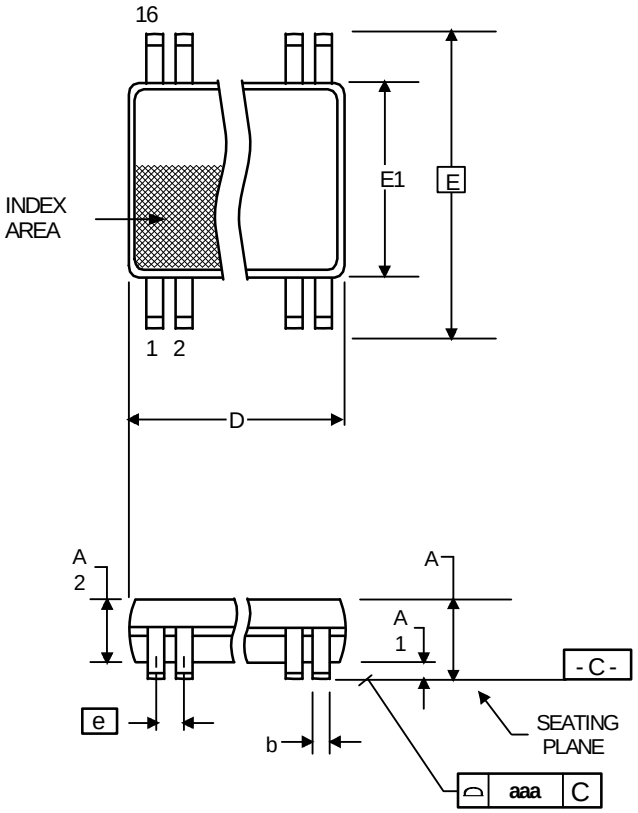
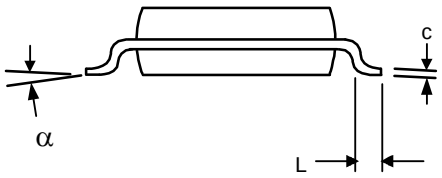
Package Outline and Package Dimensions (16-pin SOIC, 300 mil Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	2.65	--	0.104
A1	0.10	--	0.0040	--
A2	2.05	2.55	0.081	0.100
b	0.33	0.51	0.013	0.020
c	0.18	0.32	0.007	0.013
D	10.10	10.50	0.397	0.413
E	10.00	10.65	0.394	0.419
E1	7.40	7.60	0.291	0.299
e	1.27 Basic		0.050 Basic	
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°
aaa	-	0.10	-	0.004

*For reference only. Controlling dimensions in mm.



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Ordering Information

Part / Order Number	Markings	Shipping Packaging	Package	Temperature
1337AGDVGI	see page 20	Tubes	8-pin MSOP	-40 to +85° C
1337AGDVGI8		Tape and Reel	8-pin MSOP	-40 to +85° C
1337AGCSRGI		Tubes	16-pin SOIC	-40 to +85° C
1337AGCSRGI8		Tape and Reel	16-pin SOIC	-40 to +85° C
1337AGDCGI		Tubes	8-pin SOIC	-40 to +85° C
1337AGDCGI8		Tape and Reel	8-pin SOIC	-40 to +85° C

The 1337AGC packages are RoHS compliant. Packages without the integrated crystal are Pb-free; packages that include the integrated crystal (as designated with a "C" before the two-letter package code) may include lead that is exempt under RoHS requirements. The lead finish is JESD91 category e3.

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Revision History

Rev.	Date	Originator	Description of Change
A	08/02/13	J. Chao	Initial release
B	10/31/13	J. Chao	1. Update Alarm/Interrupt table. 2. Update Bit2 and Bit descriptions.
C	01/15/14	J. Chao	Removed all references to VFQFPN (16NLG) package.
D	07/14/17	C. Chen	Updated marking diagram for 8MSOP.

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