



**THE DATASHEET OF
C3M0120065J**

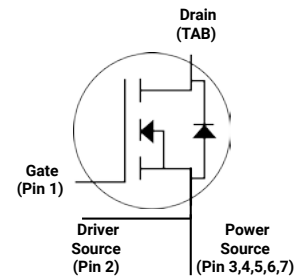


C3M0120065J

Silicon Carbide Power MOSFET C3M™ MOSFET Technology
N-Channel Enhancement Mode

Features

- 3rd Generation SiC MOSFET technology
- Low inductance package with driver source pin
- 7mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant



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Ordering Part Number	Package	Marking
C3M0120065J	TO-263-7	C3M0120065J

Applications

- Solar inverters
- DC/DC converters
- Switch Mode Power Supplies
- EV battery chargers
- UPS

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Easy to parallel and simple to drive
- Enable new hard switching PFC topologies (Totem-Pole)

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	v	$T_C = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			21	A	$V_{GS} = 15\text{ V}, T_C = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19
				15		$V_{GS} = 15\text{ V}, T_C = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Note 2
Pulsed Drain Current	I_{DM}			51		t_{Pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_C = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			86	W	$T_C = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design



Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650	—	—	V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	Fig. 11
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.3	3.6		$V_{DS} = V_{GS}, I_D = 1.86\ \text{mA}$	
		—	1.9	—		$V_{DS} = V_{GS}, I_D = 1.86\ \text{mA}, T_J = 175^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	μA	$V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	$V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	120	157	m Ω	$V_{GS} = 15\ \text{V}, I_D = 6.76\ \text{A}$	Fig. 4, 5, 6
		—	168	—		$V_{GS} = 15\ \text{V}, I_D = 6.76\ \text{A}, T_J = 175^\circ\text{C}$	
Transconductance	g_{fs}	—	5.0	—	S	$V_{DS} = 20\ \text{V}, I_{DS} = 6.76\ \text{A}$	Fig. 7
			4.9			$V_{DS} = 20\ \text{V}, I_{DS} = 6.76\ \text{A}, T_J = 175^\circ\text{C}$	
Input Capacitance	C_{iss}	—	640	—	pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V to } 400\ \text{V}$ $f = 1\ \text{Mhz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18
Output Capacitance	C_{oss}	—	45	—			
Reverse Transfer Capacitance	C_{rss}	—	2.3	—			
Effective Output Capacitance (Energy Related)	$C_{o(er)}$	—	57	—			
Effective Output Capacitance (Time Related)	$C_{o(tr)}$	—	79	—			
C_{oss} Stored Energy	E_{oss}	—	4.3	—	μJ	$V_{DS} = 400\ \text{V}, f = 1\ \text{Mhz}$	Fig. 16
Turn-On Switching Energy (Body Diode)	E_{on}	—	28	—	μJ	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 6.76\ \text{A},$ $R_{G(ext)} = 10\ \Omega, L = 237\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode of MOSFET	Fig. 25
Turn Off Switching Energy (Body Diode)	E_{off}	—	6	—			
Turn-On Delay Time	$t_{d(on)}$	—	8	—	ns	$V_{DD} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 6.76\ \text{A}, R_{G(ext)} = 10\ \Omega$ Timing relative to V_{DS} Inductive load	Fig. 26
Rise Time	t_r	—	9	—			
Turn-Off Delay Time	$t_{d(off)}$	—	18	—			
Fall Time	t_f	—	9	—			
Internal Gate Resistance	$R_{G(int)}$	—	6	—	Ω	$f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$	
Gate to Source Charge	Q_{gs}	—	8	—	nC	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 6.76\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	7	—			
Total Gate Charge	Q_g	—	26	—			

Note:

³ $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{DS} is rising from 0 to 400V



Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	V_{SD}	4.5	—	V	$V_{GS} = -4\text{ V}, I_{SD} = 3.4\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.0	—		$V_{GS} = -4\text{ V}, I_{SD} = 3.4\text{ A}, T_J = 175^\circ\text{C}$	
Continuous Diode Forward Current	I_S	—	15	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
Diode pulse Current	$I_{S, pulse}$	—	51		$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{jmax}	
Reverse Recovery Time	t_{rr}	8	—	ns	$V_{GS} = -4\text{ V}, I_{SD} = 6.76\text{ A}, V_R = 400\text{ V}$ $di_f/dt = 5470\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	78	—	nC		
Peak Reverse Recovery Current	I_{RRM}	16	—	A		
Reverse Recovery Time	t_{rr}	9	—	ns	$V_{GS} = -4\text{ V}, I_{SD} = 6.76\text{ A}, V_R = 400\text{ V}$ $di_f/dt = 3650\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	41	—	nC		
Peak Reverse Recovery Current	I_{RRM}	7	—	A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	1.73	$^\circ\text{C}/\text{W}$	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40		



Typical Performance

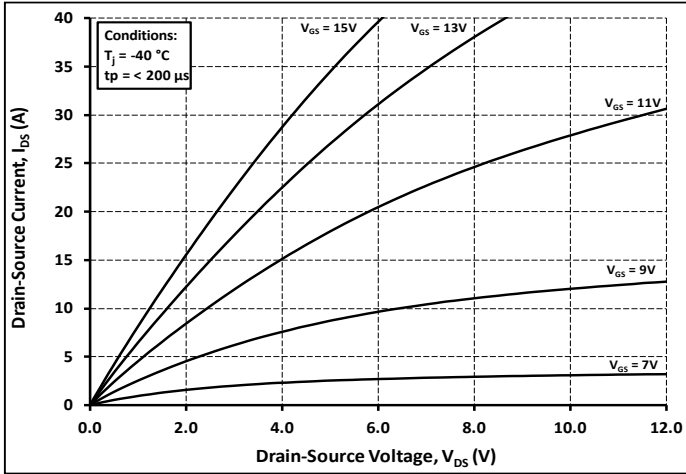


Figure 1. Output Characteristics $T_j = -40^\circ\text{C}$

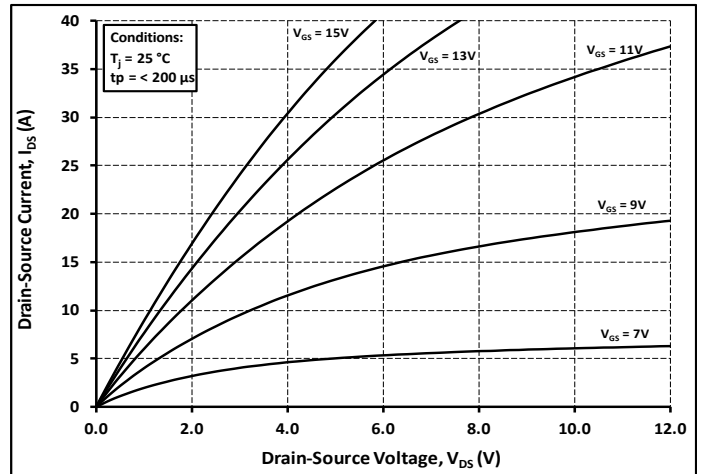


Figure 2. Output Characteristics $T_j = 25^\circ\text{C}$

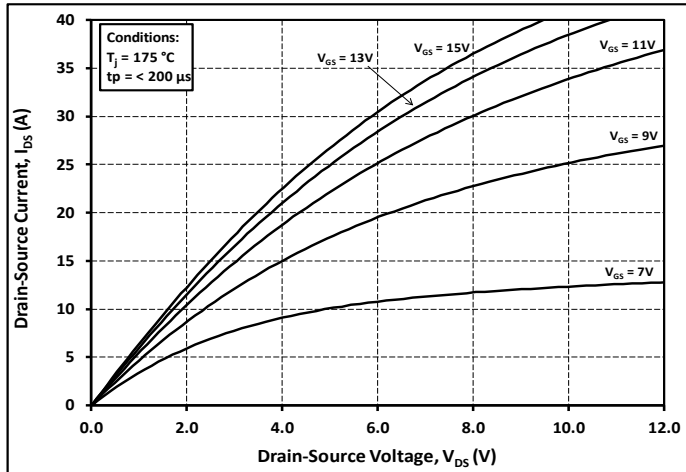


Figure 3. Output Characteristics $T_j = 175^\circ\text{C}$

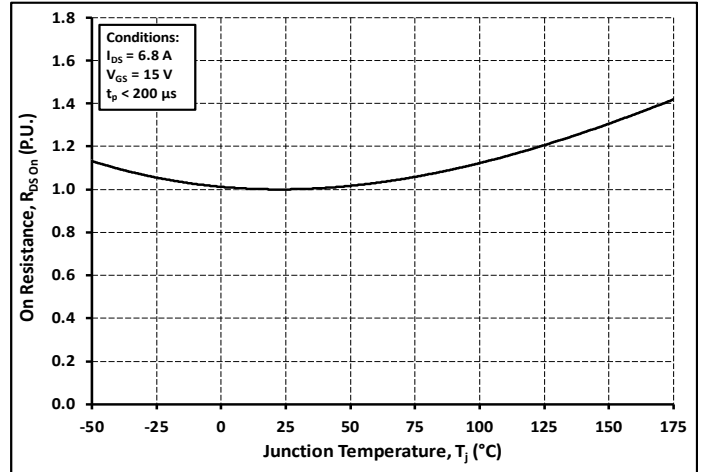


Figure 4. Normalized On-Resistance vs. Temperature

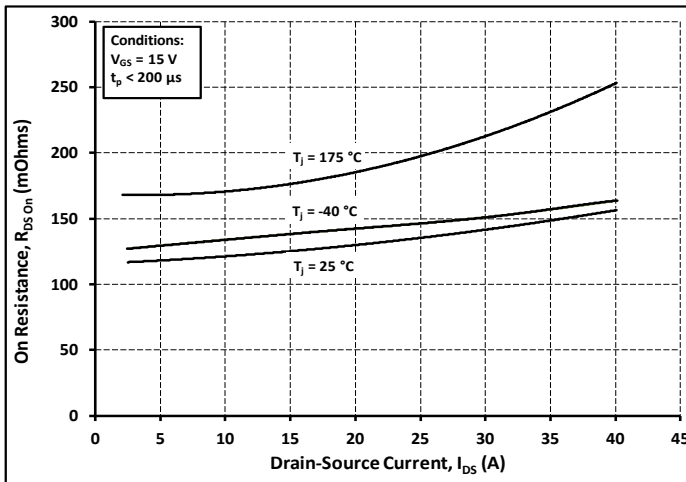


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

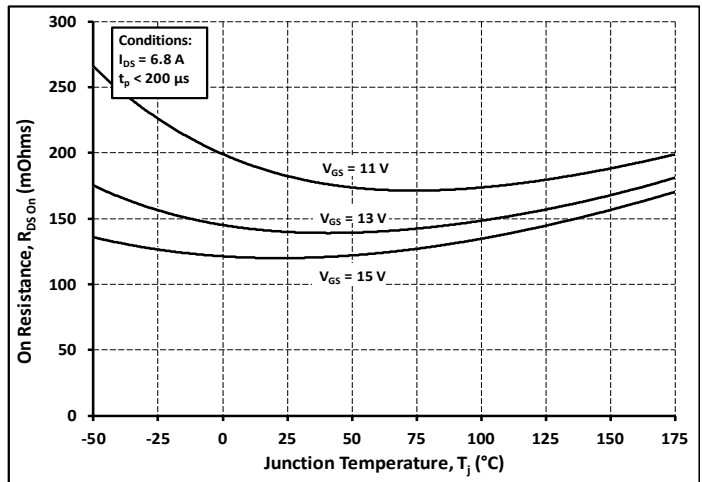


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

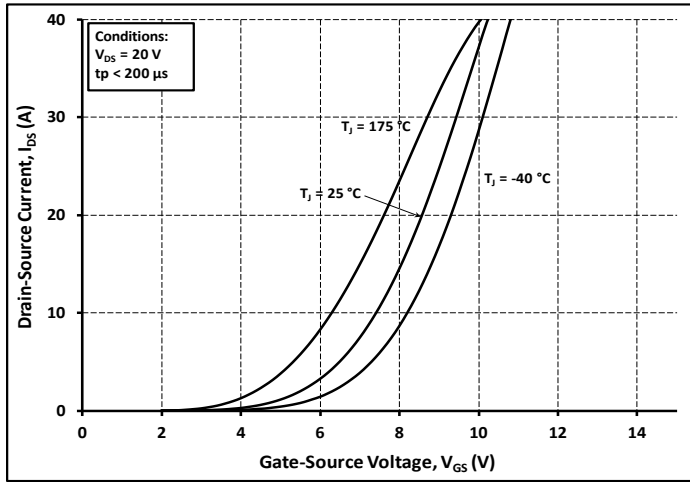


Figure 7. Transfer Characteristic for Various Junction Temperatures

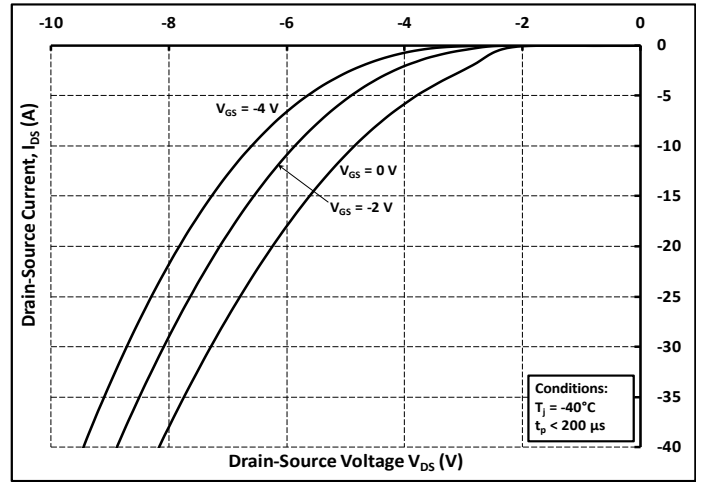


Figure 8. Body Diode Characteristic at -40°C

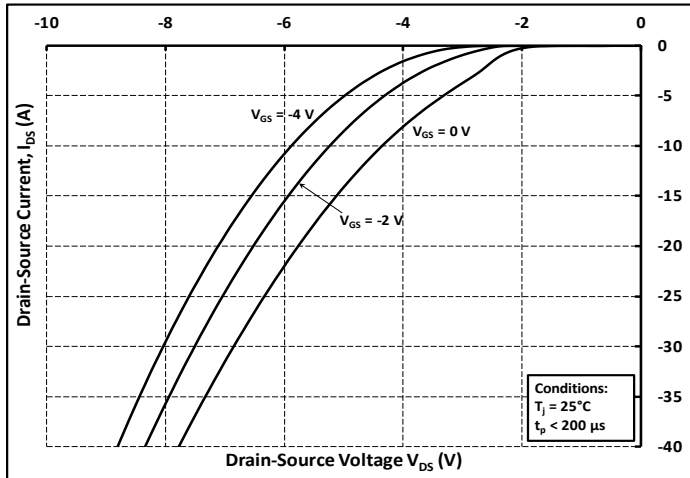


Figure 9. Body Diode Characteristic at 25°C

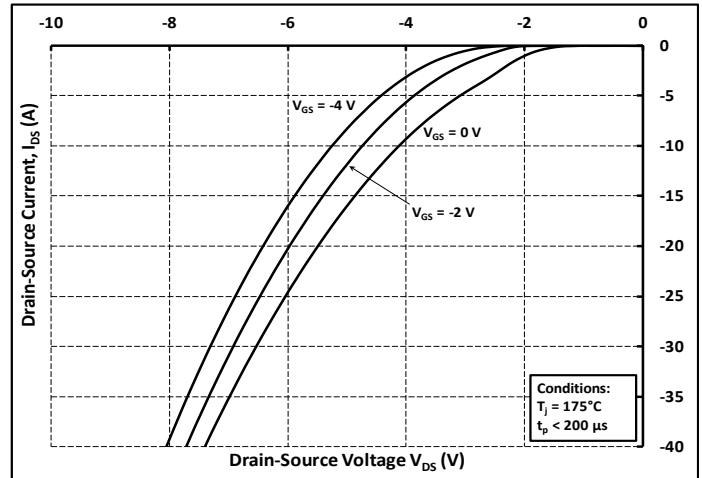


Figure 10. Body Diode Characteristic at 175°C

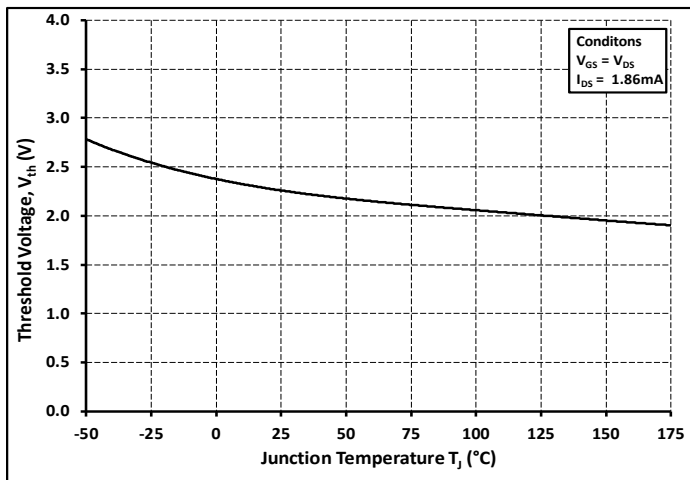


Figure 11. Threshold Voltage vs. Temperature

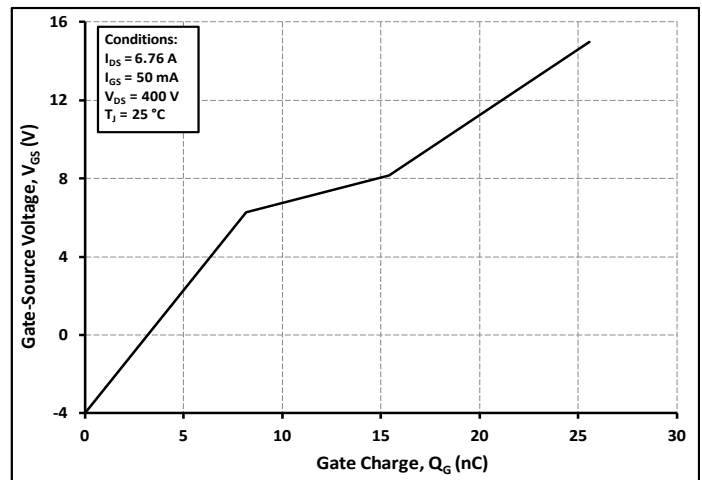


Figure 12. Gate Charge Characteristics



Typical Performance

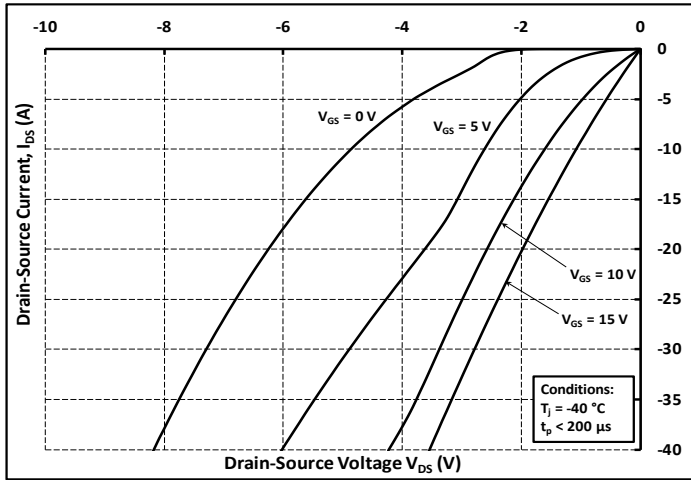


Figure 13. 3rd Quadrant Characteristic at -40°C

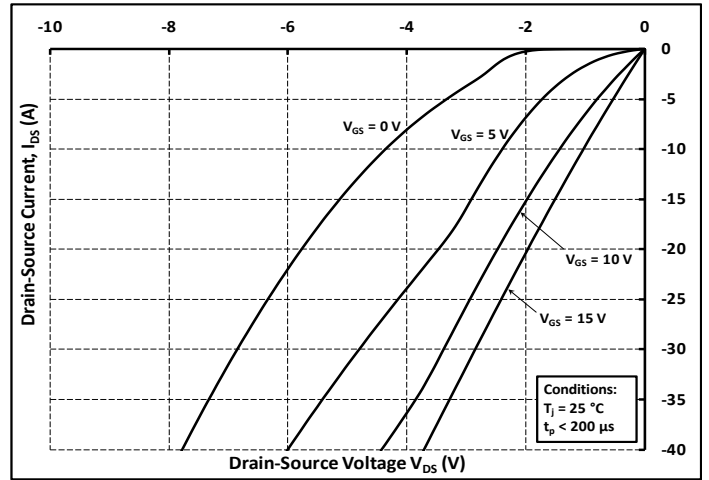


Figure 14. 3rd Quadrant Characteristic at 25°C

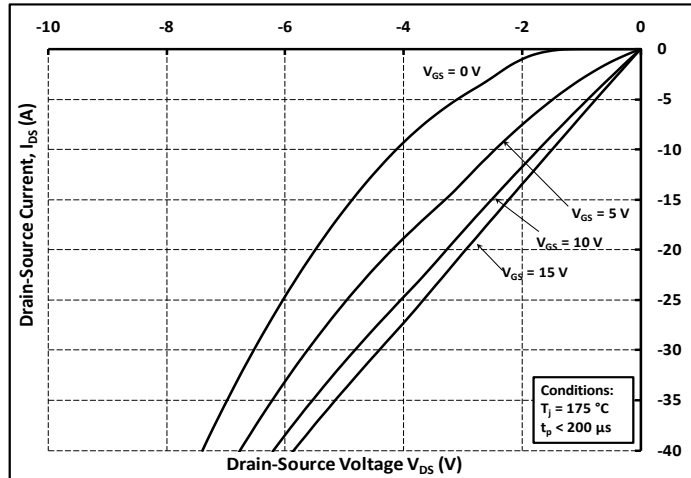


Figure 15. 3rd Quadrant Characteristic at 175°C

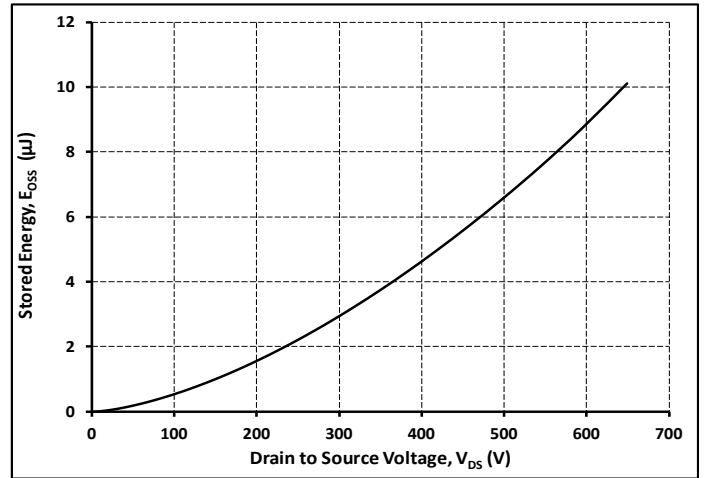


Figure 16. Output Capacitor Stored Energy

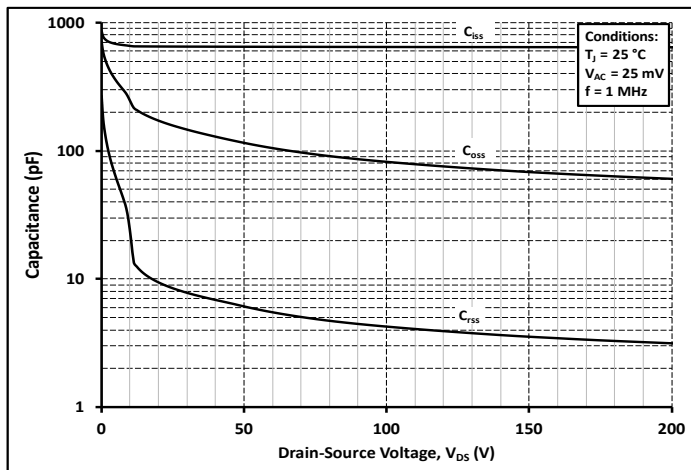


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

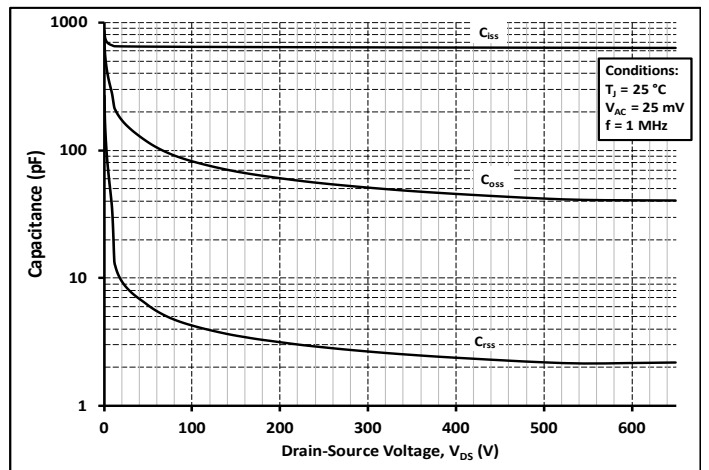


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650 V)



Typical Performance

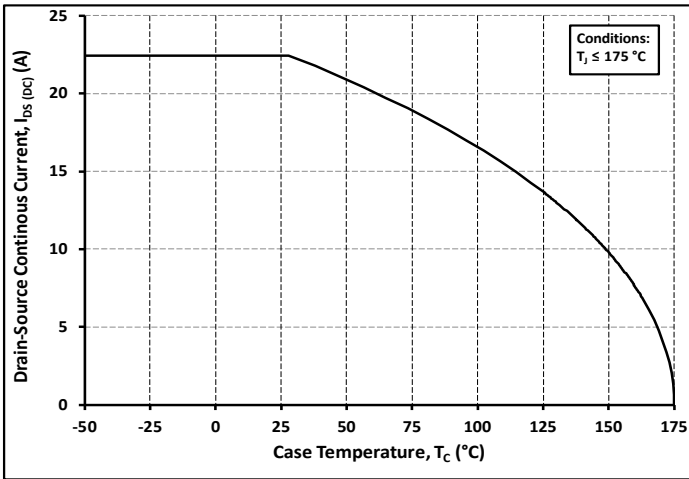


Figure 19. Continuous Drain Current Derating vs. Case Temperature

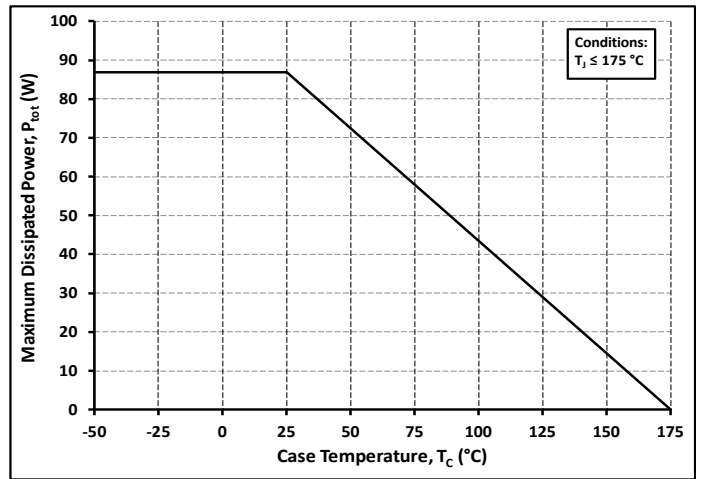


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

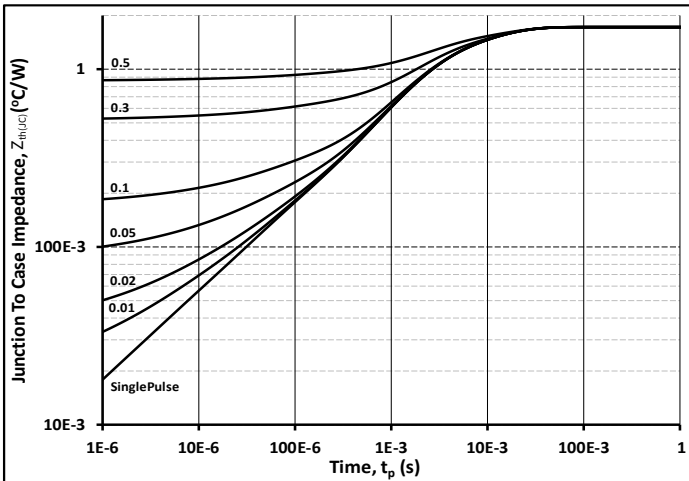


Figure 21. Transient Thermal Impedance (Junction - Case)

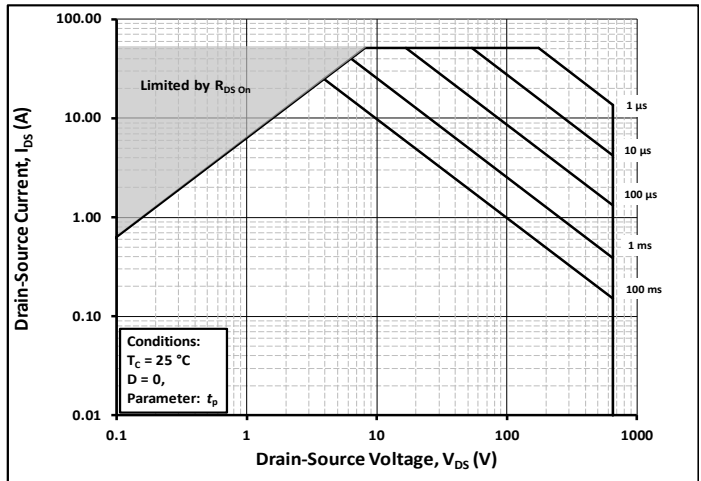


Figure 22. Safe Operating Area

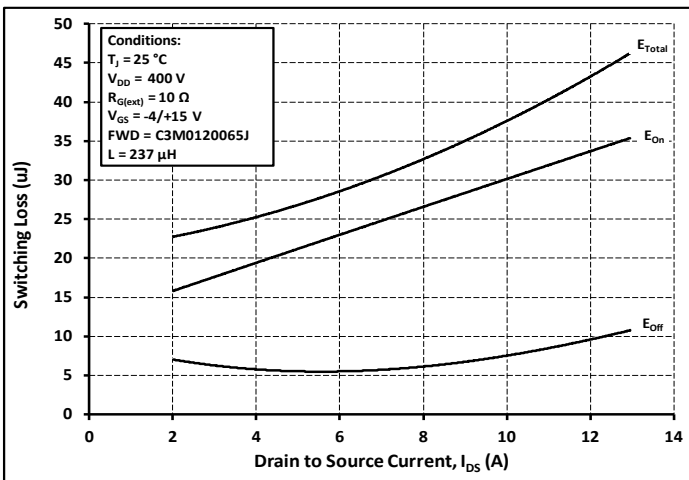


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400\text{ V}$)

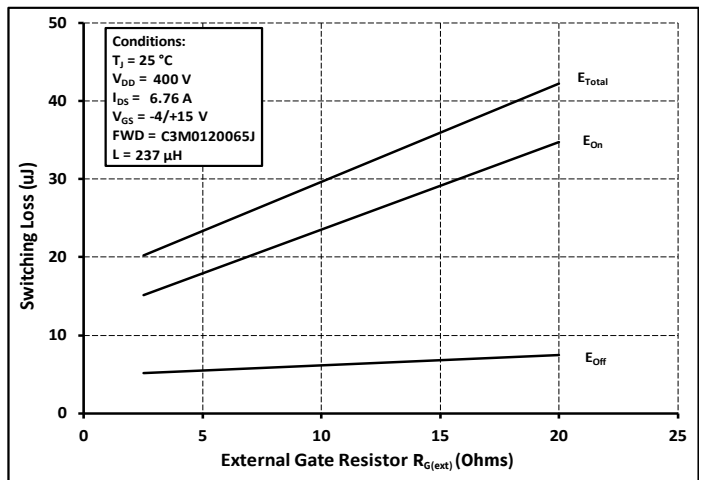


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$



Typical Performance

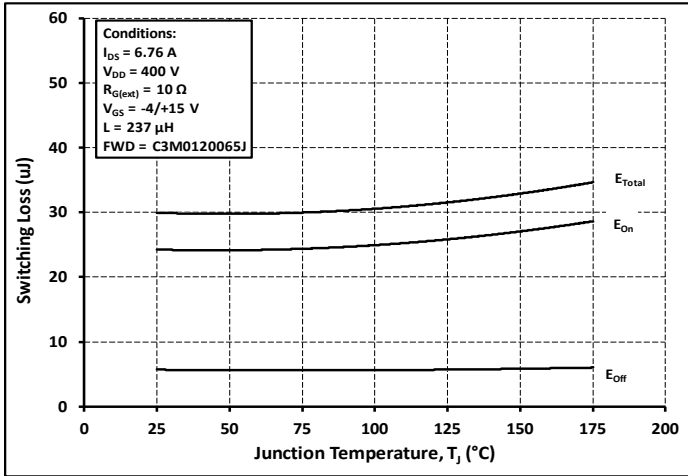


Figure 25. Clamped Inductive Switching Energy vs. Temperature

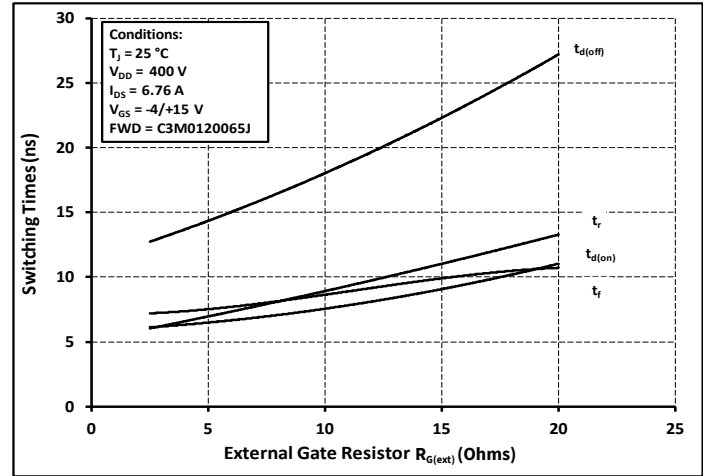


Figure 26. Switching Times vs. $R_{G(ext)}$

Test Circuit Schematic

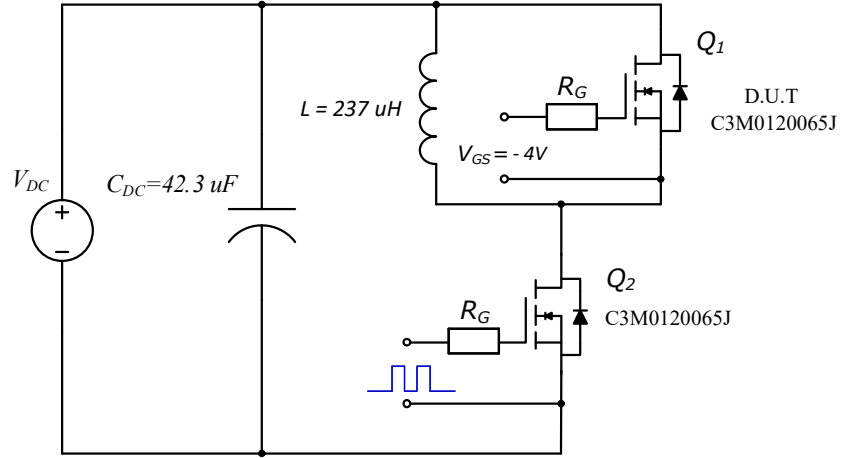
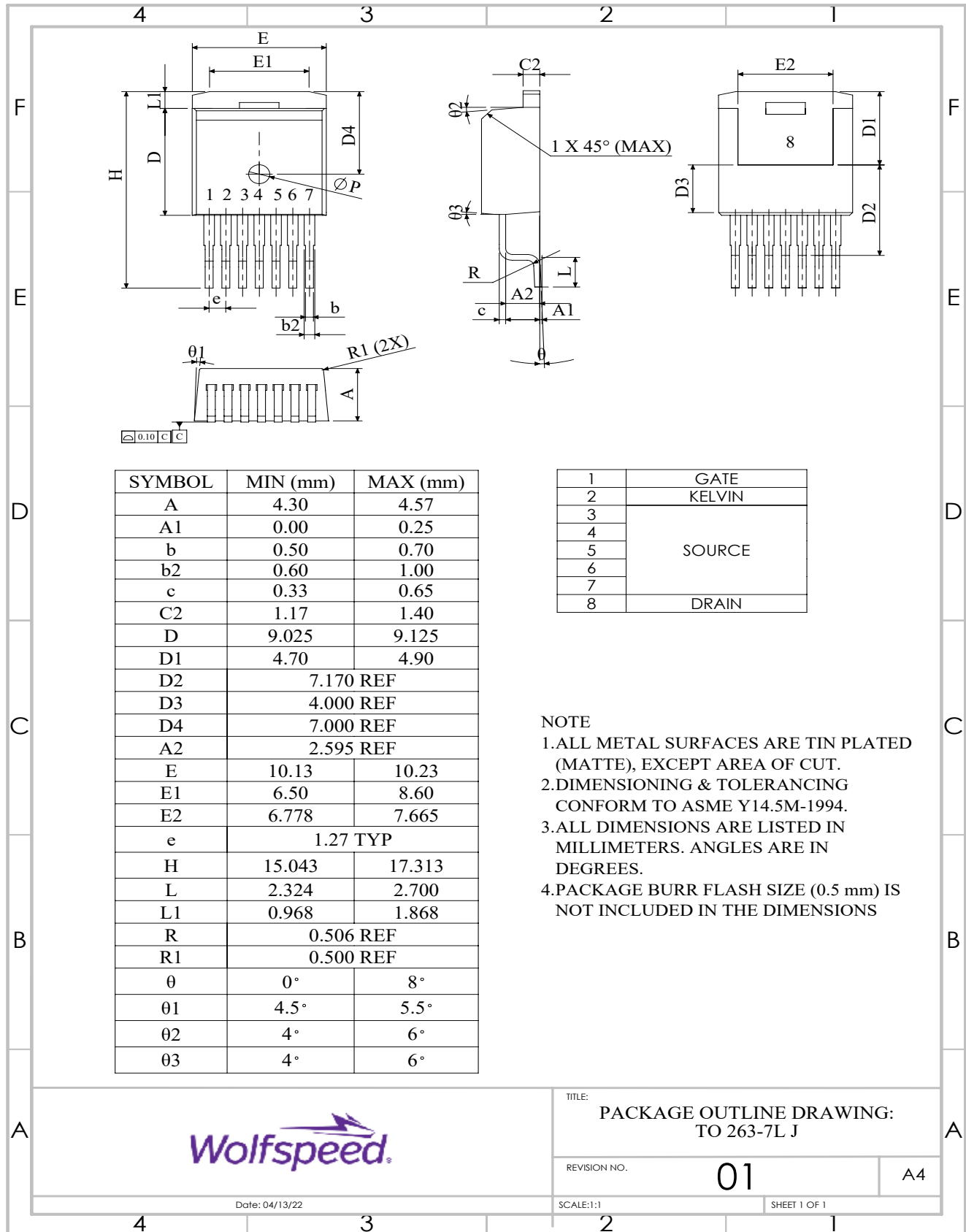


Figure 27. Clamped Inductive Switching Waveform Test Circuit



Package Dimensions – Package 7L D2PAK



- NOTE**
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
 2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
 3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
 4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS



TITLE:
PACKAGE OUTLINE DRAWING:
TO 263-7L J

REVISION NO. **01** A4

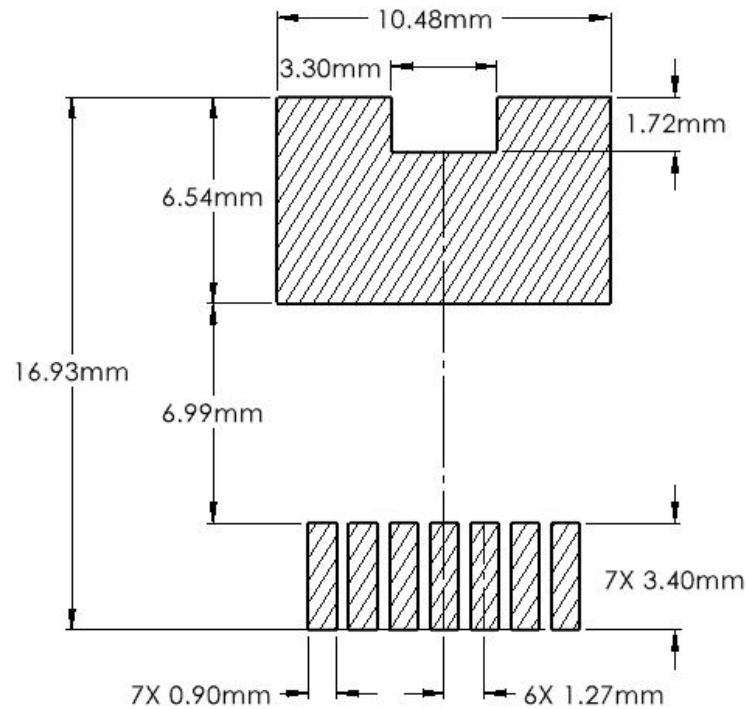
Date: 04/13/22

SCALE: 1:1

SHEET 1 OF 1



Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
1	January-2021	N/A
2	December-2023	Updated Wolfspeed branding, package drawing, package image, solder pad layout, added Rev history, Table 1 layout revised

Related Links

- [SPICE Models](#)
- [SiC MOSFET Isolated Gate Driver reference design](#)
- [SiC MOSFET Evaluation Board](#)



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The Silicon Carbide MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of www.wolfspeed.com.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

Contact info:

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power

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