



**THE DATASHEET OF
IMW65R057M1HXKSA1**



MOSFET

650 V CoolSiC™ M1 SiC Trench Power Device

The 650 V CoolSiC™ is built over the solid silicon carbide technology developed in Infineon in more than 20 years. Leveraging the wide bandgap SiC material characteristics, the 650V CoolSiC™ MOSFET offers a unique combination of performance, reliability and ease of use. Suitable for high temperature and harsh operations, it enables the simplified and cost effective deployment of the highest system efficiency.

Features

- Optimized switching behavior at higher currents
- Commutation robust fast body diode with low Q_{rr}
- Superior gate oxide reliability
- $T_{j,max}=175^{\circ}\text{C}$ and excellent thermal behavior
- Lower $R_{DS(on)}$ and pulse current dependency on temperature
- Increased avalanche capability
- Compatible with standard drivers (recommended driving voltage: 18V)

Benefits

- Unique combination of high performance, high reliability and ease of use
- Ease of use and integration
- Suitable for topologies with continuous hard commutation
- Higher robustness and system reliability
- Efficiency improvement
- Reduced system size leading to higher power density

Potential applications

- SMPS
- UPS (uninterruptable power supplies)
- Solar PV inverters
- EV charging infrastructure
- Energy storage and battery formation
- Class D amplifiers

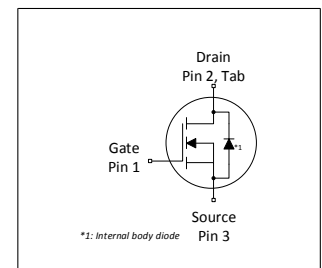
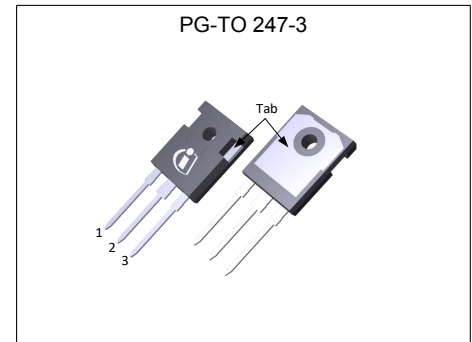
Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_J = 25^{\circ}\text{C}$	650	V
$R_{DS(on),typ}$	57	m Ω
$R_{DS(on),max}$	74	m Ω
$Q_{G,typ}$	28	nC
$I_{D,pulse}$	85	A
$Q_{oss} @ 400\text{ V}$	65	nC
$E_{oss} @ 400\text{ V}$	9.8	μJ

Type / Ordering Code	Package	Marking	Related Links
IMW65R057M1H	PG-TO247-3	65R057M1	see Appendix A



RoHS

Table of Contents

Description	1
Maximum ratings	3
Thermal characteristics	4
Electrical characteristics	5
Electrical characteristics diagrams	7
Test Circuits	12
Package Outlines	13
Appendix A	14
Revision History	15
Trademarks	15
Disclaimer	15

1 Maximum ratings

at $T_J = 25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	35 25	A	$T_C = 25\text{ °C}$ $T_C = 100\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	85	A	$T_C = 25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	142	mJ	$I_D = 5.3\text{ A}$, $V_{DD} = 50\text{ V}$, $L = 10.1\text{ mH}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.71	mJ	$I_D = 5.3\text{ A}$, $V_{DD} = 50\text{ V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	5.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	200	V/ns	$V_{DS} = 0...400\text{ V}$
Gate source voltage (static)	V_{GS}	-2	-	20	V	static
Gate source voltage (recommended driving voltage)	V_{GS}	0	-	18	V	-
Gate source voltage (dynamic)	V_{GS}	-5	-	23	V	$t_{pulse,negative} \leq 15\text{ ns}$ $t_{pulse,positive} \leq 1\% \text{ duty cycle}/f_{sw}$
Power dissipation	P_{tot}	-	-	133	W	$T_C = 25\text{ °C}$
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_J	-55	-	175	°C	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current ¹⁾	I_S	-	-	35	A	$T_C = 25\text{ °C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	85	A	$T_C = 25\text{ °C}$
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C = 25\text{ °C}$, $t = 1\text{ min}$

¹⁾ Limited by $T_{J,max}$

²⁾ Pulse width t_p limited by $T_{J,max}$

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.13	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at $T_J = 25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS} = 0\text{ V}$, $I_D = 0.50\text{ mA}$
Gate threshold voltage ¹⁾	$V_{(GS)th}$	3.5	4.5	5.7	V	$V_{DS} = V_{GS}$, $I_D = 5\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	1 3	150 -	μA	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 25\text{ °C}$ $V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 175\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.057 0.080	0.074 -	Ω	$V_{GS} = 18\text{ V}$, $I_D = 16.7\text{ A}$, $T_J = 25\text{ °C}$ $V_{GS} = 18\text{ V}$, $I_D = 16.7\text{ A}$, $T_J = 175\text{ °C}$
Gate resistance	R_G	-	8.0	-	Ω	$f = 1\text{ MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	930	-	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$
Reverse capacitance	C_{riss}	-	11	-	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$
Output capacitance ²⁾	C_{oss}	-	107	139	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$
Output charge ²⁾	Q_{oss}	-	65	84	nC	calculation based on C_{oss}
Effective output capacitance, energy related ³⁾	$C_{o(er)}$	-	122	-	pF	$V_{GS} = 0\text{ V}$, $V_{DS} = 0...400\text{ V}$
Effective output capacitance, time related ⁴⁾	$C_{o(tr)}$	-	162	-	pF	$I_D = \text{constant}$, $V_{GS} = 0\text{ V}$, $V_{DS} = 0...400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	11.0	-	ns	$V_{DD} = 400\text{ V}$, $V_{GS} = 18\text{ V}$, $I_D = 16.7\text{ A}$, $R_G = 1.8\text{ }\Omega$; see table 9
Rise time	t_r	-	15.0	-	ns	$V_{DD} = 400\text{ V}$, $V_{GS} = 18\text{ V}$, $I_D = 16.7\text{ A}$, $R_G = 1.8\text{ }\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	16.8	-	ns	$V_{DD} = 400\text{ V}$, $V_{GS} = 18\text{ V}$, $I_D = 16.7\text{ A}$, $R_G = 1.8\text{ }\Omega$; see table 9
Fall time	t_f	-	7.0	-	ns	$V_{DD} = 400\text{ V}$, $V_{GS} = 18\text{ V}$, $I_D = 16.7\text{ A}$, $R_G = 1.8\text{ }\Omega$; see table 9

¹⁾ Tested after 1 ms pulse at $V_{GS} = +20\text{ V}$

²⁾ Maximum specification is defined by calculated six sigma upper confidence bound

³⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

⁴⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	7	-	nC	$V_{DD} = 400\text{ V}$, $I_D = 16.7\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$
Gate to drain charge	Q_{gd}	-	6	-	nC	$V_{DD} = 400\text{ V}$, $I_D = 16.7\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$
Gate charge total	Q_g	-	28	-	nC	$V_{DD} = 400\text{ V}$, $I_D = 16.7\text{ A}$, $V_{GS} = 0\text{ to }18\text{ V}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	4.0	-	V	$V_{GS} = 0\text{ V}$, $I_F = 16.7\text{ A}$, $T_J = 25\text{ °C}$
Reverse recovery time	t_{rr}	-	28	-	ns	$V_R = 400\text{ V}$, $I_F = 16.7\text{ A}$, $di_F/dt = 1000\text{ A}/\mu\text{s}$; see table 8
Reverse recovery charge	Q_{rr}	-	113	-	nC	$V_R = 400\text{ V}$, $I_F = 16.7\text{ A}$, $di_F/dt = 1000\text{ A}/\mu\text{s}$; see table 8
Peak reverse recovery current	I_{rrm}	-	8.0	-	A	$V_R = 400\text{ V}$, $I_F = 16.7\text{ A}$, $di_F/dt = 1000\text{ A}/\mu\text{s}$; see table 8

4 Electrical characteristics diagrams

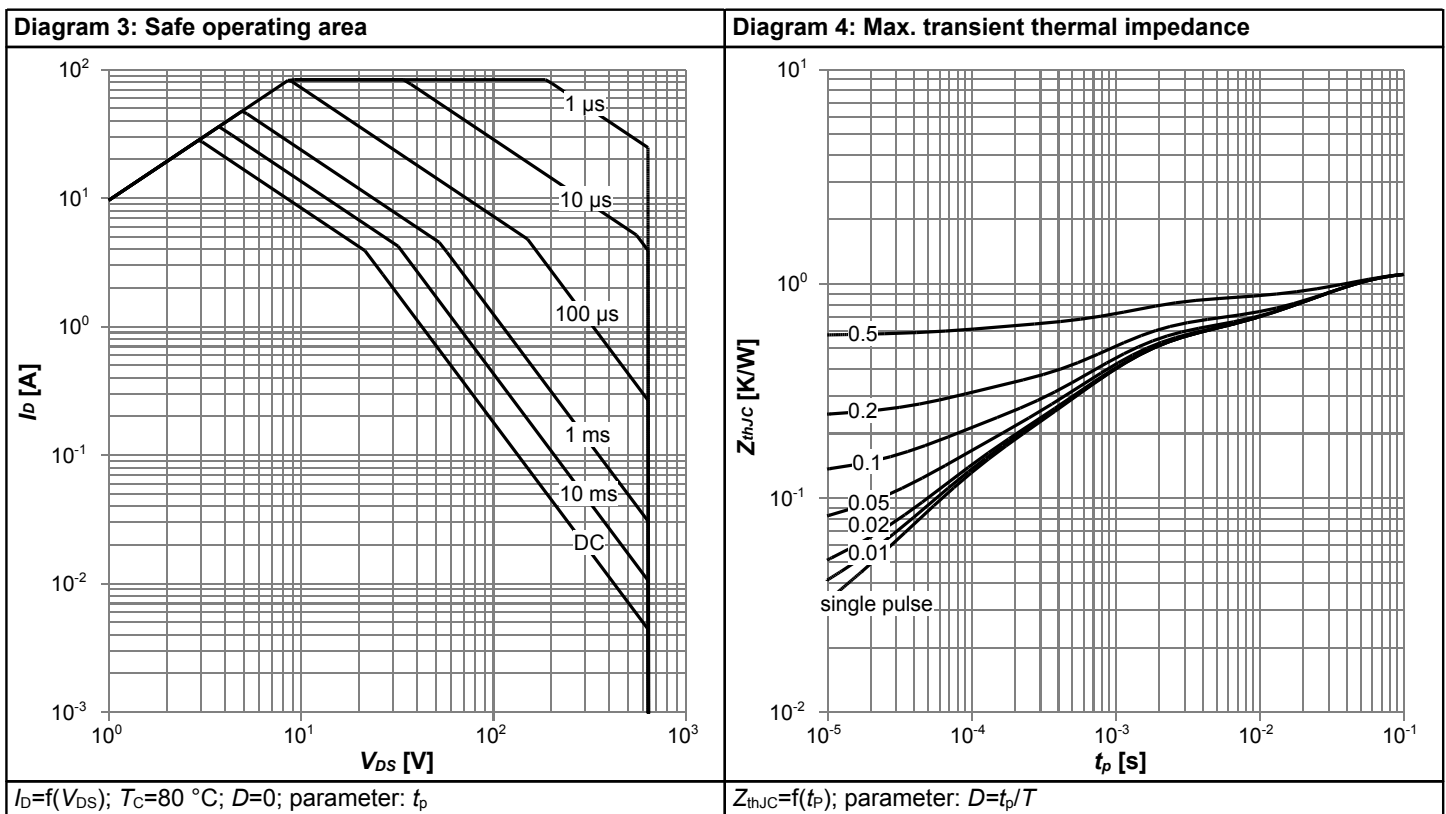
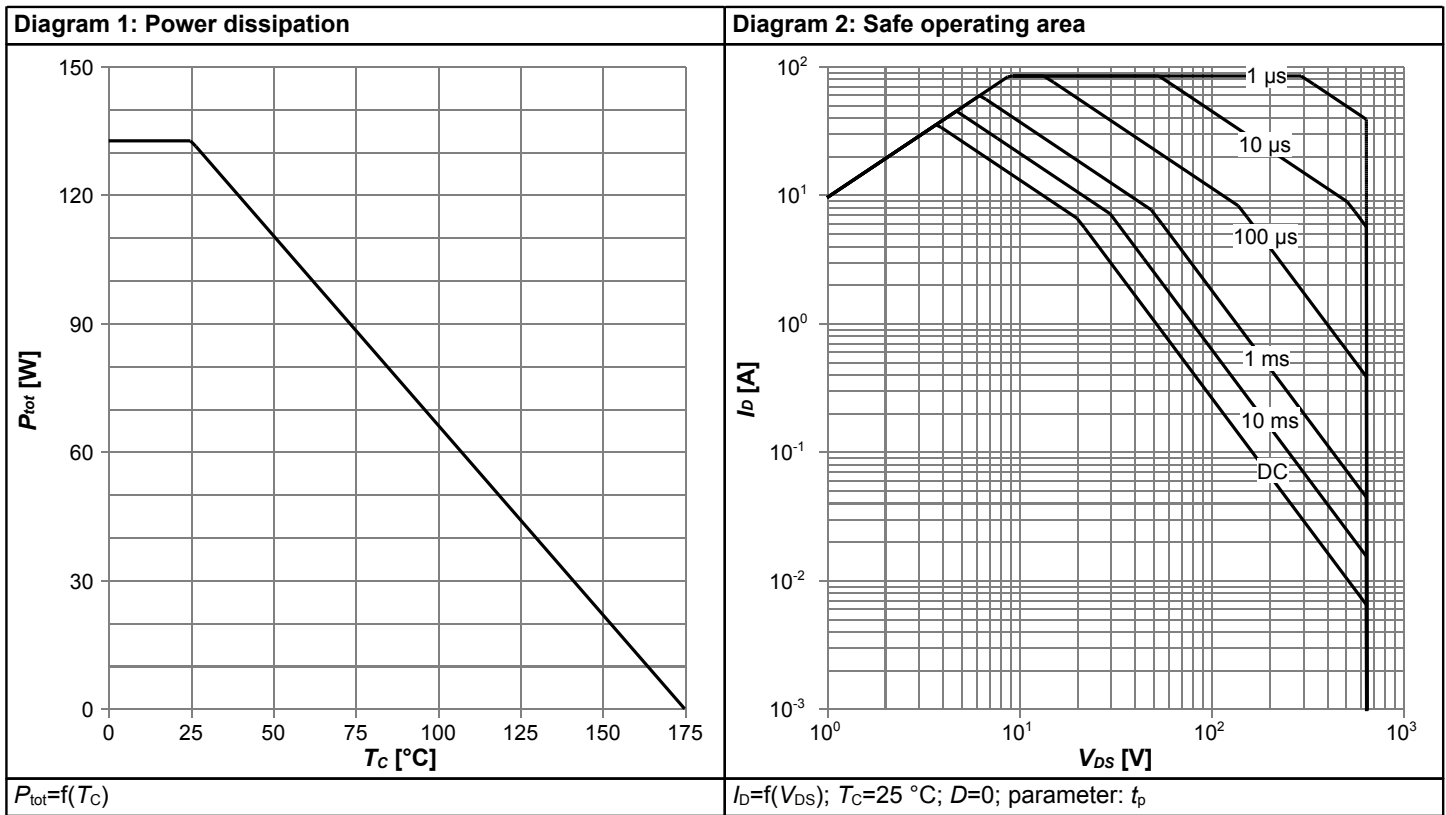
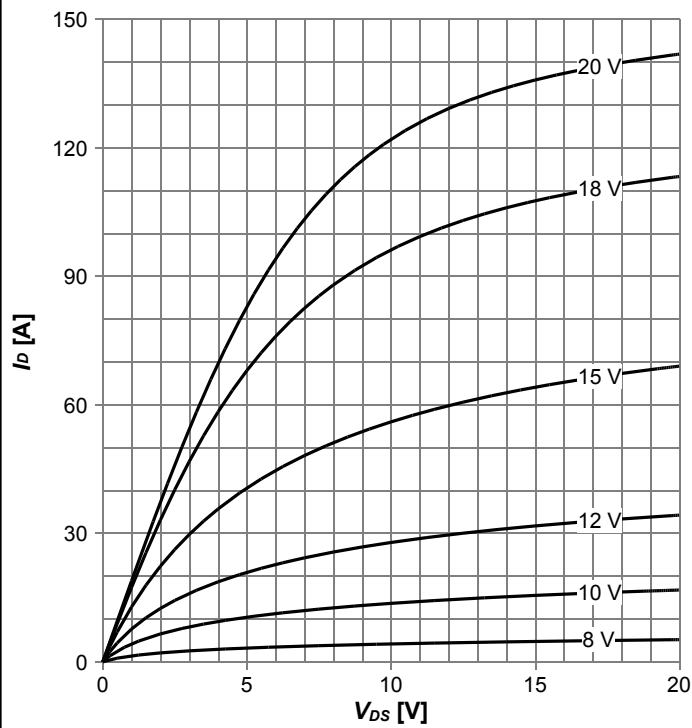
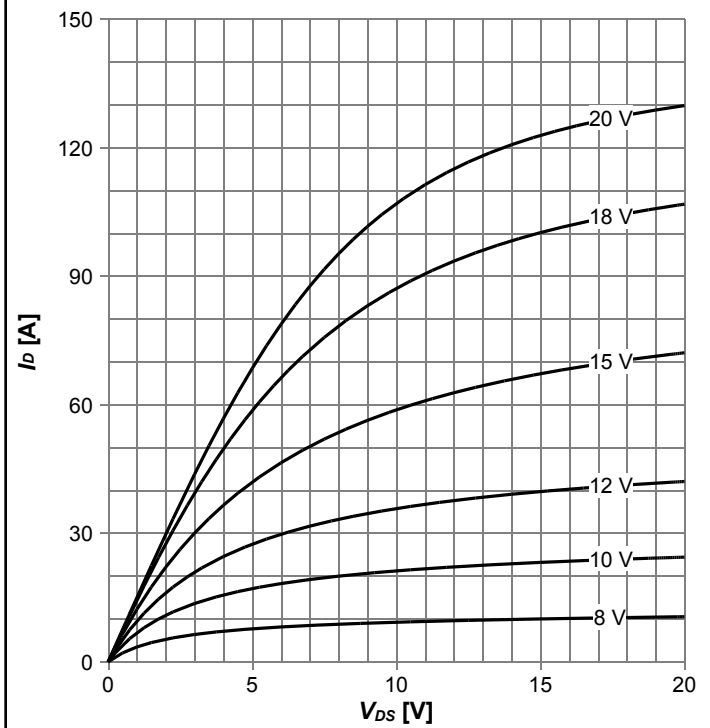


Diagram 5: Typ. output characteristics



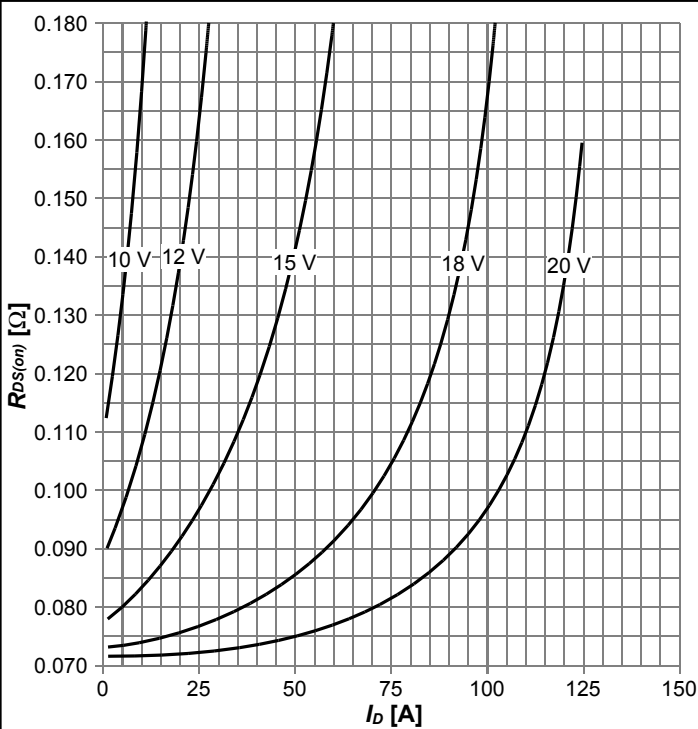
$I_D=f(V_{DS})$; $T_J=25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



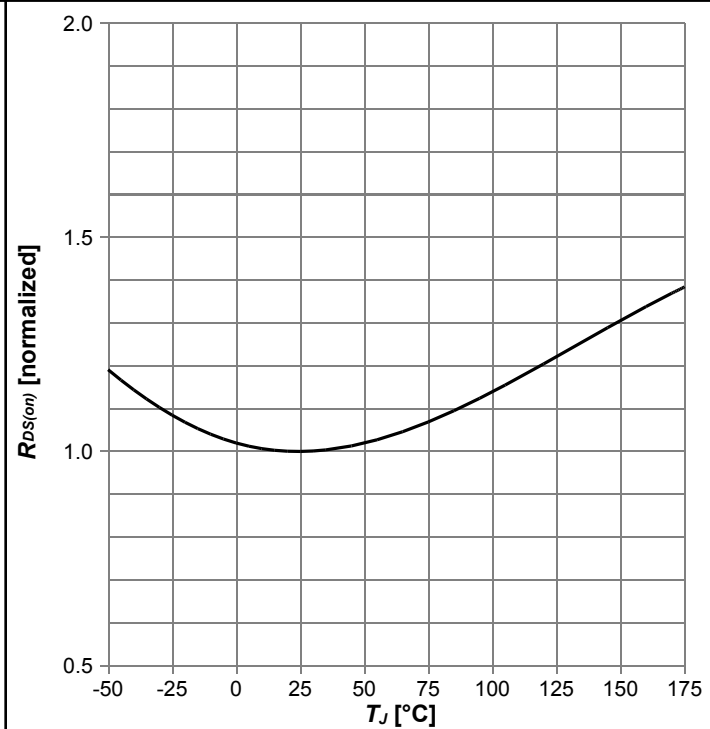
$I_D=f(V_{DS})$; $T_J=125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



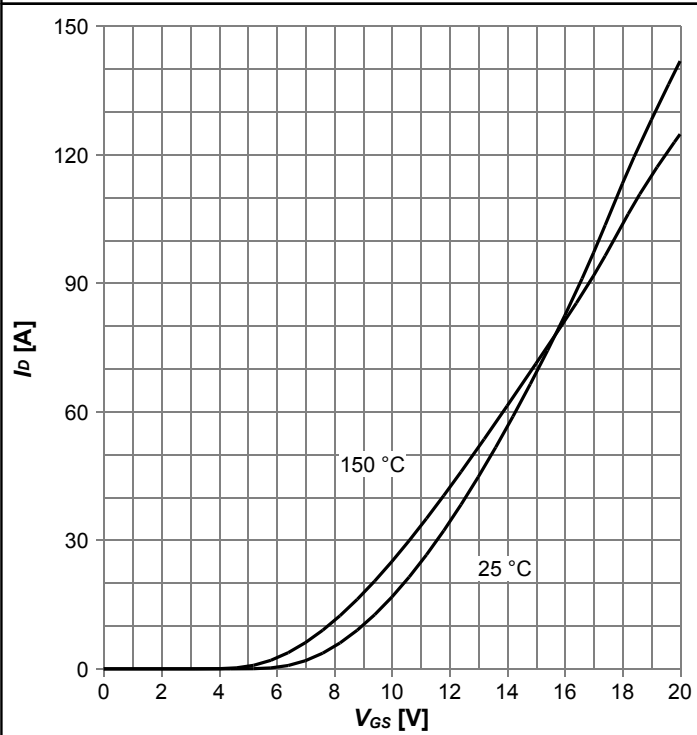
$R_{DS(on)}=f(I_D)$; $T_J=150\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



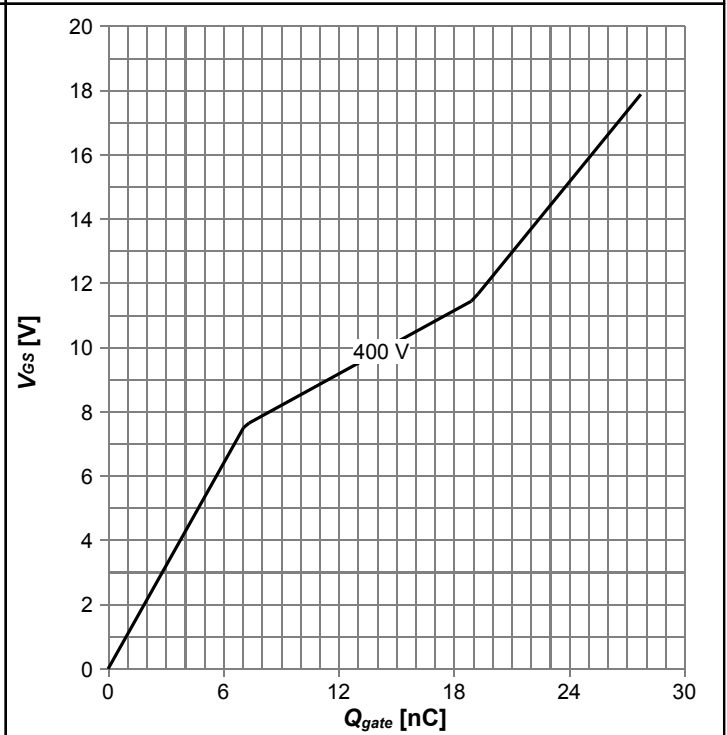
$R_{DS(on)}=f(T_J)$; $I_D=16.7\text{ A}$; $V_{GS}=18\text{ V}$

Diagram 9: Typ. transfer characteristics



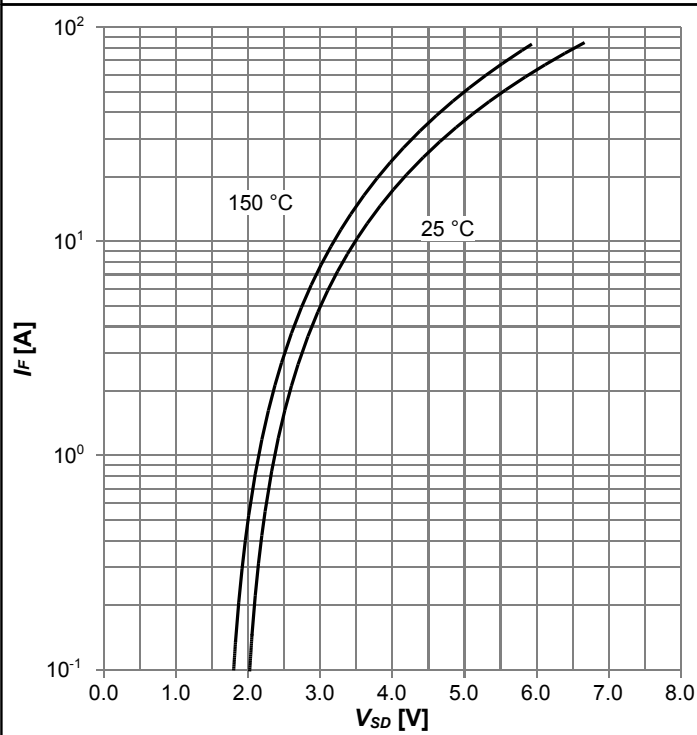
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



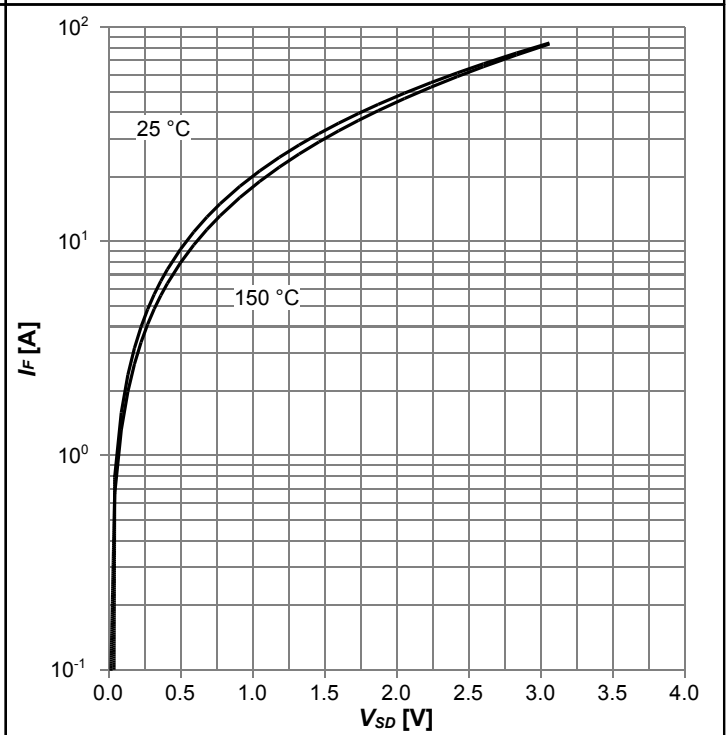
$V_{GS} = f(Q_{gate})$; $I_D = 16.7 A$ pulsed; parameter: V_{DD}

Diagram 11: Typ. forward characteristics of reverse diode



$I_F = f(V_{SD})$; parameter: T_j

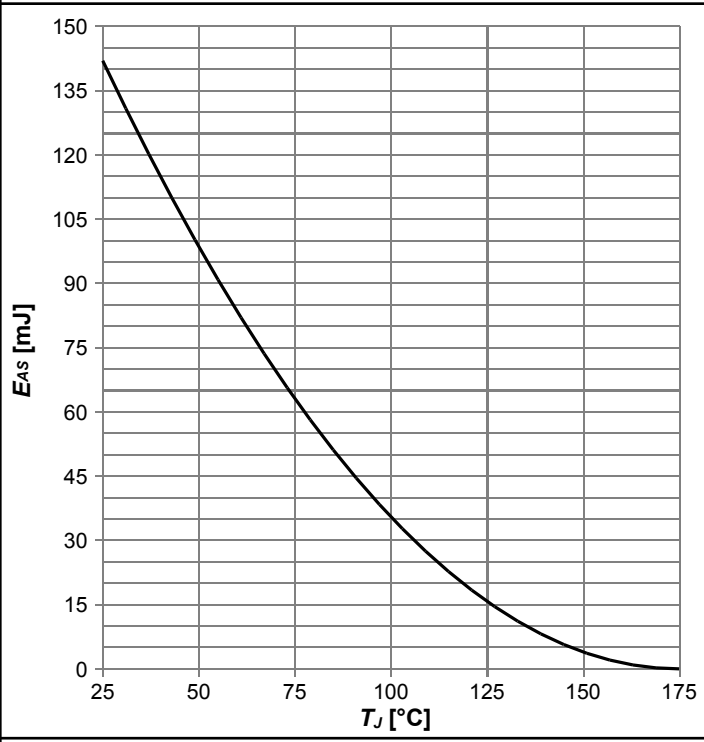
Diagram 12: Typ. channel reverse characteristics



$I_F = f(V_{SD})$; $V_{GS} = 18 V$; parameter: T_j

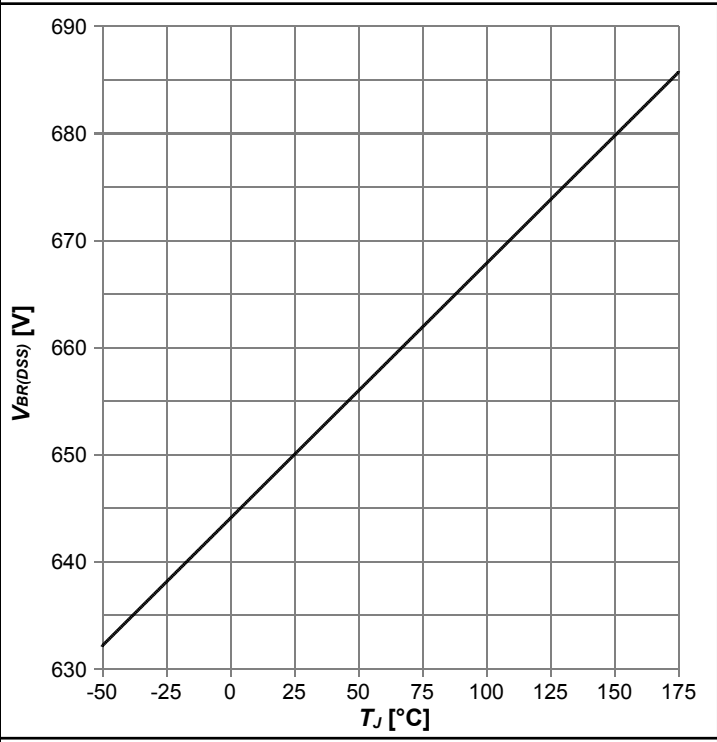


Diagram 13: Avalanche energy



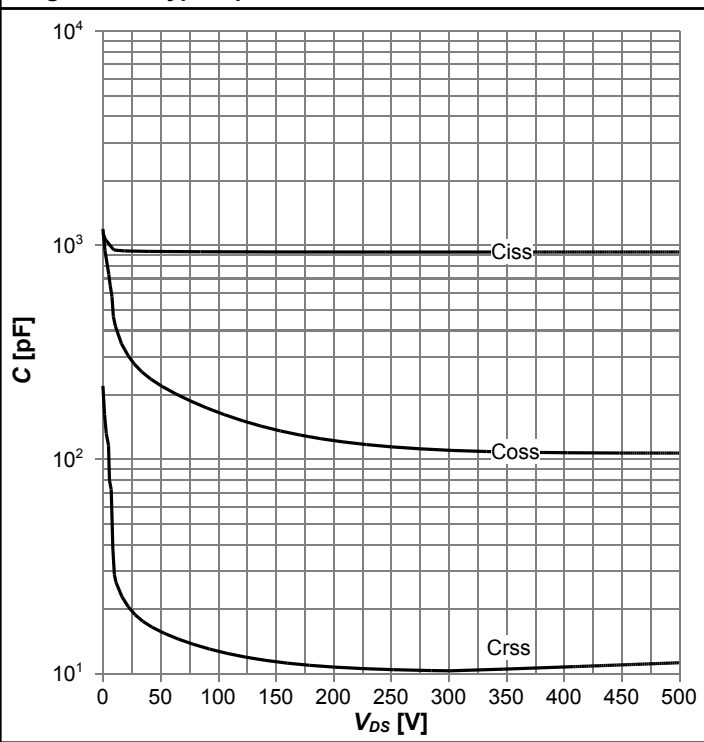
$E_{AS}=f(T_j)$; $I_D=5.3$ A; $V_{DD}=50$ V

Diagram 14: Drain-source breakdown voltage



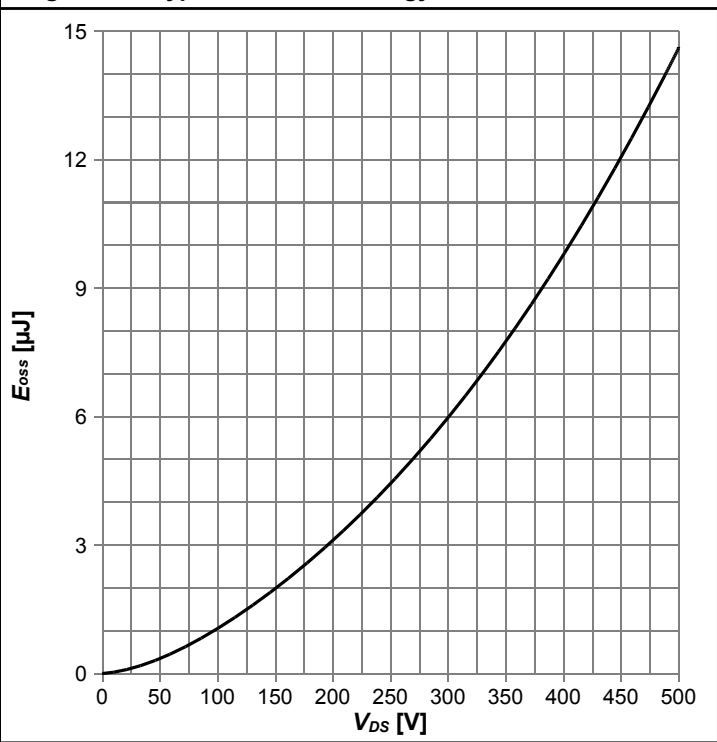
$V_{BR(DSS)}=f(T_j)$; $I_D=0.5$ mA

Diagram 15: Typ. capacitances

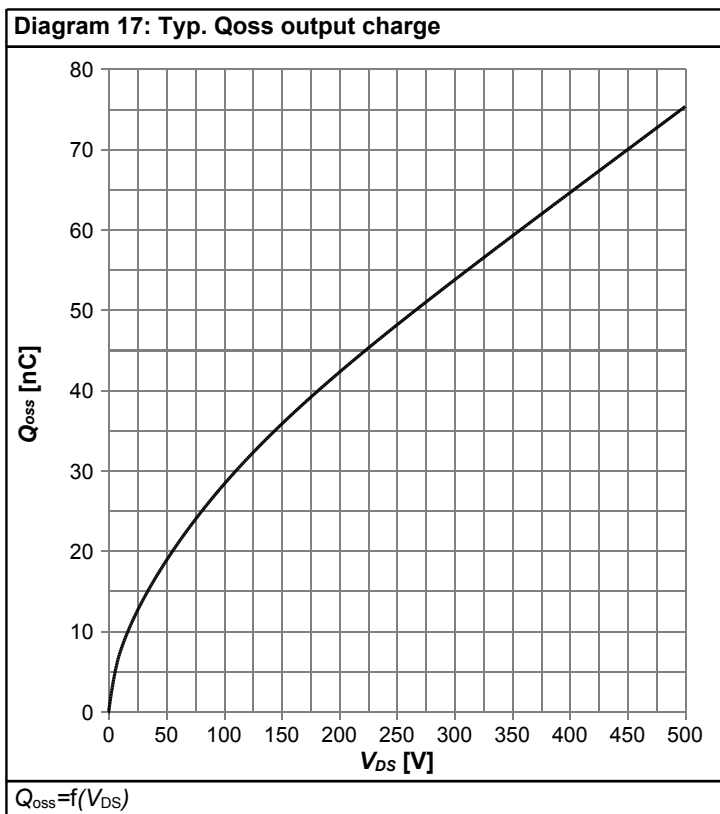


$C=f(V_{DS})$; $V_{GS}=0$ V; $f=250$ kHz

Diagram 16: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$



5 Test Circuits

Table 8 Diode characteristics (SiC)

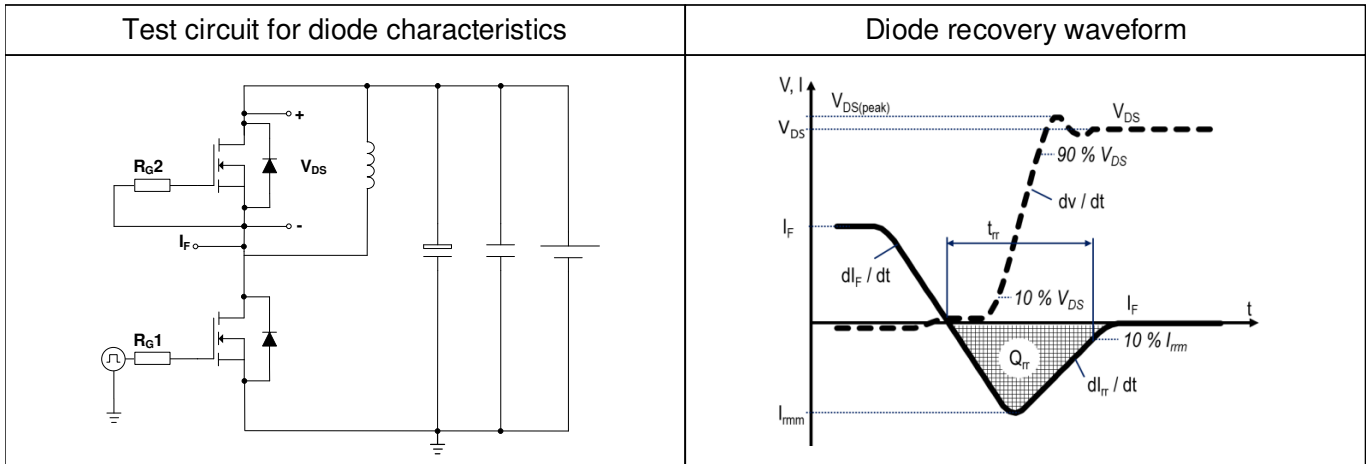


Table 9 Switching times (SiC)

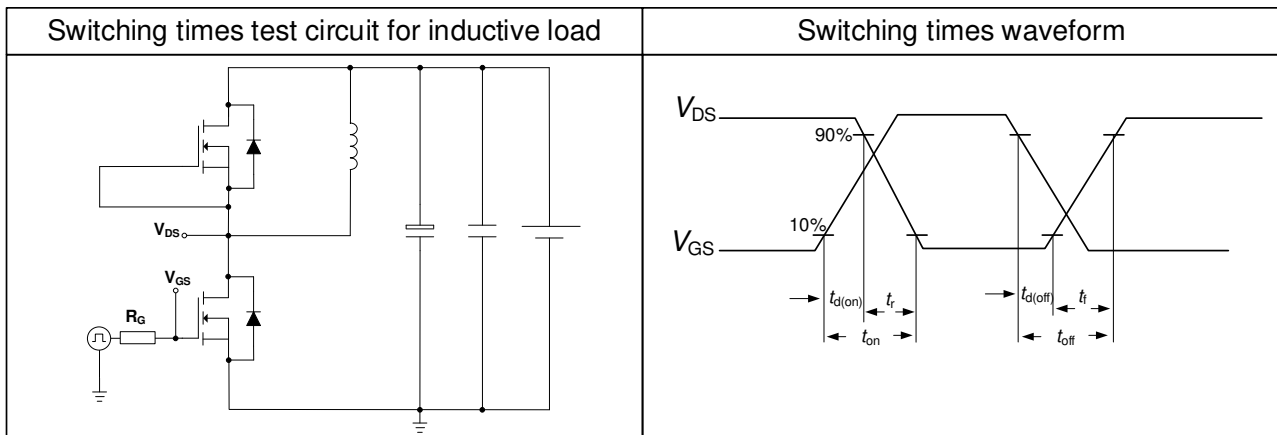
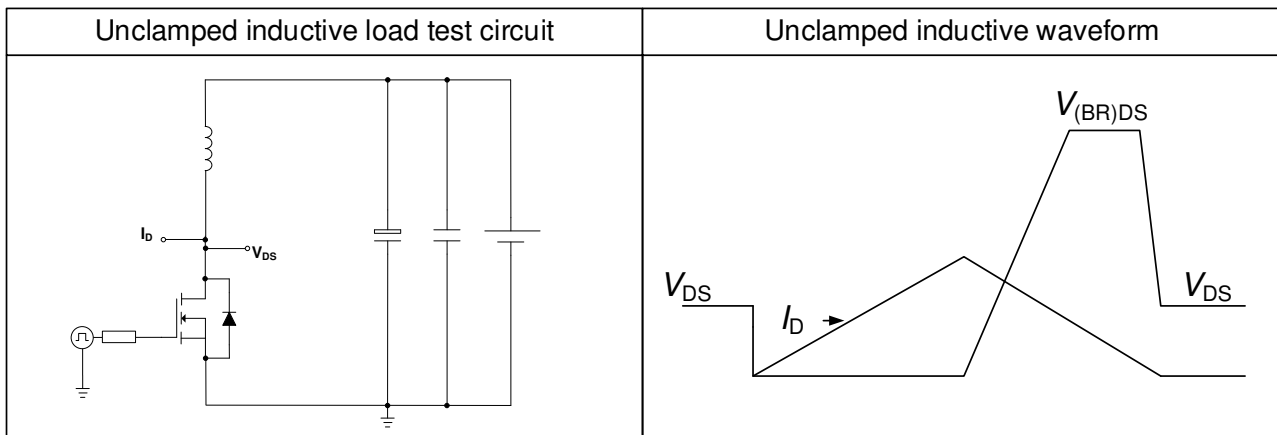
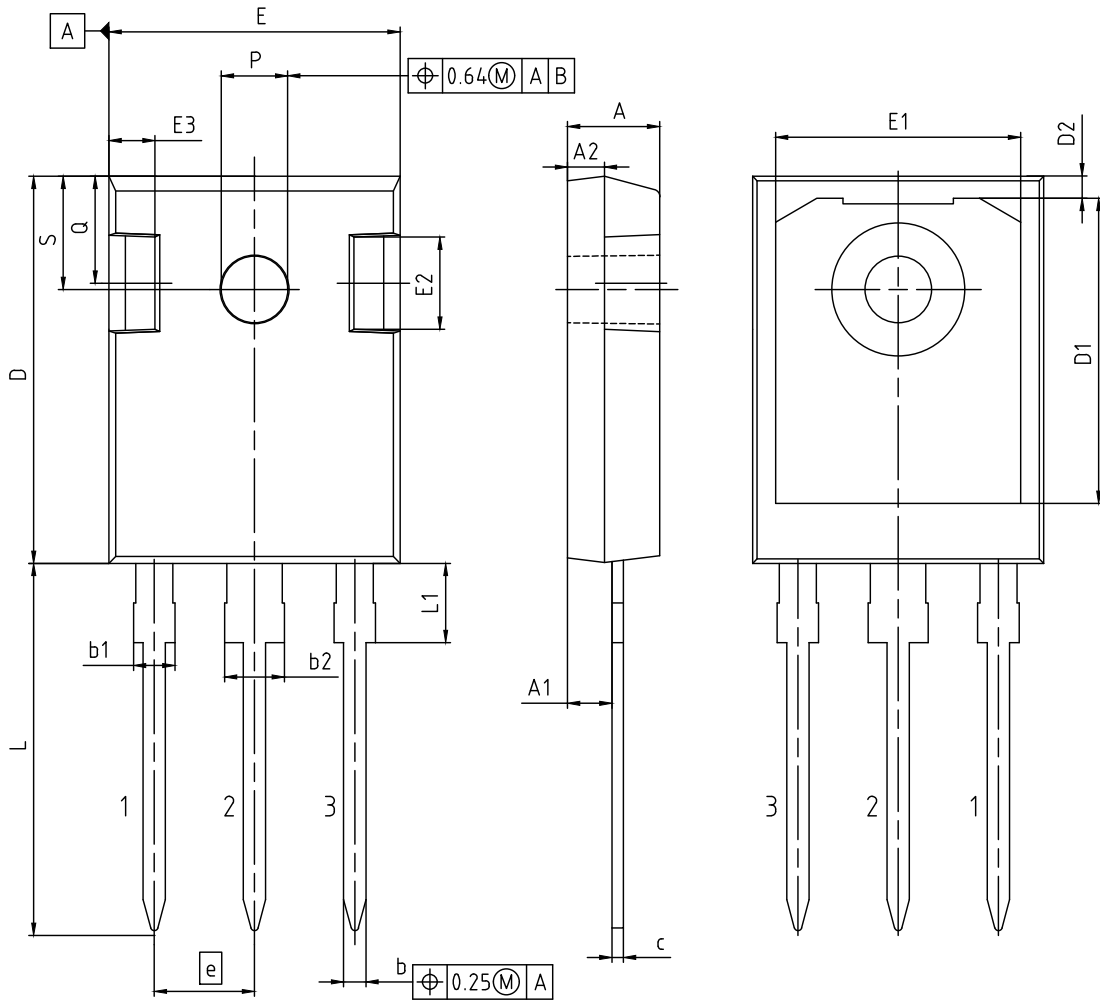


Table 10 Unclamped inductive load (SiC)



6 Package Outlines



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.70	5.30
A1	2.20	2.60
A2	1.50	2.50
b	1.00	1.40
b1	1.60	2.41
b2	2.57	3.43
c	0.38	0.89
D	20.70	21.50
D1	13.08	17.65
D2	0.51	1.35
E	15.50	16.30
E1	12.38	14.15
E2	3.40	5.10
E3	1.00	2.60
e	5.44	
L	19.80	20.40
L1	3.85	4.50
P	3.50	3.70
Q	5.35	6.25
S	6.04	6.30

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Figure 1 Outline PG-T0247-3, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolSiC M1 Webpage:** www.infineon.com
- **IFX CoolSiC M1 application note:** www.infineon.com
- **IFX CoolSiC M1 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IMW65R057M1H

Revision: 2021-03-17, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-03-17	Release of final version

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