



**THE DATASHEET OF  
IPDQ60R010S7XTMA1**



## THVD1428 3.3-V to 5-V RS-485 Transceiver with 3-kV Surge Protection

### 1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- 3-V to 5.5-V Supply voltage
- Bus I/O protection
  - $\pm 16$  kV HBM ESD
  - $\pm 4$  kV IEC 61000-4-2 Contact discharge
  - $\pm 8$  kV IEC 61000-4-2 Air-gap discharge
  - $\pm 4$  kV IEC 61000-4-4 Electrical fast transient
  - $\pm 3$  kV IEC 61000-4-5 1.2/50- $\mu$ s Surge
- Supports 20 Mbps
- Extended ambient temperature range:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Extended operational common-mode range:  $\pm 12$  V
- Receiver hysteresis for noise rejection: 30 mV
- Low power consumption
  - Standby supply current:  $< 2 \mu\text{A}$
  - Current during operation:  $< 3$  mA
- Glitch-free power-up/down for hot plug-in capability
- Open, short, and idle bus fail-safe
- 1/8 Unit load (Up to 256 bus nodes)
- Industry standard 8-Pin SOIC for drop-in compatibility

### 2 Applications

- [Wireless infrastructure](#)
- [Building automation](#)
- [HVAC systems](#)
- [Factory automation & control](#)
- [Grid infrastructure](#)
- [Smart meters](#)
- [Process analytics](#)
- [Video surveillance](#)

### 3 Description

THVD1428 is a half-duplex RS-485 transceiver with integrated surge protection. Surge protection is achieved by integrating transient voltage suppressor (TVS) diodes in the standard 8-pin SOIC (D) package. This feature provides a substantial increase in reliability for better immunity to noise transients coupled to the data cable, eliminating the need for external protection components.

This device operates from a single 3.3-V or 5-V supply and features a wide common-mode voltage range which makes it suitable for multi-point applications over long cable runs.

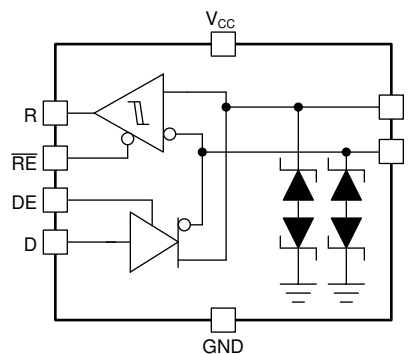
The device is available in the industry standard SOIC package for easy drop-in without any PCB changes. The device is characterized over ambient free-air temperatures from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THVD1428	SOIC (8)	4.90 mm x 3.91 mm

(1) For all available devices, see the orderable addendum at the end of the data sheet.

#### Block Diagram



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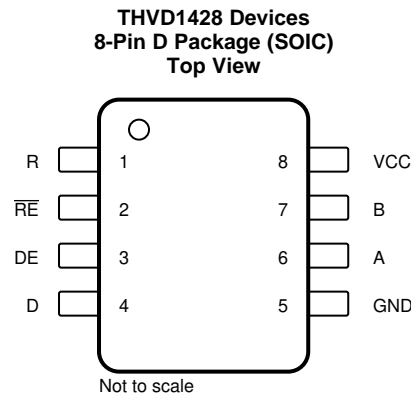
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2020	*	Initial release.

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	Bus input/output	Bus I/O port, B (complementary to A)
D	4	Digital input	Driver data input (2-M $\Omega$ internal pull-up)
DE	3	Digital input	Driver enable, active high (2-M $\Omega$ internal pull-down)
GND	5	Ground	Device ground
R	1	Digital output	Receive data output
V <sub>CC</sub>	8	Power	3.3-V to 5-V supply
$\overline{RE}$	2	Digital input	Receiver enable, active low (2-M $\Omega$ internal pull-up)

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	$V_{CC}$	-0.5	7	V
Bus voltage	Range at any bus pin (A or B) as differential or common-mode with respect to GND	-15	15	V
Input voltage	Range at any logic pin (D, DE, or /RE)	-0.3	5.7	V
Receiver output current	$I_O$	-24	24	mA
Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, 2010	±16	kV
			±8	kV
		Charged device model (CDM), per JEDEC JESD22-C101E	±1.5	kV

### 6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact Discharge, per IEC 61000-4-2	±4	kV
		Air-Gap Discharge, per IEC 61000-4-2	±8	kV
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	±4	kV
$V_{(surge)}$	Surge	Per IEC 61000-4-5, 1.2/50 $\mu$ s	±3	kV

## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3		5.5	V
V <sub>I</sub>	Input voltage at any bus terminal (separately or common mode) <sup>(1)</sup>	-12		12	V
V <sub>IH</sub>	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V <sub>ID</sub>	Differential input voltage	-12		12	V
I <sub>O</sub>	Output current, driver	-60		60	mA
I <sub>OR</sub>	Output current, receiver	-8		8	mA
R <sub>L</sub>	Differential load resistance	54			Ω
1/t <sub>UI</sub>	Signaling rate: THVD1428			20	Mbps
T <sub>A</sub>	Operating ambient temperature	-40		125	°C
T <sub>J</sub>	Junction temperature	-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		THVD1428	UNIT
		D (SOIC)	
		8-PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	120.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	62.8	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	62.2	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

## 6.6 Power Dissipation

PARAMETER	Description	TEST CONDITIONS	VALUE	UNIT
P <sub>D</sub>	Driver and receiver enabled, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = 125 °C, 50% duty cycle square wave at maximum signaling rate, THVD1428	Unterminated: R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF	350	mW
		RS-422 load: R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 50 pF	290	mW
		RS-485 load: R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF	300	mW

## 6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>Driver</b>							
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 60 \Omega, -12 \text{ V} \leq V_{\text{test}} \leq 12 \text{ V}$ , see <a href="#">Figure 7</a>		1.5	3.5		V
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 60 \Omega, -12 \text{ V} \leq V_{\text{test}} \leq 12 \text{ V}, 4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ , see <a href="#">Figure 7</a>		2.1			V
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 100 \Omega$ , see <a href="#">Figure 8</a>		2	4		V
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 54 \Omega$ , see <a href="#">Figure 8</a>		1.5	3.5		V
$\Delta V_{OD} $	Change in differential output voltage	$R_L = 54 \Omega$ , see <a href="#">Figure 8</a>		-200		200	mV
$V_{OC}$	Common-mode output voltage			1	$V_{CC} / 2$	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			-200		200	mV
$I_{OS}$	Short-circuit output current	$DE = V_{CC}, -7 \text{ V} \leq V_O \leq 12 \text{ V}$		-250		250	mA
<b>Receiver</b>							
$I_I$	Bus input current	$DE = 0 \text{ V}, V_{CC} = 0 \text{ V or } 5.5 \text{ V}$	$V_I = 12 \text{ V}$		50	125	$\mu\text{A}$
			$V_I = -7 \text{ V}$	-100	-65		$\mu\text{A}$
			$V_I = -12 \text{ V}$	-150	-100		$\mu\text{A}$
$V_{TH+}$	Positive-going input threshold voltage	Over common-mode range of $\pm 12 \text{ V}$		See <sup>(1)</sup>	-100	-20	mV
$V_{TH-}$	Negative-going input threshold voltage			-200	-130	See <sup>(1)</sup>	mV
$V_{HYS}$	Input hysteresis				30		mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, $f = 1 \text{ MHz}$			220		pF
$V_{OH}$	Output high voltage	$I_{OH} = -8 \text{ mA}$		$V_{CC} - 0.4$	$V_{CC} - 0.3$		V
$V_{OL}$	Output low voltage	$I_{OL} = 8 \text{ mA}$			0.2	0.4	V
$I_{OZR}$	Output high-impedance current	$V_O = 0 \text{ V or } V_{CC}, \overline{RE} = V_{CC}$		-1		1	$\mu\text{A}$
<b>Logic</b>							
$I_{IN}$	Input current (D, DE, $\overline{RE}$ )	$4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$		-6.2		6.2	$\mu\text{A}$
<b>Device</b>							
$I_{CC}$	Supply current (quiescent)	Driver and receiver enabled	$\overline{RE} = 0 \text{ V}, DE = V_{CC}, \text{No load}$		2.4	3	mA
		Driver enabled, receiver disabled	$\overline{RE} = V_{CC}, DE = V_{CC}, \text{No load}$		2	2.6	mA
		Driver disabled, receiver enabled	$\overline{RE} = 0 \text{ V}, DE = 0 \text{ V}, \text{No load}$		700	960	$\mu\text{A}$
		Driver and receiver disabled	$\overline{RE} = V_{CC}, DE = 0 \text{ V}, D = \text{open}, \text{No load}$		0.1	2	$\mu\text{A}$
$T_{SD}$	Thermal shutdown temperature				170		$^{\circ}\text{C}$

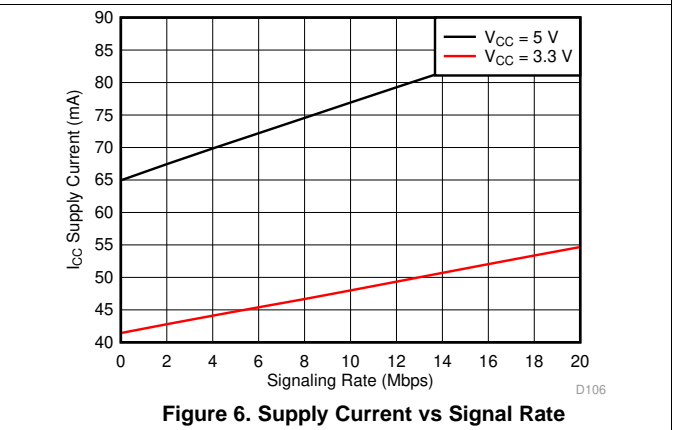
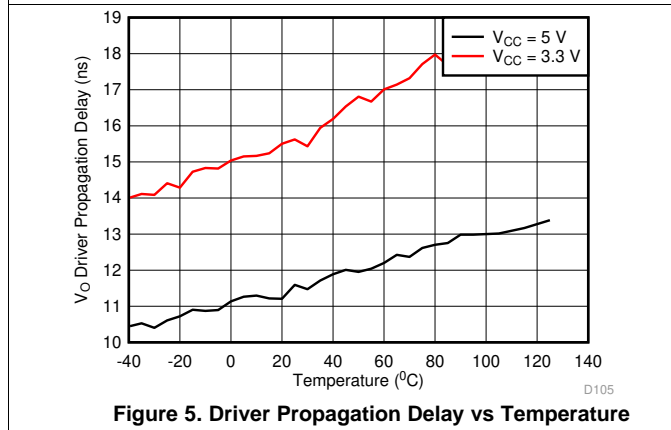
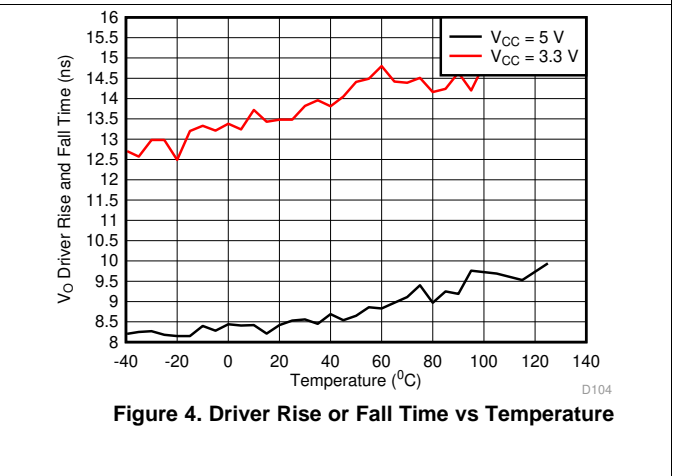
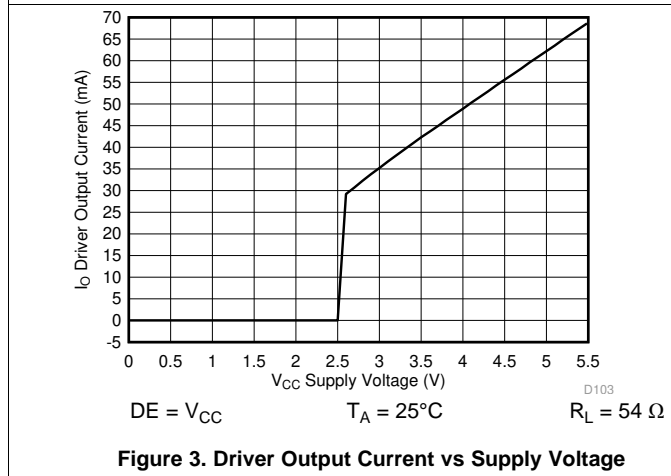
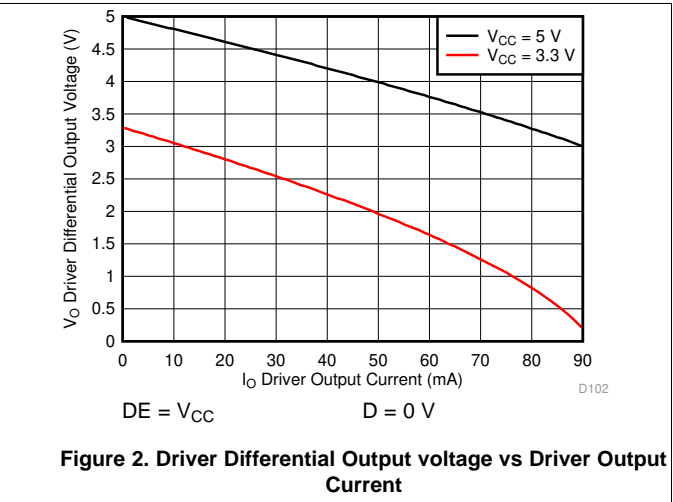
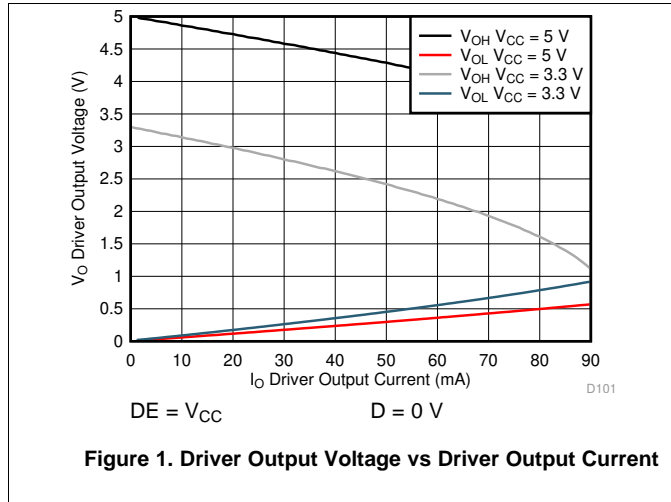
 (1) Under any specific conditions,  $V_{TH+}$  is assured to be at least  $V_{HYS}$  higher than  $V_{TH-}$ .

## 6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Driver: THVD1428</b>						
$t_r, t_f$	Differential output rise / fall time	$R_L = 54 \Omega, C_L = 50 \text{ pF}$ , see <a href="#">Figure 9</a>		9	16	ns
$t_{PHL}, t_{PLH}$	Propagation delay			12	25	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				6	ns
$t_{PHZ}, t_{PLZ}$	Disable time			18	40	ns
$t_{PZH}, t_{PZL}$	Enable time	$\overline{RE} = 0 \text{ V}$ , see <a href="#">Figure 10</a> and <a href="#">Figure 11</a>		16	40	ns
		$\overline{RE} = V_{CC}$ , see <a href="#">Figure 10</a> and <a href="#">Figure 11</a>		2.8	11	$\mu\text{s}$
<b>Receiver: THVD1428</b>						
$t_r, t_f$	Output rise / fall time	$C_L = 15 \text{ pF}$ , see <a href="#">Figure 12</a>		2	6	ns
$t_{PHL}, t_{PLH}$	Propagation delay			12	45	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				6	ns
$t_{PHZ}, t_{PLZ}$	Disable time			14	28	ns
$t_{PZH(1)}, t_{PZL(1)}, t_{PZH(2)}, t_{PZL(2)}$	Enable time	$DE = V_{CC}$ , see <a href="#">Figure 13</a>		75	110	ns
		$DE = 0 \text{ V}$ , see <a href="#">Figure 14</a>		4.8	14	$\mu\text{s}$

## 6.9 Typical Characteristics



## 7 Parameter Measurement Information

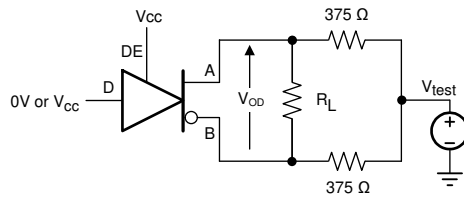


Figure 7. Measurement of Driver Differential Output Voltage With Common-Mode Load



Figure 8. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

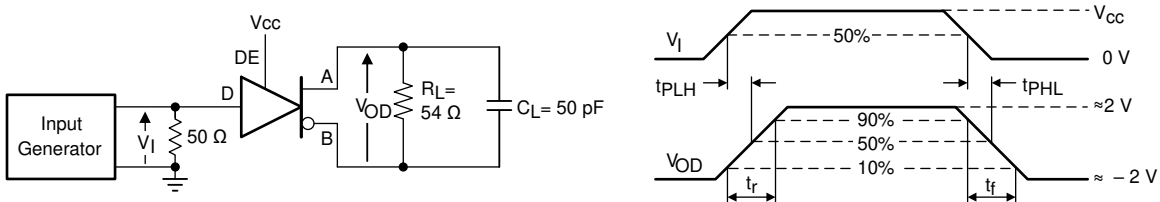


Figure 9. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

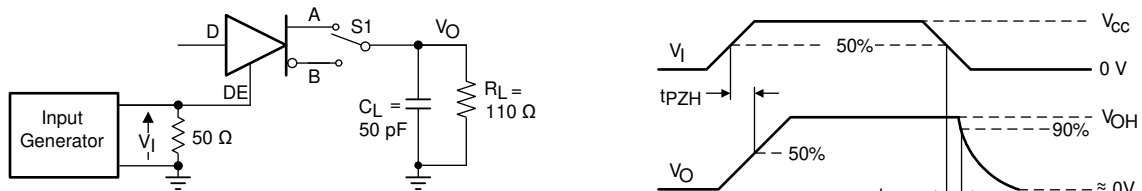


Figure 10. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

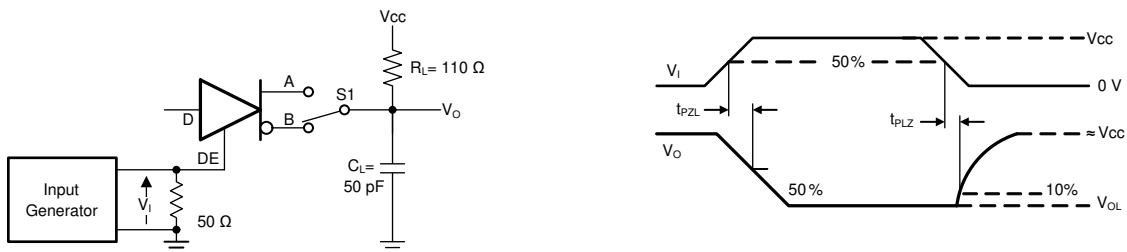


Figure 11. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

Parameter Measurement Information (continued)

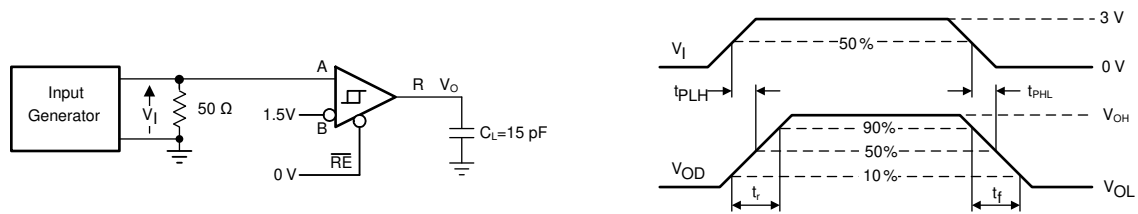


Figure 12. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

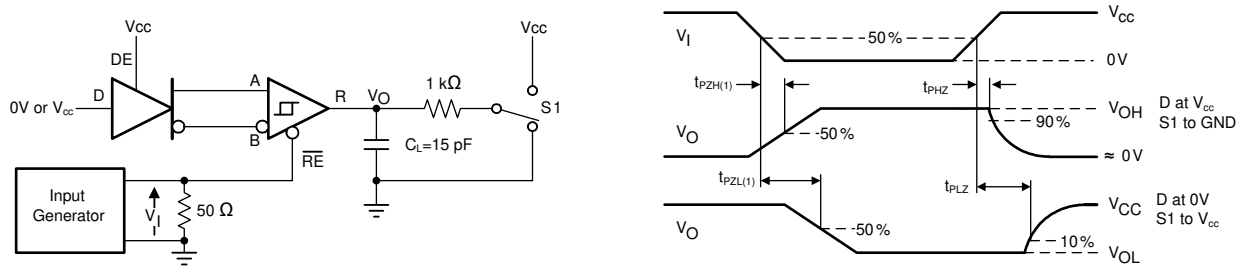


Figure 13. Measurement of Receiver Enable/Disable Times With Driver Enabled

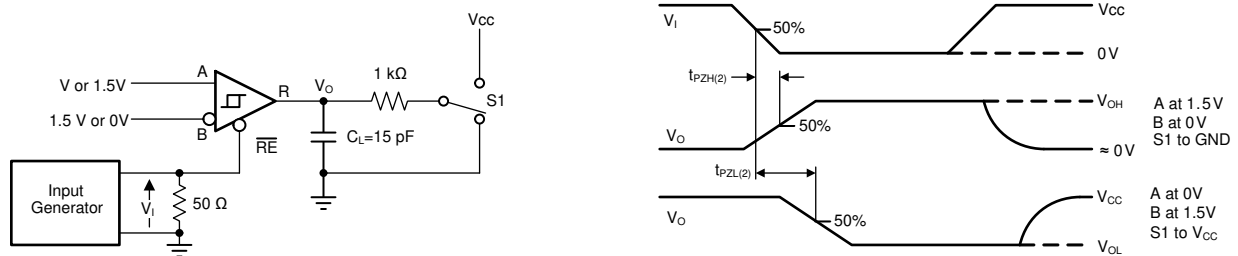


Figure 14. Measurement of Receiver Enable Times With Driver Disabled

## 8 Detailed Description

### 8.1 Overview

THVD1428 is surge-protected, half duplex RS-485 transceiver suitable for data transmission up to 20 Mbps. Surge protection is achieved by integrating transient voltage suppresser (TVS) diodes in the standard 8-pin SOIC (D) package.

The device has active-high driver enable and active-low receiver enable. A standby current of less than 2  $\mu\text{A}$  can be achieved by disabling both driver and receiver.

### 8.2 Functional Block Diagrams

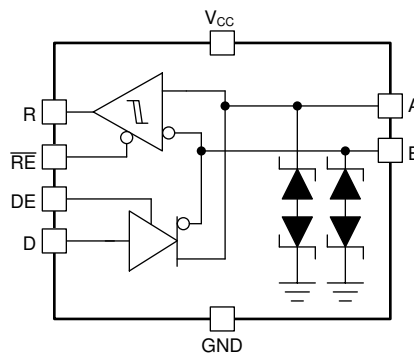


Figure 15. THVD1428 Block Diagram

### 8.3 Feature Description

#### 8.3.1 Electrostatic Discharge (ESD) Protection

The bus pins of the THVD1428 transceiver includes on-chip ESD protection against  $\pm 16\text{-kV}$  HBM and  $\pm 4\text{-kV}$  IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance,  $C_{(S)}$ , and 78% lower discharge resistance,  $R_{(D)}$ , of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

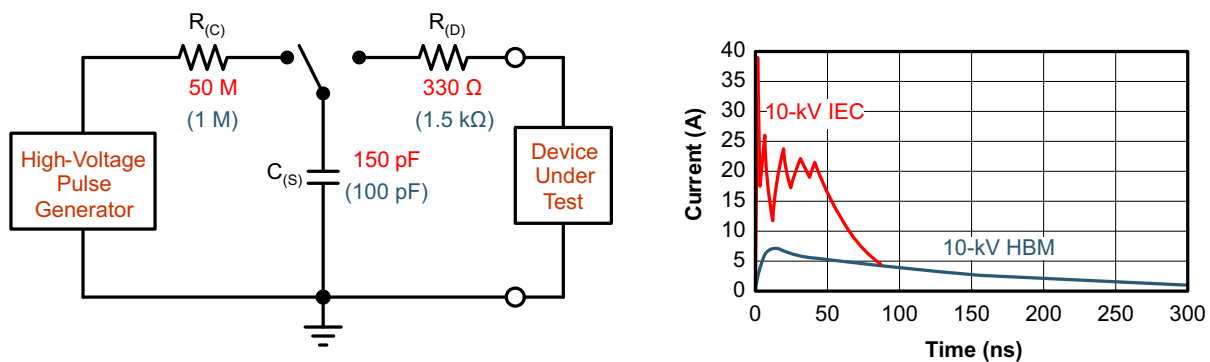


Figure 16. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables.

## Feature Description (continued)

### 8.3.2 Electrical Fast Transient (EFT) Protection

Inductive loads such as relays, switch contactors, or heavy-duty motors can create high-frequency bursts during transition. The IEC 61000-4-4 test is intended to simulate the transients created by such switching of inductive loads on AC power lines. Figure 17 shows the voltage waveforms in to 50-Ω termination as defined by the IEC standard.

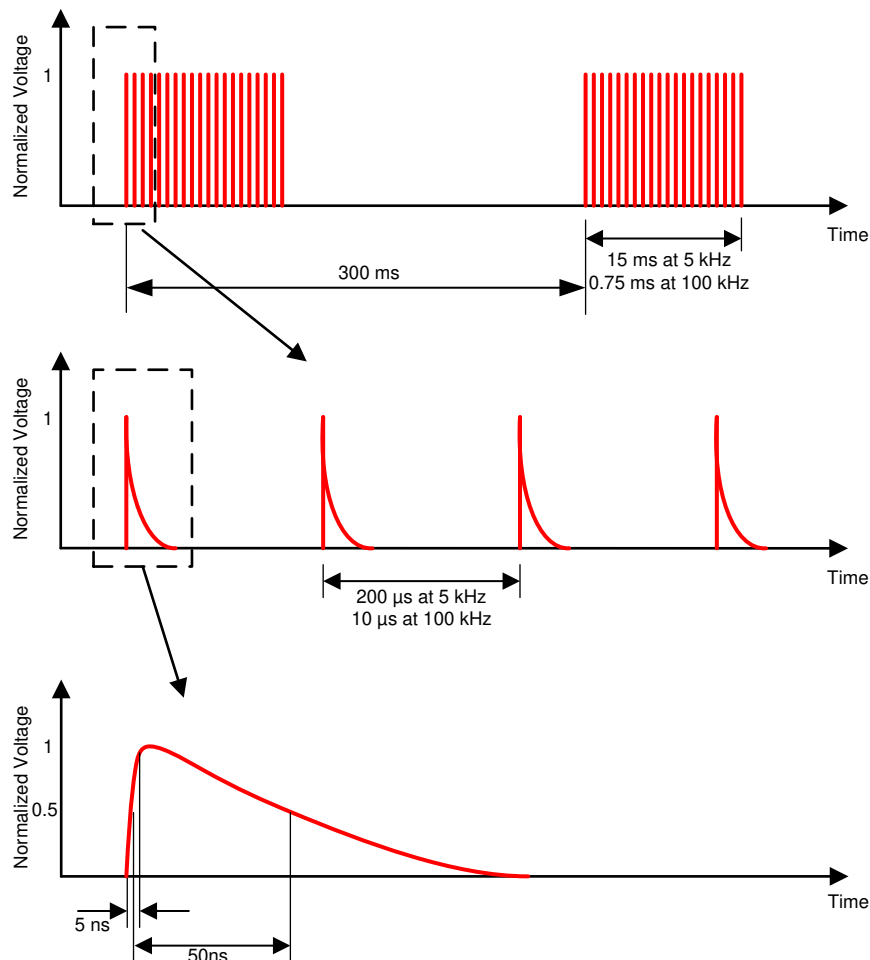


Figure 17. EFT Voltage Waveforms

Internal ESD protection circuits of the THVD1428 protect the transceiver against EFT  $\pm 4$  kV.

### 8.3.3 Surge Protection

Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 18 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

Feature Description (continued)

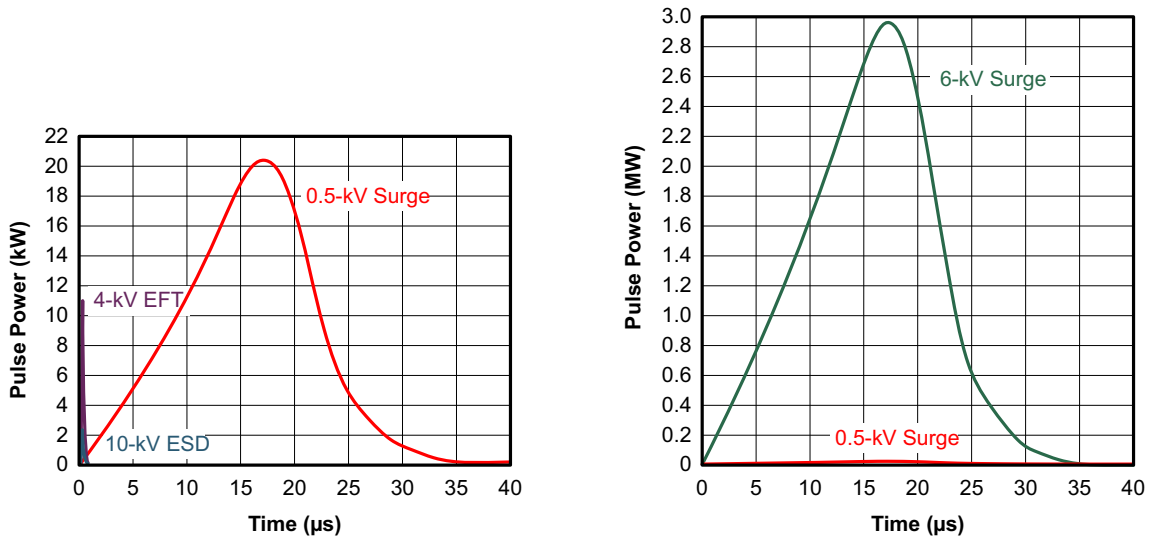


Figure 18. Power Comparison of ESD, EFT, and Surge Transients

Figure 19 shows the test setup used to validate THVD1428 surge performance according to the IEC 61000-4-5 1.2/50-µs surge pulse.

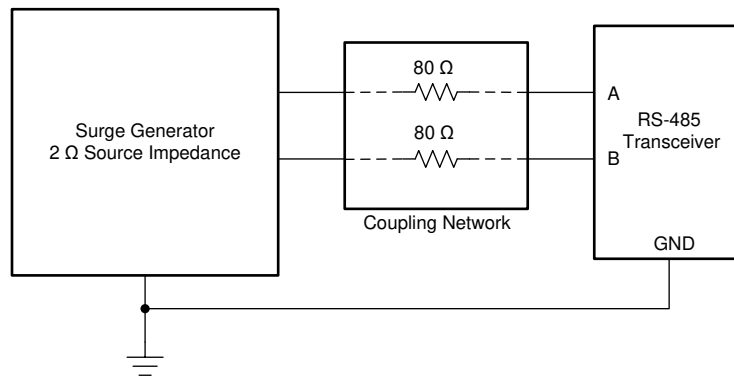


Figure 19. THVD1428 Surge Test Setup

THVD1428 is robust to ±3-kV surge transients without the need for any external components.

8.3.4 Failsafe Receiver

The differential receiver of THVD1428 is failsafe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

## 8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as  $V_{OD} = V_A - V_B$  is positive. When D is low, the output states reverse: B turns high, A becomes low, and  $V_{OD}$  is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor of 2-M $\Omega$  to  $V_{CC}$ , thus, when left open while the driver is enabled, output A turns high and B turns low.

**Table 1. Driver Function Table**

INPUT D	ENABLE DE	OUTPUTS		FUNCTION
		A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin,  $\overline{RE}$ , is logic low, the receiver is enabled. When the differential input voltage defined as  $V_{ID} = V_A - V_B$  is higher than the positive input threshold,  $V_{TH+}$ , the receiver output, R, turns high. When  $V_{ID}$  is lower than the negative input threshold,  $V_{TH-}$ , the receiver output, R, turns low. If  $V_{ID}$  is between  $V_{TH+}$  and  $V_{TH-}$ , the output is indeterminate.

When  $\overline{RE}$  is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of  $V_{ID}$  are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

**Table 2. Receiver Function Table**

DIFFERENTIAL INPUT $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	FUNCTION
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

THVD1428 is a half-duplex RS-485 transceiver with integrated system-level surge protection. Standard 8-pin SOIC (D) package allows drop-in replacement into existing systems and eliminate system-level protection components.

### 9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor,  $R_T$ , whose value matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

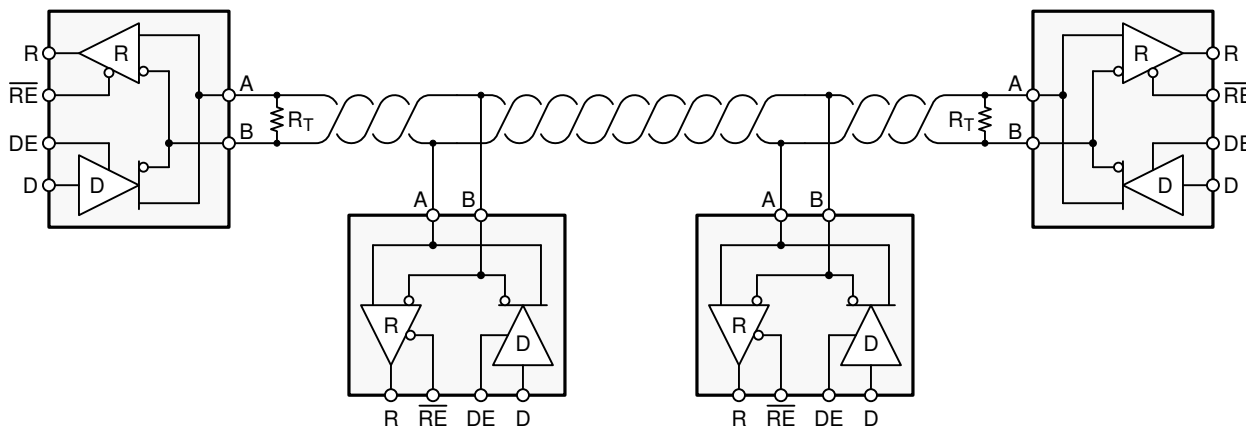


Figure 20. Typical RS-485 Network With Half-Duplex Transceivers

#### 9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

##### 9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

Typical Application (continued)

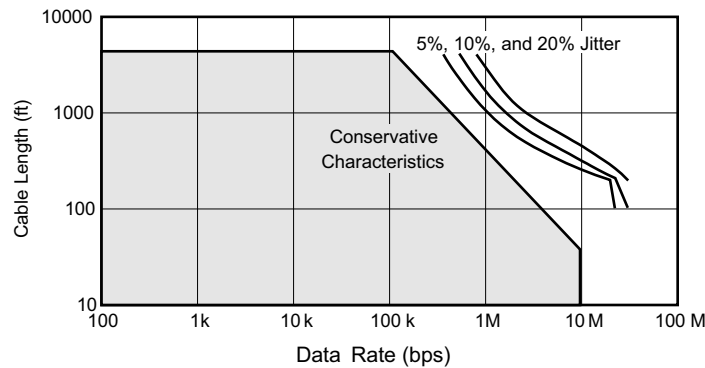


Figure 21. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 20 Mbps for the THVD1428) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c$$

where

- $t_r$  is the 10/90 rise time of the driver
- $c$  is the speed of light ( $3 \times 10^8$  m/s)
- $v$  is the signal velocity of the cable or trace as a factor of  $c$

(1)

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD1428 device consists of 1/8 UL transceiver, connecting up to 256 receivers to the bus is possible.

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

RS-485 transceivers operate in noisy industrial environments typically require surge protection at the bus pins. Figure 22 compares 1-kV surge protection implementation with a regular RS-485 transceiver (such as THVD14x0) against with the THVD1428. The internal TVS protection of the THVD1428 achieves  $\pm 3$  kV IEC 61000-4-5 surge protection without any additional external components, reducing system level bill of materials.

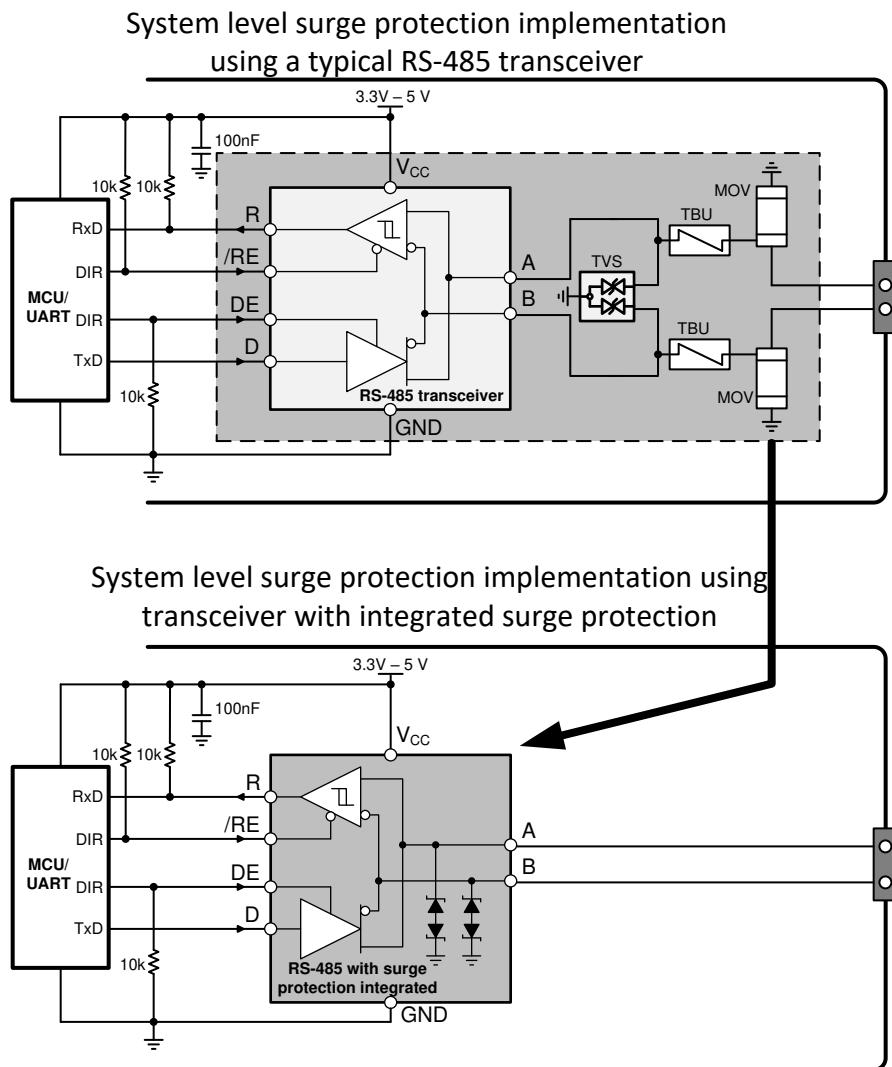
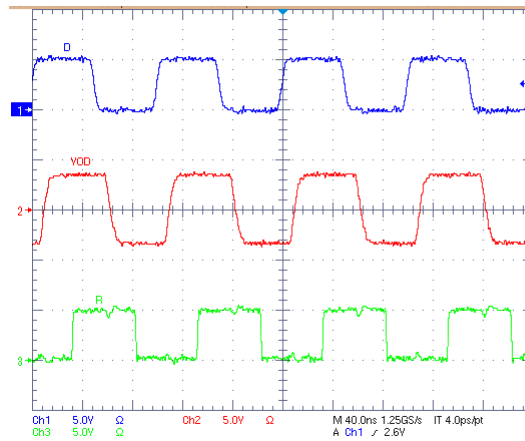


Figure 22. Implementation of System-Level Surge Protection Using THVD1428

## Typical Application (continued)

### 9.2.3 Application Curves



$V_{CC} = 5\text{ V}$     54- $\Omega$  Termination     $T_A = 25^\circ\text{C}$

**Figure 23. THVD1428 Waveforms at 20 Mbps**

## 10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

## 11 Layout

### 11.1 Layout Guidelines

Additional external protection components generally are not needed when using THVD1428 transceivers.

1. Use  $V_{CC}$  and ground planes to provide low-inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the  $V_{CC}$  pins of transceiver, UART and/or controller ICs on the board.
2. Use at least two vias for  $V_{CC}$  and ground connections of decoupling capacitors to minimize effective via-inductance.
3. Use 1-k $\Omega$  to 10-k $\Omega$  pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.

### 11.2 Layout Example

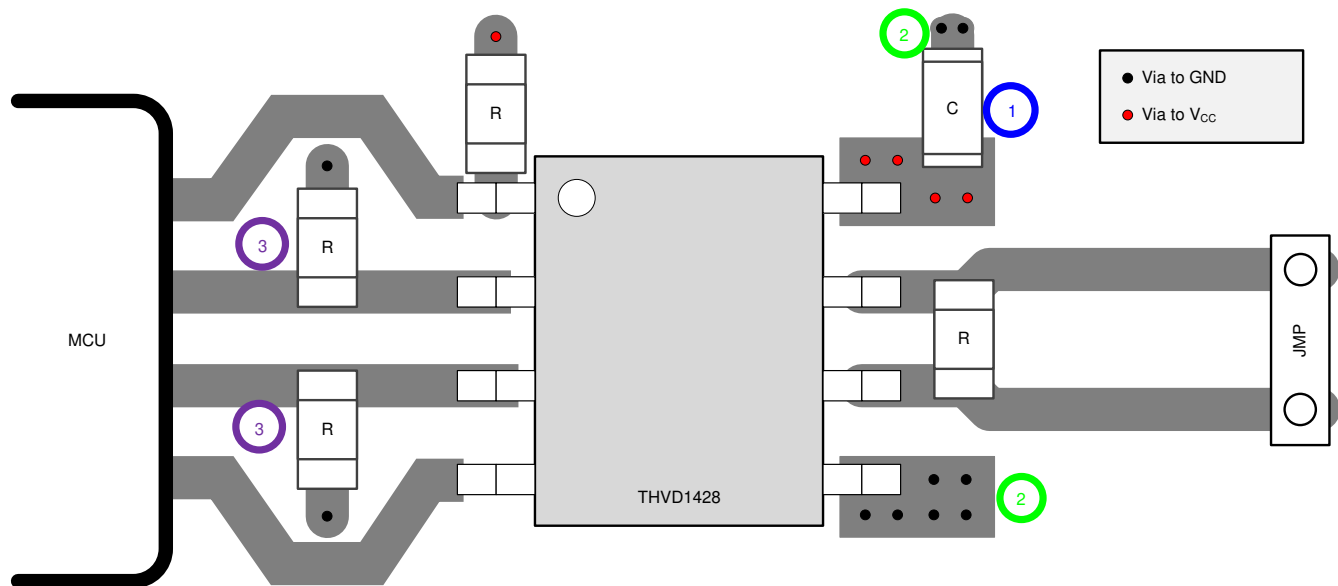


Figure 24. Half-Duplex Layout Example

## 12 Device and Documentation Support

### 12.1 Device Support

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.4 Trademarks

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### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THVD1428DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1428	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

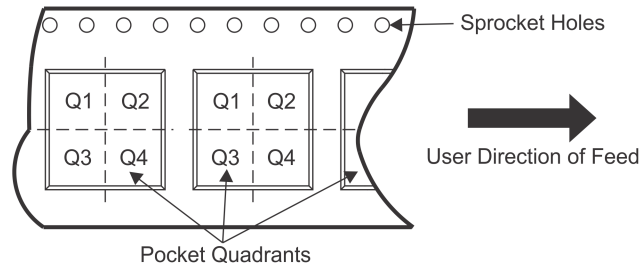
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1428DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1428DR	SOIC	D	8	2500	346.0	346.0	29.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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