# THE DATASHEET OF

# EV-SOMCRR-EZKIT

# *EV-SOMCRR-EZKIT* ® Manual

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82-EV-SOMCRR-EZKIT-01

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ANALOG DEVICES

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# Regulatory Compliance

The *EV-SOMCRR-EZKIT* evaluation board is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer-end product or as a portion of a consumer-end product. The board is an open system design, which does not include a shielded enclosure and, therefore, may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

| | |
|---|---|
| The *EV-SOMCRR-EZKIT* evaluation board contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused boards in the protective shipping package. |  |

# Contents

## Hardware Reference

# 1 Preface

Thank you for purchasing the Analog Devices, Inc. *EV-SOMCRR-EZKIT* carrier evaluation board.

The *EV-SOMCRR-EZKIT* carrier board is a backplane plug-in card designed for use with System on Module (SoM) evaluation boards. Together, these boards create a full evaluation system to demonstrate Analog Devices embedded processor feature sets. The SoM module features the processor, required power, and external memory circuitry; and the carrier board provides all the peripheral functionality necessary to evaluate an embedded application.

The *EV-SOMCRR-EZKIT* carrier board is compatible with numerous SoM boards and works with the Analog Devices development tools to test the capabilities of Analog Devices processors.

The evaluation board is designed to be used in conjunction with the CrossCore Embedded Studio® development environment for advanced application code development and debug, with features that enable the ability to:

- Create, compile, assemble, and link application programs written in C++, C, and assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers

In addition to the system peripherals, there is an on-board debugger on the *EV-SOMCRR-EZKIT* carrier board. The on-board debugger eliminates the need to purchase the In-Circuit Emulator (ICE) that is necessary when using a SoM module in standalone mode.

## Purpose of This Manual

This manual provides instructions for installing the product hardware (board). This manual describes operation and configuration of the board components and provides guidelines for running code on the board.

## Manual Contents

The manual consists of:

- ***Using the board***

  Provides basic board information.

- *Hardware Reference*

  Provides information about the hardware aspects of the board.

- *Bill of Materials*

  A companion file in PDF format that lists all of the components used on the board is available on the website at http://www.analog.com/EV-SOMCRR-EZKIT .

- *Schematic*

  A companion file in PDF format documenting all of the circuits used on the board is available on the website at http://www.analog.com/EV-SOMCRR-EZKIT .

# Technical Support

You can reach Analog Devices technical support in one of the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:

  http://ez.analog.com/community/dsp

- Submit your questions to technical support directly at:

  http://www.analog.com/support

- E-mail your questions about processors, DSPs, and tools development software from ***CrossCore Embedded Studio*** or ***VisualDSP++***®:

  If using CrossCore Embedded Studio or VisualDSP++ choose ***Help*** > ***Email Support***. This creates an e-mail to processor.tools.support@analog.com and automatically attaches your CrossCore Embedded Studio or VisualDSP++ version information and `license.dat` file.

- E-mail your questions about processors and processor applications to:

  processor.support@analog.com

  processor.china@analog.com

- Contact your Analog Devices sales office or authorized distributor. Locate one at:

  http://www.analog.com/adi-sales

# Supported Tools

Information about code development tools for the *EV-SOMCRR-EZKIT* evaluation board and SHARC product family is available at:

http://www.analog.com/EV-SOMCRR-EZKIT

# Product Information

Product information can be obtained from the Analog Devices website and the online help system.

## Analog Devices Website

The Analog Devices website, http://www.analog.com, provides information about a broad range of products - analog integrated circuits, amplifiers, converters, transceivers, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, MyAnalog.com is a free feature of the Analog Devices website that allows customization of a web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

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## EngineerZone

EngineerZone is a technical support forum from Analog Devices, Inc. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

# 2 Using the Board

This chapter provides information on the major components and peripherals on the board, along with instructions for installing and setting up the emulation software.

## Product Overview

Below is an image of the *EV-SOMCRR-EZKIT* carrier board connected to a SoM board.

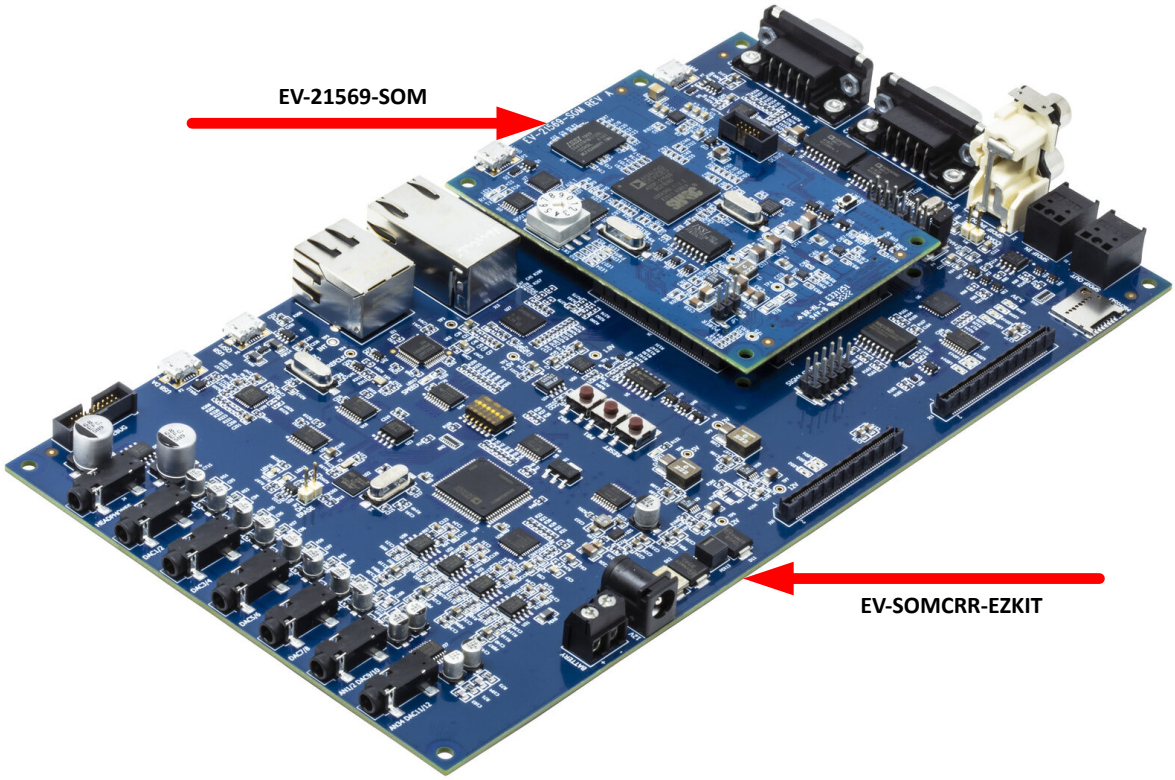


**Figure 2-1:** Board View

The board features:

- System-on-Module (SoM) connector

    - Compatible with Analog Devices DSP SoMs
- Octal SPI flash (`SPI2`) memory
    - 1Gbit
    - Macronix MX66LM1G45G - 1G-bit Serial Flash Memory with Single and Octal SPI
    - Single/Octal SPI
- SPI EEPROM
    - Microchip 25LC010AT - 1K SPI Serial EEPROM
- Audio
    - Analog Devices ADAU1962A - 12 Channel, High Performance, 192kHz, 24-Bit DAC
    - Analog Devices ADAU1979 - Quad Analog-to-Digital Converter
    - 7 3.5mm Stereo connectors: 12 outputs or 8 outputs/4 inputs and stereo headphone output
- $A^2B$
    - Two $A^2B$ interface connectors for the $A^2B$ mini modules
- Gigabit ethernet
    - TI DP83867 10/100/1000 Gigabit Ethernet
- Debug Interface (JTAG)
    - On-Board debug agent
- LEDs
    - 12 LEDs: one power (green), one board reset (red), three general-purpose (amber), six $A^2B$ LEDs, and one RGB LED for on-board debug agent
- Pushbuttons
    - Three pushbuttons: one reset and two IRQ/Flag
- External power supply
    - CE compliant
    - 12V @1.6 Amps

# Package Contents

Your *EV-SOMCRR-EZKIT* package contains the following items.

- *EV-SOMCRR-EZKIT* board

- Universal 12V DC power supply
- Two USB 2.0 type A to micro-B cable

Contact the vendor where you purchased your *EV-SOMCRR-EZKIT* evaluation board or contact Analog Devices, Inc. if any item is missing.

# Default Configuration

The ***Default Hardware Setup*** figure shows the default settings for jumpers and switches and the location of the jumpers, switches, connectors, and LEDs. Confirm that your board is in the default configuration before using the board.

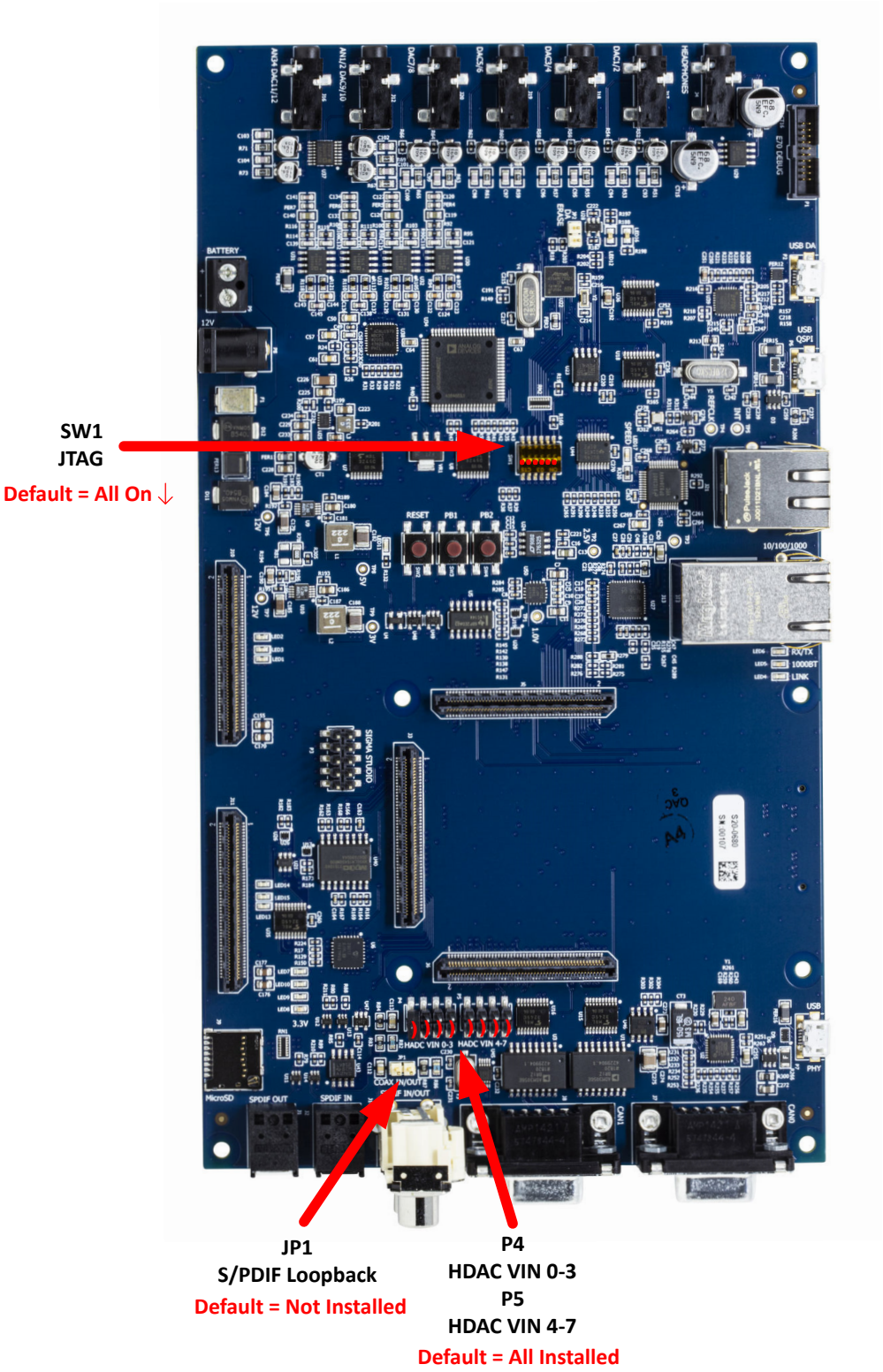


**Figure 2-2:** Default Hardware Setup

# CrossCore Embedded Studio (CCES) Setup

Information on using the CCES tools is available at: https://analog.com/cces-quickstart

# Debug Agent

The *EV-SOMCRR-EZKIT* provides a JTAG connection via an onboard Debug Agent. The Debug Agent uses a microUSB connection to the PC and allows debugging of processor SoM modules without the need of an external ICE.

To use this Debug Agent, all postions on SW1 must be in the ON position. If an emulator, such as the ICE-2000, all postions on SW1 must be in the OFF position.

# Power-On-Self Test

The Power-On-Self-Test Program (POST) tests all the EZ-KIT carrier board peripherals and validates functionality as well as connectivity to the processor. Once assembled, each EZ-KIT carrier board is fully tested for an extended period of time with POST for all the compatible SoM modules. All EZ-KIT carrier boards are shipped with POST preloaded into flash memory. The POST is executed by resetting the board and connecting the USB To UART to your PC with an open terminal window. The POST also can be used as a reference for a custom software design or hardware troubleshooting.

Note that the source code for the POST program is included in the Board Support Package (BSP) along with the readme file that describes how the board is configured to run POST.

# Reference Design Information

A reference design info package is available for download on the Analog Devices Web site. The package provides information on the schematic design, layout, fabrication, and assembly of the board.

The information can be found at:

http://www.analog.com/EV-SOMCRR-EZKIT

# Automotive Audio Bus A$^2$B Interface

The Automotive Audio Bus (A$^2$B®) provides a multichannel, I$^2$S/TDM link over distances of up to 15 m between nodes. It embeds bidirectional synchronous pulse-code modulation (PCM) data (for example, digital audio), clock, and synchronization signals onto a single differential wire pair. A$^2$B supports a direct point to point connection and allows multiple, daisy-chained nodes at different locations to contribute and/or consume time division multiplexed channel content.

The $A^2B$ Interface connects processor evaluation boards, such as the EV-SOMCRR-EZKIT to $A^2B$ daugher cards, such as the ADZS-AD2428MINI board. This allows for an expandable and configurable evaluation system for ADI DSPs and $A^2B$ technologies.

# 25LC010AT - 1K SPI Serial EEPROM

The Microchip Technology Inc. 25LC010AT is a 1 Kbit Serial Electrically Erasable Programmable Read-Only Memory (EEPROM). The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select (CS) input.

# ADAU1962A - 12 Channel, High Performance, 192kHz, 24-Bit DAC

The ADAU1962A is a high performance, single-chip digital-to-analog converter (DAC) that provides 12 DACs with differential or single-ended output using the patented Analog Devices, Inc., sigma-delta (Σ-Δ) architecture. A SPI/$I^2C$ port is included, allowing a micro-controller to adjust volume and many other parameters. The ADAU1962A operates from 2.5 V digital and 3.3 V analog supplies. A linear regulator is included to generate the digital supply voltage from the analog supply voltage.

The ADAU1962A is designed for low EMI. This consideration is apparent in both the system and circuit design architectures. By using the on-board PLL to derive the internal master clock from an external LRCLK, the ADAU1962A can eliminate the need for a separate high frequency master clock and can be used with or without a bit clock. The DACs are designed using the latest Analog Devices continuous time architectures to further minimize EMI.

# ADAU1979 - Quad Analog-to-Digital Converter

The ADAU1979 incorporates four high performance, analog-to-digital converters (ADCs) with 4.5 V rms capable ac-coupled inputs. The ADCs use a multibit sigma-delta (Σ-Δ) architecture with continuous time front end for low EMI. An $I^2C$/SPI control port is included that allows a microcontroller to adjust volume and many other parameters. The ADAU1979 uses only a single 3.3 V supply. The device internally generates the required digital DVDD supply. The low power architecture reduces the power consumption. The on-chip PLL can derive the master clock from an external clock input or frame clock (sample rate clock). When fed with the frame clock, it eliminates the need for a separate high frequency master clock in the system.

# ADM3056E - Signal and Power Isolated CAN Transceiver

The ADM3056E is a 5.7 kV rms isolated controller area network (CAN) physical layer transceiver. The ADM3056E fully meets the CAN-FD ISO 11898-2: 2016 requirements and is further capable of supporting data rates as high as 12 Mbps.

The device employs Analog Devices, Inc., iCoupler® technology to combine a highly robust 3-channel isolator and a CAN transceiver into a single SOIC, surface-mount package. The ADM3056E provides galvanic isolation between the CAN controller and physical layer bus.

Safety and regulatory approvals (pending) for 5.7 kV rms isolation withstand voltage, 849 VPEAK working insulation voltage, 8 kV surge, and 8.3 mm creepage and clearance, ensure that the ADM3056E meets isolation requirements for high voltage applications.

Low propagation delays through the isolation support longer bus cables. Slope control mode is available for standard CAN at low data rates. Standby mode can minimize power consumption when the bus is idle, or if the node goes offline. Silent mode allows the TXD input to be ignored for listen only functionality.

Dominant timeout functionality protects against bus lock-up in a fault condition, and current limiting and thermal shutdown features protect against output short circuits. The device is fully specified over the –40°C to +125°C industrial temperature range and is available in a 16-lead, increased creepage, wide-body SOIC package.

# ADM6315 - Open-Drain Microprocessor Supervisory Circuit

The ADM6315is a reliable voltage-monitoring device that is suitable for use in most voltage-monitoring applications.

The ADM6315 is designed to monitor as little as a 1.8% degradation of a power supply voltage. The ADM6315 can monitor all voltages (at 100 mV increments) from 2.5 V to 5 V.

Included in this circuit is a debounced manual reset input. RESET can be activated using an ordinary switch (pulling MR low), a low input from another digital device, or a degradation of the supply voltage.

The manual reset function is very useful, especially if the circuit in which the ADM6315 is operating enters into a state that can be detected only by the user. Allowing the user to reset a system manually can reduce the damage or danger that could otherwise be caused by an out-of-control or locked-up system.

# CS2100 - Fractional-N Clock Multiplier

The CS2100-CP is an extremely versatile system clocking device that utilizes a programmable phase lock loop. The CS2100-CP is based on a hybrid analog- digital PLL architecture comprised of a unique combination of a Delta-Sigma Fractional-N Frequency Synthesizer and a Digital PLL. This architecture allows for generation of a low-jitter clock relative to an external noisy synchronization clock at frequencies as low as 50 Hz. The CS2100-CP supports both I²C and SPI for full software control.

# DP83848C - 10/100 Ethernet Physical Layer

The DP83848C is a robust fully featured 10/100 single port Physical Layer device offering low power consumption, including several intelligent power down states. These low power modes increase overall product reliability due to decreased power dissipation. Supporting multiple intelligent power modes allows the application to use the absolute minimum amount of power needed for operation.

The DP83848C includes a 25MHz clock out. This means that the application can be designed with a minimum of external parts, which in turn results in the lowest possible total cost of the solution.

The DP83848C easily interfaces to twisted pair media via an external transformer. Both MII and RMII are supported ensuring ease and flexibility of design.

The DP83848C features integrated sublayers to support both 10BASE-T and 100BASE-TX Ethernet protocols, which ensures compatibility and interoperability with all other standards based Ethernet solutions.

## DP83867 - 10/100/1000 Ethernet Physical Layer

The DP83867 device is a robust, low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols. Optimized for ESD protection, the DP83867 exceeds 8-kV IEC 61000-4-2 (direct contact).

The DP83867 is designed for easy implementation of 10/100/1000 Mbps Ethernet LANs. It interfaces directly to twisted pair media via an external transformer. This device interfaces directly to the MAC layer through the IEEE 802.3 Standard Media Independent Interface (MII), the IEEE 802.3 Gigabit Media Independent Interface (GMII) or Reduced GMII (RGMII). The QFP package supports MII/GMII/RGMII whereas the QFN package supports RGMII.

The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low latency and provides IEEE 1588 Start of Frame Detection.

## MX66LM1G45G - 1G-bit Serial Flash Memory with Single and Octal SPI

MX66LM1G45G is 1Gbit Serial NOR Flash memory, which is configured as 134,217,728 x 8 internally. MX66LM1G45G feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by a chip-select (CS#) input.

The MX66LM1G45G MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

# 3 Hardware Reference

This chapter describes the hardware design of the *EV-SOMCRR-EZKIT* carrier board.

## System Architecture

The board's configuration is shown in the ***Block Diagram*** figure.

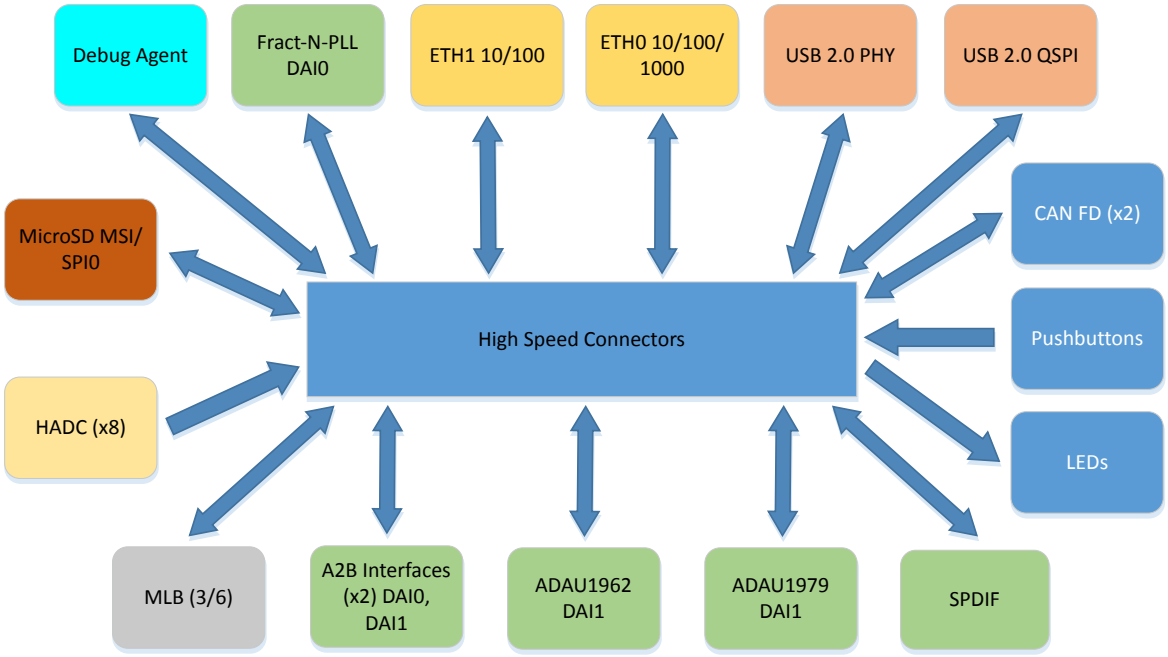


**Figure 3-1:** Block Diagram

This Carrier board is designed to demonstrate the connected System on Module processor's capabilities. The peripherals help evalaute the processor's features with audio DAC and ADCs, S/PDIF, 10/100/1000 ethernet, CAN, MLB and A$^2$B expansion.

User I/O to the processor is provided in the form of two pushbuttons and three LEDs.

The software-controlled switches (SoftConfig) facilitate the switch multi-functionality by disconnecting the pushbuttons from their associated processor pins and reusing the pins elsewhere on the board.

# Software-Controlled Switches (SoftConfig)

On the board, most of the functionality traditionally controlled by mechanical switches and jumpers is controlled by $I^2C$ software-controlled switches. The mechanical switches the remain are provided for the boot mode and push buttons. Reference any `SoftConfig*.c` file found in the installation directory for an example of how to set up the SoftConfig feature of the board through software. The SoftConfig section of this manual serves as a reference to any user that intends to modify an existing software example. If software provided by ADI is used, there should be little need to reference this section.

**NOTE:** Be careful when changing SoftConfig settings. When connecting extender cards, configure the settings to avoid conflict among interfaces so multiple signals are not driven on the same pins.

## Overview of SoftConfig

In order to further clarify the use of electronic single FET switches and multi-channel bus switches, an example of each is illustrated and compared to a traditional mechanical switching solution. This is a generic example that uses similar FET and bus switch components that are on the board.

After this generic discussion, there is a detailed explanation of the SoftConfig interface specific to the *EV-SOMCRR-EZKIT* carrier board.

The ***Example of Individual FET Switches*** figure shows two individual FET switches (Pericom PI3A125CEX) with reference designators `UA` and `UB`. Net names `ENABLE_A` and `ENABLE_B` control `UA` and `UB`. The default FET switch enable settings in this example are controlled by resistors `RA` and `RB`, which pull the enable pin 1 of `UA` and `UB` to ground (low), respectively. In a real example, these enable signals are controlled by the Microchip I/O expander. The default pull-down resistors connects the signals `EXAMPLE_SIGNAL_A` and `EXAMPLE_SIGNAL_B` and also connects signals `EXAMPLE_SIGNAL_C` and `EXAMPLE_SIGNAL_D`. To disconnect `EXAMPLE_SIGNAL_A` from `EXAMPLE_SIGNAL_B`, the Microchip I/O expander is used to change `ENABLE_A` to a logic 1 through software that interfaces with the Microchip I/O expander. The same procedure for `ENABLE_B` disconnects `EXAMPLE_SIGNAL_C` from `EXAMPLE_SIGNAL_D`.

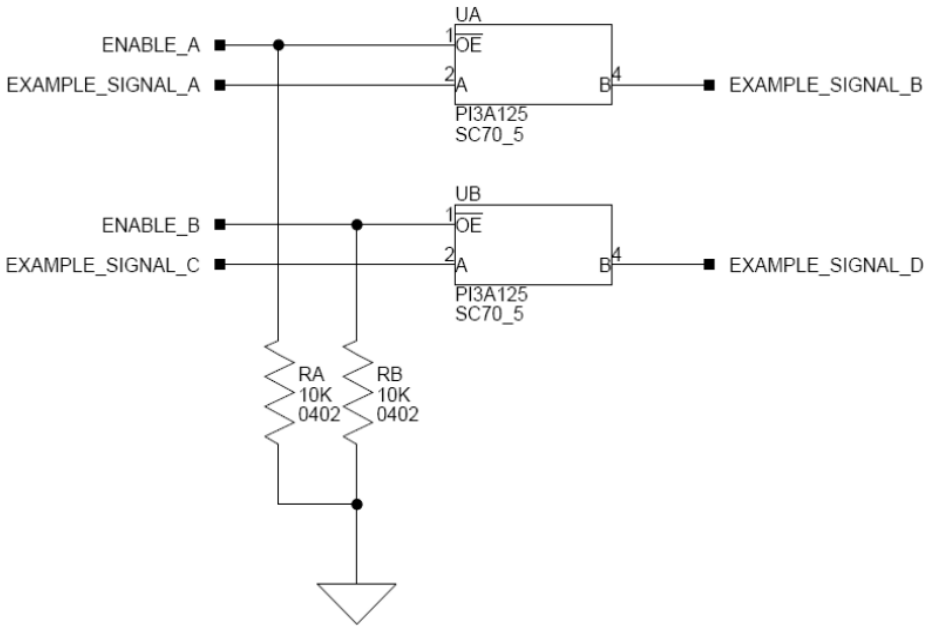


**Figure 3-2:** Example of Individual FET Switches

The following figure shows the equivalent circuit to the ***Example of Individual FET Switches*** figure but utilizes mechanical switches that are in the same package. Notice the default is shown by black boxes located closer to the ***ON*** label of the switches. In order to disconnect these switches, physically move the switch to the OFF position.

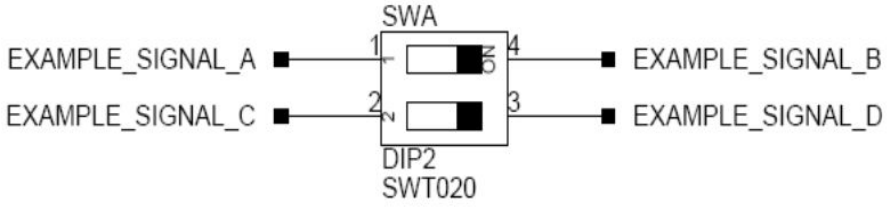


**Figure 3-3:** Example of a Mechanical Switch (Equivalent to Example of Individual FET Switches Figure)

The ***Example of Bus Switch*** figure shows a bus switch example, reference designator `UC` (Pericom PI3LVD512ZHE), selecting between lettered functionality and numbered functionality. The signals on the left side are multiplexed signals with naming convention letter_number. The right side of the circuit shows the signals separated into letter and number, with the number on the lower group (`0B1`) and the letter on the upper group (`0B2`). The default setting is controlled by the signal `CONTROL_LETTER_NUMBER` which is pulled low. This selects the number signals on the right to be connected to the multiplexed signals on the left by default. In this example, the Microchip IO expander is not shown but controls the signal `CONTROL_LETTER_NUMBER` and allows the user to change the selection through software.

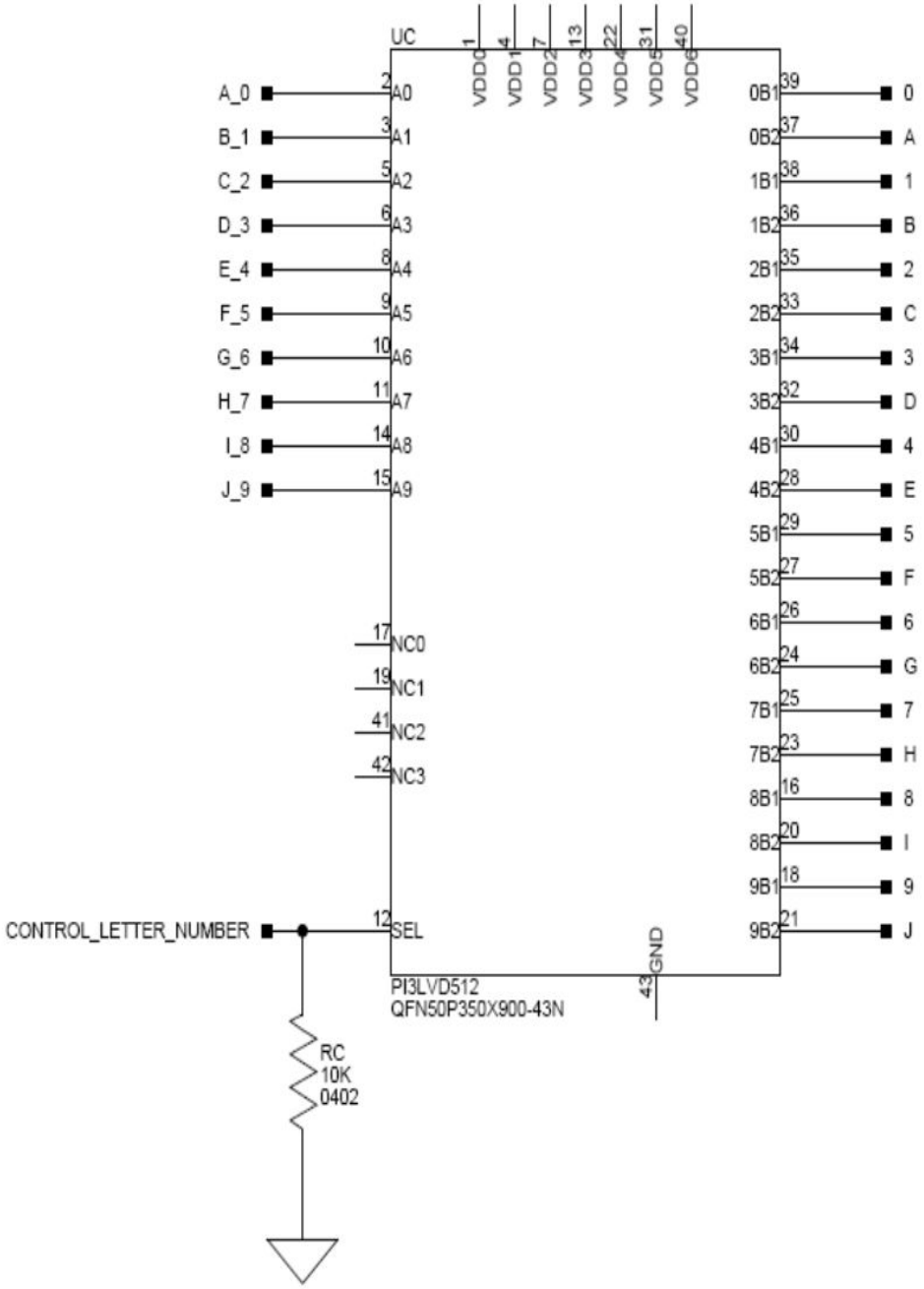


**Figure 3-4:** Example of a Bus Switch

The following figure shows the equivalent circuit to the ***Example of Bus Switch*** figure but utilizes mechanical switches. Notice the default for reference designators SWC and SWD is illustrated by black boxes located closer to the ***ON*** label of the switches to enable the number signals by default. Also notice the default setting for reference designators SWE and SWF is OFF. In order to connect the letters instead of the numbers, the user physically changes all switches on SWC and SWD to the OFF position and all switches on SWE and SEF to the ON position.

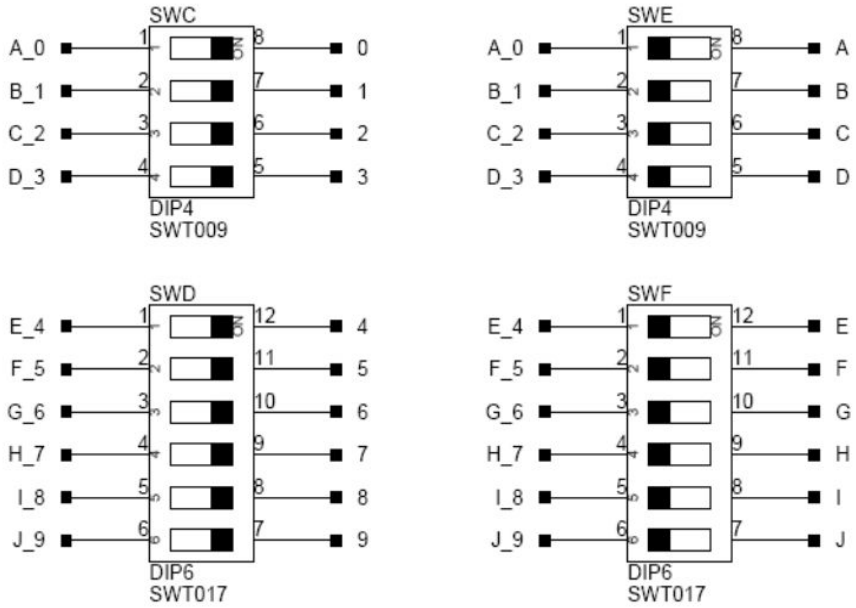


**Figure 3-5:** Example of a Mechanical Switch (Equivalent to Example of Bus Switch)

## SoftConfig on the Board

Two Microchip MCP23017 GPIO expanders provide control for individual electronic switches. The TWI2 interface of the processor communicates with the Microchip devices. There are individual switches with default settings that enable basic board functionality.

The ***Default Processor Interface Availability*** table lists the processor and board interfaces that are available by default. Note that only interfaces affected by software switches are listed in the table.

**Table 3-1:** Default Processor Interface Availability

| *Interface* | *Availability by Default* |
|---|---|
| Audio Connectors | 4 inputs/8 outputs |
| S/PDIF Digital | S/PDIF RCA input and output connectors enabled |
| Pushbuttons | Enabled |
| LEDs | Enabled |

## Programming SoftConfig Switches

On the board, two Microchip MCP23017 devices exist. Each of these devices has the following programming characteristics:

- Each GPIO register controls eight signals (software switches).

| *GPIO Register* | *Register Address* |
|---|---|
| GPIOA | 0x12 |
| GPIOB | 0x13 |

- By default, the Microchip MCP23017 GPIO signals function as input signals.

  The signals must be programmed as output signals to override their default values. A zero is programmed into the register to enable the signal as an output. The following table shows the Microchip GPIO expander register addresses.

| *IODIR Register* | *IODIR Register Address* |
|---|---|
| IODIRA | 0x00 |
| IODIRB | 0x01 |

Each example in the Board Support Package (BSP) includes source files that program the soft switches, even if the default settings are being used. The `README` for each example identifies only the signals that are being changed from their default values. The code that programs the soft switches is located in the `SoftConfig_XXX.c` file in each example ,where XXX is the name of the baord.

The following table ***I²C Hardware Address (0x22***) outline the default values for the Microchip MCP23017 device.

**Table 3-2:** I²C Hardware Address (0x22)

| *GPIO* | *MCP23017 Register Address* | *Default Value* |
|---|---|---|
| GPIOA | 0x12 | 0x00 |
| GPIOB | 0x13 | 0x00 |

The board schematic shows how the two Microchip GPIO expanders are connected to the board's ICs.

Tables ***Output Signals of Microchip GPIO Expander (U6 Port A)*** and ***Signals of Microchip GPIO Expander (U6 Port B)*** show the output signals of the Microchip GPIO expander (***U6***), with a TWI address of `0100 010X`, where `X` represents the read or write bit. The signals that control an individual FET have an entry in the ***FET*** column. The ***Component Connected*** column shows the board IC that is connected if the FET is enabled. However, in most cases, the Microchip GPIO exapnder (`U6`) is controlling the enable signal of a FET switch. Also note that if a particular functionality of the processor signal is being used, it is in ***bold*** font in the ***Processor Signal*** column.

**Table 3-3:** Output Signals of Microchip GPIO Expander (U6 Port A)

| *Bit* | *Signal Name* | *Description* | *FET* | *Processor Signal (if applicable)* | *Connected* | *Default* |
|---|---|---|---|---|---|---|
| `0` | EEPROM_EN | $\overline{\text{SPI0\_SS}}$ for EEPROM chip select | U26 | $\overline{\text{SPI0\_SS}}$ | U21 | High |
| `1` | PUSHBUTTON_EN | Enable Push buttons | U19,U20 | PUSHBUTTON_1,PUSHBUTTON_2 | PB1, PB2 | High |

**Table 3-3:** Output Signals of Microchip GPIO Expander (U6 Port A) (Continued)

| *Bit* | *Signal Name* | *Description* | *FET* | *Processor Signal (if applicable)* | *Connected* | *Default* |
|---|---|---|---|---|---|---|
| 2 | $\overline{\text{MicroSD\_SPI}}$ | SPI0 Signals to MicroSD socket | U35 | SPI0_MISO, SPI0_MOSI, SPI0_SSb, SPI0_CLK | J9 | High |
| 3 | $\overline{\text{FTDI\_USB\_EN}}$ | FT4222H USB Enable | U36 | OSPI_CLK, OSPI_MISO, OSPI_MOSI, OSPI_D2, OSPI_D3, SPI2_SSb, TWI2_SCL, TWI2_SDA | U39 | High |
| 4 | $\overline{\text{CAN\_EN}}$ | CAN0/1 Enable | U15, U16 | CAN0_RX, CAN0_SILENT, CAN0_STDBY, CAN1_RX, CAN1_SILENT, CAN1_STDBY | U1, U3 | High |
| 5 | $\overline{\text{ADAU\_RESET}}$ | Reset all audio devices on board | N/A | N/A | U34, U38 | High |
| 6 | $\overline{\text{ADAU1962\_EN}}$ | Enable ADAU1962 | U8 | $\overline{\text{ADAU\_RESET}}$, ADAU1962A_CLKIN, DAI1_PIN05, DAI1_PIN04, DAI1_PIN01, DAI1_PIN02, DAI1_PIN10 | U34 | High |
| 7 | $\overline{\text{ADAU1979\_EN}}$ | Enable ADAU1979 | U7 | $\overline{\text{ADAU\_RESET}}$, DAI1_PIN20, DAI1_PIN12, DAI1_PIN06, DAI1_PIN07 | U38 | High |

**Table 3-4:** Output Signals of Microchip GPIO Expander (U6 Port B)

| *Bit* | *Signal Name* | *Description* | *FET* | *Processor Signal (if applicable)* | *Connected* | *Default* |
|---|---|---|---|---|---|---|
| 0 | OC-TAL_SPI_CS_EN | Enable Chip Select to OSPI flash device | U17 | $\overline{\text{SPI2\_SS}}$ | U40 | Low |
| 1 | $\overline{\text{SPDIF\_DIGI-TAL\_EN}}$ | Enable Digital SPDIF connector | U13 | DAI0_PIN09 | J14 | High |
| 2 | $\overline{\text{SPDIF\_OPTI-CAL\_EN}}$ | Enable Optical SPDIF connector | U14 | DAI0_PIN09 | J2 | High |
| 3 | AU-DIO_JACK_SEL | Set J4 to Input or Output | U37 | | J4 | High |
| 4 | $\overline{\text{MLB\_EN}}$ | Configure MLB for MLB3 or MLB6 | J15 | | J15 | High |

**Table 3-4:** Output Signals of Microchip GPIO Expander (U6 Port B) (Continued)

| *Bit* | *Signal Name* | *Description* | *FET* | *Processor Signal (if applicable)* | *Connected* | *Default* |
|---|---|---|---|---|---|---|
| 5 | $\overline{\text{ETH1\_EN}}$ | Enable signals for ETH1 | U41, U42, U44 | ETH1_MDIO, ETH1_MDC, ETH1_CRS, ETH1_RXD0, ETH1_RXD1, ETH1_TXD0, ETH1_TXD1, ETH1_TXEN, ETH1_CLKIN, ETH1_INTb | U52 | Low |
| 6 | $\overline{\text{ETH1\_RESET}}$ | Reset signal for ETH1 | N/A | N/A | U52 | N/A |
| 7 | $\overline{\text{GIGE\_RESET}}$ | Reset signal for Gigabit Ethernet | N/A | N/A | U27 | High |

# Switches

This section describes operation of the switches. The switch locations are shown in the ***Switch/Jumper Locations*** figure.

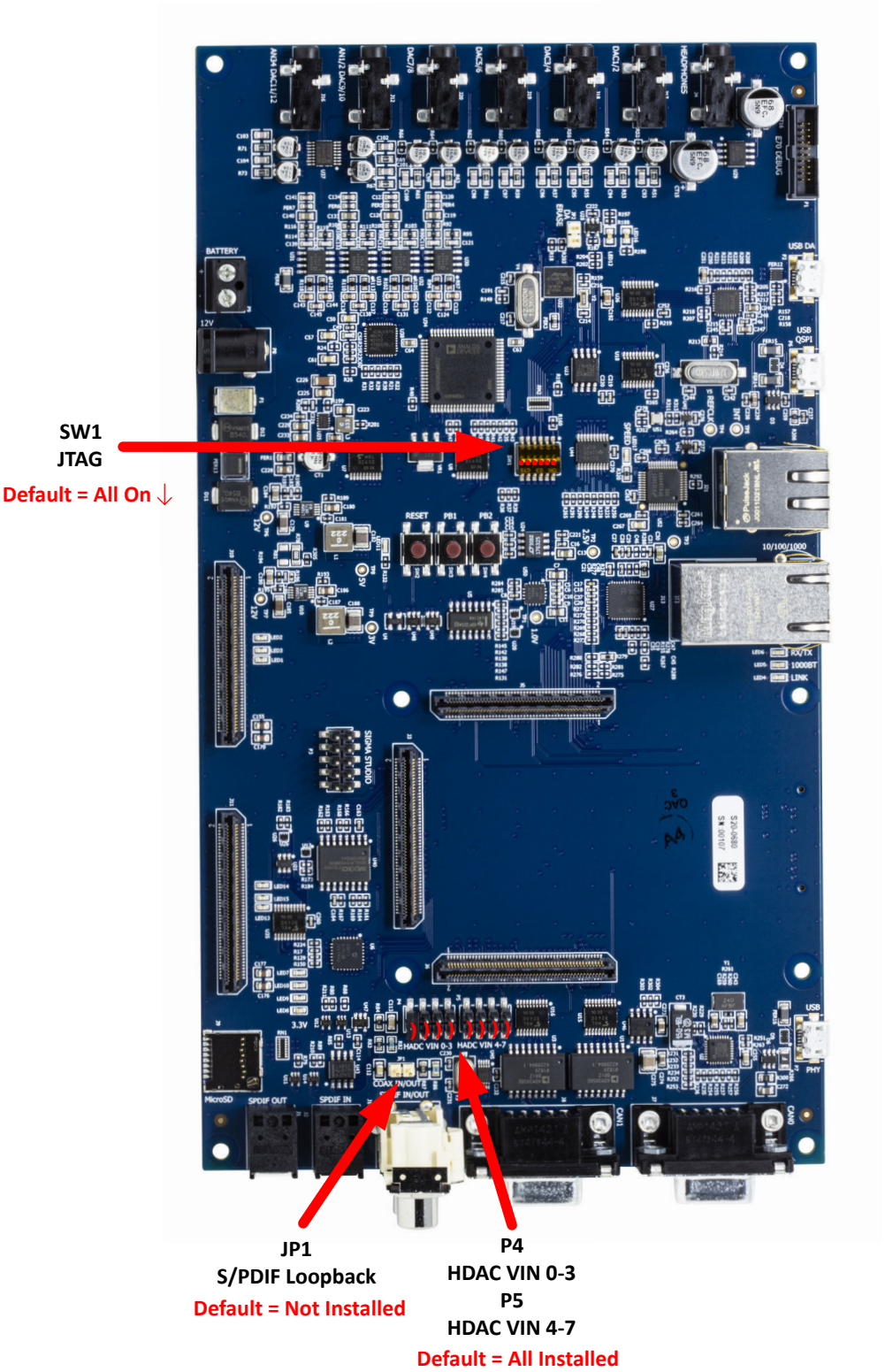


**Figure 3-6:** Switch/Jumper Locations

## Reset Pushbutton ( SW2 )

The reset pushbutton resets the ADI processor. The reset signal also is connected to the SoM interface connectors via the SYS_HWRST signal. Reset ( LED11 ) is used to indicate when the board is in reset.

## GPIO Pushbuttons ( SW4 and SW3 )

The GPIO pushbuttons are connected to the processor's signals GPIO1 and GPIO2 , respectively.

The GPIO pushbuttons can be disconnected from the processor by setting SoftConfig. See Software-Controlled Switches (SoftConfig) for more information.

## JTAG Interface ( SW1 )

The JTAG Interface switch enables/disables the on-board debug agent. When in the disabled configuration, an ICE can be attached to the JTAG header on the SoM module to provide on-chip debug capabilities.

**Table 3-5:** Debug Agent Enable

| Location | Position |
|---|---|
| SW1.1 | ON |
| SW1.2 | ON |
| SW1.3 | ON |
| SW1.4 | ON |
| SW1.5 | ON |
| SW1.6 | ON |

**Table 3-6:** Debug Agent Disable

| Location | Position |
|---|---|
| SW1.1 | OFF |
| SW1.2 | OFF |
| SW1.3 | OFF |
| SW1.4 | OFF |
| SW1.5 | OFF |
| SW1.6 | OFF |

# Jumpers

This section describes the functionality of the configuration jumpers. The ***Switch/Jumper Locations*** figure shows the jumper locations.

## S/PDIF Loopback ( JP1 )

The S/PDIF loopback jumper is used to connect the S/PDIF input and output signals together and bypass the two RCA connectors.

## HADC ( P4 and P5 )

The HADC jumper is used to connect the HADC of the processor to various voltages on the board for monitoring.

| P4 Jumper | Voltage |
|---|---|
| 1 and 2 | VDD_INT |
| 3 and 4 | VDD_A |
| 5 and 6 | VDD_DMC |
| 7 and 8 | 1.0V |

| P5 Jumper | Voltage |
|---|---|
| 1 and 2 | VDD_REF |
| 3 and 4 | VDD_INT |
| 5 and 6 | GND |
| 7 and 8 | GND |

# LEDs

This section describes the on-board LEDs. The ***LED Locations*** figure shows the LED locations.

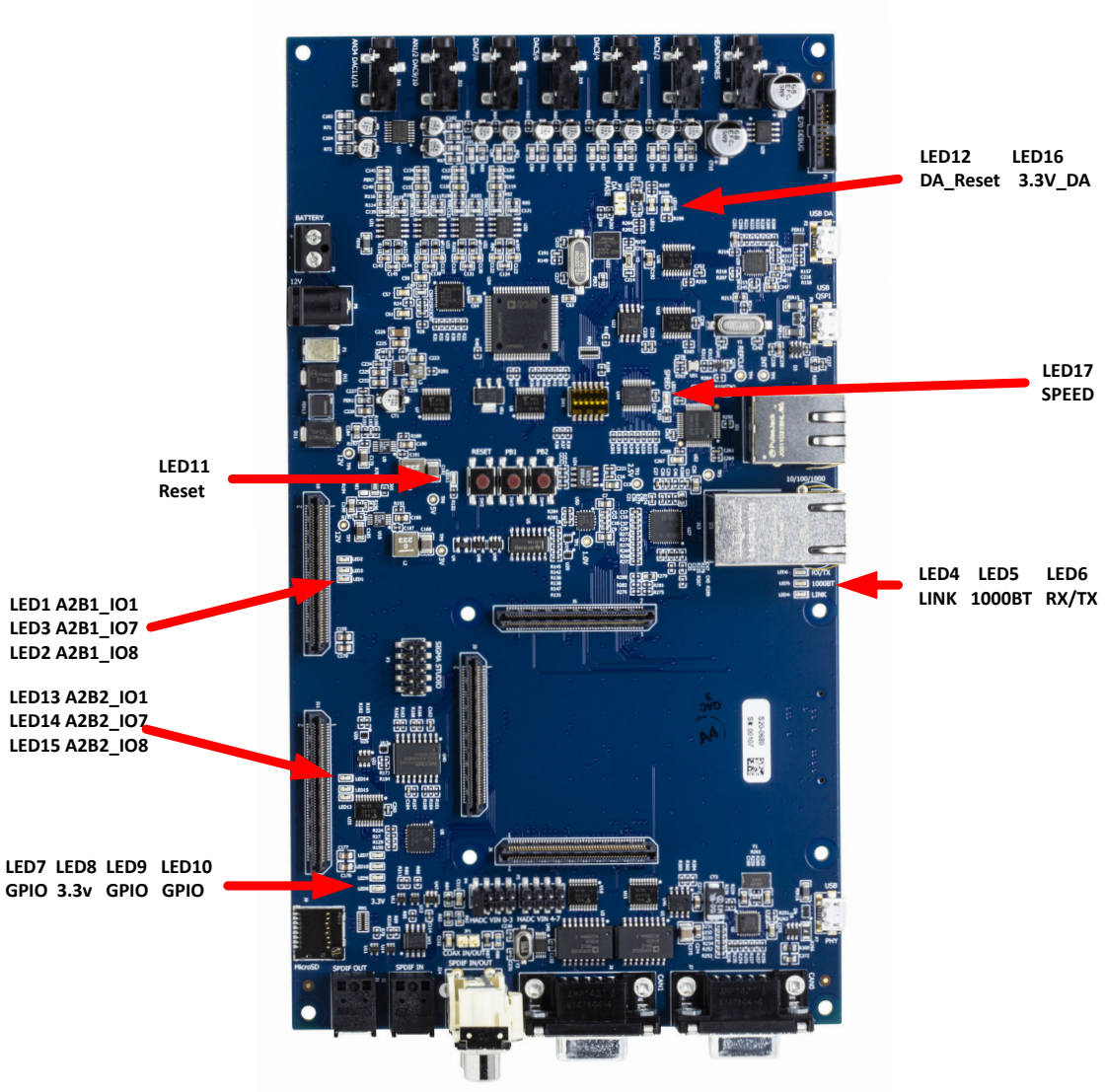


**Figure 3-7:** LED Locations

## A²B Interface LEDs ( `LED1, LED2, LED3, LED13, LED14, LED15` )

The A²B Interface LEDs are driven by the connected A2B daughter card on the A2B Interface Connectors. These are connected to A2B IRQ and GPIO signals. Refere to the schematics of the connected A2B or related daughter card for more information.

## Power ( `LED8` )

When ON (green), it indicates that power is being supplied to the board properly.

### GPIO ( LED7, LED9, LED10 )

Three LEDs are connected to the general-purpose I/O pins of the processor (see the ***GPIO LEDs*** table). The LEDs are active high and are turned ON (amber) by writing a 1 to the correct processor signal.

**Table 3-7:** GPIO LEDs

| *Reference Designator* | *Programmable Flag Pin* |
|---|---|
| *LED7* | LED3_KIT |
| *LED9* | LED1_KIT |
| *LED10* | LED2_KIT |

### Reset ( LED11 )

When ON (red), it indicates that the board is in reset. A master reset is asserted by pressing SW2 , which activates the LED. For more information, see Reset Pushbutton ( SW2 ).

## Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in the ***Connector Top*** and ***Connector Bottom*** figures.

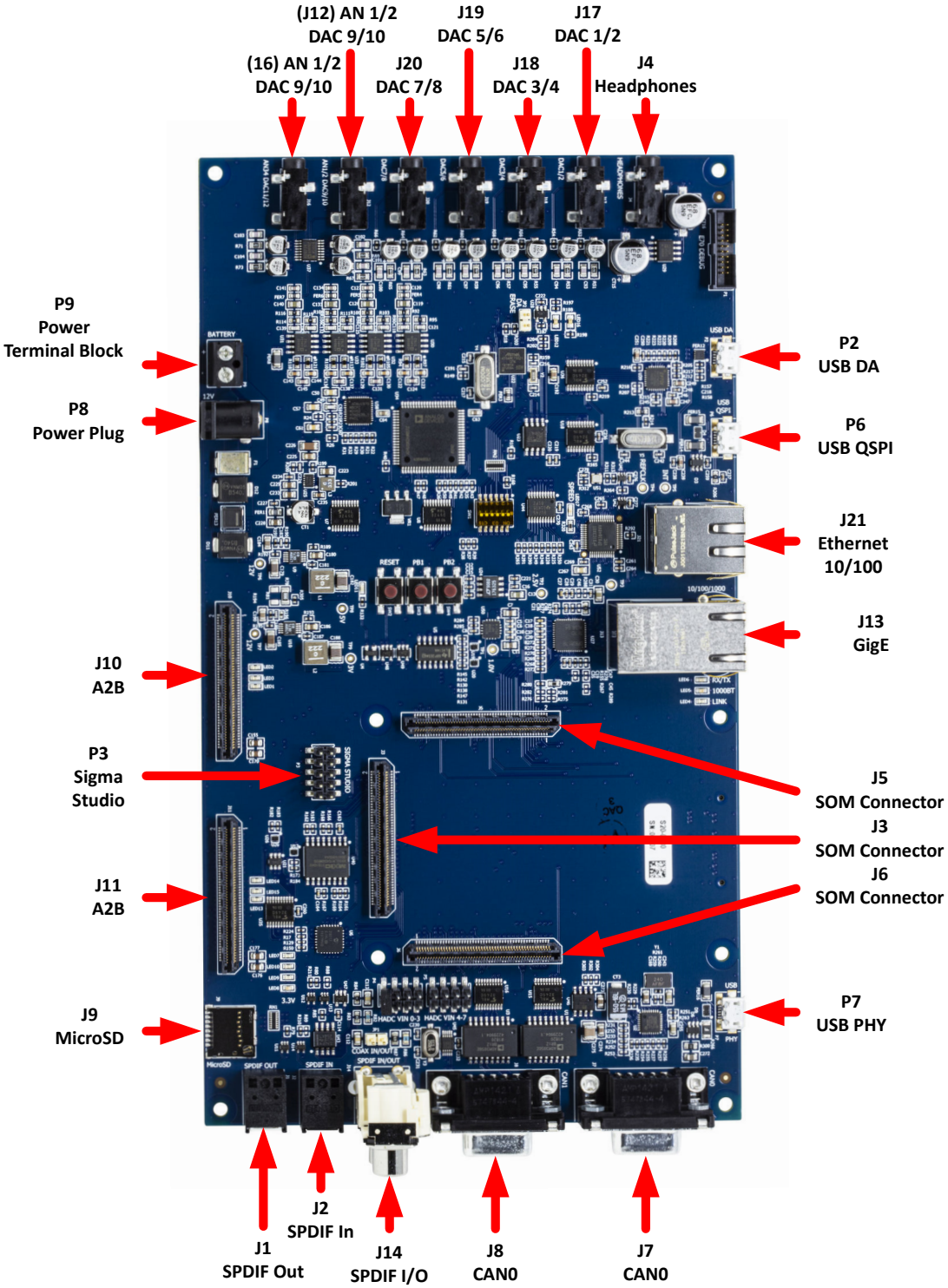


**Figure 3-8:** Connector Top

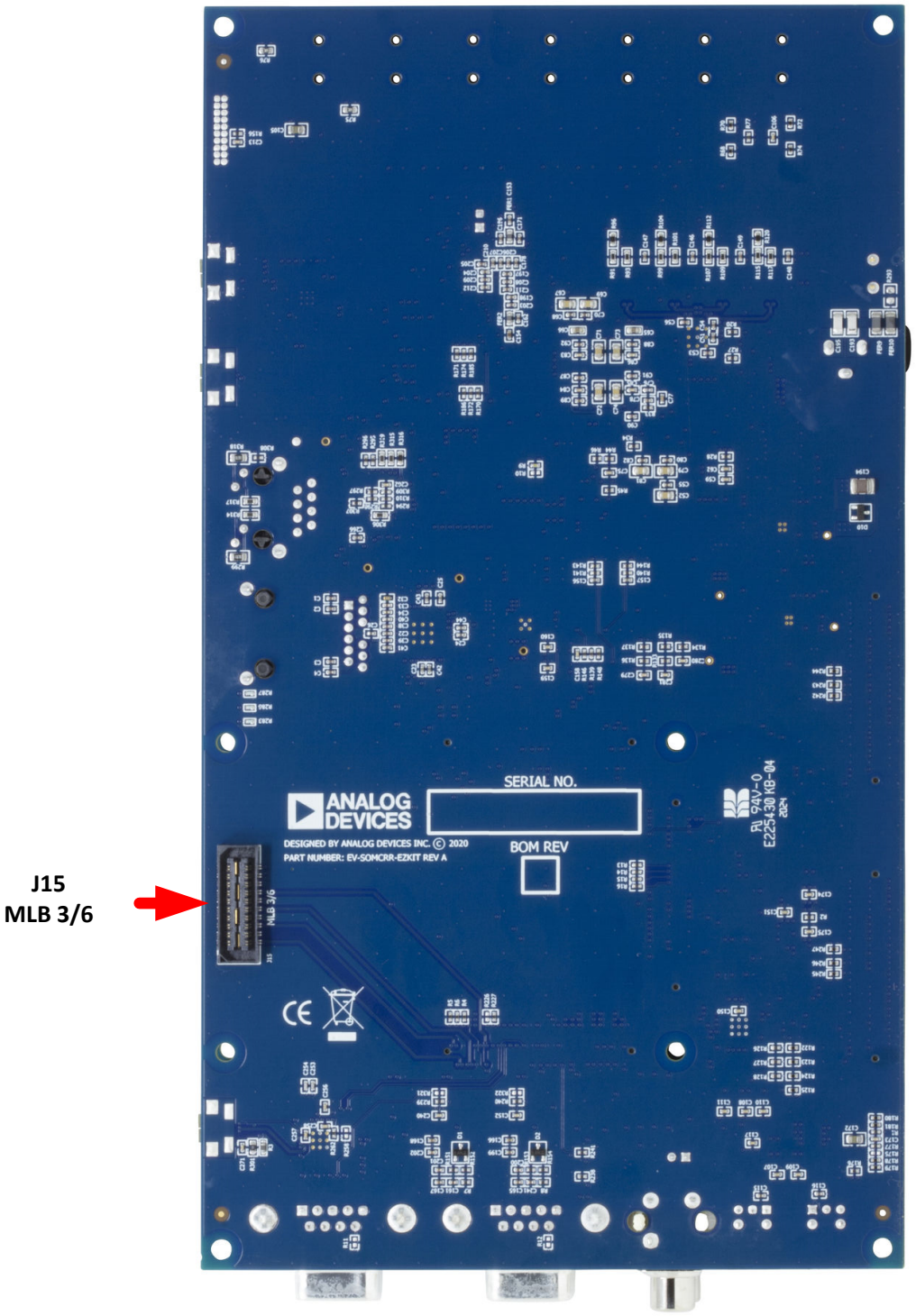


**Figure 3-9:** Connector Bottom

## S/PDIF Optical Tx ( J1 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| Fiber optic transmitter | Everlight | PLT133/T10W |
| *Mating Cable* | | |
| Standard TOSLINK optical digital cable | | |

## Audio Input/Output ( J12 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| 3.5mm Stereo female | CUI | SJ-3523-SMT |
| *Mating Cable* | | |
| Standard 3.5mm stereo cable | | |

## S/PDIF Optical Rx ( J2 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| Fiber optic receiver | Everlight | PLR135/T10 |
| *Mating Cable* | | |
| Standard TOSLINK optical digital cable | | |

## Audio Output ( J4 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| 3.5mm Stereo female | CUI | SJ-3523-SMT |
| *Mating Cable* | | |
| Standard 3.5mm stereo cable | | |

## S/PDIF Digital ( J11 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| RCA 1x2 female | Switchcraft | PJRAS1X2S02X |
| *Mating Cable* | | |
| Standard S/PDIF cable with RCA connectors | | |

## MLB ( J15 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| 40-pin high speed socket | Samtec | QSH-020-01-L-D-DP-A |
| *Mating Connector* | | |
| 40-pin high speed header | Samtec | QTH-0202-01-L-D-DP-A |

## Headphone ( J16 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| 3.5mm headphone connector | CUI | SJ1-3525NG |
| *Mating Cable* | | |
| Standard audio cable with 3.5mm connector | | |

## Sigma Studio ( P3 )

This connector interfaces with SigmaStudio® through the EVAL-ADUSB2EBZ board. The connector is a 0.1" header. The pinout can be found in the schematic.

## A2B ( J10 and J11 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| 100-pin, 0.64mm | SAMTEC | LSS-150-01-L-DV-A-K |
| *Mating Connector* | | |
| 100-pin, 0.64mm | SAMTEC | LSS-150-01-L-DV-A-K |

## Ethernet 100 ( J21 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| RJ45 | Pulse Engineering | J0011D21BNL |
| *Mating Cable* | | |
| Standard CAT5e Ethernet cable | | |

## Ethernet 1000 ( J13 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| RJ45 | Assmann | A-2004-2-4-LPS-N-R |
| *Mating Cable* | | |

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| Standard CAT5e Ethernet cable | | |

## Power Plug ( P8 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| 2.1 mm power jack | CUI | PJ-102AH |
| *Mating Cable* | | |
| 12.0VDC@1.5A power supply | CUI | EMSA120150-P5RP-SZ |

## Power Terminal Block ( P9 )

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| 5.08mm power jack | Weidmuller | 1760510000 |
| *Mating Cable* | | |
| 12.0VDC discrete wires | | |

## SoM Interface Connection ( J3, J5, J6 )

The SoM Interface consists of three SAMTEC high speed connectors that provide the DSP peripheral signals for use with a plug in SoM module. These signals are based upon the peripheral signal needs, which allows multiple processors to be used with this connection. These connectors are self-mating, and the pinout here reflects the connectors of the associated SoM board.

The *SoM Interface A Connector (J5)*, *SoM Interface B Connector (J3)*, and *SoM Interface C Connector (J6)* tables show the signal associated with each pin on the connectors.

**Table 3-8:** SoM Interface A Connector (J5)

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GND1 | 21 | DAI0_PIN10 | 41 | DAI0_PIN20 | 61 | USB0_ID | 81 | GPIO3 |
| 2 | GND2 | 22 | DAI1_PIN10 | 42 | DAI1_PIN20 | 62 | USB_D2 | 82 | $\overline{\text{USB\_RESET}}$ |
| 3 | DAI0_PIN01 | 23 | DAI0_PIN11 | 43 | GND3 | 63 | USB0_VBUS | 83 | GPIO4 |
| 4 | DAI1_PIN01 | 24 | DAI1_PIN11 | 44 | GND4 | 64 | USB_D3 | 84 | GPIO6 |
| 5 | DAI0_PIN02 | 25 | DAI0_PIN12 | 45 | GND5 | 65 | USB0_VBC | 85 | GPIO5 |
| 6 | DAI1_PIN02 | 26 | DAI1_PIN12 | 46 | GND6 | 66 | USB_D4 | 86 | GPIO7 |
| 7 | DAI0_PIN03 | 27 | DAI0_PIN13 | 47 | HADC_VIN0 | 67 | USB1_DP | 87 | GND9 |
| 8 | DAI1_PIN03 | 28 | DAI0_PIN13 | 48 | HADC_VIN4 | 68 | USB_D5 | 88 | GPIO8 |

**Table 3-8:** SoM Interface A Connector (J5) (Continued)

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|---|---|
| 9 | DAI0_PIN04 | 29 | DAI0_PIN14 | 49 | HADC_VIN1 | 69 | USB1_DM | 89 | MLB_CLKP |
| 10 | DAI1_PIN04 | 30 | DAI1_PIN14 | 50 | HADC_VIN5 | 70 | USB_D6 | 90 | GPIO9 |
| 11 | DAI0_PIN05 | 31 | DAI0_PIN15 | 51 | HADC_VIN2 | 71 | USB1_ID | 91 | MLB_CLKN |
| 12 | DAI1_PIN05 | 32 | DAI1_PIN15 | 52 | HADC_VIN6 | 72 | USB_D7 | 92 | GPIO10 |
| 13 | DAI0_PIN06 | 33 | DAI0_PIN16 | 53 | HADC_VIN3 | 73 | USB1_VBUS | 93 | MLB_SIGP |
| 14 | DAI1_PIN06 | 34 | DAI1_PIN16 | 54 | HADC_VIN7 | 74 | USB_NXT | 94 | GND10 |
| 15 | DAI0_PIN07 | 35 | DAI0_PIN17 | 55 | GND7 | 75 | USB1_VBC | 95 | MLB_SIGN |
| 16 | DAI1_PIN07 | 36 | DAI1_PIN17 | 56 | GND8 | 76 | USB_STP | 96 | MLB_CLK |
| 17 | DAI0_PIN08 | 37 | DAI0_PIN18 | 57 | USB0_DP | 77 | GPIO1 | 97 | MLB_DATP |
| 18 | DAI1_PIN08 | 38 | DAI1_PIN18 | 58 | USB_D0 | 78 | USB_DIR | 98 | MLB_SIG |
| 19 | DAI0_PIN09 | 39 | DAI0_PIN19 | 59 | USB0_DM | 79 | GPIO2 | 99 | MLB_DATN |
| 20 | DAI1_PIN09 | 40 | DAI1_PIN19 | 60 | USB_D1 | 80 | USB_CLK | 100 | MLB_DAT |

**Table 3-9:** SoM Interface B Connector (J3)

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GND1 | 21 | OSPI_D7 | 41 | TWI2_SDA | 61 | MSI_D3 | 81 | LINKPORT0_D7 |
| 2 | GND2 | 22 | SPI1_SEL2b | 42 | UART2_RXb | 62 | GND8 | 82 | LINKPORT1_D7 |
| 3 | SP2_OSPI_MISO | 23 | SPI2_SEL2b | 43 | UART0_TXb | 63 | MSI_D4 | 83 | LINKPORT0_D6 |
| 4 | SPI0_CLK | 24 | GND3 | 44 | UART2_RTSb | 64 | CAN0_TX | 84 | LINKPORT1_D6 |
| 5 | SP2_OSPI_MOSI | 25 | GND4 | 45 | UART0_RXb | 65 | MSI_D5 | 85 | LINKPORT0_D5 |
| 6 | SPI0_MISO | 26 | NU | 46 | UART2_CTSb | 66 | CAN0_RX | 86 | LINKPORT1_D5 |
| 7 | SPI2_OSPI_D2 | 27 | NU | 47 | UART0_RTSb | 67 | MSI_D6 | 87 | LINKPORT0_D4 |
| 8 | SPI0_MOSI | 28 | NU | 48 | GND6 | 68 | GND | 88 | LINKPORT1_D4 |
| 9 | SP2_OSPI_D3 | 29 | NU | 49 | UART0_CTSb | 69 | MSI_D7 | 89 | LINKPORT0_D3 |
| 10 | SPI0_SSb | 30 | NU | 50 | GPIO1 | 70 | CAN1_TX | 90 | LINKPORT1_D3 |
| 11 | SP2_OSPI_CLK | 31 | TWI0_SCL | 51 | GND5 | 71 | GND7 | 91 | LINKPORT0_D2 |
| 12 | SPI0_SEL2b | 32 | UART1_TXb | 52 | GPIO2 | 72 | CAN1_RX | 92 | LINKPORT1_D2 |
| 13 | SP2_OSPI_SSb | 33 | TWI0_SDA | 53 | NU | 73 | NU | 93 | LINKPORT0_D1 |
| 14 | SPI1_CLK | 34 | UART1_RXb | 54 | NU | 74 | NU | 94 | LINKPORT1_D1 |
| 15 | OSPI_D4 | 35 | TWI1_SCL | 55 | MSI_D0 | 75 | NU | 95 | LINKPORT0_D0 |
| 16 | SPI1_MISO | 36 | UART1_RTSb | 56 | MSI_CLK | 76 | NU | 96 | LINKPORT1_D0 |
| 17 | OSPI_D5 | 37 | TWI1_SDA | 57 | MSI_D1 | 77 | NU | 97 | LINKPORT0_ACK |

**Table 3-9:** SoM Interface B Connector (J3) (Continued)

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|---|---|
| 18 | SPI1_MOSI | 38 | UART1_CTSb | 58 | MSI_CMD | 78 | NU | 98 | LINKPORT1_ACK |
| 19 | OSPI_D6 | 39 | TWI2_SCL | 59 | MSI_D2 | 79 | GND9 | 99 | LINKPORT0_CLK |
| 20 | SPI1_SSb | 40 | UART2_TXb | 60 | MSI_CDb | 80 | GND10 | 100 | LINKPORT1_CLK |

**Table 3-10:** SoM Interface C Connector (J6)

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GND1 | 21 | ETH0_ RXCLK_REFCLK | 41 | GND7 | 61 | PPI_D05 | 81 | PPI_D15 |
| 2 | GND2 | 22 | GND4 | 42 | CLK1 | 62 | PPI_D17 | 82 | GPIO3 |
| 3 | ETH0_MDIO | 23 | ETH0_RXCTL_CRS | 43 | PPI_CLK | 63 | PPI_D06 | 83 | PPI_D16 |
| 4 | ETH1_MDIO | 24 | ETH0_PTPCLKIN0 | 44 | CLK2 | 64 | PPI_D18 | 84 | GPIO4 |
| 5 | ETH0_MDC | 25 | GND3 | 45 | PPI_FS1 | 65 | PPI_D07 | 85 | GND11 |
| 6 | ETH1_MDC | 26 | ETH0_PTPAUX-IN0 | 46 | GND8 | 66 | PPI_D19 | 86 | GPIO5 |
| 7 | ETH0_MD_INT | 27 | ETH0_TXD3 | 47 | PPI_FS2 | 67 | PPI_D08 | 87 | VDD_EXT |
| 8 | ETH0_RXD1 | 28 | ETH0_PTPPPS0 | 48 | JTG0_TMS/ SWDIO | 68 | PPI_D20 | 88 | GPIO6 |
| 9 | ETH0_GPIO_1 | 29 | ETH0_TXD2 | 49 | PPI_FS3 | 69 | PPI_D09 | 89 | VDD_VREF |
| 10 | ETH0_RXD0 | 30 | ETH0_PTPPPS1 | 50 | JTG0_TCK/ SWCLK | 70 | PPI_D21 | 90 | GND12 |
| 11 | ETH0_GPIO_2 | 31 | ETH0_TXD1 | 51 | PPI_D00 | 71 | PPI_D10 | 91 | VDD_A |
| 12 | ETH0_TXEN | 32 | ETH0_PTPPPS2 | 52 | JTG0_TDO/SW0 | 72 | PPI_D22 | 92 | VDD_DMC |
| 13 | ETH0_RXD3 | 33 | ETH0_TXD0 | 53 | PPI_D01 | 73 | PPI_D11 | 93 | VDD_INT |
| 14 | ETH0_TXD0 | 34 | ETH0_PTPPPS3 | 54 | JTG0_TDI | 74 | PPI_D23 | 94 | $\overline{\text{SYS\_HWRST}}$ |
| 15 | ETH0_RXD2 | 35 | ETH0_TCLK | 55 | PPI_D02 | 75 | PPI_D12 | 95 | PWR_SEQ_GOOD |
| 16 | ETH0_TXD1 | 36 | GND5 | 56 | $\overline{\text{JTG0\_TRST}}$ | 76 | GND10 | 96 | $\overline{\text{SoM\_Reset}}$ |
| 17 | ETH0_RXD1 | 37 | ETH0_TXEN | 57 | PPI_D03 | 77 | PPI_D13 | 97 | VDD1 |
| 18 | ETH1_CRS | 38 | SYS_CLKOUT | 58 | $\overline{\text{TARGET\_RESET}}$ | 78 | GPIO1 | 98 | VSS1 |
| 19 | ETH0_RXD0 | 39 | GND6 | 59 | PPI_D04 | 79 | PPI_D14 | 99 | VDD2 |
| 20 | ETH1_INTb | 40 | AUDIO_CLK | 60 | GND9 | 80 | GPIO2 | 100 | VSS2 |

**Table 3-11:** Mating Connector

| *Part Description* | *Manufacturer* | *Part Number* |
|---|---|---|
| 100-pin, 0.64 mm | SAMTEC | LSS-150-01-L-DV-A-K |
| *Mating Connector* | | |
| 100-pin, 0.64 mm | SAMTEC | LSS-150-01-L-DV-A-K |

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