



**THE DATASHEET OF
DS4077L-0C0**



50MHz to 122.88MHz VCXO

DS4077

General Description

The DS4077 is an integrated voltage-controlled crystal oscillator (VCXO) module designed to provide reference clock generation in base stations, telecom/datacom, and wireless applications. The DS4077 is developed using a fundamental quartz crystal plus a unique integrated circuit design. The internal fundamental quartz crystal determines the frequency of operation. Custom frequencies are available. Contact the factory for availability.

The DS4077 is designed for use with applications requiring low phase noise and jitter. Jitter performance of better than 0.8ps RMS is achieved over the 12kHz to 20MHz range. Phase noise performance of better than -125dBc/Hz at 1kHz is achieved with this design.

Applications

Clock-Data Recovery in Telecom/Datacom Applications

Data Retiming

Reference Clock Generation in Base Stations and Wireless Applications

Features

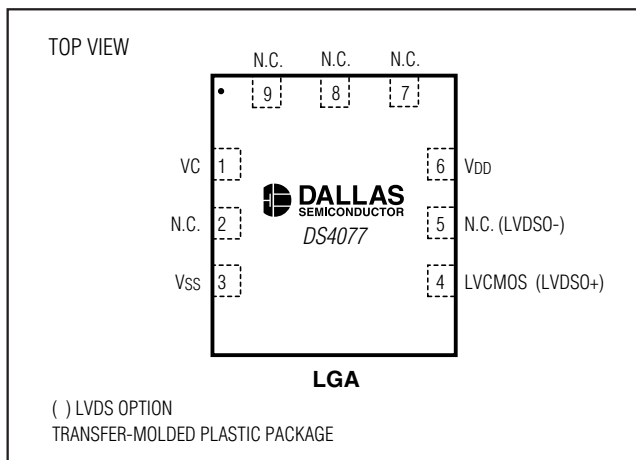
- ◆ 50MHz to 122.88MHz Frequency
- ◆ 3.135V to 3.465V Operation
- ◆ Low Jitter: < 0.8ps RMS
- ◆ ± 69 ppm Absolute Pull Range (APR)
- ◆ Output Options:
 - LVC MOS Output Buffer
 - LVDS Complementary Output Buffer
- ◆ Minimum ± 110 ppm Tuning Range (+25°C)
- ◆ 14mm x 9mm x 3.06mm Plastic LGA Package

Ordering Information

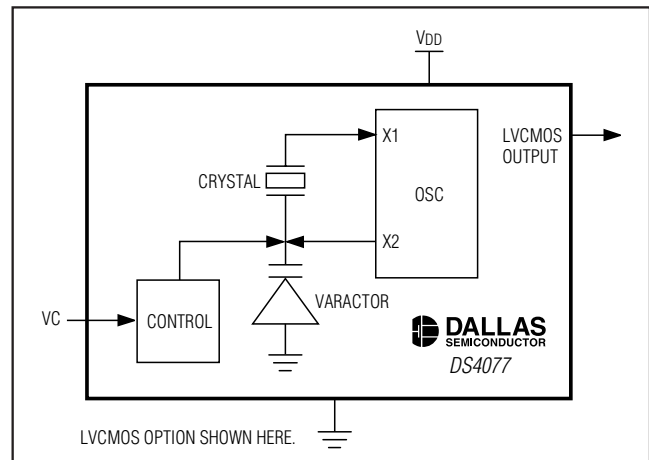
PART	TEMP RANGE	OUTPUT TYPE	FREQUENCY (f _{NOM}) (MHz)	PIN-PACKAGE	TOP MARK
DS4077L-DCN	-40°C to +85°C	LVC MOS	54	9 LGA	DS4077L-DCN
DS4077L-DDN	-40°C to +85°C	LVDS	54	9 LGA	DS4077L-DDN
DS4077L-CCN	-40°C to +85°C	LVC MOS	61.44	9 LGA	DS4077L-CCN
DS4077L-CDN	-40°C to +85°C	LVDS	61.44	9 LGA	DS4077L-CDN

Ordering Information continued at end of data sheet.

Pin Configuration



Block Diagram



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ABSOLUTE MAXIMUM RATINGS

VC, V _{DD} , LVCMOS, LVDSO+, LVDSO- Output-0.3V, +3.6V
Operating Temperature Range (noncondensing)-40°C to +85°C
Junction Temperature+150°C
Thermal Resistance	
Junction to Ambient91.06°C/W
Junction to Case44.51°C/W

Storage Temperature Range-55°C to +125°C
Soldering Temperature (reflow, 2 passes max)See IPC/JEDEC STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.) (Typical values at +25°C, V_{DD} = 3.3V, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD} Operating Supply Range	V _{DD}		3.135	3.3	3.465	V
V _{DD} Supply Current	I _{DD}	Output open	f _{OUT} ≤ 106.25MHz	20	30	mA
			f _{OUT} > 106.25MHz	25	35	
Frequency	f _{OUT}	VC = 1.6V, V _{DD} = 3.3V, T _A = +25°C (Note 2)	f _{NOM} -8ppm	f _{NOM}	f _{NOM} +8ppm	MHz
Frequency vs. V _{DD} Sensitivity	V _{DD} ppm	V _{DD} = 3.3V ±5%	-3.5		+11.5	ppm
Frequency vs. Load Sensitivity	LOADppm	10pF to 20pF (Note 3)		-1		ppm/pF
Frequency vs. Temperature	TEMPppm	From +25°C	-20		+20	ppm
VC Voltage Range	VCRANGE		0.3	1.60	2.8	V
Frequency Tuning Sensitivity	VC _{SEN}		41		164	ppm/V
Tuning Voltage Bandwidth	VC _{BW}	(Note 3)	10			kHz
Absolute Pull Range	f _{TUNE}	VC = 0.3V to 2.8V (Note 2)	-69		+69	ppm
VC Input Leakage	I _{LCV}	VC = 0V to V _{DD}	-500		+500	nA
Aging, First Year	AGEppm		-5		+5	ppm
Aging, Years 0–10	t _{AGE}	Total aging	-10		+10	ppm
LVDS OUTPUT						
Output High Voltage	VOHLVDSO	(Note 4)			1.475	V
Output Low Voltage	VOLLVDSO	(Note 4)	0.925			V
Differential Output Voltage	VODLVDSO	(Note 4)	250		400	mV
Output Common-Mode Variation	VLVDSOCOM	(Note 4)			150	mV
Offset Output Voltage	VOFFLVDSO	(Note 4)	1.125		1.275	V
Differential Output Impedance	ROLVDSO	(Note 3)	80		140	Ω
Output Current	I _{VSSLVDSO}	Short ground			40	mA
Output Current	I _{LVDSO}	Short together (Note 3)			12	mA
Output Rise Time (Differential)	t _{RLVDSO}	20% to 80% (Note 3)	150			ps
Output Fall Time (Differential)	t _{FLVDSO}	80% to 20% (Note 3)	150			ps

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 3.135V$ to $3.465V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.) (Typical values at $+25^{\circ}C$, $V_{DD} = 3.3V$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVC MOS OUTPUT						
Output Logic 0	V_{OL}	Output Current $-450\mu A$	0		0.4	V
Output Logic 1	V_{OH}	Output Current $+450\mu A$	$V_{DD} - 0.8V$		V_{DD}	V
Output Rise Time	t_R	Load condition: 10pF to ground; 10% to 90% V_{DD} (Note 3)			2	ns
Output Fall Time	t_F	Load condition: 10pF to ground; 90% to 10% V_{DD} (Note 3)			2	ns
Duty Cycle	DC_{CYC}	Load condition: 10pF, $V_{DD} / 2$ (Note 3)	40		60	%
Harmonics	H	$V_{DD} = 3.3V$, $T_A = +25^{\circ}C$ (Note 3)		-18	-8	dBc/Hz
SSB PHASE NOISE AND JITTER, $V_{DD} = 3.3$, $T_A = +25^{\circ}C$ (Note 3)						
10Hz Offset		LVC MOS		-70		dBc/Hz
100Hz Offset				-100		
1kHz Offset				-125		
10kHz Offset				-145		
100kHz Offset				-150		
Jitter (12kHz to 20MHz)				0.8		psRMS

Note 1: Limits at $-40^{\circ}C$ are guaranteed by design and not production tested.

Note 2: 10pF, LVC MOS.

Note 3: Guaranteed by design and not production tested.

Note 4: 100Ω differential load.

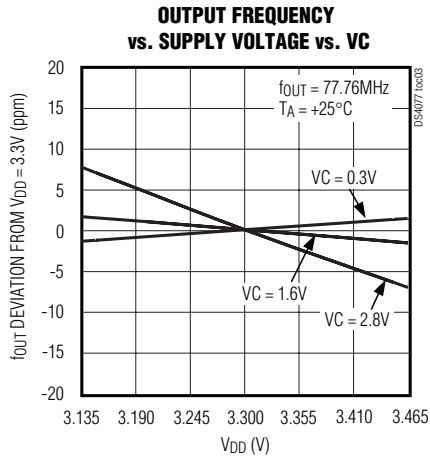
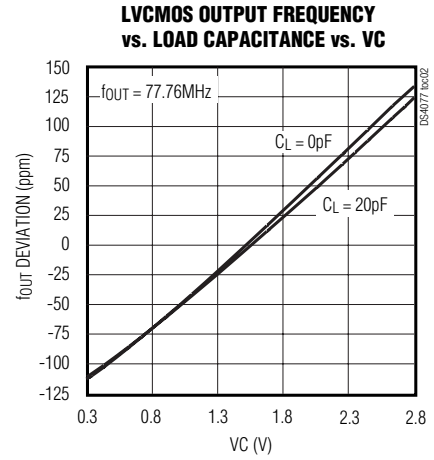
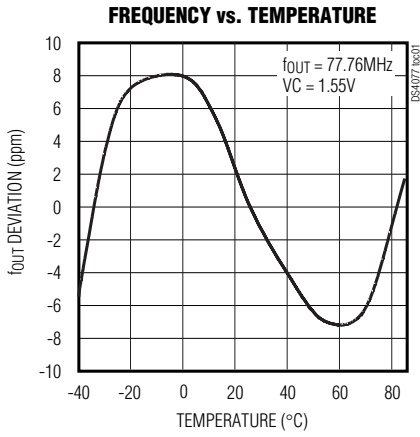
Pin Description

PIN		NAME	FUNCTION
LVC MOS	LVDS		
1	1	VC	VCXO Control Voltage
2, 5, 7, 8, 9	2, 7, 8, 9	N.C.	No Connection
3	3	V_{SS}	Ground
4	—	LVC MOS	LVC MOS Output
6	6	V_{DD}	DC Power
—	4, 5	LVDSO+/LVDSO-	LVDS Positive and Negative Outputs

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Typical Operating Characteristics

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



50MHz to 122.88MHz VCXO

Ordering Information (continued)

PART	TEMP RANGE	OUTPUT TYPE	FREQUENCY (f _{NOM}) (MHz)	PIN-PACKAGE	TOP MARK
DS4077L-ECN	-40°C to +85°C	LVC MOS	74.17582	9 LGA	DS4077L-ECN
DS4077L-EDN	-40°C to +85°C	LVDS	74.17582	9 LGA	DS4077L-EDN
DS4077L-FCN	-40°C to +85°C	LVC MOS	74.25	9 LGA	DS4077L-FCN
DS4077L-FDN	-40°C to +85°C	LVDS	74.25	9 LGA	DS4077L-FDN
DS4077L-ACN	-40°C to +85°C	LVC MOS	76.8	9 LGA	DS4077L-ACN
DS4077L-ADN	-40°C to +85°C	LVDS	76.8	9 LGA	DS4077L-ADN
DS4077L-0CN	-40°C to +85°C	LVC MOS	77.76	9 LGA	DS4077L-0CN
DS4077L-0DN	-40°C to +85°C	LVDS	77.76	9 LGA	DS4077L-0DN
DS4077L-GCN	-40°C to +85°C	LVC MOS	106.25	9 LGA	DS4077L-GCN
DS4077L-GDN	-40°C to +85°C	LVDS	106.25	9 LGA	DS4077L-GDN
DS4077L-BDN	-40°C to +85°C	LVDS	122.88	9 LGA	DS4077L-BDN

DS4077

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
9 LGA	L949A-1	21-0265

Revision History

- Rev 0; 8/05: Initial release.
- Rev 1; 12/05: Added LVDS option.
- Rev 2; 6/06: Changed device description/frequency range; changed jitter typical value from 1 to 0.8psRMS; added new parts numbers to Ordering Information table; changed jitter range upper limits from 80MHz to 20MHz.
- Rev 3; 9/06: Changed V_{DDppm} units from ppm/PF to ppm; added separate I_{DD} parameter for parts with f_{OUT} greater than 106.25MHz.

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Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 _____ 5

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