THE DATASHEET OF

LTC2704CGW-16#TRPBF

Quad 12-, 14- and 16-Bit Voltage Output SoftSpan DACs with Readback

FEATURES

- **Six Programmable Output Ranges:**
  Unipolar: 0V to 5V, 0V to 10V
  Bipolar: ±5V, ±10V, ±2.5V, –2.5V to 7.5V
- **Serial Readback of All On-Chip Registers**
- **1LSB INL and DNL Over the Industrial Temperature Range (LTC2704-14/LTC2704-12)**
- **Force/Sense Outputs Enable Remote Sensing**
- **Glitch Impulse: < 2nV-sec**
- Outputs Drive ±5mA
- Pin Compatible 12-, 14- and 16-Bit Parts
- Power-On and Clear to Zero Volts
- 44-Lead SSOP Package

APPLICATIONS

- Process Control and Industrial Automation
- Direct Digital Waveform Generation
- Software Controlled Gain Adjustment
- Automated Test Equipment

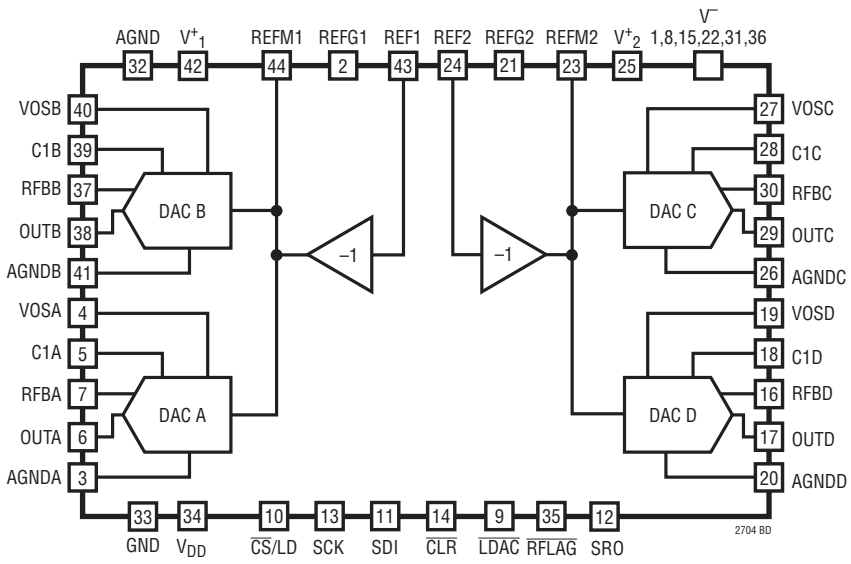
DESCRIPTION

The LTC®2704-16/LTC2704-14/LTC2704-12 are serial input, 12-, 14- or 16-bit, voltage output SoftSpan™ DACs that operate from 3V to 5V logic and ±5V to ±15V analog supplies. SoftSpan offers six output spans—two unipolar and four bipolar—fully programmable through the 3-wire SPI serial interface. INL is accurate to 1LSB (2LSB for the LTC2704-16). DNL is accurate to 1LSB for all versions.

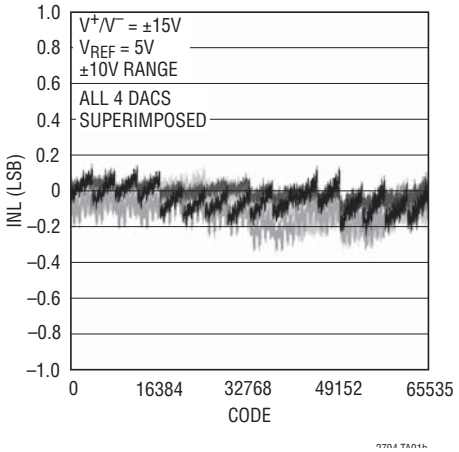
Readback commands allow verification of any on-chip register in just one 24- or 32- bit instruction cycle. All other commands produce a "rolling readback" response from the LTC2704, dramatically reducing the needed number of instruction cycles.

A Sleep command allows any combination of DACs to be powered down. There is also a reset flag and an offset adjustment pin for each channel.

BLOCK DIAGRAM



LTC2704-16
Integral Nonlinearity (INL)

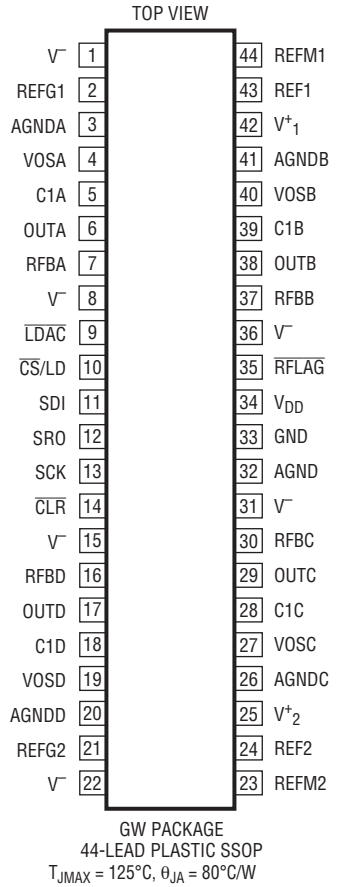


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage V^+_1, V^+_2 to V^- ..... –0.3V to 36V
V^+_1, V^+_2, REF1, REF2, REFM1, REFM2, OUTx, RFBx, V_{OSx} to GND, AGND, AGNDx, C1x, REFG1, REFG2 .....18V
GND, AGND, AGNDx, C1x, REFG1, REFG2 to V^+_1, V^+_2, V^-, REF1, REF2, REFM1, REFM2, OUTx, RFBx, V_{OSx} 18V
OUTA, RFBA, V_{OSA}, OUTB, RFBB, VOSB, REF1, REFM1 to GND, AGND ..... V^- – 0.3V to V^+_1 + 0.3V
OUTC, RFBC, V_{OSC}, OUTD, RFBD, V_{OSD}, REF2, REFM2 to GND, AGND..... V^- – 0.3V to V^+_2 + 0.3V
V_{DD}, Digital Inputs/Outputs to GND ..... –0.3V to 7V
Digital Inputs/Outputs to V_{DD} 0.3V
GND, AGNDx, REFG1, REFG2 to AGND.....±0.3V
C1x to AGNDx.....±0.3V
V^- to Any Pin 0.3V
Maximum Junction Temperature..... 150°C
Operating Temperature Range
LTC2704C ..... 0°C to 70°C
LTC2704I.....–40°C to 85°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....300°C

PIN CONFIGURATION



GW PACKAGE
44-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 80°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2704CGW-16#PBF	LTC2704CGW-16#TRPBF	LTC2704CGW-16	44-Lead Plastic SSOP	0°C to 70°C
LTC2704IGW-16#PBF	LTC2704IGW-16#TRPBF	LTC2704IGW-16	44-Lead Plastic SSOP	–40°C to 85°C
LTC2704CGW-14#PBF	LTC2704CGW-14#TRPBF	LTC2704CGW-14	44-Lead Plastic SSOP	0°C to 70°C
LTC2704IGW-14#PBF	LTC2704IGW-14#TRPBF	LTC2704IGW-14	44-Lead Plastic SSOP	–40°C to 85°C
LTC2704CGW-12#PBF	LTC2704CGW-12#TRPBF	LTC2704CGW-12	44-Lead Plastic SSOP	0°C to 70°C
LTC2704IGW-12#PBF	LTC2704IGW-12#TRPBF	LTC2704IGW-12	44-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C, $V^+_1 = V^+_2$ = 15V, V^- = –15V, V_{DD} = 5V, REF1 = REF2 = 5V, AGND = AGNDx = REFG1 = REFG2 = GND = 0V.

SYMBOL	PARAMETER	CONDITIONS		LTC2704-12 MIN	LTC2704-12 TYP	LTC2704-12 MAX	LTC2704-14 MIN	LTC2704-14 TYP	LTC2704-14 MAX	LTC2704-16 MIN	LTC2704-16 TYP	LTC2704-16 MAX	UNITS
Accuracy													
	Resolution		●	12			14			16			Bits
	Monotonicity		●	12			14			16			Bits
INL	Integral Nonlinearity	V_{REF} = 5V	●			±1			±1			±2	LSB
DNL	Differential Nonlinearity	V_{REF} = 5V	●			±1			±1			±1	LSB
GE	Gain Error	V_{REF} = 5V	●		±0.5	±2		±1	±5		±4	±20	LSB
	Gain Temperature Coefficient	ΔGain/ΔTemperature	●		±2			±2			±2		ppm/°C
V_{OS}	Unipolar Zero-Scale Error	Span = 0V to 5V, T_A = 25°C			±80	±200		± 80	±200		±80	±200	µV
		Span = 0V to 10V, T_A = 25°C			±100	±300		±100	±300		±100	±300	µV
		Span = 0V to 5V	●		±140	±400		±140	±400		±140	±400	µV
		Span = 0V to 10V	●		±150	±600		±150	±600		±150	±600	µV
	V_{OS} Temperature Coefficient	0V to 5V Range	●		±2			±2			±2		µV/°C
		0V to 10V Range	●		±2			±2			±2		µV/°C
BZE	Bipolar Zero Error	All Bipolar Ranges			±0.25	±1		±0.5	±2		±2	±8	LSB
			●			±2			±2.5			±12	LSB
PSRR	Power Supply Rejection Ratio	V_{DD} = 5V ±10% (Note 3)			±0.003			±0.013			±0.05		LSB/V
		V_{DD} = 3V ±10% (Note 3)			±0.006			±0.025			±0.1		LSB/V
		0V to 10V Range, Code = 0											
		V^+/V^- = ±15V ±10% (Note 2)	●		±0.001	±0.06		±0.005	±0.25		±0.02	±0.1	LSB/V
		V^+/V^- = ±5V ±10%, V_{REF} = 2V (Note 2)	●		±0.002	±0.05		±0.01	±0.13		±0.04	±0.5	LSB/V
Analog Outputs (Note 4)													
	Settling Time	0V to 5V Range, 5V Step, to ±1LSB			3			3.5			4		µs
		0V to 10V or ±5V Range, 10V Step, to ±1LSB			5			5.5			6		µs
		±10V Range, 20V Step, to ±1LSB			8			9			10		µs
	Output Swing	V^+/V^- = ±15V, V_{REF} = ±7.25V, 0V to 10V Range, I_{LOAD} = ±3mA (Note 2)	●	–14.3		14.3	–14.3		14.3	–14.3		14.3	V
		V^+/V^- = ±5V, V_{REF} = ±2.25V, 0V to 10V Range, I_{LOAD} = ±2.5mA (Note 2)	●	–4.5		4.5	–4.5		4.5	–4.5		4.5	V
	Load Current	V^+/V^- = ±10.8V to ±16.5V, V_{REF} = ±5V, 0V to 10V Range, V_{OUT} = ±10V (Note 2)				±5			±5			±5	mA
			●			±4			±4			±4	mA
		V^+/V^- = ±4.5V to ±16.5V, V_{REF} = ±2V, 0V to 10V Range, V_{OUT} = ±4V (Note 2)				±3			±3			±3	mA
			●			±2.7			±2.7			±2.7	mA
	Load Regulation	V^+/V^- = ±15V, V_{REF} = 5V, 0V to 10V Range, Code = 0, ±5mA Load (Note 2)	●			±0.005			±0.01			±0.04	LSB/mA
		V^+/V^- = ±5V, V_{REF} = 2V, 0V to 10V Range, Code = 0, ±3mA Load (Note 2)	●			±0.01			±0.013			±0.05	LSB/mA
	Output Impedance	V_{REF} = 5V, 0V to 10V Range, Code = 0, ±5mA Load	●			0.015			0.006			0.006	Ω
I_{SC}	Short-Circuit Current	V^+/V^- = ±16.5V, V_{REF} = 5V, ±10V Range Code = 0, V_{OUT} Shorted to V^+ (Note 2)	●			38			38			38	mA
		Code = Full Scale, V_{OUT} Shorted to V^-	●	–36			–36			–36			mA
		V^+/V^- = ±5.5V, V_{REF} = 2V, ±10V Range Code = 0, V_{OUT} Shorted to V^+ (Note 2)	●			38			38			38	mA
		Code = Full Scale, V_{OUT} Shorted to V^-	●	–36			–36			–36			mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C, V^+_1 = V^+_2 = 15V, V^- = –15V, V_{DD} = 5V, REF1 = REF2 = 5V, AGND = AGNDx = REFG1 = REFG2 = GND = 0V.

SYMBOL	PARAMETER	CONDITIONS		LTC2704-12 MIN	LTC2704-12 TYP	LTC2704-12 MAX	LTC2704-14 MIN	LTC2704-14 TYP	LTC2704-14 MAX	LTC2704-16 MIN	LTC2704-16 TYP	LTC2704-16 MAX	UNITS
SR	Slew Rate	R_L= 2k, V^+/V^- = ±15V (Note 2) R_L= 2k, V^+/V^- = ±5V (Note 2)	● ●	2.2 2.0	3 2.8		2.2 2.0	3 2.8		2.2 2.0	3 2.8		V/µs V/µs
	Capacitive Load Driving	Within Maximum Load Current			1000			1000			1000		pF

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C, V^+_1 = V^+_2 = 15V, V^- = –15V, V_{DD} = 5V, REF1 = REF2 = 5V, AGND = AGNDx = REFG1 = REFG2 = GND = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Inputs							
	REF1, REF2 Input Voltage	V^+/V^- = ±15V, 0V to 5V Span (Note 2)	●	–14.5		14.5	V
Resistances							
R_{REF1}, R_{REF2}	Reference Input Resistance		●	5	7		kΩ
R_{FBx}	Output Feedback Resistance		●	7	10		kΩ
R_{VOSX}	Offset Adjust Input Resistance		●	700	1000		kΩ
AC Performance (Note 4)							
	Glitch Impulse	0V to 5V Range, Midscale Transition			2		nV-s
	Crosstalk	10V Step on V_{OUTA} DAC B: 0V to 5V Range, Full Scale DAC B: 0V to 10V Range, Full Scale			 2 3		 nV-s nV-s
	Digital Feedthrough	±10V Range, Midscale			0.2		nV-s
	Multiplying Feedthrough Error	0V to 10V Range, V_{REF} = ±5V, 10kHz Sine Wave			0.35		mV_{P-P}
	Multiplying Bandwidth	Span = 0V to 5V, Full Scale Span = 0V to 10V, Full Scale			300 250		kHz kHz
	Output Noise Voltage Density	10kHz Span = 0V to 5V, Midscale Span = 0V to 10V, Midscale			 30 50		 $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Output Noise Voltage	0.1Hz to 10Hz Span = 0V to 5V, Midscale Span = 0V to 10V, Midscale			 0.8 1.2		 μV_{RMS} μV_{RMS}
Power Supply							
I_{DD}	Supply Current, V_{DD}	Digital Inputs = 0V or V_{DD}	●		0.5	2	µA
I_S	Supply Current, V^+/V^-	V^+/V^- = ±15V, ±10%; V_{REF} = 5V, V_{OUT} = 0V (Note 2) V^+/V^- = ±5V, ±10%; V_{REF} = 2V, V_{OUT} = 0V (Note 2) Sleep Mode—All DACs (Note 4)	● ● 		17.5 17.0 	20 18 1	mA mA mA
V_{DD}	Logic Supply Voltage		●	2.7		5.5	V
V^+_1/V^+_2	Positive Analog Supply Voltage		●	4.5		16.5	V
V^-	Negative Analog Supply Voltage		●	–16.5		–4.5	V
Digital Inputs/Outputs							
V_{IH}	Digital Input High Voltage	V_{DD} = 2.7V to 5.5V V_{DD} = 2.7V to 3.3V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{DD} = 2.7V to 5.5V V_{DD} = 4.5V to 5.5V	● ●			0.6 0.8	V V
V_{OH}	Digital Output High Voltage	I_{OH} = 200µA	●	V_{CC} – 0.4			V
V_{OL}	Digital Output Low Voltage	I_{OL} = 200µA	●			0.4	V
I_{IN}	Digital Input Current		●		0.001	±1	µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	Digital Input Capacitance	V_{IN} = 0V (Note 3)	●			5	pF

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} = 4.5V to 5.5V							
t_1	SDI Valid to SCK Setup		●	7			ns
t_2	SDI Valid to SCK Hold		●	7			ns
t_3	SCK High Time		●	11			ns
t_4	SCK Low Time		●	11			ns
t_5	$\overline{CS}$/LD Pulse Width		●	9			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	0			ns
t_7	$\overline{CS}$/LD Low to SCK Positive Edge		●	12			ns
t_8	$\overline{CS}$/LD High to SCK Positive Edge		●	12			ns
t_9	SRO Propagation Delay	C_{LOAD} = 10pF	●			18	ns
t_{10}	$\overline{CLR}$ Pulse Width		●	50			ns
t_{11}	$\overline{LDAC}$ Pulse Width		●	15			ns
t_{12}	$\overline{CLR}$ Low to $\overline{RFLAG}$ Low	C_{LOAD} = 10pF (Note 3)	●			50	ns
t_{13}	$\overline{CS}$/LD High to $\overline{RFLAG}$ High	C_{LOAD} = 10pF (Note 3)	●			40	ns
	SCK Frequency	50% Duty Cycle (Note 5)	●			40	MHz
V_{DD} = 2.7V to 3.3V							
t_1	SDI Valid to SCK Setup		●	9			ns
t_2	SDI Valid to SCK Hold		●	9			ns
t_3	SCK High Time		●	15			ns
t_4	SCK Low Time		●	15			ns
t_5	$\overline{CS}$/LD Pulse Width		●	12			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	0			ns
t_7	$\overline{CS}$/LD Low to SCK Positive Edge		●	12			ns
t_8	$\overline{CS}$/LD High to SCK Positive Edge		●	12			ns
t_9	SRO Propagation Delay	C_{LOAD} = 10pF	●			26	ns
t_{10}	$\overline{CLR}$ Pulse Width		●	90			ns
t_{11}	$\overline{LDAC}$ Pulse Width		●	20			ns
t_{12}	$\overline{CLR}$ Low to $\overline{RFLAG}$ Low	C_{LOAD} = 10pF	●			70	ns
t_{13}	$\overline{CS}$/LD High to $\overline{RFLAG}$ High	C_{LOAD} = 10pF	●			60	ns
	SCK Frequency	50% Duty Cycle (Note 5)	●			25	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The notation V^+ is used to denote both V^+_1 and V^+_2 when the same voltage is applied to both pins.

Note 3: Guaranteed by design, not subject to test.

Note 4: Measured in unipolar 0V to 5V mode.

Note 5: When using SRO, maximum SCK frequency f_{MAX} is limited by SRO propagation delay as follows:

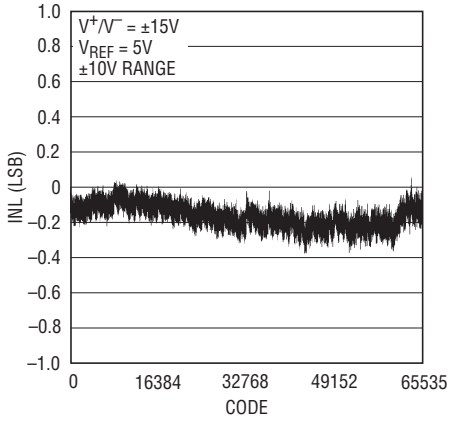
$$f_{MAX} = \left(\frac{1}{2(t_9 + t_S)}\right)$$

, where t_s is the setup time of the receiving device.

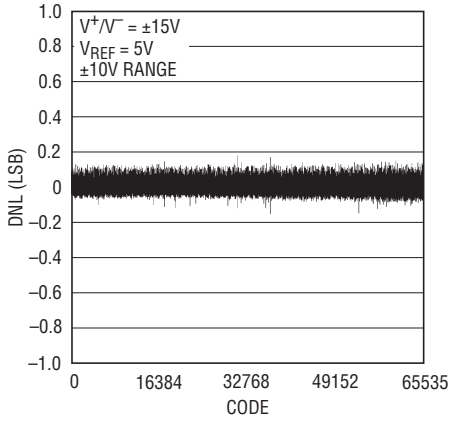
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2704-16

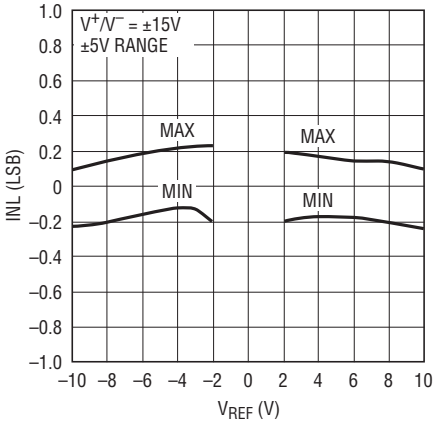
Integral Nonlinearity (INL)



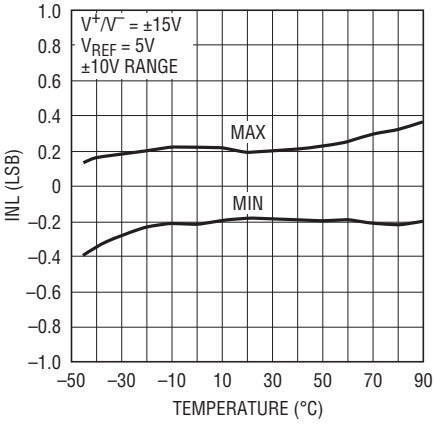
Differential Nonlinearity (DNL)



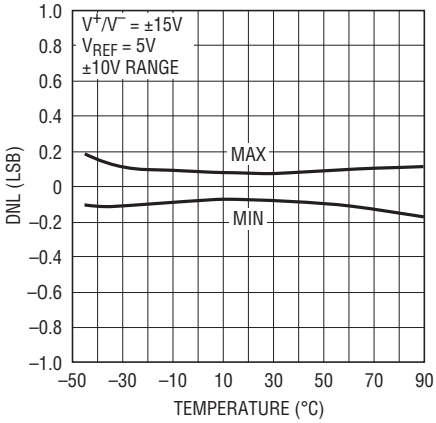
INL vs V_{REF}



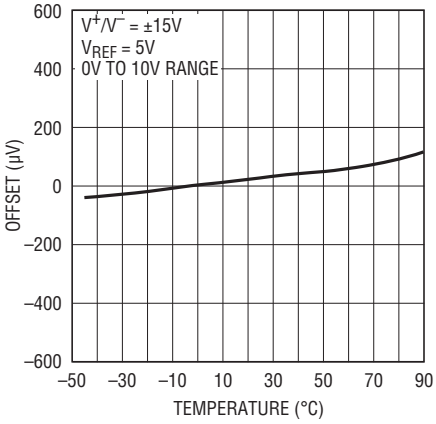
INL vs Temperature



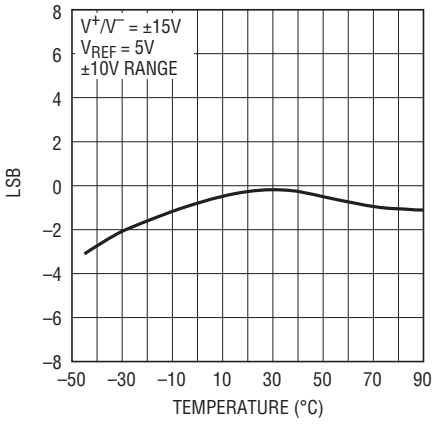
DNL vs Temperature



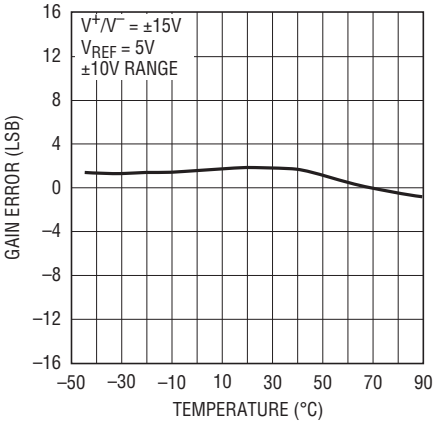
Offset vs Temperature



Bipolar Zero vs Temperature



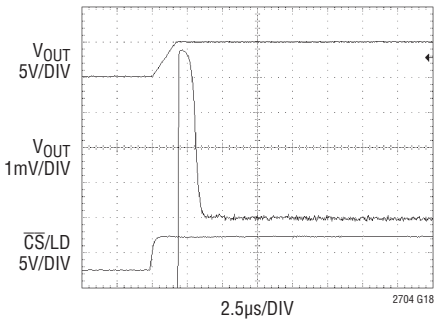
Gain Error vs Temperature



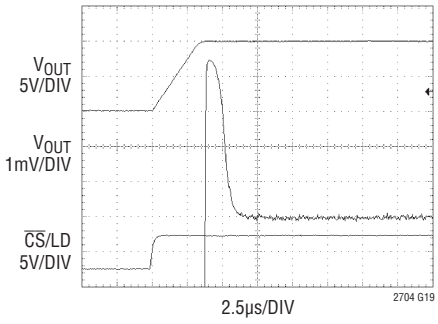
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2704-16

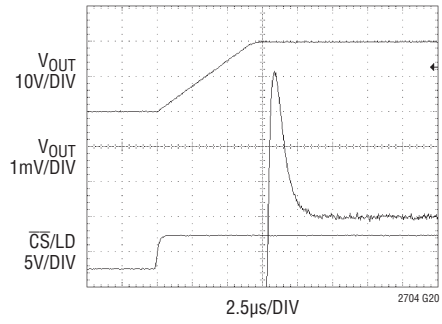
Settling 0V to 5V



Settling 0V to 10V

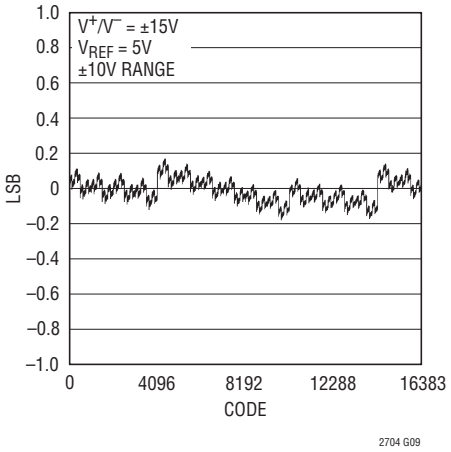


Settling ±10V

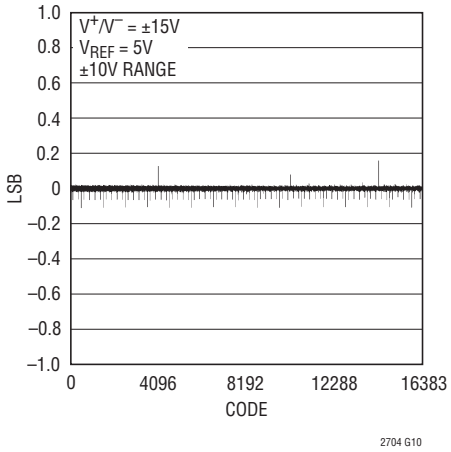


LTC2704-14

Integral Nonlinearity (INL)

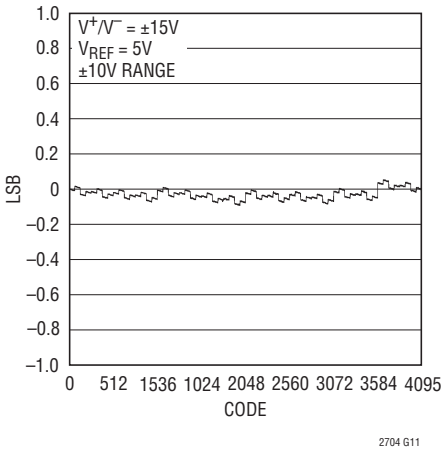


Differential Nonlinearity (DNL)

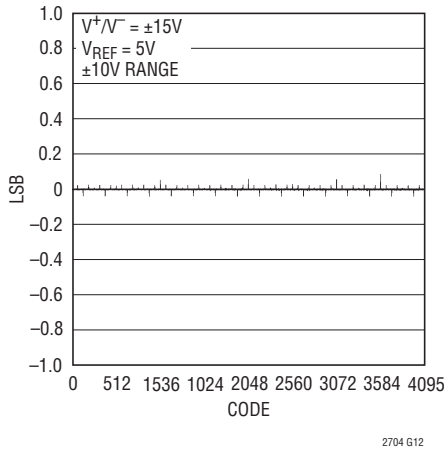


LTC2704-12

Integral Nonlinearity (INL)



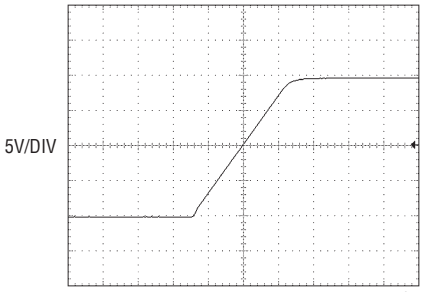
Differential Nonlinearity (DNL)



TYPICAL PERFORMANCE CHARACTERISTICS

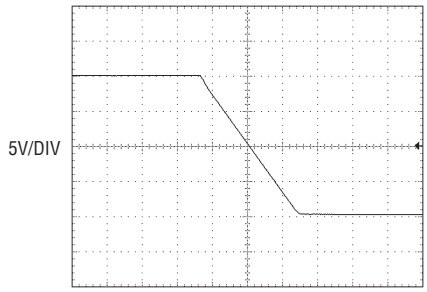
LTC2704-16/LTC2704-14/LTC2704-12

Positive Slew



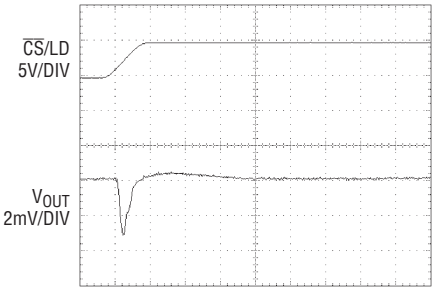
V^+/V^- = ±15V 2.5µs/DIV
V_{REF} = 5V
±10V RANGE
20V STEP

Negative Slew

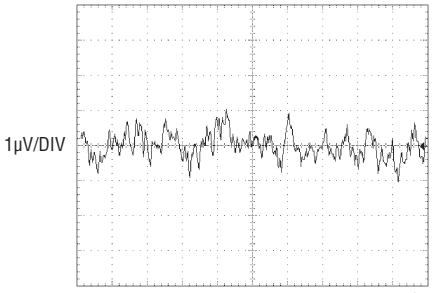


V^+/V^- = ±15V 2.5µs/DIV
V_{REF} = 5V
±10V RANGE
20V STEP

Midscale Glitch

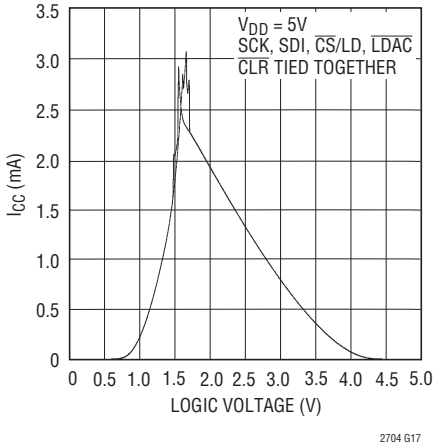


0.1Hz to 10Hz Noise



V^+/V^- = ±15V 1s/DIV
V_{REF} = 5V
0V TO 5V RANGE
CODE = 0

V_{CC} Supply Current vs Logic Voltage



PIN FUNCTIONS

V^- (Pins 1, 8, 15, 22, 31, 36): Analog Negative Supply, Typically –15V. –4.5V to –16.5V Range.

REFG1 (Pin 2): Reference 1 Ground. High impedance input, does not carry supply currents. Tie to clean analog ground.

AGNDA (Pin 3): DAC A Signal Ground. High impedance input, does not carry supply currents. Tie to clean analog ground.

VOSA (Pin 4): Offset Adjust for DAC A. Nominal input range is ±5V. V_{OS}(DAC A) = –0.01• V(VOSA) [0V to 5V, ±2.5V modes]. See Operation section.

C1A (Pin 5): Feedback Capacitor Connection for DAC A Output. This pin provides direct access to the negative input of the channel A output amplifier.

OUTA (Pin 6): DAC A Voltage Output Pin. For best load regulation, this open-loop amplifier output is connected to RFBA as close to the load as possible.

RFBA (Pin 7): DAC A Output Feedback Resistor Pin.

$\overline{\text{LDAC}}$ (Pin 9): Asynchronous DAC Load Input. When $\overline{\text{LDAC}}$ is a logic low, all DACs are updated.

PIN FUNCTIONS

$\overline{CS}$/LD (Pin 10): Synchronous Chip Select and Load Pin.

SDI (Pin 11): Serial Data Input. Data is clocked in on the rising edge of the serial clock when $\overline{CS}$/LD is low.

SRO (Pin 12): Serial Readback Data Output. Data is clocked out on the falling edge of SCK. Readback data begins clocking out after the last address bit A0 is clocked in.

SCK (Pin 13): Serial Clock.

$\overline{CLR}$ (Pin 14): Asynchronous Clear Pin. When this pin is low, all code and span B2 registers are cleared to zero. All DAC outputs are cleared to zero volts.

RFBD (Pin 16): DAC D Voltage Output Feedback Resistor Pin.

OUTD (Pin 17): DAC D Voltage Output Pin. For best load regulation, this open-loop amplifier output is connected to RFBD as close to the load as possible.

C1D (Pin 18): Feedback Capacitor Connection for DAC D Output. This pin provides direct access to the negative input of the channel D output amplifier.

VOSD (Pin 19): Offset Adjust for DAC D. Nominal input range is ±5V. V_{OS}(DAC D) = –0.01• V(VOSD) [0V to 5V, ±2.5V modes]. See Operation section.

AGNDD (Pin 20): DAC D Signal Ground. High impedance input, does not carry supply currents. Tie to clean analog ground.

REFG2 (Pin 21): Reference 2 Ground. High impedance input, does not carry supply currents. Tie to clean analog ground.

REFM2 (Pin 23): Reference 2 Inverting Amp Output. The gain from REF2 to REFM2 is –1. Can swing to within 0.5V of the analog supplies V^+/V^-.

REF2 (Pin 24): DAC C and DAC D Reference Input.

V^+_2 (Pin 25): Analog Positive Supply for DACs C and D. Typically 15V. 4.5V to 16.5V Range. Can be different from V^+_1.

AGNDC (Pin 26): DAC C Signal Ground. High impedance input, does not carry supply currents. Tie to clean analog ground.

VOSC (Pin 27): Offset Adjust for DAC C. Nominal input range is ±5V. V_{OS}(DAC C) = –0.01• V(VOSC) [0V to 5V, ±2.5V modes]. See Operation section.

C1C (Pin 28): Feedback Capacitor Connection for DAC C Output. This pin provides direct access to the negative input of the channel C output amplifier.

OUTC (Pin 29): DAC C Voltage Output Pin. For best load regulation, this open-loop amplifier output is connected to RFBC as close to the load as possible.

RFBC (Pin 30): DAC C Output Feedback Resistor Pin.

AGND (Pin 32): Analog Ground Pin. Tie to clean analog ground.

GND (Pin 33): Ground Pin. Tie to clean analog ground.

V_{DD} (Pin 34): Logic Supply. 2.7V to 5.5V Range.

$\overline{RFLAG}$ (Pin 35): Reset Flag Pin. An active low output is asserted when there is a power on reset or a clear event. Returns high when an update command is executed.

RFBB (Pin 37): DAC B Output Feedback Resistor Pin.

OUTB (Pin 38): DAC B Voltage Output Pin. For best load regulation, this open-loop amplifier output is connected to RFBB as close to the load as possible.

C1B (Pin 39): Feedback Capacitor Connection for DAC B Output. This pin provides direct access to the negative input of the channel B output amplifier.

VOSB (Pin 40): Offset Adjust for DAC B. Nominal input range is ±5V. V_{OS}(DAC B) = –0.01 • V(VOSB) [0V to 5V, ±2.5V modes]. See Operation section.

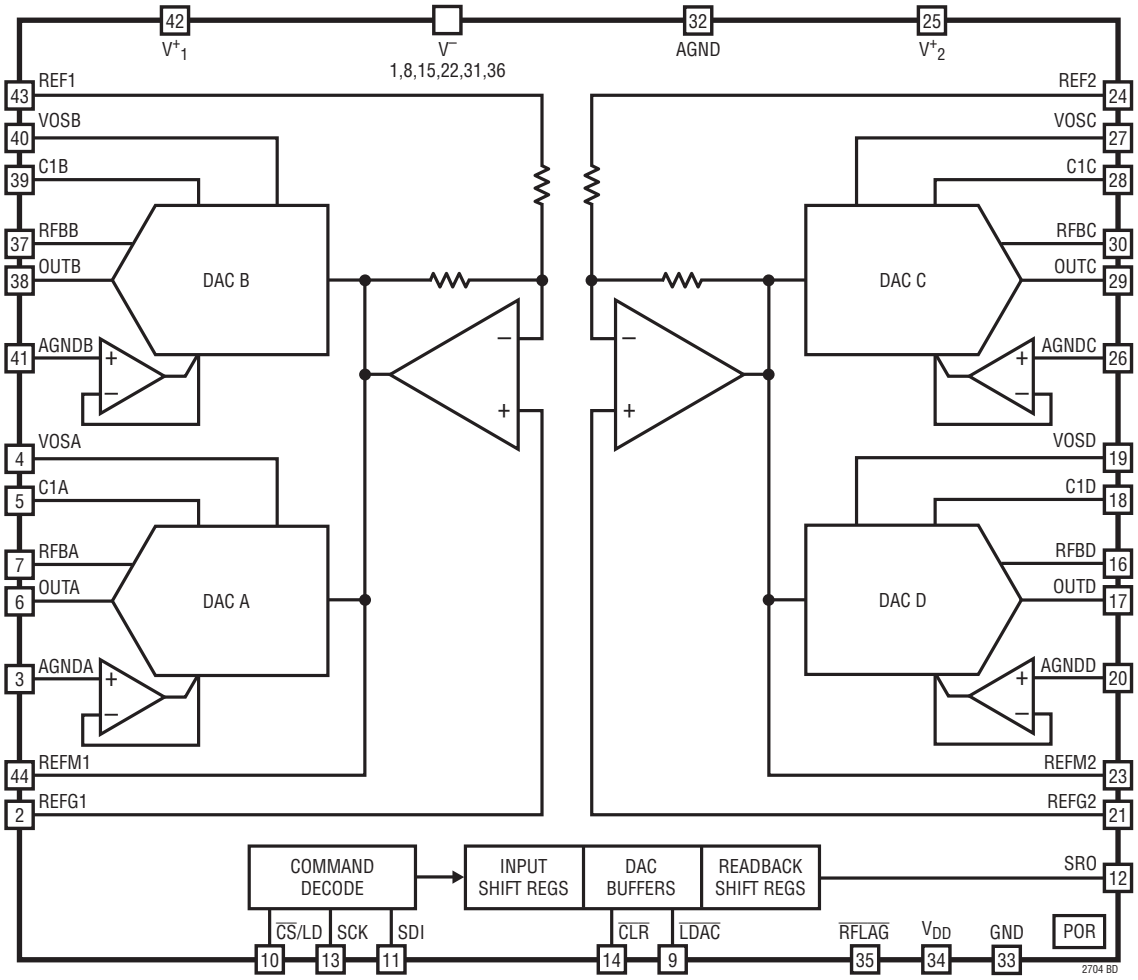
AGNDB (Pin 41): DAC B Signal Ground. High impedance input, does not carry supply currents. Tie to clean analog ground.

V^+_1 (Pin 42): Analog Positive Supply for DACs A DND B. Typically 15V. 4.5V to 16.5V Range. Can be different from V^+_2.

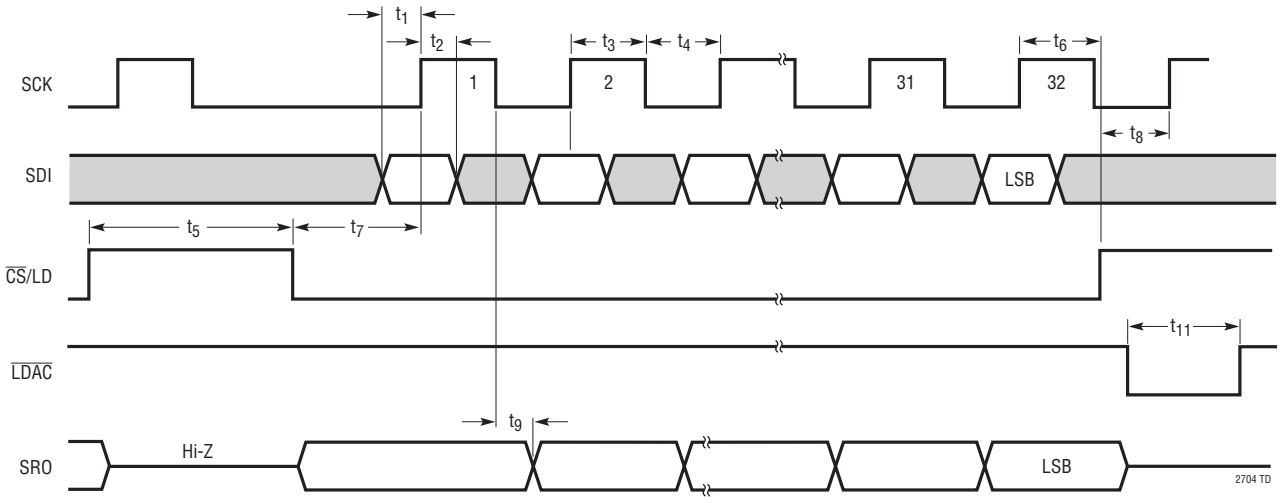
REF1 (Pin 43): DAC A and DAC B Reference Input.

REFM1 (Pin 44): Reference 1 Inverting Amp Output. The gain from REF1 to REFM1 is –1. Can swing to within 0.5V of the analog supplies V^+/V^-.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

SERIAL INTERFACE

When the $\overline{CS}$/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock signal (SCK pin). The minimum (24-bit wide) loading sequence required for the LTC2704 is a 4-bit command word (C3 C2 C1 C0), followed by a 4-bit address word (A3 A2 A1 A0) and 16 data (span or code) bits, MSB first. Figure 1 shows the SDI input word syntax to use when writing a code or span. If a 32-bit input sequence is needed, the first eight bits must be zeros, followed by the same sequence as for a 24-bit wide input. Figure 2 shows the input and readback sequences for both 24-bit and 32-bit operations.

When $\overline{CS}$/LD is low, the Serial Readback Output (SRO) pin is an active output. The readback data begins after the command (C3-C0) and address (A3-A0) words have been shifted into SDI. For a 24-bit load sequence, the 16 readback bits are shifted out on the falling edges of clocks 8-23, suitable for shifting into a microprocessor on the rising edges of clocks 9-24. For a 32-bit load sequence, add 8 to these clock cycle counts; see Figure 2b.

When $\overline{CS}$/LD is high, the SRO pin presents a high impedance (three-state) output. At the beginning of a load sequence, when $\overline{CS}$/LD is taken low, SRO outputs a logic low until the readback data begins.

When the asynchronous load pin, $\overline{LDAC}$, is taken low, all DACs are updated with code and span data (data in B1 buffers is copied into B2 buffers). $\overline{CS}$/LD must be high during this operation. The use of $\overline{LDAC}$ is functionally identical to the "Update B1→B2" commands.

The codes for the command word (C3-C0) are defined in Table 1; Table 2 defines the codes for the address word (A3-A0).

READBACK

Each DAC has two pairs of double-buffered digital registers, one pair for DAC code and the other for the output span (four buffers per DAC). Each double-buffered pair comprises two registers called buffer 1 (B1) and buffer 2 (B2).

B1 is the holding buffer. When data is shifted into B1 via a write operation, DAC outputs are not affected. The contents of B2 can only be changed by copying the contents of B1 into B2 via an update operation (B1 and B2 can be changed together, see commands 0110-1001 in Table 1). The contents of B2 (DAC code or DAC span) directly control the DAC output voltage or the DAC output range.

Additionally each DAC has one readback register associated with it. When a readback command is issued to a DAC, the contents of one of its four buffers is copied into its readback register and serially shifted out onto the SRO pin. Figure 2 shows the loading and readback sequences. In the 16-bit data field (D15-D0 for the LTC2704-16, see Figure 2a) of any write or update command, the readback pin (SRO) shifts out the contents of the buffer which was specified in the preceding command. This "rolling readback" mode of operation can be used to reduce the number of operations, since any command can be verified during succeeding commands with no additional overhead. Table 1 shows the location (readback pointer) of the data which will be output from SRO during the next instruction.

For readback commands, the data is shifted out during the readback instruction itself (on the 16 falling SCK edges immediately after the last address bit is shifted in on SDI).

When programming the span of a DAC, the span bits are the last four bits shifted in; and when checking the span of a DAC using SRO, the span bits are likewise the last four bits shifted out. Table 3 shows the span codes.

When span information is read back on SRO, the sleep status of the addressed DAC is also output. The sleep status bit, SLP, occurs sequentially just before the four span bits. The sequence is shown in Figures 2a and 2b. See Table 4 for SLP codes. Note that SLP is an output bit only; sleep is programmed by using command code 1110 along with the desired address. Any update command, including the use of $\overline{LDAC}$, wakes the addressed DAC(s).

OPERATION

OUTPUT RANGES

The LTC2704 is a quad DAC with software-programmable output ranges. SoftSpan provides two unipolar output ranges (0V to 5V and 0V to 10V), and four bipolar ranges (±2.5V, ±5V, ±10V and –2.5V to 7.5V). These ranges are obtained when an external precision 5V reference and analog supplies of ±12V to ±15V are used. When a reference voltage of 2V and analog supplies of ±5V are used, the SoftSpan ranges become: 0V to 2V, 0V to 4V, ±1V, ±2V, ±4V and –1V to 3V. The output ranges are linearly scaled for references other than 2V and 5V (appropriate analog supplies should be used within the range ±5V to ±15V). Each of the four DACs can be programmed to any one of the six output ranges. DAC outputs can swing to ±10V on ±10.8V supplies (±12V supplies with ±10% tolerance) while sourcing or sinking 5mA of load current.

Table 1. Command Codes

CODE						
C3	C2	C1	C0	COMMAND	READBACK POINTER— CURRENT INPUT WORD W_0	READBACK POINTER— NEXT INPUT WORD W_{+1}
0	0	1	0	Write to B1 Span DAC n	Set by Previous Command	B1 Span DAC n
0	0	1	1	Write to B1 Code DAC n	Set by Previous Command	B1 Code DAC n
0	1	0	0	Update B1→B2 DAC n	Set by Previous Command	B2 Span DAC n
0	1	0	1	Update B1→B2 All DACs	Set by Previous Command	B2 Code DAC n
0	1	1	0	Write to B1 Span DAC n Update B1→B2 DAC n	Set by Previous Command	B2 Span DAC n
0	1	1	1	Write to B1 Code DAC n Update B1→B2 DAC n	Set by Previous Command	B2 Code DAC n
1	0	0	0	Write to B1 Span DAC n Update B1→B2 All DACs	Set by Previous Command	B2 Span DAC n
1	0	0	1	Write to B1 Code DAC n Update B1→B2 All DACs	Set by Previous Command	B2 Code DAC n
1	0	1	0	Read B1 Span DAC n	B1 Span DAC n	
1	0	1	1	Read B1 Code DAC n	B1 Code DAC n	
1	1	0	0	Read B2 Span DAC n	B2 Span DAC n	
1	1	0	1	Read B2 Code DAC n	B2 Code DAC n	
1	1	1	0	Sleep DAC n (Note 1)	Set by Previous Command	B2 Span DAC n
1	1	1	1	No Operation	Set by Previous Command	B2 Code DAC n

Codes not shown are reserved and should not be used.
Note 1: Normal operation can be resumed by issuing any update B1→B2 command to the sleeping DAC.

Table 2. Address Codes

A3	A2	A1	A0	n	READBACK POINTER n
0	0	0	0	DAC A	DAC A
0	0	1	0	DAC B	DAC B
0	1	0	0	DAC C	DAC C
0	1	1	0	DAC D	DAC D
1	1	1	1	All DACs	DAC A

Codes not shown are reserved and should not be used.

Table 3. Span Codes

S3	S2	S1	S0	SPAN
0	0	0	0	Unipolar 0V to 5V
0	0	0	1	Unipolar 0V to 10V
0	0	1	0	Bipolar –5V to 5V
0	0	1	1	Bipolar –10V to 10V
0	1	0	0	Bipolar –2.5V to 2.5V
0	1	0	1	Bipolar –2.5V to 7.5V

Codes not shown are reserved and should not be used.

OPERATION

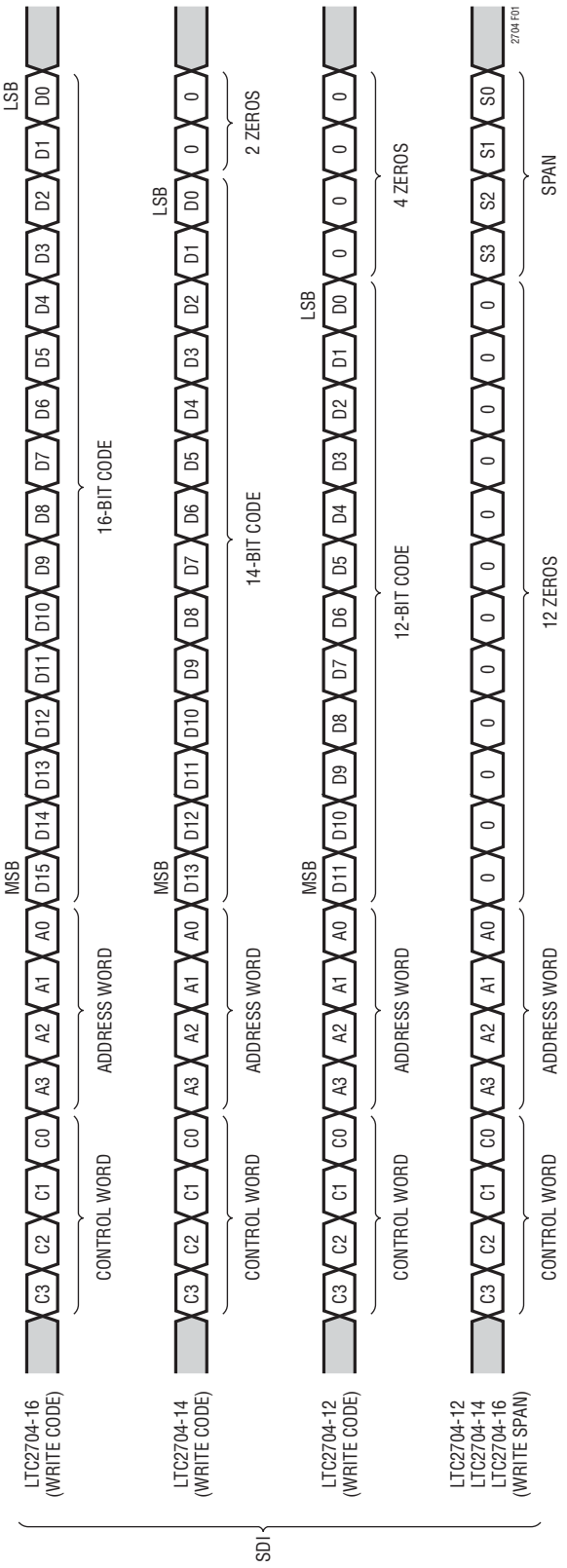


Figure 1. Input Words

OPERATION

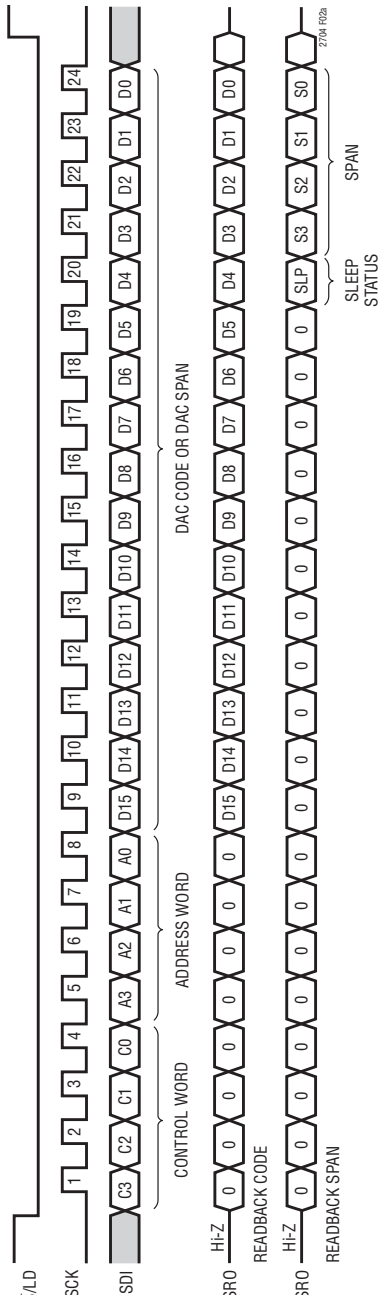


Figure 2a. 24-Bit Load Sequence

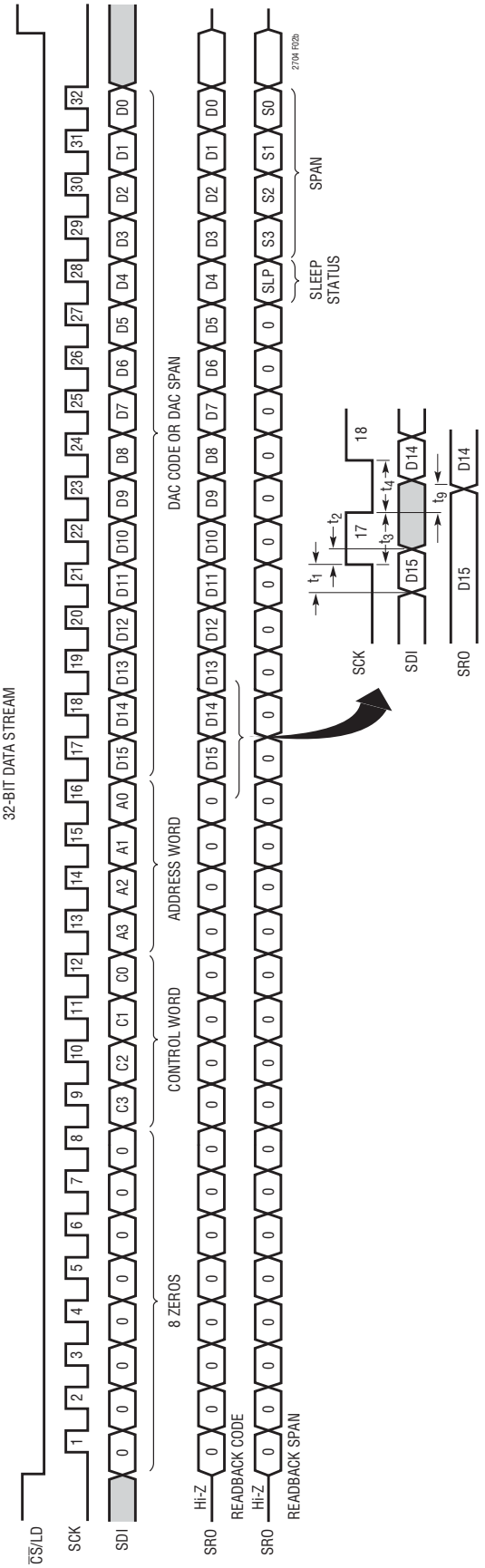


Figure 2b. 32-Bit Load Sequence

OPERATION

Examples

1. Using a 24-bit loading sequence, load DAC A with the unipolar range of 0V to 10V, output at zero volts and all other DACs with the bipolar range of ±10V, outputs at zero volts. Note all DAC outputs should change at the same time.
   a) $\overline{CS}$/LD↓
   b) Clock SDI = 0010 1111 0000 0000 0000 0011
   c) $\overline{CS}$/LD↑
      B1-Range of all DACs set to bipolar ±10V.
   d) $\overline{CS}$/LD↓
      Clock SDI = 0010 0000 0000 0000 0000 0001
   e) $\overline{CS}$/LD↑
      B1-Range of DAC A set to unipolar 0V to 10V.
   f) $\overline{CS}$/LD↓
      Clock SDI = 0011 1111 1000 0000 0000 0000
   g) $\overline{CS}$/LD↑
      B1-Code of all DACs set to midscale.
   h) $\overline{CS}$/LD↓
      Clock SDI = 0011 0000 0000 0000 0000 0000
   i) $\overline{CS}$/LD↑
      B1-Code of DAC A set to zero code.
   j) $\overline{CS}$/LD↓
      Clock SDI = 0100 1111 XXXX XXXX XXXX XXXX
   k) $\overline{CS}$/LD↑
      Update all DACs B1s into B2s for both Code and Range.
   l) Alternatively steps j and k could be replaced with $\overline{LDAC}$ ⎍.
2. Using a 32-bit load sequence, load DAC C with bipolar ±2.5V and its output at zero volts. Use readback to check B1 contents before updating the DAC output (i.e., before copying B1 contents into B2).
   a) $\overline{CS}$/LD↓ (Note that after power-on, the Code in B1 is zero)
   b) Clock SDI = 0000 0000 0011 0100 1000 0000 0000 0000
   c) $\overline{CS}$/LD↑
      B1-Code of DAC C set to midscale setting.
   d) $\overline{CS}$/LD↓
      Clock SDI = 0000 0000 0010 0100 0000 0000 0000 0100
   e) Read Data out on SRO = 1000 0000 0000 0000
      Verifies that B1-Code DAC C is at midscale setting.
   f) $\overline{CS}$/LD↑
      B1-Range of DAC C set to Bipolar ±2.5V range.
   g) $\overline{CS}$/LD↓
      Clock SDI = 0000 0000 1010 0100 xxxx xxxx xxxx xxxx
      Data Out on SRO = 0000 0000 0000 0100
      Verifies that B1-Range of DAC C set to Bipolar ±2.5V Range.
      $\overline{CS}$/LD↑
   h) $\overline{CS}$/LD↓
      Clock SDI = 0000 0000 0100 0100 xxxx xxxx xxxx xxxx
   i) $\overline{CS}$/LD↑
      Update DAC C B1 into B2 for both Code and Range
   j) Alternatively steps h and i could be replaced with $\overline{LDAC}$ ⎍.

System Offset Adjustment

Many systems require compensation for overall system offset, which may be an order of magnitude or more greater than the excellent offset of the LTC2704.

The LTC2704 has individual offset adjust pins for each of the four DACs. VOSA, VOSB, VOSC and VOSD are referred to their corresponding signal grounds, AGNDA, AGNDB, AGNDC and AGNDD. For noise immunity and ease of adjustment, the control voltage is attenuated to the DAC output:

V_{OS} = –0.01 • V(VOSx) [0V to 5V, ±2.5V spans]

V_{OS} = –0.02 • V(VOSx) [0V to 10V, ±5V, –2.5V to 7.5V spans]

V_{OS} = –0.04 • V(VOSx) [±10V span]

The nominal input range of these pins is ±5V; other reference voltages of up to ±15V may be used if needed.

The VOSx pins have an input impedance of 1MΩ. To preserve the settling performance of the LTC2704, these pins

OPERATION

should be driven with a Thevenin-equivalent impedance of 10kΩ or less. If not used, they should be shorted to their respective signal grounds, AGNDx.

POWER-ON RESET AND CLEAR

When power is first applied to the LTC2704, all DACs power-up in 5V unipolar mode (S3 S2 S1 S0 = 0000). All internal DAC registers are reset to 0 and the DAC outputs are zero volts.

When the $\overline{CLR}$ pin is taken low, a system clear results. The command and address shift registers, and the code and configuration B2 buffers, are reset to 0; the DAC outputs are all reset to zero volts. The B1 buffers are left intact, so that any subsequent "Update B1→B2" command (including the use of $\overline{LDAC}$) restores the addressed DACs to their respective previous states.

If $\overline{CLR}$ is asserted during an operation, i.e., when $\overline{CS}$/LD is low, the operation is aborted. Integrity of the relevant input (B1) buffers is not guaranteed under these conditions, therefore the contents should be checked using readback or replaced.

The $\overline{RFLAG}$ pin is used as a flag to notify the system of a loss of data integrity. The $\overline{RFLAG}$ output is asserted low at power-up, system clear, or if the logic supply V_{DD} dips below approximately 2V; and stays asserted until any valid update command is executed.

SLEEP MODE

When a sleep command (C3 C2 C1 C0 = 1110) is issued, the addressed DAC or DACs go into power-down mode. DACs A and B share a reference inverting amplifier as do DACs C and D. If either DAC A or DAC B (similarly for DACs C and D) is powered down, its shared reference inverting amplifier remains powered on. When both DAC A and DAC B are powered down together, their shared reference inverting amplifier is also powered down (similarly for DACs C and D). To determine the sleep status of a particular DAC, a direct read span command is performed by addressing the DAC and reading its status on the readback pin SRO. The fifth LSB is the sleep status bit (see Figures 2a and 2b). Table 4 shows the sleep status bit's functionality.

Table 4. Readback Sleep Status Bit

SLP	STATUS
0	DAC n Awake
1	DAC n in Sleep Mode

APPLICATIONS INFORMATION

Overview

The LTC2704 is a highly integrated device, greatly simplifying design and layout as compared to a design using multiple current output DACs and separate amplifiers. A similar design using four separate current output DACs would require six precision op amps, compensation capacitors, bypass capacitors for each amplifier, several times as much PCB area and a more complicated serial interface. Still, it is important to avoid some common mistakes in order to achieve full performance. DC752A is the evaluation board for the LTC2704. It is designed to meet all data sheet specifications, and to allow the LTC2704 to be integrated into other prototype circuitry. All force/sense lines are available to allow the addition of current booster stages or other output circuits.

The DC752A design is presented as a tutorial on properly applying the LTC2704. This board shows how to properly return digital and analog ground currents, and how to compensate for small differences in ground potential between the two banks of two DACs. There are other ways to ground the LTC2704, but the one requirement is that analog and digital grounds be connected at the LTC2704 by a very low impedance path. It is NOT advisable to split the ground planes and connect them with a jumper or inductor. When in doubt, use a single solid ground plane rather than separate planes.

The LTC2704 does allow the ground potential of the DACs to vary by ±300mV with respect to analog ground, allowing compensation for ground return resistance.

Power Supply Grounding and Noise

LTC2704 V^+ and V^- pins are the supplies to all of the output amplifiers, ground sense amplifiers and reference inversion amplifiers. These amplifiers have good power supply rejection, but the V^+ and V^- supplies must be free from wideband noise. The best scheme is to prefilter low noise regulators such as the LT®1761 (positive) and LT1964 (negative). Refer to Linear Technology Application Note 101, Minimizing Switching Regulator Residue in Linear Regulator Outputs.

The LTC2704 V_{DD} pin is the supply for the digital logic and analog DAC switches and is very sensitive to noise. It must be treated as an analog supply. The evaluation board uses an LT1790 precision reference as the V_{DD} supply to minimize noise.

The GND pin is the return for digital currents and the AGND pin is a bias point for internal analog circuitry. Both of these pins must be tied to the same point on a quiet ground plane.

Each DAC has a separate ground sense pin that can be used to compensate for small differences in ground potential within a system. Since DACs A and B are associated with REF1 and DACs C and D are associated with REF2, the grounds must be grouped together as follows:

AGNDA, AGNDB and REFG1 tied together (“GND1” on DC752A)

AGNDC, AGNDD and REFG2 tied together (“GND2” on DC752A)

This scheme allows compensation for ground return IR drops, as long as the resistance is shared by both DACs in a group. This implies that the ground return for DACs A and B must be as close as possible, and GND1 must be connected to this point through a low current, low resistance trace. (Similar for DACs C and D.)

Figure 3 shows the top layer of the evaluation board. The GND1 trace connects REFG1, AGNDA, AGNDB and the ground pin of the LT1236 precision reference (U4.) This point is the ground reference for DACs A and B. The GND2 trace connects REFG2, AGNDC, AGNDD and the ground pin of the other LT1236 precision reference (U5). This point is the ground reference for DACs C and D.

Voltage Reference

A high quality, low noise reference such as the LT1236 or LT1027 must be used to achieve full performance. The ground terminal of this reference must be connected directly to the common ground point. If GND1 and GND2 are separate, then two references must be used.

APPLICATIONS INFORMATION

Voltage Output/Feedback and Compensation

The LTC2704 provides separate voltage output and feedback pins for each DAC. This allows compensation for resistance between the output and load, or a current boosting stage such as an LT1970 may be inserted without affecting accuracy. When OUTx is connected directly to RFBx and no additional capacitance is present, the internal frequency compensation is sufficient for stability and is optimized for fast settling time. If a low bandwidth booster stage is used, then a compensation capacitor from OUTx to C1x may be required. Similarly, extra compensation may be required to drive a heavy capacitive load.

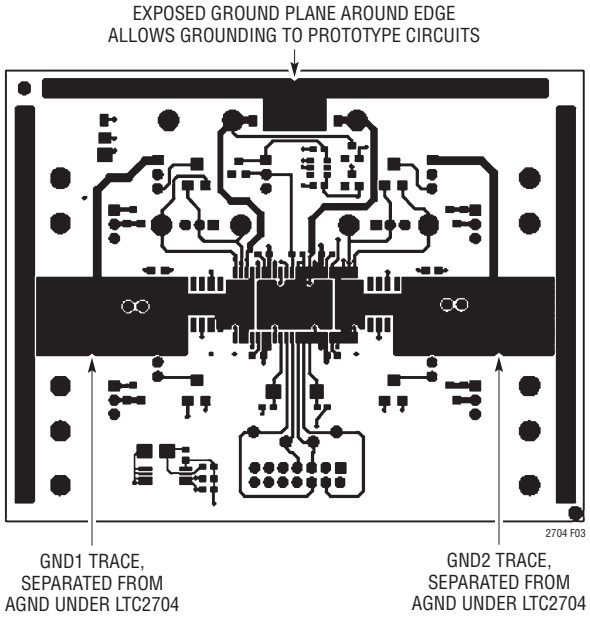


Figure 3. DC752 Top Layer

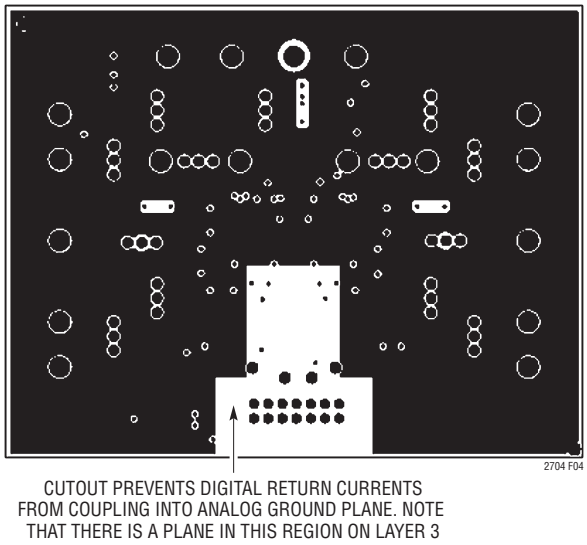


Figure 4. DC752 Analog Ground Layer. No Currents Are Returned to this Plane, so it May Be Used As a Reference Point for Precise Voltage Measurements

APPLICATIONS INFORMATION

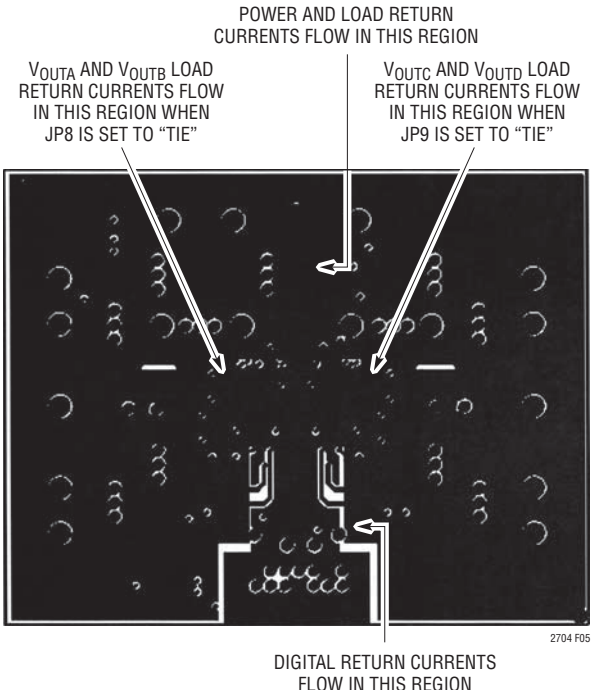


Figure 5. DC752A Load Return, Power Return and Digital Return

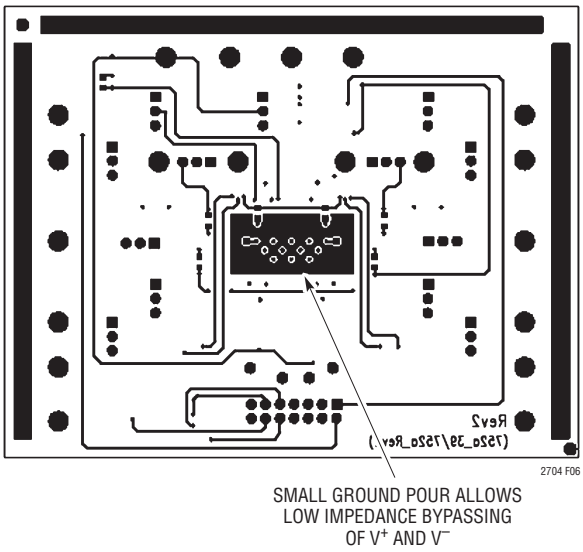
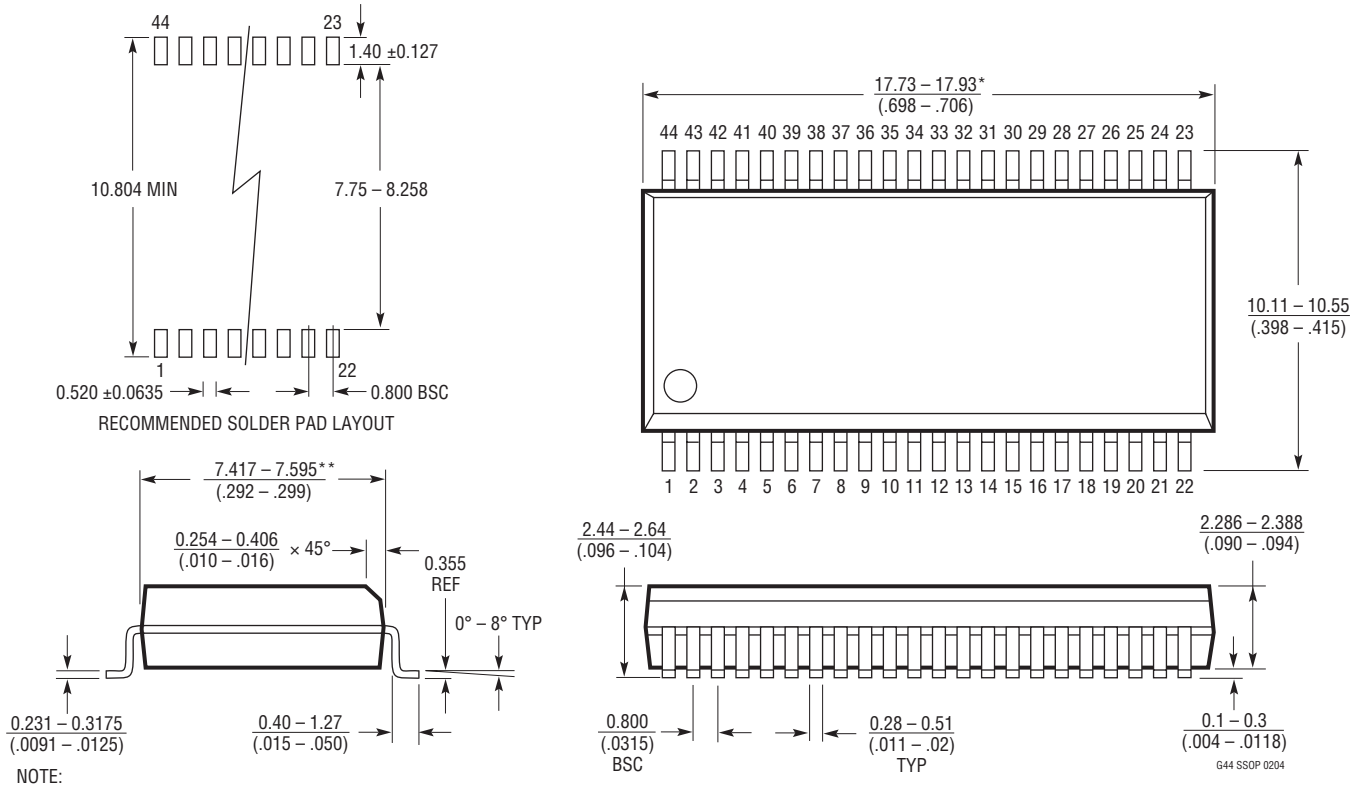


Figure 6. DC752A Routing, Bypass

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GW Package
44-Lead Plastic SSOP (Wide .300 Inch)
(Reference LTC DWG # 05-08-1642)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

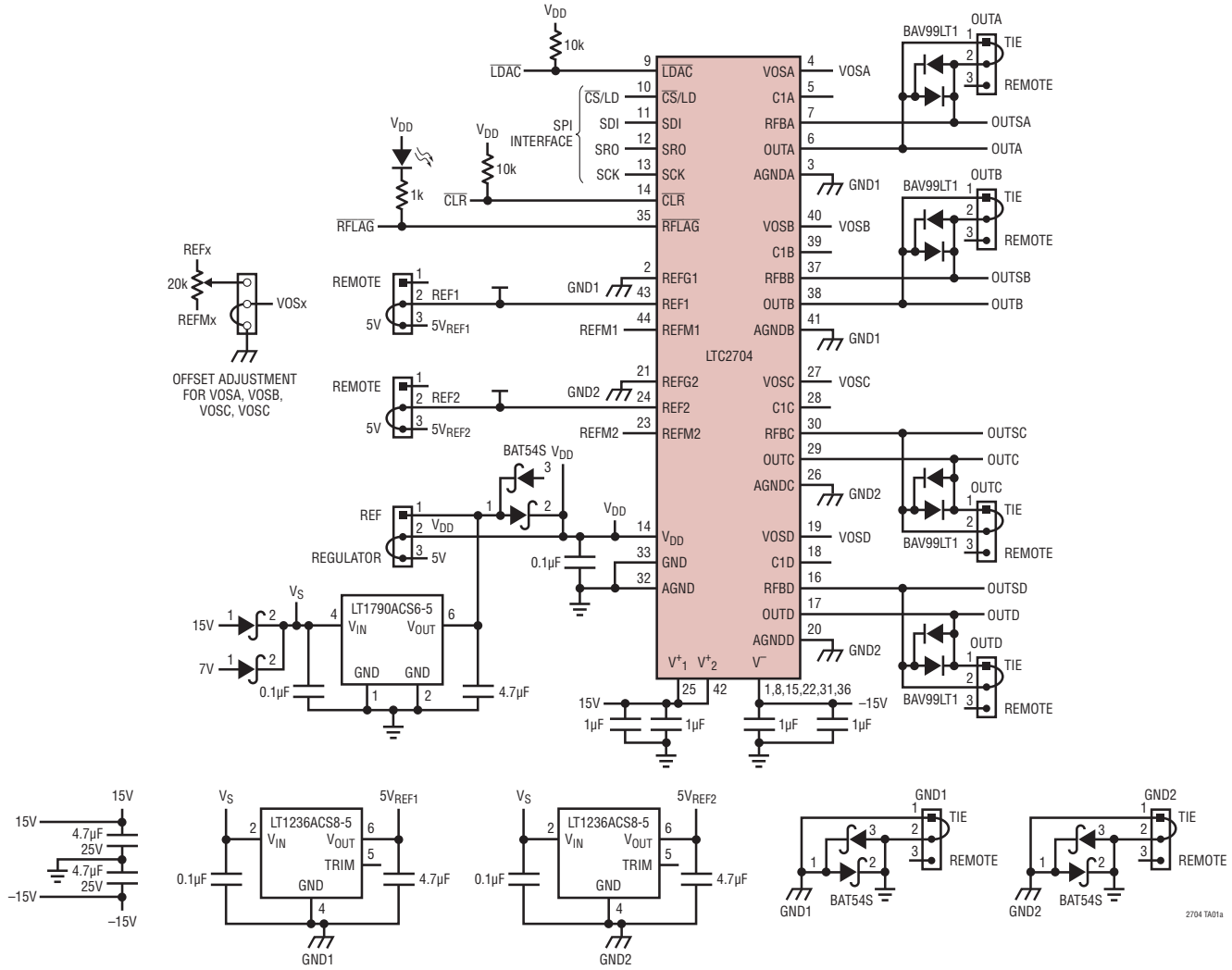
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	10/09	Title Change to Block Diagram	1
		Electrical Characteristics Text Changes to Analog Outputs Section	3
		Text and Figure Deletion in Operation Section	16
C	08/10	Revised Note 1 to remove power supply sequencing reference	5
		Changed “DAC A” to DAC n in Table 1	12
D	12/12	Corrected Output Noise Voltage Density Units From μV/$\sqrt{Hz}$ to nV/$\sqrt{Hz}$	4

TYPICAL APPLICATION

Evaluation Board Schematic. Force/Sense Lines Allow for Remote Sensing and Optimal Grounding



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1019	Precision Reference	Ultralow Drift, 3ppm/°C, 0.05% Accuracy
LT1236	Precision Reference	Ultralow Drift, 10ppm/°C, 0.05% Accuracy
LTC1588/LTC1589 LTC1592	12-/14-/16-Bit, Serial, SoftSpan I_{OUT} DACs	Software-Selectable Spans, ±1LSB INL/DNL
LTC1595	16-Bit Serial Multiplying I_{OUT} DAC in SO-8	±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade
LTC1596	16-Bit Serial Multiplying I_{OUT} DAC	±1LSB Max INL/DNL, Low Glitch, AD7543/DAC8143 16-Bit Upgrade
LTC1597	16-Bit Parallel, Multiplying DAC	±1LSB Max INL/DNL, Low Glitch, 4 Quadrant Resistors
LTC1650	16-Bit Serial V_{OUT} DAC	Low Power, Low Gritch, 4-Quadrant Multiplication
LTC1857/LTC1858 LTC1859	12-/14-/16-Bit, Serial 100ksps SoftSpan ADC	Software-Selectable Spans, 40mW, Fault Protected to ±25V
LT1970	500mA Power Op Amp	Adjustable Sink/Source Current Limits

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