



**THE DATASHEET OF
AP22953CW12-7**



SWITCH FOR VBUS LINE WITH OVERVOLTAGE, SURGE, AND ESD PROTECTION

Description

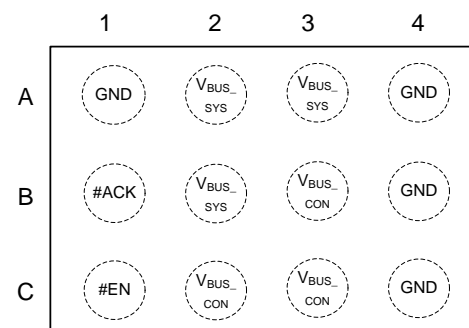
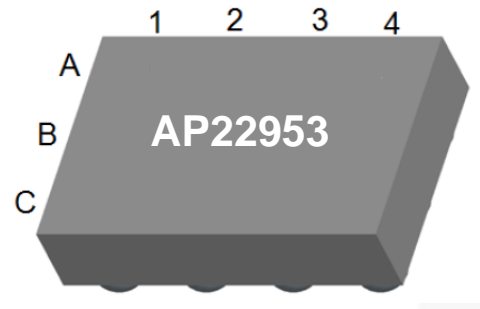
The AP22953 device is a single-chip solution for USB 2.0/3.0/Type-C connector VBUS line protection. The bidirectional MOSFET switch ensures normal current flow in both charging and host mode while protecting the internal circuits from overvoltage conditions at the V_{BUS_CON} pin. On the V_{BUS_CON} pin, the device has overvoltage protection up to 30V. After the #EN pin is pulled low, the AP22953 counts 20ms before turning on the MOSFET via soft-start delay. The #ACK pin indicates the MOSFET is fully turned ON.

The typical application interface for the AP22953 is the V_{BUS} line in USB connectors. Typical end equipment for the AP22953 include smartphones, tablet PCs, wearables, and electronic-point-of-sale (EPOS) systems. The AP22953 can also be used with other devices that use a 5V power rail interface.

Overtemperature protection turns off the switch at 145°C (typical).

The AP22953 is available in the wafer level chip scale W-WLB2013-12 1.988mm x 1.288mm x 0.64mm package with backside laminate.

Pin Assignments



WL-CSP (Top View)

Features

- Surge protection
 - IEC61000-4-5 >100V
- Integrated 39mΩ (typ) N-Channel MOSFET Switch
- Overvoltage Protection (OVP) at V_{BUS_CON} Up to 30VDC
- Integrated Input Enable and Status Output Signal
- Overtemperature Protection (OTP)
- ESD Protection
 - Human Body Model >4kV
 - Charged Device Model >1kV
 - IEC61000-4-2 Air Discharge >15kV
 - IEC61000-4-2 Contact Discharge >15kV
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.**

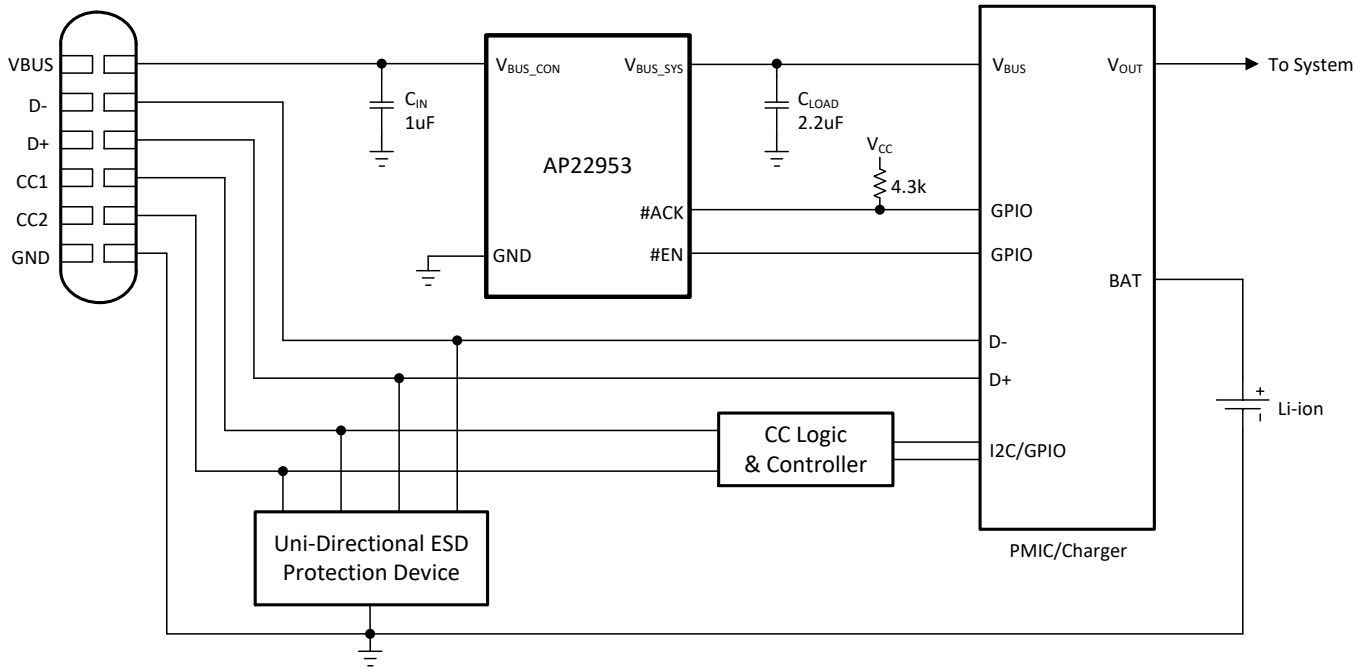
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Applications

- Smartphones
- Tablet PCs
- Wearables
- Electronic-Point-of-Sale (EPOS) Systems

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

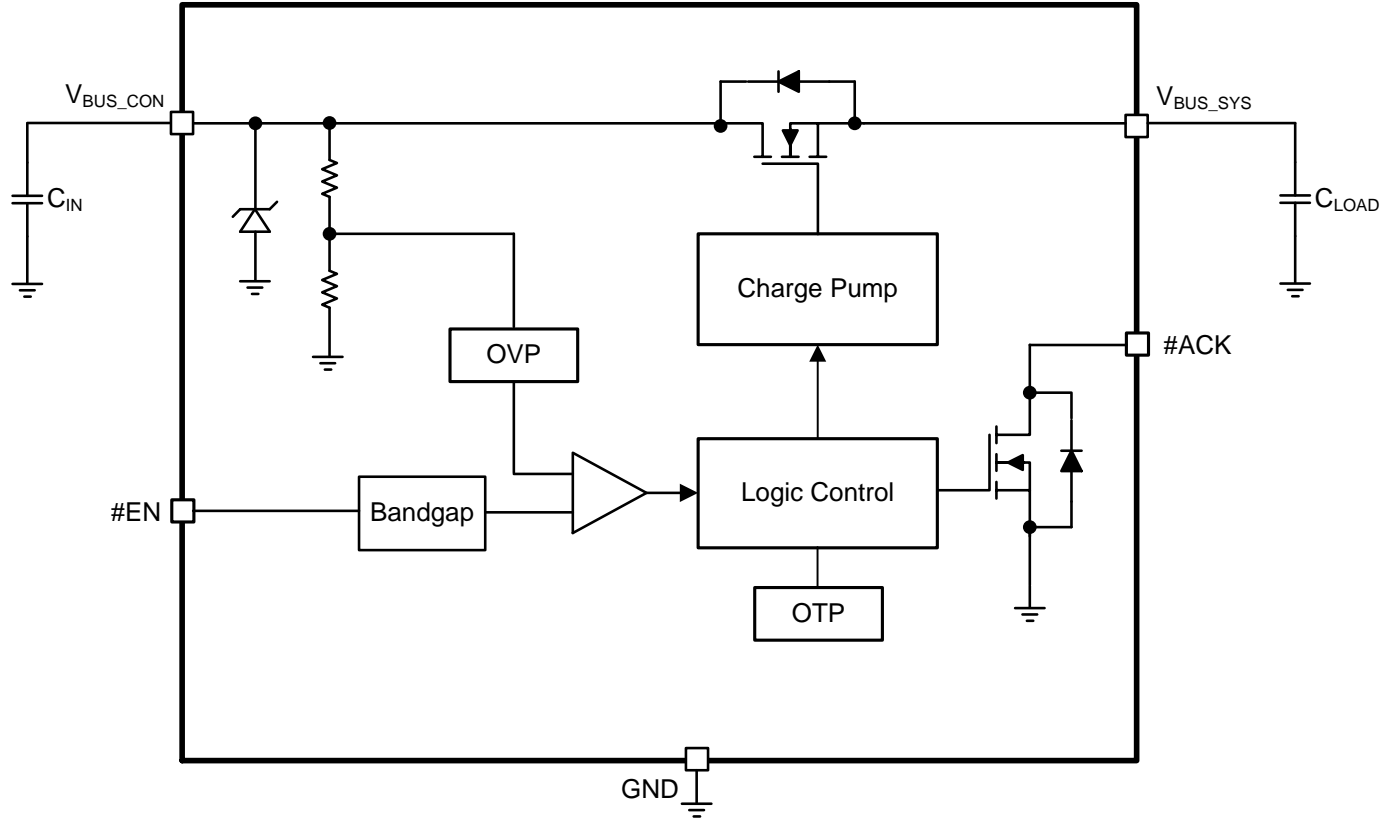
Typical Applications Circuit



Pin Descriptions

Pin Name	Pin Number	I/O	Function
V _{BUS_CON}	B3, C2, C3	I/O	Supply voltage from USB connector V _{BUS} pin. Bypass V _{BUS_CON} with a 1μF ceramic capacitor as close as possible to the device.
V _{BUS_SYS}	A2, A3, B2	I/O	Internal supply voltage rail to PMIC V _{BUS} plane. Bypass V _{BUS_SYS} with a 2.2μF ceramic capacitor as close as possible to the device.
#ACK	B1	O	Open-Drain Acknowledge pin.
#EN	C1	I	Enable Active-Low Input. Drive #EN low to enable the switch. Drive #EN high to disable the switch.
GND	A1, A4, B4, C4	Ground	Device ground. Connect to PCB ground plane

Functional Block Diagram



Absolute Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Symbol		Parameter	Ratings	Unit
ESD	HBM	Human Body Model ESD Protection	4	kV
	CDM	Charged Device Model ESD Protection	1	kV
	IEC system level	IEC 61000-4-2. Contact Discharge, V_{BUS_CON} (Note 4)	15	kV
	IEC system level	IEC 61000-4-2. Air Gap Discharge, V_{BUS_CON} (Note 4)	15	kV
Surge		IEC 61000-4-5 Surge Protection, V_{BUS_CON} (Note 4)	100	V
V_{BUS_CON}		Supply voltage from USB connector	-0.3 to +30	V
V_{BUS_SYS}		Internal supply DC voltage rail on the PCB	-0.3 to +7	V
#ACK, #EN		$V_{\#ACK}$, $V_{\#EN}$ Voltages	-0.3 to +7	V
I_{CON} , I_{SYS}		Switch I/O Current (Continuous)	3.5	A
T_A		Operating Ambient Temperature	-40 to +85	$^\circ\text{C}$
T_{ST}		Storage Temperature Range	-40 to +150	$^\circ\text{C}$
P_D		Power Dissipation	670	mW
$R_{\theta JA}$		Thermal Resistance, Junction to Ambient	89	$^\circ\text{C/W}$
$R_{\theta JC}$		Thermal Resistance, Junction to Case	0.6	$^\circ\text{C/W}$

- Notes:
- The JEDEC high-K (2s2p) board used to derive this data was a 3in x 3in, multilayer board with 1oz internal power and ground planes with 2oz copper traces on top and bottom of the board.
 - EVM has been tested per typical circuit with capacitors connected to the V_{BUS_CON} and V_{BUS_SYS} .

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Recommended Operating Conditions (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Min	Nom	Max	Unit
V_{BUS_CON}	Supply voltage from USB connector	—	—	5.9	V
V_{BUS_SYS}	Internal supply DC voltage rail on the PCB	—	—	5.9	V
C_{LOAD}	Output load capacitance, V_{BUS_SYS} pin	—	2.2	—	μF
C_{IN}	Input capacitance, V_{BUS_CON} pin	—	1	—	μF
$R_{PULL-UP}$	Pull-up resistor, #ACK	—	4.3	100	k Ω
I_{VBUS}	Continuous current on V_{BUS_CON} and V_{BUS_SYS} pins	—	—	3.5	A
I_{DIODE}	Continuous current through the MOSFET body diode	—	—	1	A

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified. $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 2.2\mu\text{F}$.
 Typical values are at $V_{BUS} = +5.0\text{V}$, $I_{VBUS} \leq 3.5\text{A}$) (Note 6)

Symbol	Parameter	Test Conditions (Note 7)	Min	Typ	Max	Unit
Supply						
I_{VBUS_SLEEP}	V_{BUS_CON} operating current consumption	Measured at V_{BUS_CON} pin, $V_{BUS_CON} = 5\text{V}$, #EN = 5V	—	30	70	μA
I_{VBUS}		Measured at V_{BUS_CON} pin, $V_{BUS_CON} = 5\text{V}$, #EN = 0V and no load	—	175	373	μA
I_{VBUS_SYS}	V_{BUS_CON} operating current consumption	Measured at V_{BUS_SYS} pin, $V_{BUS_SYS} = 5\text{V}$, #EN = 0V and $V_{BUS_CON} = \text{Hi-Z}$	—	175	373	μA
I_{HOST_LEAK}	Host mode leakage current	Measured at V_{BUS_SYS} pin, $V_{BUS_SYS} = 5\text{V}$, #EN = 5V and $V_{BUS_CON} = \text{Hi-Z}$	—	110	—	μA
I/O Voltage Protection						
V_{OVP_RISING}	Input overvoltage protection threshold, V_{BUS_CON}	V_{BUS_CON} increasing from 5V	6	6.2	6.4	V
V_{HYS_OVP}	Hysteresis on OVP, V_{BUS_CON}	V_{BUS_CON} decreasing from 7V to 5V	—	50	—	mV
$V_{OVP_FALLING}$	Input overvoltage protection threshold, V_{BUS_CON}	V_{BUS_CON} decreasing from 7V to 5V	5.93	—	6.37	V
V_{UVLO}	Input undervoltage lockout, V_{BUS_CON}	V_{BUS_CON} voltage rising from 0V to 5V	2.3	2.75	3.2	V
V_{HYS_UVLO}	Hysteresis on UVLO, V_{BUS_CON}	Difference between rising and falling UVLO thresholds	—	100	—	mV
$V_{UVLO_FALLING}$	Input undervoltage lockout, V_{BUS_CON}	V_{BUS_CON} voltage rising from 5V to 0V	—	2.65	—	V
V_{UVLO_SYS}	V_{BUS_SYS} undervoltage lockout, V_{BUS_SYS}	V_{BUS_SYS} voltage rising from 0V to 5V	2.9	3.35	3.8	V
$V_{HYS_UVLO_SYS}$	V_{BUS_SYS} UVLO Hysteresis, V_{BUS_SYS}	Difference between rising and falling UVLO thresholds on V_{BUS_SYS}	—	700	—	mV
$V_{UVLO_SYS_FALL}$	V_{BUS_SYS} undervoltage lockout, V_{BUS_SYS}	V_{BUS_SYS} voltage falling from 7V to 5V	—	2.65	—	V
t_{OVP_RES}	OVP response time	Measured from OVP condition to MOSFET Turn Off. V_{BUS_CON} rises at 1V/100 ns (Notes 8)	—	—	100	ns
t_{OVP_RECOV}	Recovery time	Measured from OVP Clear to MOSFET Turn ON (Notes 9)	—	15	—	ms
Switching Characteristics						
$R_{DS(on)}$	Switch ON-resistance	$V_{BUS_CON} = 5\text{V}$, $I_{OUT} = 1\text{A}$, $T_A = 25^\circ\text{C}$	—	39	50	m Ω
Digital Signals						
V_{IH}	High-level input voltage, #EN	—	1.2	—	—	V
V_{IL}	Low-level input voltage, #EN	—	—	—	0.7	V
I_{IL}	Input leakage current, #EN	$V_I = 3.3\text{V}$	—	—	1	μA
V_{OL}	Low-level output voltage, #ACK	$I_{OL} = 1\text{mA}$	—	—	0.4	V
Timing Characteristics						
t_{DELAY}	USB charging turn-on delay	Measured from #EN asserted Low to MOSFET Turn On, excluding soft-start time	—	15	—	ms
t_{SS}	USB charging rise time (soft-start delay)	Measure from V_{BUS_SYS} rises above 25% until #ACK goes Low 10%, $R_{LOAD} = 1\text{M}\Omega$ and $C_{LOAD} = \text{NC}$	—	18	—	ms
t_{OFF_DELAY}	USB charging turn-off time	Measured from #EN asserted High to V_{BUS_SYS} falling to 10%, $R_{LOAD} = 10\Omega$ and $C_{LOAD} = \text{NC}$	—	4	—	ns
Thermal Protection						
T_{SHDN}	Thermal Shutdown	Junction temperature	—	145	—	$^\circ\text{C}$
T_{HYS}	Thermal Shutdown Hysteresis	Junction temperature	—	35	—	$^\circ\text{C}$

- Notes:
- Specifications are over -40°C to $+85^\circ\text{C}$ and are guaranteed by characterization and design.
 - Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
 - Parameters provided for reference only, and do not constitute part of DIODES's published device specifications.
 - Excludes soft-start time.

Timing Diagrams ($V_{BUS_CON} = 5V$, $C_{IN} = 1\mu F$, $C_{LOAD} = 2.2\mu F$, $\#EN = \text{Enable}$, $T_A = 25^\circ C$.)

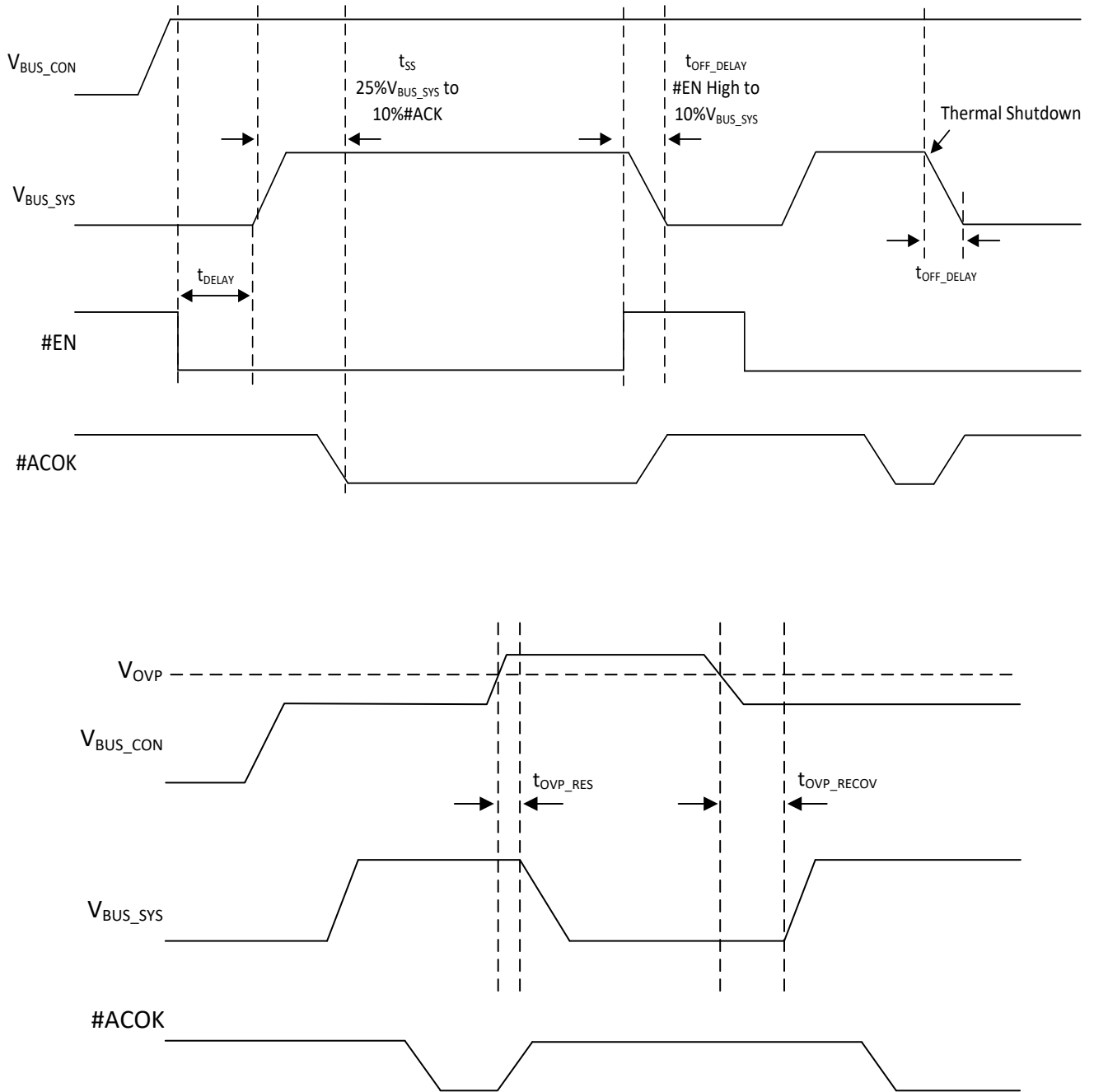
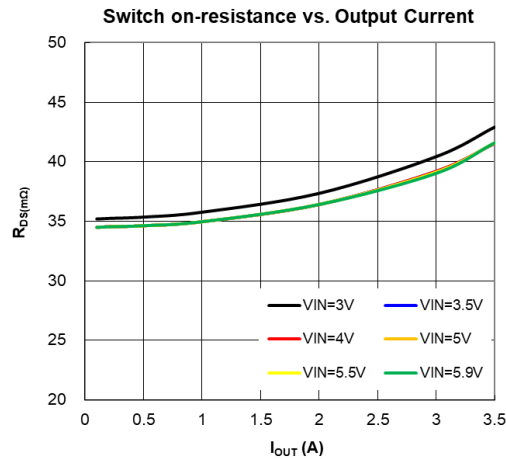
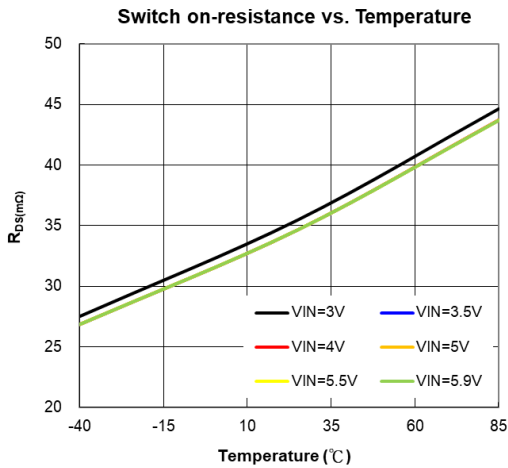
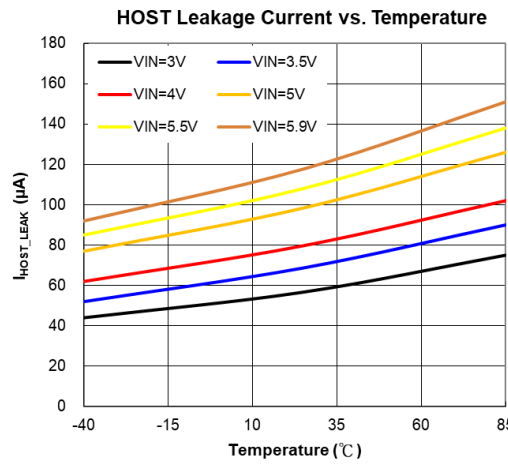
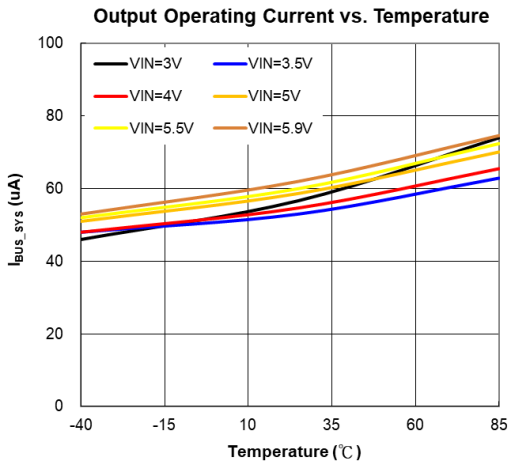
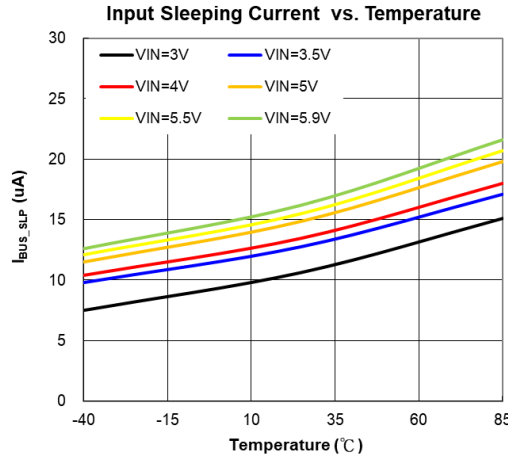
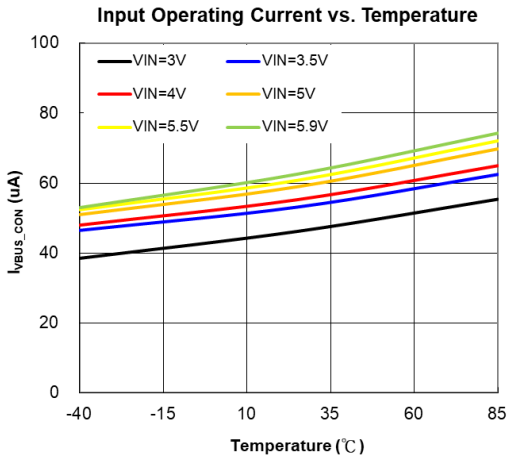
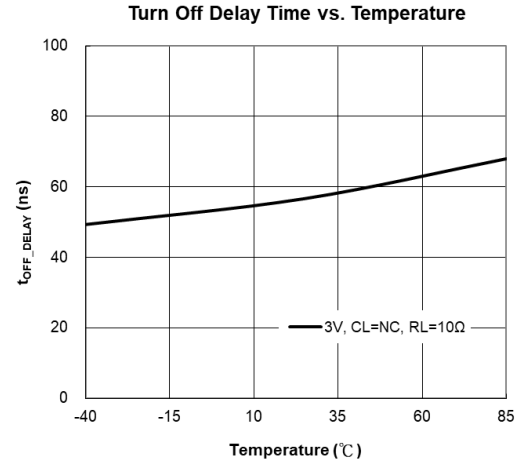
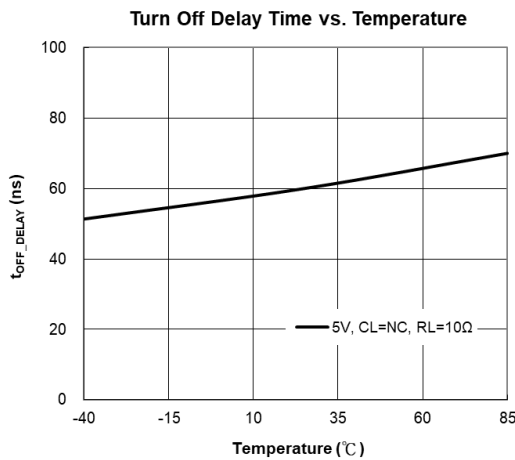
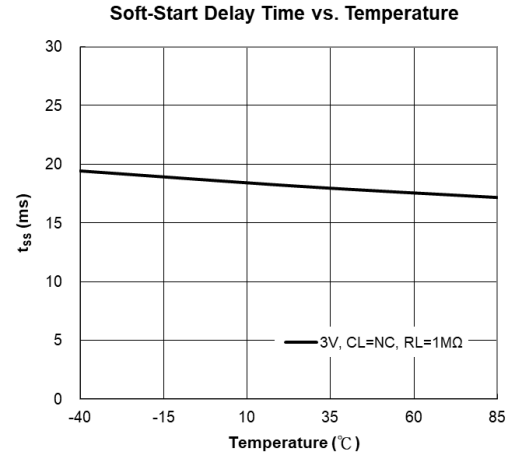
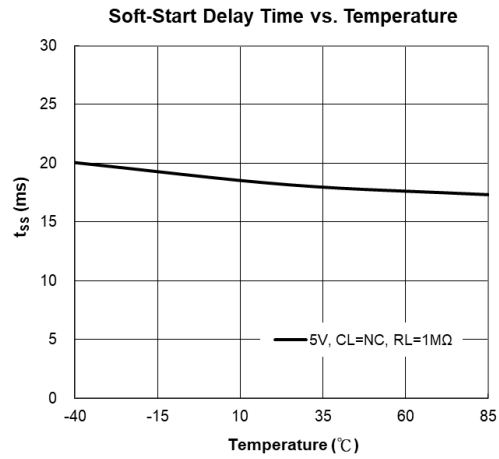
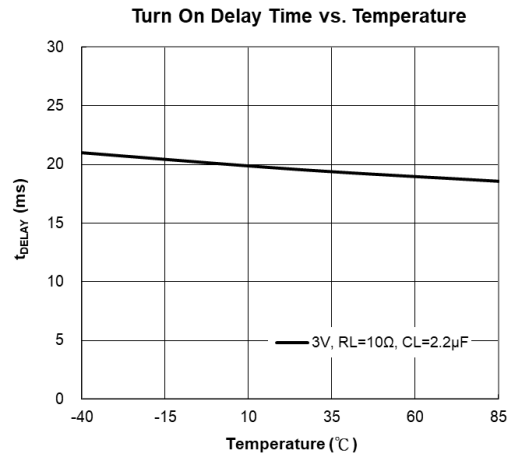
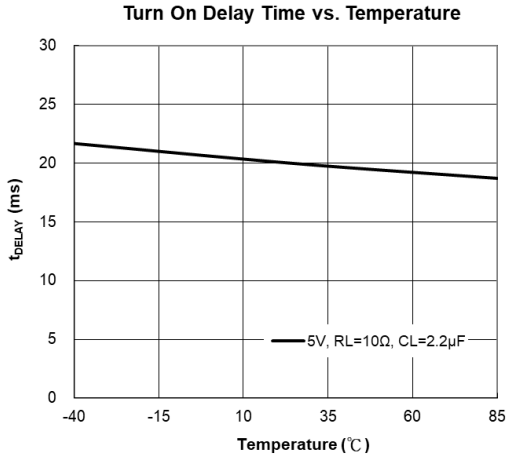


Figure 1. Timing for Power up, Normal operation, OTP and OVP protection

Typical Performance Characteristics ($C_{IN} = 1\mu F$, $C_{LOAD} = 2.2\mu F$, unless otherwise specified.)



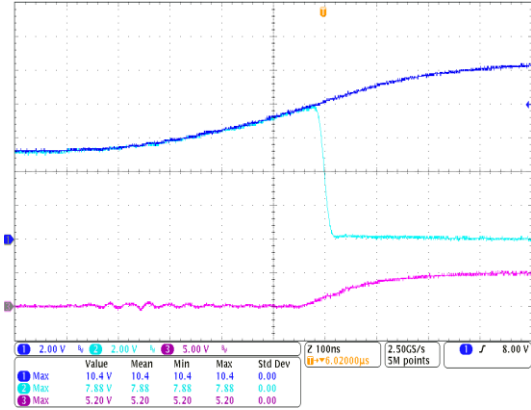
Typical Performance Characteristics ($C_{IN} = 1\mu F$, $C_{LOAD} = 2.2\mu F$, unless otherwise specified.)



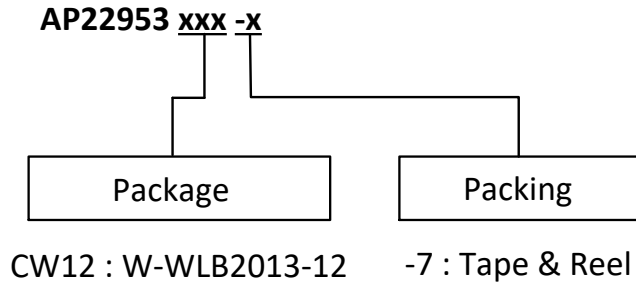
Typical Performance Characteristics ($C_{IN} = 1\mu F$, $C_{LOAD} = 2.2\mu F$, unless otherwise specified.)

OVP Response Time

CH1 = V_{BUS_CON} , CH2 = V_{BUS_SYS} , CH3 = #ACK
 V_{BUS_CON} ramp from 5V to 10V



Ordering Information

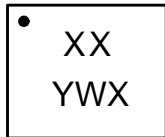


Part Number	Package Code	Packaging	7" Tape and Reel	
			Quantity	Part Number Suffix
AP22953CW12-7	CW12	W-WLB2013-12	3,000/Tape & Reel	-7

Marking Information

W-WLB1318-12

(Top View)



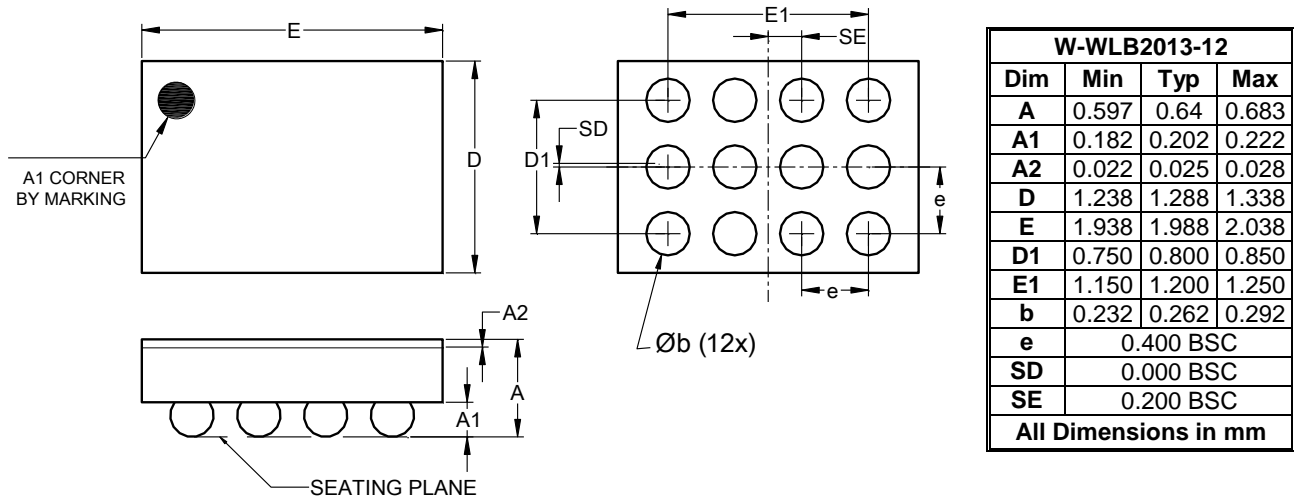
- XX : Identification Code
- Y : Year : 0~9
- W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
- X : Internal Code

Part Number	Package	Identification Code
AP22953CW12-7	W-WLB2013-12	HW

Package Outline Dimensions

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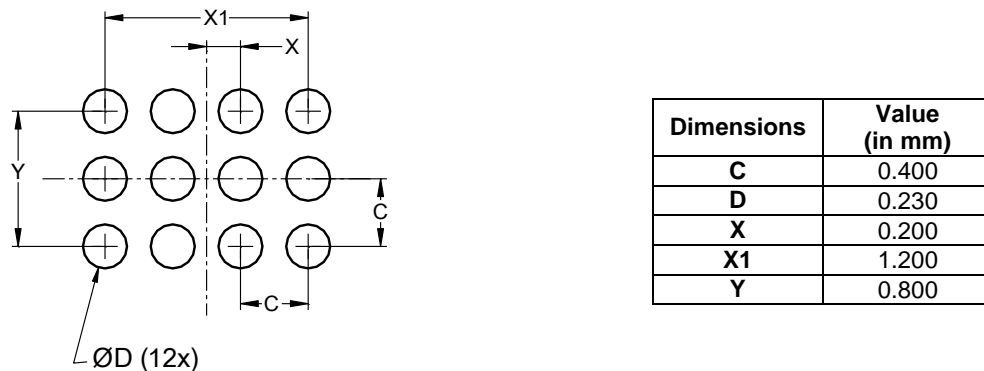
(1) Package Type: W-WLB2013-12



Suggested Pad Layout

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