THE DATASHEET OF

AD5335BRU

www.win-source.net 0086-755-83957316

2.5 V to 5.5 V, 500 μA, Parallel Interface Quad Voltage-Output 8-/10-/12-Bit DACs

AD5334/AD5335/AD5336/AD5344*

FEATURES

AD5334: Quad 8-Bit DAC in 24-Lead TSSOP
AD5335: Quad 10-Bit DAC in 24-Lead TSSOP
AD5336: Quad 10-Bit DAC in 28-Lead TSSOP
AD5344: Quad 12-Bit DAC in 28-Lead TSSOP
Low Power Operation: 500 μA @ 3 V, 600 μA @ 5 V
Power-Down to 80 nA @ 3 V, 200 nA @ 5 V via $\overline{PD}$ Pin
2.5 V to 5.5 V Power Supply
Double-Buffered Input Logic
Guaranteed Monotonic by Design Over All Codes
Output Range: 0–V_{REF} or 0–2 V_{REF}
Power-On Reset to Zero Volts
Simultaneous Update of DAC Outputs via $\overline{LDAC}$ Pin
Asynchronous $\overline{CLR}$ Facility
Low Power Parallel Data Interface
On-Chip Rail-to-Rail Output Buffer Amplifiers
Temperature Range: –40°C to +105°C

APPLICATIONS

Portable Battery-Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators
Industrial Process Control

GENERAL DESCRIPTION

The AD5334/AD5335/AD5336/AD5344 are quad 8-, 10-, and 12-bit DACs. They operate from a 2.5 V to 5.5 V supply consuming just 500 μA at 3 V, and feature a power-down mode that further reduces the current to 80 nA. These devices incorporate an on-chip output buffer that can drive the output to both supply rails.

The AD5334/AD5335/AD5336/AD5344 have a parallel interface. $\overline{CS}$ selects the device and data is loaded into the input registers on the rising edge of $\overline{WR}$.

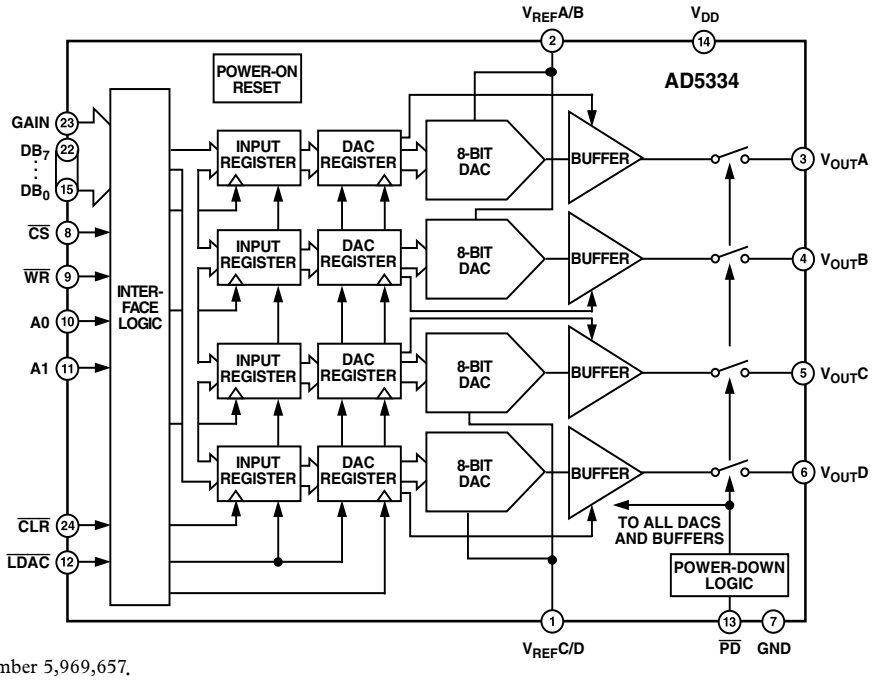
The GAIN pin on the AD5334 and AD5336 allows the output range to be set at 0 V to V_{REF} or 0 V to 2 × V_{REF}.

Input data to the DACs is double-buffered, allowing simultaneous update of multiple DACs in a system using the $\overline{LDAC}$ pin.

On the AD5334, AD5335 and AD5336 an asynchronous $\overline{CLR}$ input is also provided. This resets the contents of the Input Register and the DAC Register to all zeros. These devices also incorporate a power-on-reset circuit that ensures that the DAC output powers on to 0 V and remains there until valid data is written to the device.

The AD5334/AD5335/AD5336/AD5344 are available in Thin Shrink Small Outline Packages (TSSOP).

AD5334 FUNCTIONAL BLOCK DIAGRAM
(Other Diagrams Inside)



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
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AD5334/AD5335/AD5336/AD5344–SPECIFICATIONS

(V_{DD} = 2.5 V to 5.5 V, V_{REF} = 2 V. R_L = 2 kΩ to GND; C_L =200 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	B Version[2] Min	Typ	Max	Unit	Conditions/Comments
DC PERFORMANCE[3, 4]					
AD5334					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed Monotonic By Design Over All Codes
AD5335/AD5336					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed Monotonic By Design Over All Codes
AD5344					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Differential Nonlinearity		±0.2	±1	LSB	Guaranteed Monotonic By Design Over All Codes
Offset Error		±0.4	±3	% of FSR	
Gain Error		±0.1	±1	% of FSR	
Lower Deadband[5]		10	60	mV	Lower Deadband Exists Only if Offset Error Is Negative
Upper Deadband		10	60	mV	V_{DD} = 5 V. Upper Deadband Exists Only if V_{REF} = V_{DD}
Offset Error Drift[6]		–12		ppm of FSR/°C	
Gain Error Drift[6]		–5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[6]		–60		dB	ΔV_{DD} = ±10%
DC Crosstalk[6]		200		µV	R_L = 2 kΩ to GND, 2 kΩ to V_{DD}; C_L = 200 pF to GND; Gain = 0
DAC REFERENCE INPUT[6]					
V_{REF} Input Range	0.25		V_{DD}	V	
V_{REF} Input Impedance		180		kΩ	Gain = 1. Input Impedance = R_{DAC} (AD5336/AD5344)
		90		kΩ	Gain = 2. Input Impedance = R_{DAC} (AD5336)
		90		kΩ	Gain = 1. Input Impedance = R_{DAC} (AD5334/AD5335)
		45		kΩ	Gain = 2. Input Impedance = R_{DAC} (AD5334)
Reference Feedthrough		–90		dB	Frequency = 10 kHz
Channel-to-Channel Isolation		–90		dB	Frequency = 10 kHz
OUTPUT CHARACTERISTICS[6]					
Minimum Output Voltage[4, 7]		0.001		V min	Rail-to-Rail Operation
Maximum Output Voltage[4, 7]		V_{DD} – 0.001		V max	
DC Output Impedance		0.5		Ω	
Short Circuit Current		50		mA	V_{DD} = 5 V
		20		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming Out of Power-Down Mode. V_{DD} = 5 V
		5		µs	Coming Out of Power-Down Mode. V_{DD} = 3 V
LOGIC INPUTS[6]					
Input Current		±1		µA	
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = 5 V ± 10%
			0.6	V	V_{DD} = 3 V ± 10%
			0.5	V	V_{DD} = 2.5 V
V_{IH}, Input High Voltage	2.4			V	V_{DD} = 5 V ± 10%
	2.1			V	V_{DD} = 3 V ± 10%
	2.0			V	V_{DD} = 2.5 V
Pin Capacitance		3.5		pF	
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	
I_{DD} (Normal Mode)					All DACs active and excluding load currents.
V_{DD} = 4.5 V to 5.5 V		600	900	µA	V_{IH} = V_{DD}, V_{IL} = GND.
V_{DD} = 2.5 V to 3.6 V		500	700	µA	I_{DD} increases by 50 µA at V_{REF} > V_{DD} – 100 mV.
I_{DD} (Power-Down Mode)					
V_{DD} = 4.5 V to 5.5 V		0.2	1	µA	
V_{DD} = 2.5 V to 3.6 V		0.08	1	µA	

NOTES

[1]See Terminology section.

[2]Temperature range: B Version: –40°C to +105°C; typical specifications are at 25°C.

[3]Linearity is tested using a reduced code range: AD5334 (Code 8 to 255); AD5335/AD5336 (Code 28 to 1023); AD5344 (Code 115 to 4095).

[4]DC specifications tested with outputs unloaded.

[5]This corresponds to x codes. x = Deadband voltage/LSB size.

[6]Guaranteed by design and characterization, not production tested.

[7]In order for the amplifier output to reach its minimum voltage, Offset Error must be negative. In order for the amplifier output to reach its maximum voltage, V_{REF} = V_{DD} and "Offset plus Gain" Error must be positive.

Specifications subject to change without notice.

AC CHARACTERISTICS[1] (V_{DD} = 2.5 V to 5.5 V. R_L = 2 kΩ to GND; C_L = 200 pF to GND. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Version[3] Min	Typ	Max	Unit	Conditions/Comments
Output Voltage Settling Time					V_{REF} = 2 V. See Figure 20
AD5334		6	8	µs	1/4 Scale to 3/4 Scale Change (40 H to C0 H)
AD5335		7	9	µs	1/4 Scale to 3/4 Scale Change (100 H to 300 H)
AD5336		7	9	µs	1/4 Scale to 3/4 Scale Change (100 H to 300 H)
AD5344		8	10	µs	1/4 Scale to 3/4 Scale Change (400 H to C00 H)
Slew Rate		0.7		V/µs	
Major Code Transition Glitch Energy		8		nV-s	1 LSB Change Around Major Carry
Digital Feedthrough		0.5		nV-s	
Digital Crosstalk		3		nV-s	
Analog Crosstalk		0.5		nV-s	
DAC-to-DAC Crosstalk		3.5		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p. Unbuffered Mode
Total Harmonic Distortion		–70		dB	V_{REF} = 2.5 V ± 0.1 V p-p. Frequency = 10 kHz

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]See Terminology section.
[3]Temperature range: B Version: –40°C to +105°C; typical specifications are at 25°C.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2, 3] (V_{DD} = 2.5 V to 5.5 V, All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Condition/Comments
t_1	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	20	ns min	$\overline{WR}$ Pulsewidth
t_4	5	ns min	Data, GAIN, HBEN Setup Time
t_5	4.5	ns min	Data, GAIN, HBEN Hold Time
t_6	5	ns min	Synchronous Mode. $\overline{WR}$ Falling to $\overline{LDAC}$ Falling.
t_7	5	ns min	Synchronous Mode. $\overline{LDAC}$ Falling to $\overline{WR}$ Rising.
t_8	4.5	ns min	Synchronous Mode. $\overline{WR}$ Rising to $\overline{LDAC}$ Rising.
t_9	5	ns min	Asynchronous Mode. $\overline{LDAC}$ Rising to $\overline{WR}$ Rising.
t_{10}	4.5	ns min	Asynchronous Mode. $\overline{WR}$ Rising to $\overline{LDAC}$ Falling.
t_{11}	20	ns min	$\overline{LDAC}$ Pulsewidth
t_{12}	20	ns min	$\overline{CLR}$ Pulsewidth
t_{13}	50	ns min	Time Between $\overline{WR}$ Cycles
t_{14}	20	ns min	A0, A1 Setup Time
t_{15}	0	ns min	A0, A1 Hold Time

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3]See Figure 1.
Specifications subject to change without notice.

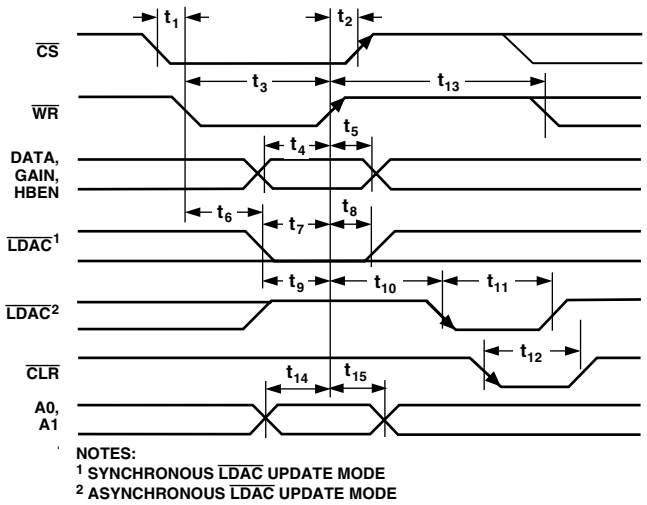


Figure 1. Parallel Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Digital Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND . . . . –0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +105°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
TSSOP Package
Power Dissipation . . . . . (T_J max – T_A)/θ_{JA} mW
θ_{JA} Thermal Impedance (24-Lead TSSOP) . . . . . 128°C/W
θ_{JA} Thermal Impedance (28-Lead TSSOP) . . . . . 97.9°C/W
θ_{JC} Thermal Impedance (24-Lead TSSOP) . . . . . 42°C/W
θ_{JC} Thermal Impedance (28-Lead TSSOP) . . . . . 14°C/W

Reflow Soldering
Peak Temperature . . . . . 220 +5/–0°C
Time at Peak Temperature . . . . . 10 sec to 40 sec

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

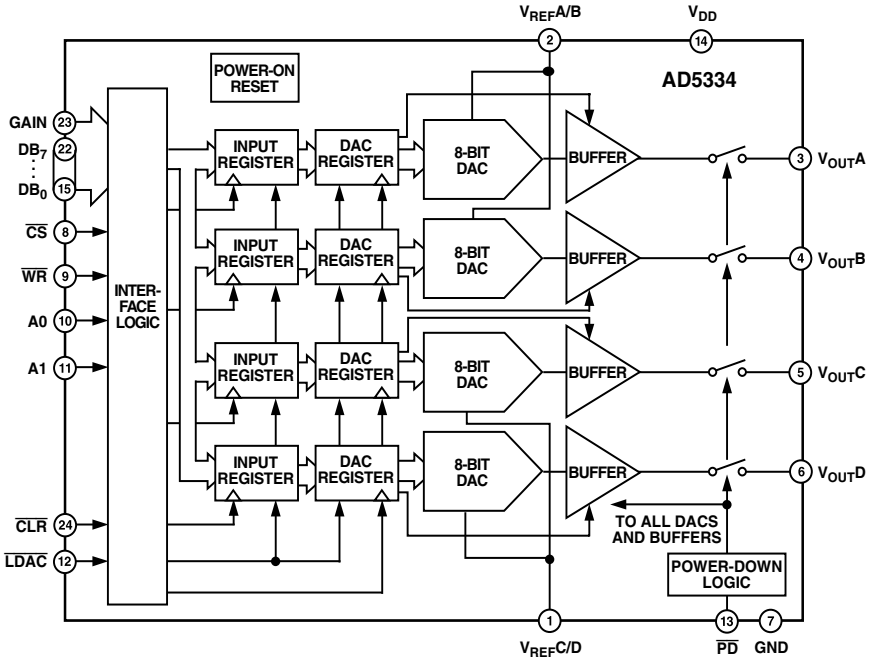
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5334BRU	–40°C to +105°C	TSSOP (Thin Shrink Small Outline Package)	RU-24
AD5335BRU	–40°C to +105°C	TSSOP (Thin Shrink Small Outline Package)	RU-24
AD5336BRU	–40°C to +105°C	TSSOP (Thin Shrink Small Outline Package)	RU-28
AD5344BRU	–40°C to +105°C	TSSOP (Thin Shrink Small Outline Package)	RU-28

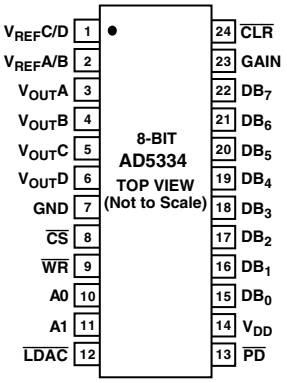
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5334/AD5335/AD5336/AD5344 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD5334 FUNCTIONAL BLOCK DIAGRAM



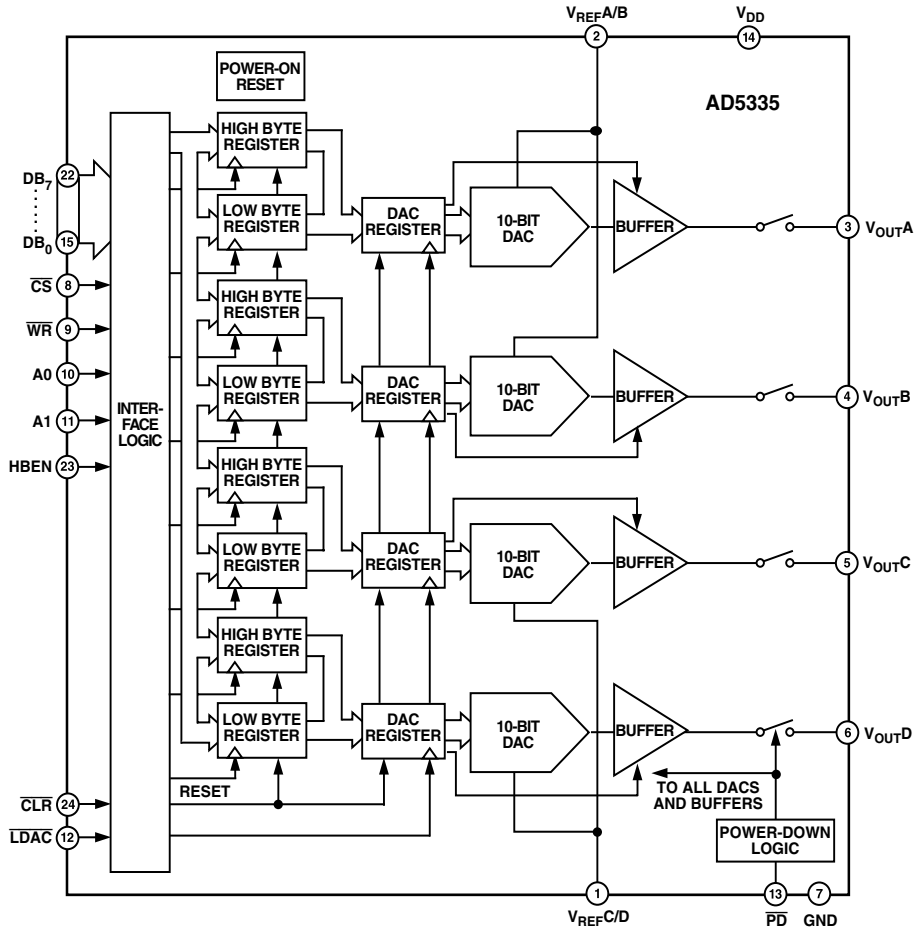
AD5334 PIN CONFIGURATION



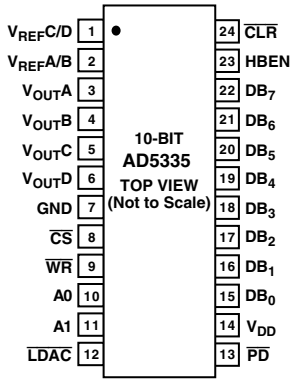
AD5334 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$V_{REF}C/D$	Unbuffered Reference Input for DACs C and D.
2	$V_{REF}A/B$	Unbuffered Reference Input for DACs A and B.
3	$V_{OUT}A$	Output of DAC A. Buffered Output with Rail-to-Rail Operation.
4	$V_{OUT}B$	Output of DAC B. Buffered Output with Rail-to-Rail Operation.
5	$V_{OUT}C$	Output of DAC C. Buffered Output with Rail-to-Rail Operation.
6	$V_{OUT}D$	Output of DAC D. Buffered Output with Rail-to-Rail Operation.
7	GND	Ground Reference Point for All Circuitry on the Part.
8	$\overline{CS}$	Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
9	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
10	A0	LSB Address Pin for Selecting which DAC Is to Be Written to.
11	A1	MSB Address Pin for Selecting which DAC Is to Be Written to.
12	$\overline{LDAC}$	Active Low Control Input that Updates the DAC Registers with the Contents of the Input Registers. This allows all DAC outputs to be simultaneously updated.
13	$\overline{PD}$	Power-Down Pin. This active low control pin puts all DACs into power-down mode.
14	V_{DD}	Power Supply Pin. This part can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
15–22	DB_0–DB_7	Eight Parallel Data Inputs. DB_7 is the MSB of these eight bits.
23	GAIN	Gain Control Pin. This controls whether the output range from the DAC is 0–V_{REF} or 0–2 V_{REF}
24	$\overline{CLR}$	Asynchronous Active Low Control Input that Clears All Input Registers and DAC Registers to Zeros.

AD5335 FUNCTIONAL BLOCK DIAGRAM



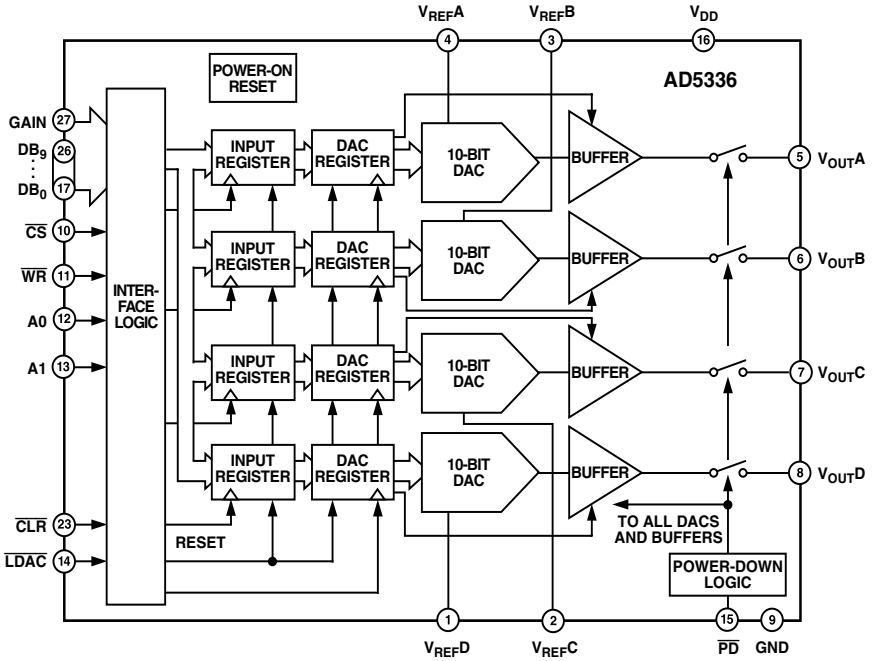
AD5335 PIN CONFIGURATION



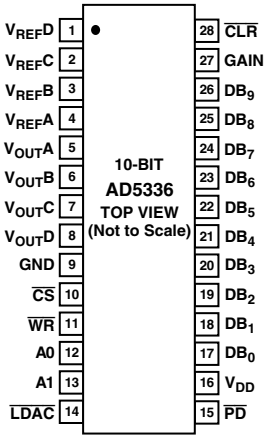
AD5335 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$V_{REF}C/D$	Unbuffered Reference Input for DACs C and D.
2	$V_{REF}A/B$	Unbuffered Reference Input for DACs A and B.
3	$V_{OUT}A$	Output of DAC A. Buffered output with rail-to-rail operation.
4	$V_{OUT}B$	Output of DAC B. Buffered output with rail-to-rail operation.
5	$V_{OUT}C$	Output of DAC C. Buffered output with rail-to-rail operation.
6	$V_{OUT}D$	Output of DAC D. Buffered output with rail-to-rail operation.
7	GND	Ground Reference Point for All Circuitry on the Part.
8	$\overline{CS}$	Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
9	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
10	A0	LSB Address Pin for Selecting which DAC Is to Be Written to.
11	A1	MSB Address Pin for Selecting which DAC Is to Be Written to.
12	$\overline{LDAC}$	Active Low Control Input that Updates the DAC Registers with the Contents of the Input Registers. This allows all DAC outputs to be simultaneously updated.
13	$\overline{PD}$	Power-Down Pin. This active low control pin puts all DACs into power-down mode.
14	V_{DD}	Power Supply Pin. This part can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
15–22	DB_0–DB_7	Eight Parallel Data Inputs. DB_7 is the MSB of these eight bits.
23	HBEN	This pin is used when writing to the device to determine if data is written to the high byte register or the low byte register.
24	$\overline{CLR}$	Asynchronous Active Low Control Input that Clears All Input Registers and DAC Registers to Zeros.

AD5336 FUNCTIONAL BLOCK DIAGRAM



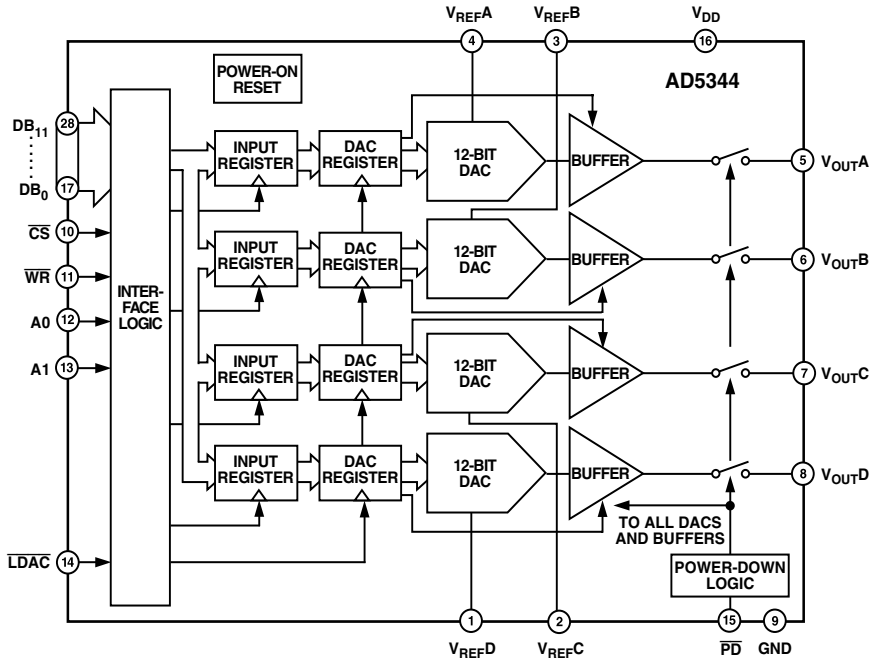
AD5336 PIN CONFIGURATION



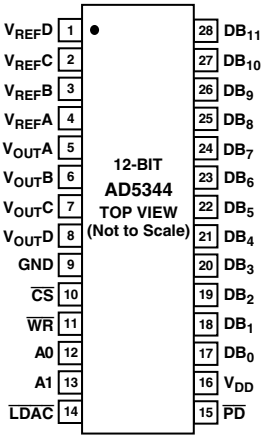
AD5336 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$V_{REF}D$	Unbuffered Reference Input for DAC D.
2	$V_{REF}C$	Unbuffered Reference Input for DAC C.
3	$V_{REF}B$	Unbuffered Reference Input for DAC B.
4	$V_{REF}A$	Unbuffered Reference Input for DAC A.
5	$V_{OUT}A$	Output of DAC A. Buffered output with rail-to-rail operation.
6	$V_{OUT}B$	Output of DAC B. Buffered output with rail-to-rail operation.
7	$V_{OUT}C$	Output of DAC C. Buffered output with rail-to-rail operation.
8	$V_{OUT}D$	Output of DAC D. Buffered output with rail-to-rail operation.
9	GND	Ground Reference Point for All Circuitry on the Part.
10	$\overline{CS}$	Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
11	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
12	A0	LSB Address Pin for Selecting which DAC Is to Be Written to.
13	A1	MSB Address Pin for Selecting which DAC is to Be Written to.
14	$\overline{LDAC}$	Active Low Control Input that Updates the DAC Registers with the Contents of the Input Registers. This allows all DAC outputs to be simultaneously updated.
15	$\overline{PD}$	Power-Down Pin. This active low control pin puts all DACs into power-down mode.
16	V_{DD}	Power Supply Pin. This part can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
17–26	DB_0–DB_9	10 Parallel Data Inputs. DB_9 is the MSB of these 10 bits.
27	GAIN	Gain Control Pin. This controls whether the output range from the DAC is 0–V_{REF} or 0–2 V_{REF}.
28	$\overline{CLR}$	Asynchronous Active Low Control Input that Clears All Input Registers and DAC Registers to Zeros.

AD5344 FUNCTIONAL BLOCK DIAGRAM



AD5344 PIN CONFIGURATION



AD5344 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$V_{REF}D$	Unbuffered Reference Input for DAC D.
2	$V_{REF}C$	Unbuffered Reference Input for DAC C.
3	$V_{REF}B$	Unbuffered Reference Input for DAC B.
4	$V_{REF}A$	Unbuffered Reference Input for DAC A.
5	$V_{OUT}A$	Output of DAC A. Buffered output with rail-to-rail operation.
6	$V_{OUT}B$	Output of DAC B. Buffered output with rail-to-rail operation.
7	$V_{OUT}C$	Output of DAC C. Buffered output with rail-to-rail operation.
8	$V_{OUT}D$	Output of DAC D. Buffered output with rail-to-rail operation.
9	GND	Ground Reference Point for All Circuitry on the Part.
10	$\overline{CS}$	Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
11	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
12	A0	LSB Address Pin for Selecting which DAC Is to Be Written to.
13	A1	MSB Address Pin for Selecting which DAC Is to Be Written to.
14	$\overline{LDAC}$	Active Low Control Input that Updates the DAC Registers with the Contents of the Input Registers. This allows all DAC outputs to be simultaneously updated.
15	$\overline{PD}$	Power-Down Pin. This active low control pin puts all DACs into power-down mode.
16	V_{DD}	Power Supply Pin. This part can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
17–28	DB_0–DB_{11}	12 Parallel Data Inputs. DB_{11} is the MSB of these 12 bits.

TERMINOLOGY

RELATIVE ACCURACY

For the DAC, Relative Accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the actual endpoints of the DAC transfer function. Typical INL versus Code plot can be seen in Figures 5, 6, and 7.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL versus Code plot can be seen in Figures 8, 9, and 10.

OFFSET ERROR

This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range.

If the offset voltage is positive, the output voltage will still be positive at zero input code. This is shown in Figure 3. Because the DACs operate from a single supply, a negative offset cannot appear at the output of the buffer amplifier. Instead, there will be a code close to zero at which the amplifier output saturates (amplifier footroom). Below this code there will be a deadband over which the output voltage will not change. This is illustrated in Figure 4.

GAIN ERROR

This is a measure of the span error of the DAC (including any error in the gain of the buffer amplifier). It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range. This is illustrated in Figure 2.

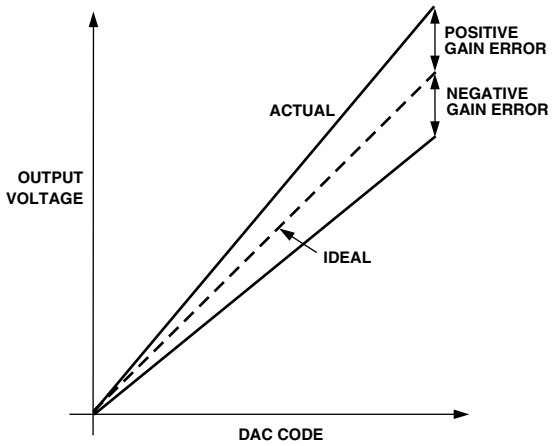


Figure 2. Gain Error

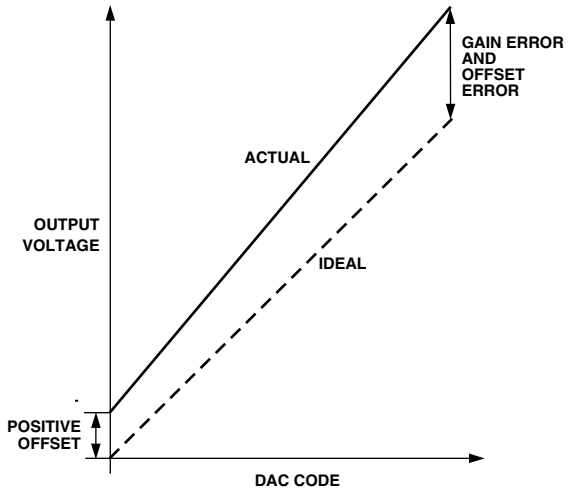


Figure 3. Positive Offset Error and Gain Error

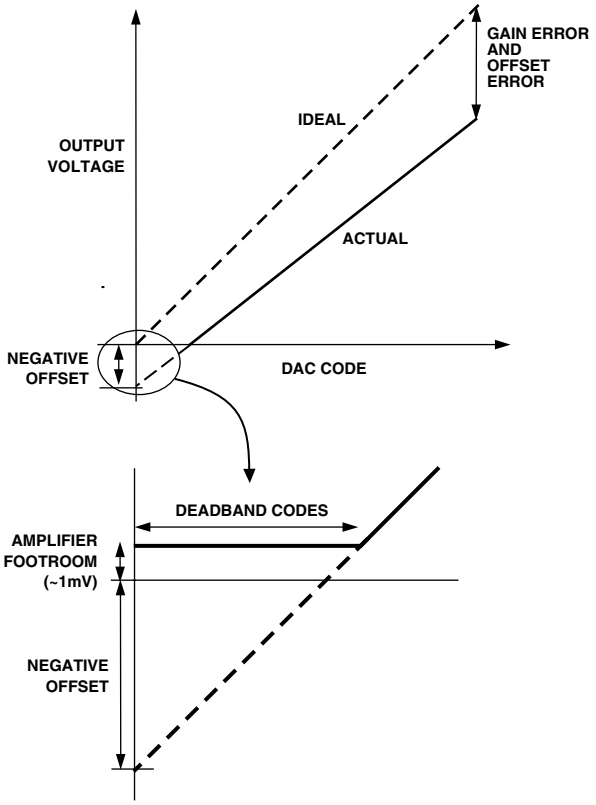


Figure 4. Negative Offset Error and Gain Error

OFFSET ERROR DRIFT
This is a measure of the change in Offset Error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

GAIN ERROR DRIFT
This is a measure of the change in Gain Error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

DC POWER-SUPPLY REJECTION RATIO (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dBs. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

DC CROSSTALK
This is the dc change in the output level of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) and output change of another DAC. It is expressed in µV.

REFERENCE FEEDTHROUGH
This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e., $\overline{LDAC}$ is high). It is expressed in dBs.

CHANNEL-TO-CHANNEL ISOLATION
This is a ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference inputs of the other DACs. It is measured by grounding one V_{REF} pin and applying a 10 kHz, 4 V peak-to-peak sine wave to the other V_{REF} pins. It is expressed in dBs.

MAJOR-CODE TRANSITION GLITCH ENERGY
Major-Code Transition Glitch Energy is the energy of the impulse injected into the analog output when the DAC changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

DIGITAL FEEDTHROUGH
Digital Feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device but is measured when the DAC is not being written to ($\overline{CS}$ held high). It is specified in nV-secs and is measured with a full-scale change on the digital input pins, i.e. from all 0s to all 1s and vice versa.

DIGITAL CROSSTALK
This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is expressed in nV secs.

ANALOG CROSSTALK
This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{LDAC}$ high. Then pulse $\overline{LDAC}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV secs.

DAC-TO-DAC CROSSTALK
This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with the $\overline{LDAC}$ pin set low and monitoring the output of another DAC. The energy of the glitch is expressed in nV secs.

MULTIPLYING BANDWIDTH
The amplifiers within the DAC have a finite bandwidth. The Multiplying Bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The Multiplying Bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

TOTAL HARMONIC DISTORTION
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and the THD is a measure of the harmonics present on the DAC output. It is measured in dBs.

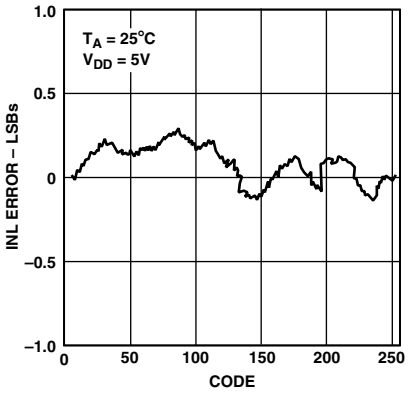


Figure 5. AD5334 Typical INL Plot

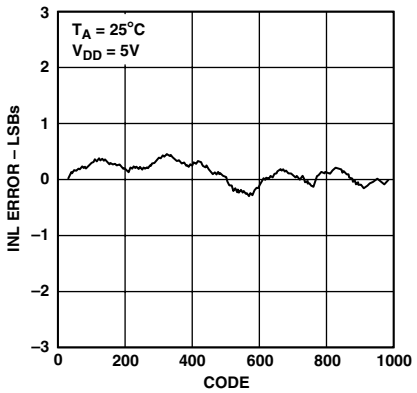


Figure 6. AD5335 Typical INL Plot

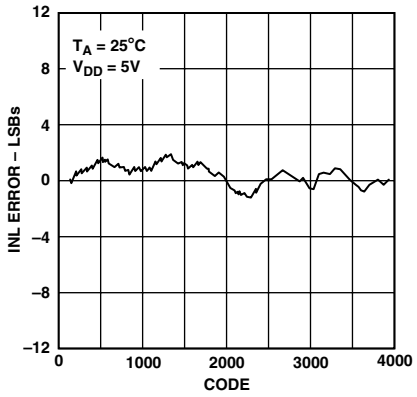


Figure 7. AD5336 Typical INL Plot

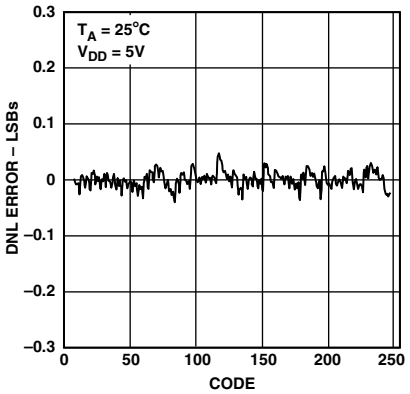


Figure 8. AD5334 Typical DNL Plot

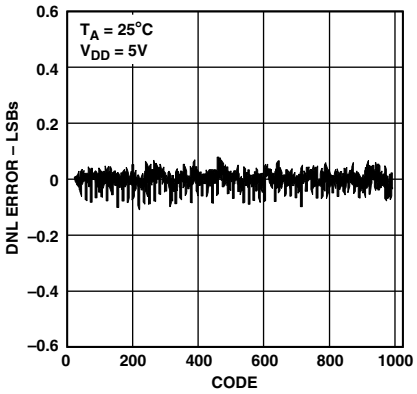


Figure 9. AD5335 Typical DNL Plot

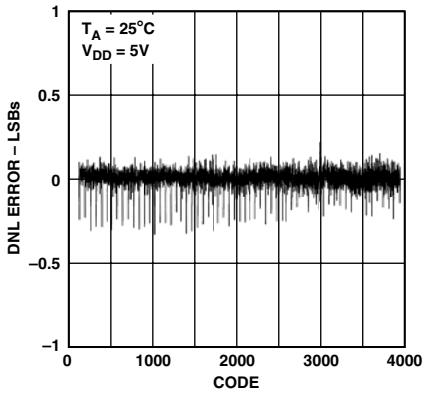


Figure 10. AD5336 Typical DNL Plot

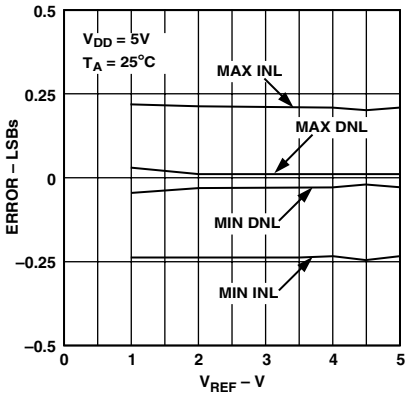


Figure 11. AD5334 INL and DNL Error vs. V_{REF}

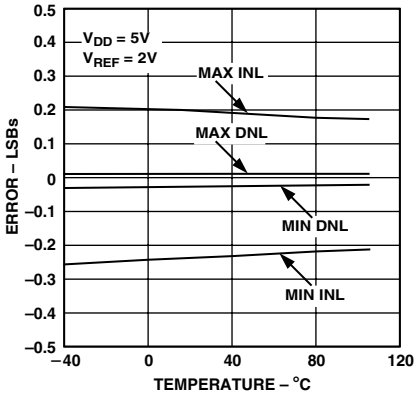


Figure 12. AD5334 INL Error and DNL Error vs. Temperature

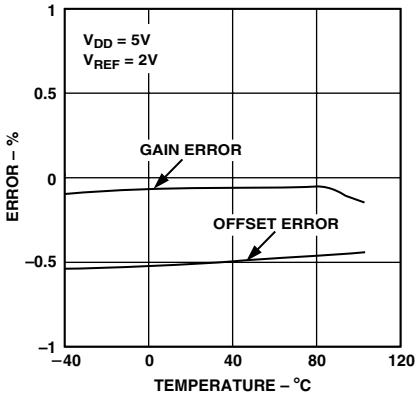


Figure 13. AD5334 Offset Error and Gain Error vs. Temperature

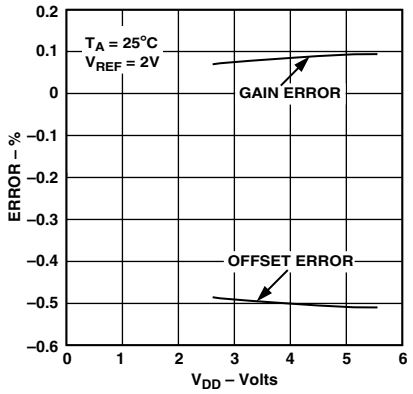


Figure 14. Offset Error and Gain Error vs. V_{DD}

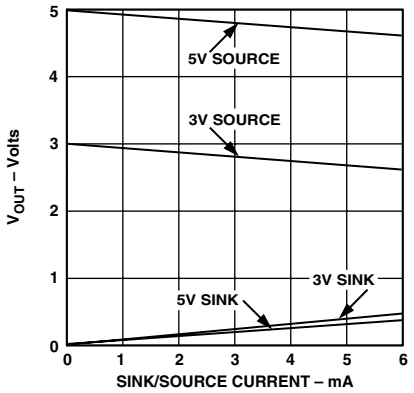


Figure 15. V_{OUT} Source and Sink Current Capability

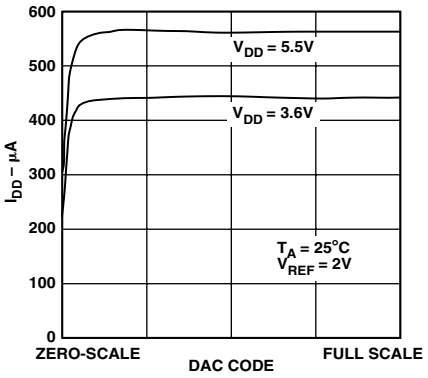


Figure 16. Supply Current vs. DAC Code

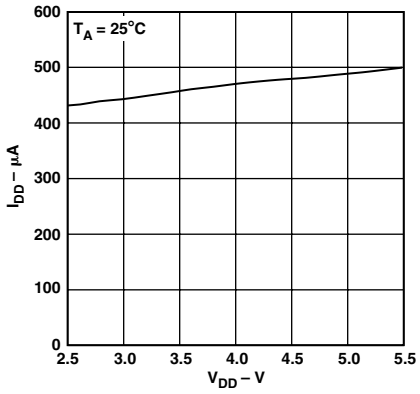


Figure 17. Supply Current vs. Supply Voltage

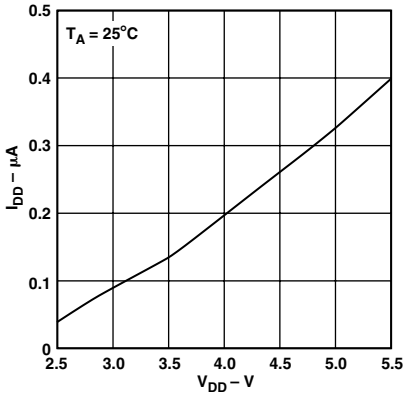


Figure 18. Power-Down Current vs. Supply Voltage

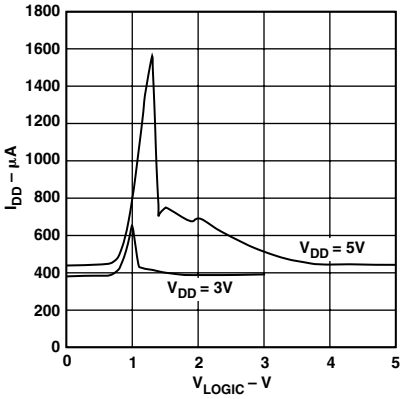


Figure 19. Supply Current vs. Logic Input Voltage

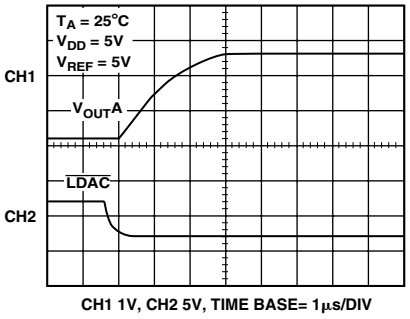


Figure 20. Half-Scale Settling (1/4 to 3/4 Scale Code Change)

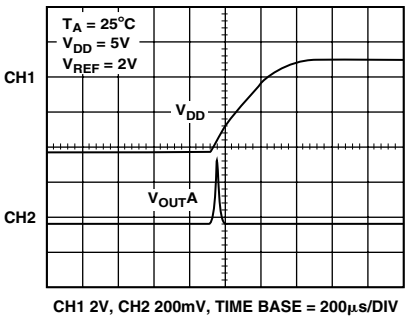


Figure 21. Power-On Reset to 0 V

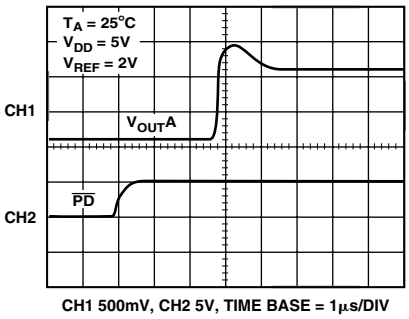


Figure 22. Exiting Power-Down to Midscale

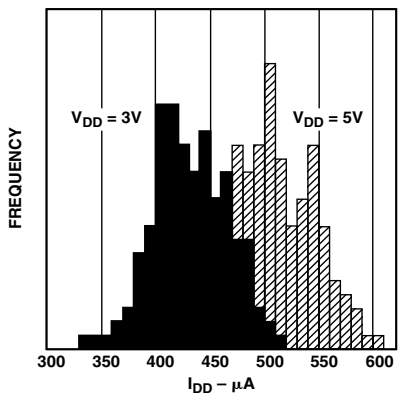


Figure 23. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

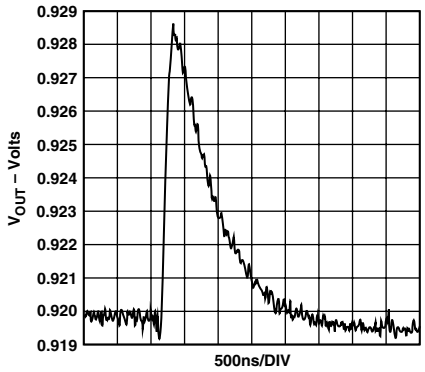


Figure 24. AD5344 Major-Code Transition Glitch Energy

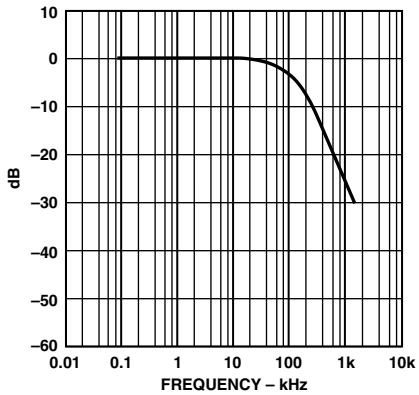


Figure 25. Multiplying Bandwidth (Small-Signal Frequency Response)

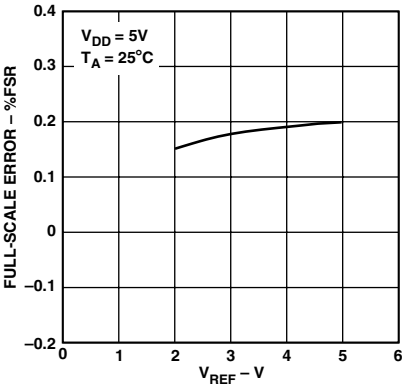


Figure 26. Full-Scale Error vs. V_{REF}

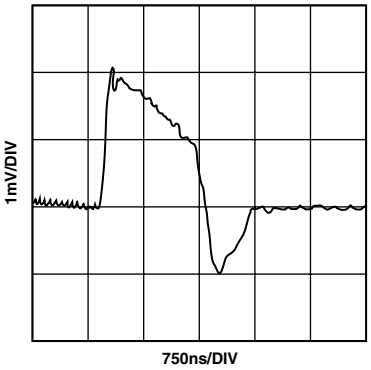


Figure 27. DAC-DAC Crosstalk

FUNCTIONAL DESCRIPTION

The AD5334/AD5335/AD5336/AD5344 are quad resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10, 10, and 12 bits, respectively. They are written to using a parallel interface. They operate from single supplies of 2.5 V to 5.5 V and the output buffer amplifiers offer rail-to-rail output swing. The gain of the buffer amplifiers in the AD5334 and AD5336 can be set to 1 or 2 to give an output voltage range of 0 to V_{REF} or 0 to 2 V_{REF}. The AD5335 and AD5344 have output buffers with unity gain.

The devices have a power-down feature that reduces current consumption to only 80 nA @ 3 V.

Digital-to-Analog Section

The architecture of one DAC channel consists of a reference buffer and a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the DAC. Figure 28 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \times Gain$$

where:

D = decimal equivalent of the binary code which is loaded to the DAC register:

0–255 for AD5334 (8 Bits)
0–1023 for AD5335/AD5336 (10 Bits)
0–4095 for AD5344 (12 Bits)

N = DAC resolution

Gain = Output Amplifier Gain (1 or 2)

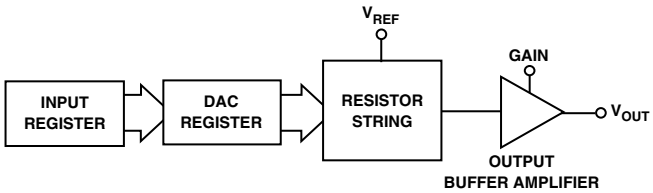


Figure 28. Single DAC Channel Architecture

Resistor String

The resistor string section is shown in Figure 29. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

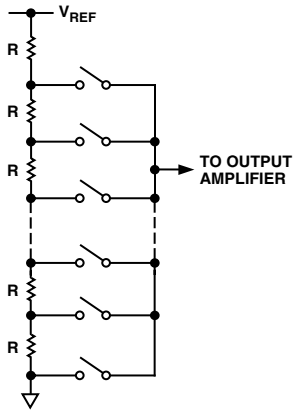


Figure 29. Resistor String

DAC Reference Input

The DACs operate with an external reference. The reference inputs are unbuffered and have an input range of 0.25 V to V_{DD}. The impedance per DAC is typically 180 kΩ for 0–V_{REF} mode and 90 kΩ for 0–2 V_{REF} mode. The AD5336 and AD5344 have separate reference inputs for each DAC, while the AD5334 and AD5335 have a reference inputs for each pair of DACS (A/B and C/D).

Output Amplifier

The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail. Its actual range depends on V_{REF}, GAIN, the load on V_{OUT}, and offset error.

If a gain of 1 is selected (GAIN = 0), the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (GAIN = 1), the output range is 0.001 V to 2 V_{REF}. However because of clamping the maximum output is limited to V_{DD} – 0.001 V.

The output amplifier is capable of driving a load of 2 kΩ to GND or V_{DD}, in parallel with 500 pF to GND or V_{DD}. The source and sink capabilities of the output amplifier can be seen in Figure 15.

The slew rate is 0.7 V/µs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 µs with the output unloaded. See Figure 20.

PARALLEL INTERFACE

The AD5334, AD5336, and AD5344 load their data as a single 8-, 10-, or 12-bit word, while the AD5335 loads data as a low byte of 8 bits and a high byte containing 2 bits.

Double-Buffered Interface

The AD5334/AD5335/AD5336/AD5344 DACs all have double-buffered interfaces consisting of an input register and a DAC register. DAC data and GAIN inputs (when available) are written to the input register under control of the Chip Select ($\overline{CS}$) and Write ($\overline{WR}$).

Access to the DAC register is controlled by the $\overline{LDAC}$ function. When $\overline{LDAC}$ is high, the DAC register is latched and the input register may change state without affecting the contents of the DAC register. However, when $\overline{LDAC}$ is brought low, the DAC register becomes transparent and the contents of the input register are transferred to it. The gain control signal is also double-buffered and is only updated when $\overline{LDAC}$ is taken low.

This is useful if the user requires simultaneous updating of all DACs and peripherals. The user may write to all input registers individually and then, by pulsing the $\overline{LDAC}$ input low, all outputs will update simultaneously.

Double-buffering is also useful where the DAC data is loaded in two bytes, as in the AD5335, because it allows the whole data word to be assembled in parallel before updating the DAC register. This prevents spurious outputs that could occur if the DAC register were updated with only the high byte or the low byte.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been updated since the last time that $\overline{LDAC}$ was brought low. Normally, when $\overline{LDAC}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5334/AD5335/AD5336/AD5344, the part will only update the DAC register if the input register has been changed since the last time the DAC register was updated. This removes unnecessary crosstalk.

Clear Input ($\overline{CLR}$)

$\overline{CLR}$ is an active low, asynchronous clear that resets the input and DAC registers. Note that the AD5344 has no $\overline{CLR}$ function.

Chip Select Input ($\overline{CS}$)

$\overline{CS}$ is an active low input that selects the device.

Write Input ($\overline{WR}$)

$\overline{WR}$ is an active low input that controls writing of data to the device. Data is latched into the input register on the rising edge of $\overline{WR}$.

Load DAC Input ($\overline{LDAC}$)

$\overline{LDAC}$ transfers data from the input register to the DAC register (and hence updates the outputs). Use of the $\overline{LDAC}$ function enables double buffering of the DAC and GAIN data. There are two $\overline{LDAC}$ modes:

Synchronous Mode: In this mode the DAC register is updated after new data is read in on the rising edge of the $\overline{WR}$ input. $\overline{LDAC}$ can be tied permanently low or pulsed as in Figure 1.

Asynchronous Mode: In this mode the outputs are not updated at the same time that the input register is written to. When $\overline{LDAC}$ goes low the DAC register is updated with the contents of the input register.

High-Byte Enable Input (HBEN)

High-Byte Enable is a control input on the AD5335 only that determines if data is written to the high-byte input register or the low-byte input register.

The low data byte of the AD5335 consists of data bits 0 to 7 at data inputs DB_0 to DB_7, while the high byte consists of Data Bits 8 and 9 at data inputs DB_0 and DB_1. DB_2 to DB_7 are ignored during a high byte write. See Figure 30.

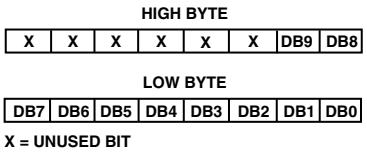


Figure 30. Data Format For AD5335

POWER-ON RESET

The AD5334/AD5335/AD5336/AD5344 are provided with a power-on reset function, so that they power up in a defined state. The power-on state is:

- Normal operation
- 0 – V_{REF} output range
- Output voltage set to 0 V

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

POWER-DOWN MODE

The AD5334/AD5335/AD5336/AD5344 have low power consumption, dissipating typically 1.5 mW with a 3 V supply and 3 mW with a 5 V supply. Power consumption can be further reduced when the DACs are not in use by putting them into power-down mode, which is selected by taking pin $\overline{PD}$ low.

When the $\overline{PD}$ pin is high, the DACs work normally with a typical power consumption of 600 µA at 5 V (500 µA at 3 V). In power-down mode, however, the supply current falls to 200 nA at 5 V (80 nA at 3 V) when the DACs are powered down. Not only does the supply current drop, but the output stage is also internally switched from the output of the amplifier, making it open-circuit. This has the advantage that the outputs are three-state while the part is in power-down mode, and provides a defined input condition for whatever is connected to the outputs of the DAC amplifiers. The output stage is illustrated in Figure 31.

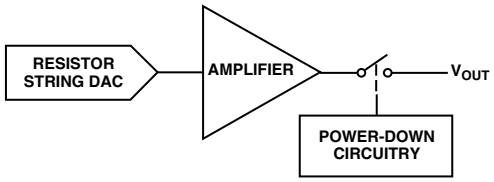


Figure 31. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string, and all other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for V_{DD} = 5 V and 5 µs when V_{DD} = 3 V. This is the time from a rising edge on the $\overline{PD}$ pin to when the output voltage deviates from its power-down voltage. See Figure 22.

Table I. AD5334/AD5336/AD5344 Truth Table

$\overline{CLR}$	$\overline{LDAC}$	$\overline{CS}$	$\overline{WR}$	A1	A0	Function
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	Clear All Registers
1	1	0	0→1	0	0	Load DAC A Input Register, GAIN A (AD5334/AD5336)
1	1	0	0→1	0	1	Load DAC B Input Register, GAIN B (AD5334/AD5336)
1	1	0	0→1	1	0	Load DAC C Input Register, GAIN C (AD5334/AD5336)
1	1	0	0→1	1	1	Load DAC D Input Register, GAIN D (AD5334/AD5336)
1	0	X	X	X	X	Update DAC Registers

X = don't care.

Table II. AD5335 Truth Table

$\overline{CLR}$	$\overline{LDAC}$	$\overline{CS}$	$\overline{WR}$	A1	A0	HBEN	Function
1	1	1	X	X	X	X	No Data Transfer
1	1	X	1	X	X	X	No Data Transfer
0	X	X	X	X	X	X	Clear All Registers
1	1	0	0→1	0	0	0	Load DAC A Low Byte Input Register
1	1	0	0→1	0	0	1	Load DAC A High Byte Input Register
1	1	0	0→1	0	1	0	Load DAC B Low Byte Input Register
1	1	0	0→1	0	1	1	Load DAC B High Byte Input Register
1	1	0	0→1	1	0	0	Load DAC C Low Byte Input Register
1	1	0	0→1	1	0	1	Load DAC C High Byte Input Register
1	1	0	0→1	1	1	0	Load DAC D Low Byte Input Register
1	1	0	0→1	1	1	1	Load DAC D High Byte Input Register
1	0	X	X	X	X	X	Update DAC Registers

X = don't care.

SUGGESTED DATABUS FORMATS

In many applications the GAIN input of the AD5334 and AD5336 may be hard-wired. However, if more flexibility is required, it can be included in a data bus. This enables the user to software program GAIN, giving the option of doubling the resolution in the lower half of the DAC range. In a bused system GAIN may be treated as a data input since it is written to the device during a write operation and takes effect when $\overline{LDAC}$ is taken low. This means that the output amplifier gain of multiple DAC devices can be controlled using a common GAIN line.

The AD5336 databus must be at least 10 bits wide and is best suited to a 16-bit databus system.

Examples of data formats for putting GAIN on a 16-bit databus are shown in Figure 32. Note that any unused bits above the actual DAC data may be used for GAIN.

AD5336

X	X	X	X	X	GAIN	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

X = UNUSED BIT

Figure 32. AD5336 Data Format for Byte Load with GAIN Data on 8-Bit Bus

APPLICATIONS INFORMATION

Typical Application Circuits

The AD5334/AD5335/AD5336/AD5344 can be used with a wide range of reference voltages and offer full, one-quadrant multiplying capability over a reference range of 0.25 V to V_{DD}. More typically, these devices may be used with a fixed, precision reference voltage. Figure 33 shows a typical setup for the devices when using an external reference connected to the reference inputs. Suitable references for 5 V operation are the AD780 and REF192. For 2.5 V operation, a suitable external reference would be the AD589, a 1.23 V bandgap reference.

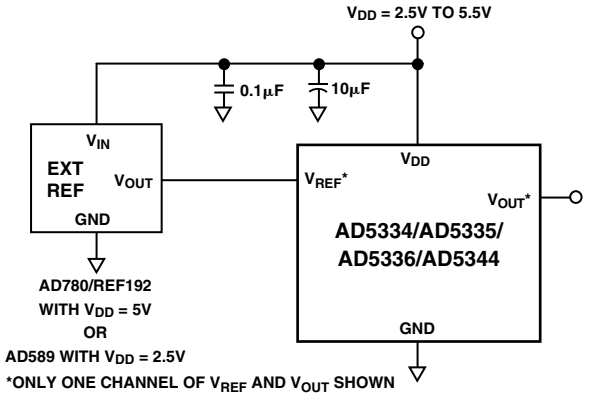


Figure 33. AD5334/AD5335/AD5336/AD5344 Using External Reference

Driving V_{DD} from the Reference Voltage

If an output range of zero to V_{DD} is required, the simplest solution is to connect the reference inputs to V_{DD}. As this supply may not be very accurate, and may be noisy, the devices may be powered from the reference voltage, for example using a 5 V reference such as the ADM663 or ADM666, as shown in Figure 34.

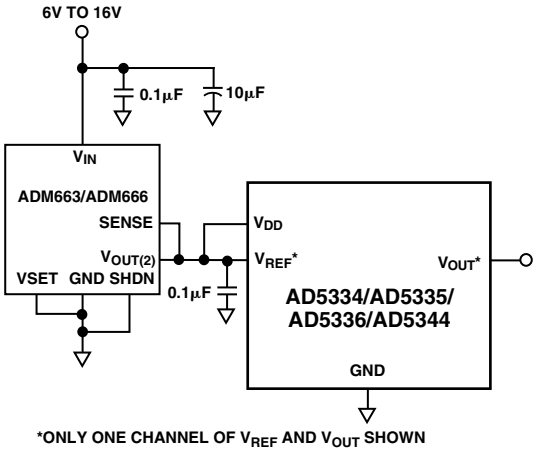


Figure 34. Using an ADM663/ADM666 as Power and Reference to AD5334/AD5335/AD5336/AD5344

Bipolar Operation Using the AD5334/AD5335/AD5336/AD5344

The AD5334/AD5335/AD5336/AD5344 have been designed for single supply operation, but bipolar operation is achievable using the circuit shown in Figure 35. The circuit shown has been configured to achieve an output voltage range of $-5\ V < V_O < +5\ V$. Rail-to-rail operation at the amplifier output is achievable using an AD820 or OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = [(1 + R4/R3) \times (R2/(R1 + R2) \times (2 \times V_{REF} \times D/2^N)] - R4 \times V_{REF}/R3$$

where:

D is the decimal equivalent of the code loaded to the DAC, N is DAC resolution and V_{REF} is the reference voltage input.

With:

$V_{REF} = 2.5$ V
R1 = R3 = 10 kΩ
R2 = R4 = 20 kΩ and $V_{DD} = 5$ V.
$V_{OUT} = (10 \times D/2^N) - 5$

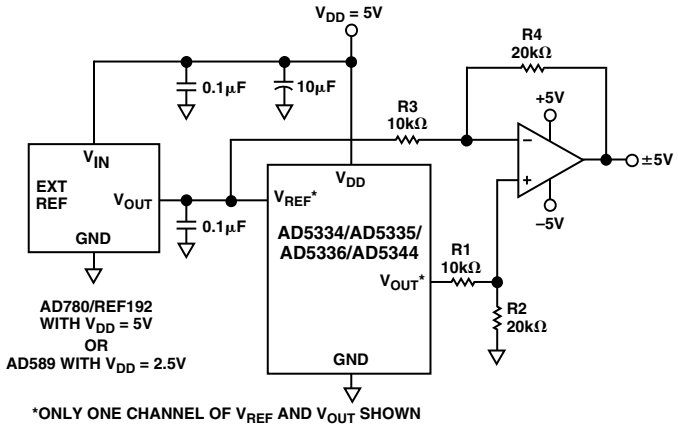


Figure 35. Bipolar Operation using the AD5334/AD5335/ AD5336/AD5344

Decoding Multiple AD5334/AD5335/AD5336/AD5344

The $\overline{CS}$ pin on these devices can be used in applications to decode a number of DACs. In this application, all DACs in the system receive the same data and $\overline{WR}$ pulses, but only the $\overline{CS}$ to one of the DACs will be active at any one time, so data will only be written to the DAC whose $\overline{CS}$ is low. If multiple AD5343s are being used, a common HBEN line will also be required to determine if the data is written to the high-byte or low-byte register of the selected DAC.

The 74HC139 is used as a 2- to 4-line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 36 shows a diagram of a typical setup for decoding multiple devices in a system. Once data has been written sequentially to all DACs in a system, all the DACs can be updated simultaneously using a common $\overline{LDAC}$ line. A common $\overline{CLR}$ line can also be used to reset all DAC outputs to zero (except on the AD5344).

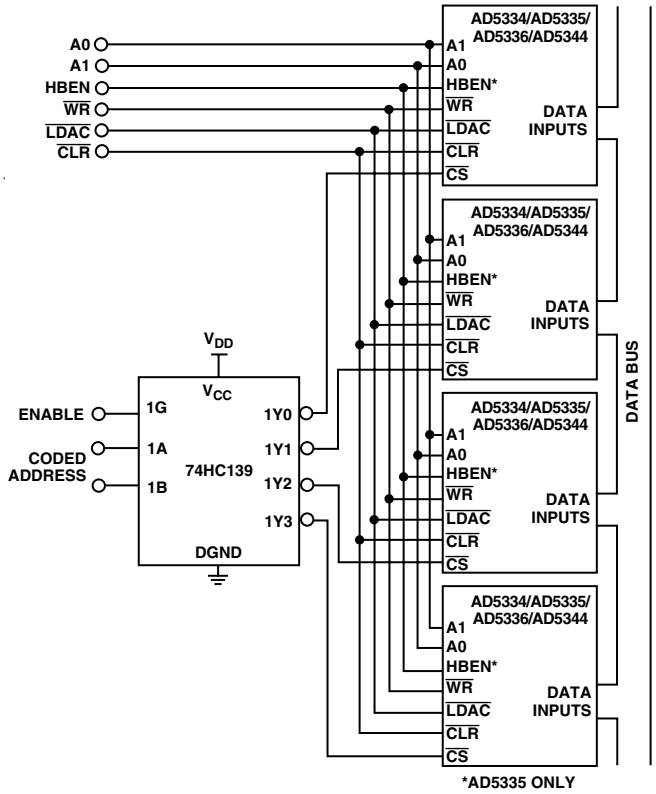


Figure 36. Decoding Multiple DAC Devices

AD5334/AD5335/AD5336/AD5344 as a Digitally Programmable Window Detector

A digitally programmable upper/lower limit detector using two of the DACs in the AD5334/AD5335/AD5336/AD5344 is shown in Figure 37.

Any pair of DACs in the device may be used, but for simplicity the description will refer to DACs A and B.

Care must be taken to connect the correct reference inputs to the reference source. The AD5334 and AD5335 have only two reference inputs, V_{REF}A/B for DACs A and B and V_{REF}C/D for DACs C and D. If DACs A and B are used (for example) then only V_{REF}A/B is needed. DACs C and D and V_{REF}C/D may be used for some other purpose. The AD5336 and AD5344 have separate reference inputs for each DAC.

The upper and lower limits for the test are loaded to DACs A and B which, in turn, set the limits on the CMP04. If a signal at the V_{IN} input is not within the programmed window, an LED will indicate the fail condition.

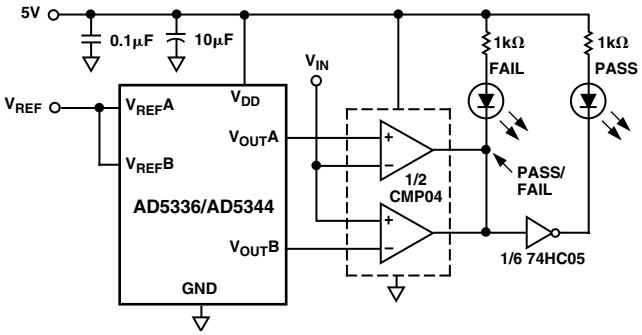


Figure 37. Programmable Window Detector

Programmable Current Source

Figure 38 shows the AD5334/AD5335/AD5336/AD5344 used as the control element of a programmable current source. In this example, the full-scale current is set to 1 mA. The output voltage from the DAC is applied across the current setting resistor of 4.7 kΩ in series with the 470 Ω adjustment potentiometer, which gives an adjustment of about ±5%. Suitable transistors to place in the feedback loop of the amplifier include the BC107 and the 2N3904, which enable the current source to operate from a minimum V_{SOURCE} of 6 V. The operating range is determined by the operating characteristics of the transistor. Suitable amplifiers include the AD820 and the OP295, both having rail-to-rail operation on their outputs. The current for any digital input code and resistor value can be calculated as follows:

$$I = G \times V_{REF} \times \frac{D}{(2^N \times R)}\ mA$$

Where:

G is the gain of the buffer amplifier (1 or 2)
D is the digital input code
N is the DAC resolution (8, 10, or 12 bits)
R is the sum of the resistor plus adjustment potentiometer in kΩ

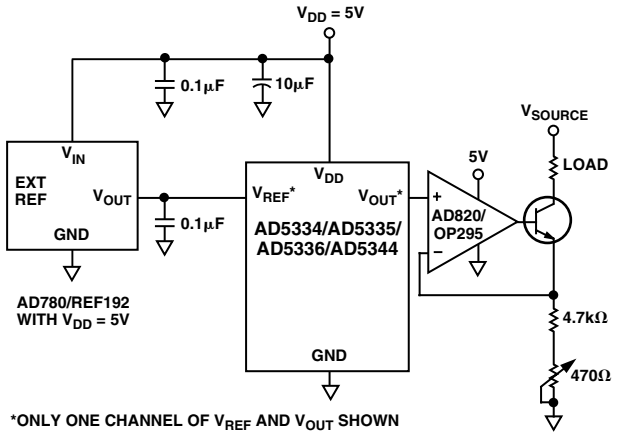


Figure 38. Programmable Current Source

Coarse and Fine Adjustment Using the AD5334/AD5335/AD5336/AD5344

Two of the DACs in the AD5334/AD5335/AD5336/AD5344 can be paired together to form a coarse and fine adjustment function, as shown in Figure 39. As with the window comparator previously described, the description will refer to DACs A, and B and the reference connections will depend on the actual device used.

DAC A is used to provide the coarse adjustment while DAC B provides the fine adjustment. Varying the ratio of R1 and R2 will change the relative effect of the coarse and fine adjustments. With the resistor values shown the output amplifier has unity gain for the DAC A output, so the output range is zero to (V_{REF} – 1 LSB). For DAC B the amplifier has a gain of 7.6×10^{-3}, giving DAC B a range equal to 2 LSBs of DAC A.

The circuit is shown with a 2.5 V reference, but reference voltages up to V_{DD} may be used. The op amps indicated will allow a rail-to-rail output swing.

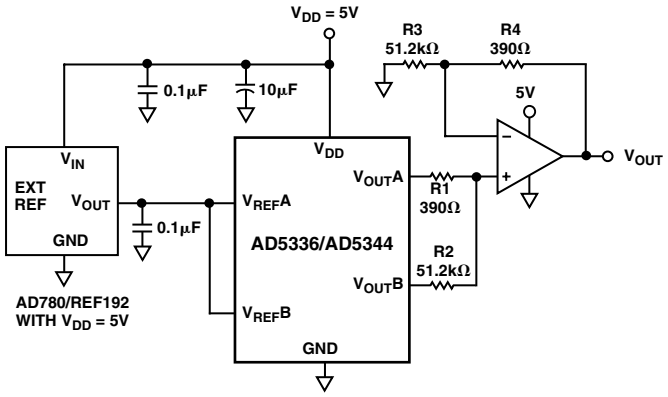


Figure 39. Coarse and Fine Adjustment

Power Supply Bypassing and Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5334/AD5335/AD5336/AD5344 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the device is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as closely as possible to the device. The AD5334/AD5335/AD5336/AD5344 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

Table III. Overview of AD53xx Parallel Devices

Part No.	Resolution	DNL	V_{REF} Pins	Settling Time	Additional Pin Functions				Package	Pins
SINGLES					**BUF**	**GAIN**	**HBEN**	**$\overline{CLR}$**		
AD5330	8	±0.25	1	6 µs	✓	✓		✓	TSSOP	20
AD5331	10	±0.5	1	7 µs		✓		✓	TSSOP	20
AD5340	12	±1.0	1	8 µs	✓	✓		✓	TSSOP	24
AD5341	12	±1.0	1	8 µs	✓	✓	✓	✓	TSSOP	20
DUALS										
AD5332	8	±0.25	2	6 µs				✓	TSSOP	20
AD5333	10	±0.5	2	7 µs	✓	✓		✓	TSSOP	24
AD5342	12	±1.0	2	8 µs	✓	✓		✓	TSSOP	28
AD5343	12	±1.0	1	8 µs			✓	✓	TSSOP	20
QUADS										
AD5334	8	±0.25	2	6 µs		✓		✓	TSSOP	24
AD5335	10	±0.5	2	7 µs			✓	✓	TSSOP	24
AD5336	10	±0.5	4	7 µs		✓		✓	TSSOP	28
AD5344	12	±1.0	4	8 µs					TSSOP	28

Table IV. Overview of AD53xx Serial Devices

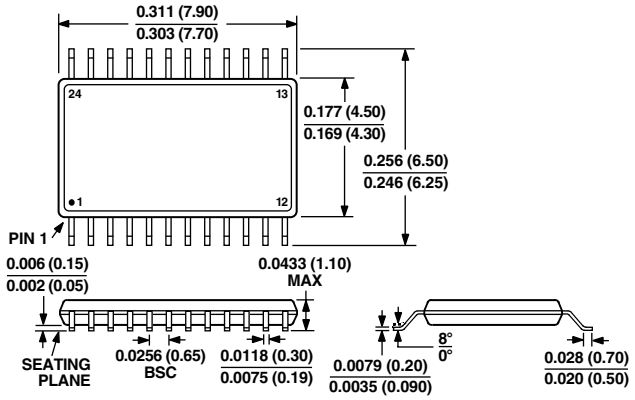
Part No.	Resolution	No. of DACS	DNL	Interface	Settling Time	Package	Pins
SINGLES							
AD5300	8	1	±0.25	SPI	4 µs	SOT-23, MicroSOIC	6, 8
AD5310	10	1	±0.5	SPI	6 µs	SOT-23, MicroSOIC	6, 8
AD5320	12	1	±1.0	SPI	8 µs	SOT-23, MicroSOIC	6, 8
AD5301	8	1	±0.25	2-Wire	6 µs	SOT-23, MicroSOIC	6, 8
AD5311	10	1	±0.5	2-Wire	7 µs	SOT-23, MicroSOIC	6, 8
AD5321	12	1	±1.0	2-Wire	8 µs	SOT-23, MicroSOIC	6, 8
DUALS							
AD5302	8	2	±0.25	SPI	6 µs	MicroSOIC	8
AD5312	10	2	±0.5	SPI	7 µs	MicroSOIC	8
AD5322	12	2	±1.0	SPI	8 µs	MicroSOIC	8
AD5303	8	2	±0.25	SPI	6 µs	TSSOP	16
AD5313	10	2	±0.5	SPI	7 µs	TSSOP	16
AD5323	12	2	±1.0	SPI	8 µs	TSSOP	16
QUADS							
AD5304	8	4	±0.25	SPI	6 µs	MicroSOIC	10
AD5314	10	4	±0.5	SPI	7 µs	MicroSOIC	10
AD5324	12	4	±1.0	SPI	8 µs	MicroSOIC	10
AD5305	8	4	±0.25	2-Wire	6 µs	MicroSOIC	10
AD5315	10	4	±0.5	2-Wire	7 µs	MicroSOIC	10
AD5325	12	4	±1.0	2-Wire	8 µs	MicroSOIC	10
AD5306	8	4	±0.25	2-Wire	6 µs	TSSOP	16
AD5316	10	4	±0.5	2-Wire	7 µs	TSSOP	16
AD5326	12	4	±1.0	2-Wire	8 µs	TSSOP	16
AD5307	8	4	±0.25	SPI	6 µs	TSSOP	16
AD5317	10	4	±0.5	SPI	7 µs	TSSOP	16
AD5327	12	4	±1.0	SPI	8 µs	TSSOP	16

Visit our web-page at http://www.analog.com/support/standard_linear/selection_guides/AD53xx.html

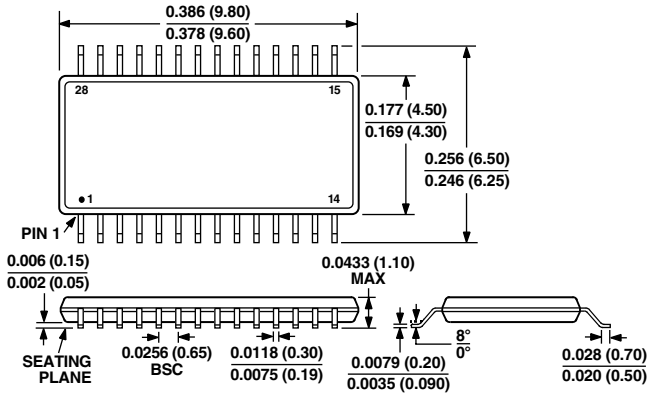
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead Thin Shrink Small Outline Package TSSOP (RU-24)



28-Lead Thin Shrink Small Outline Package TSSOP (RU-28)



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