



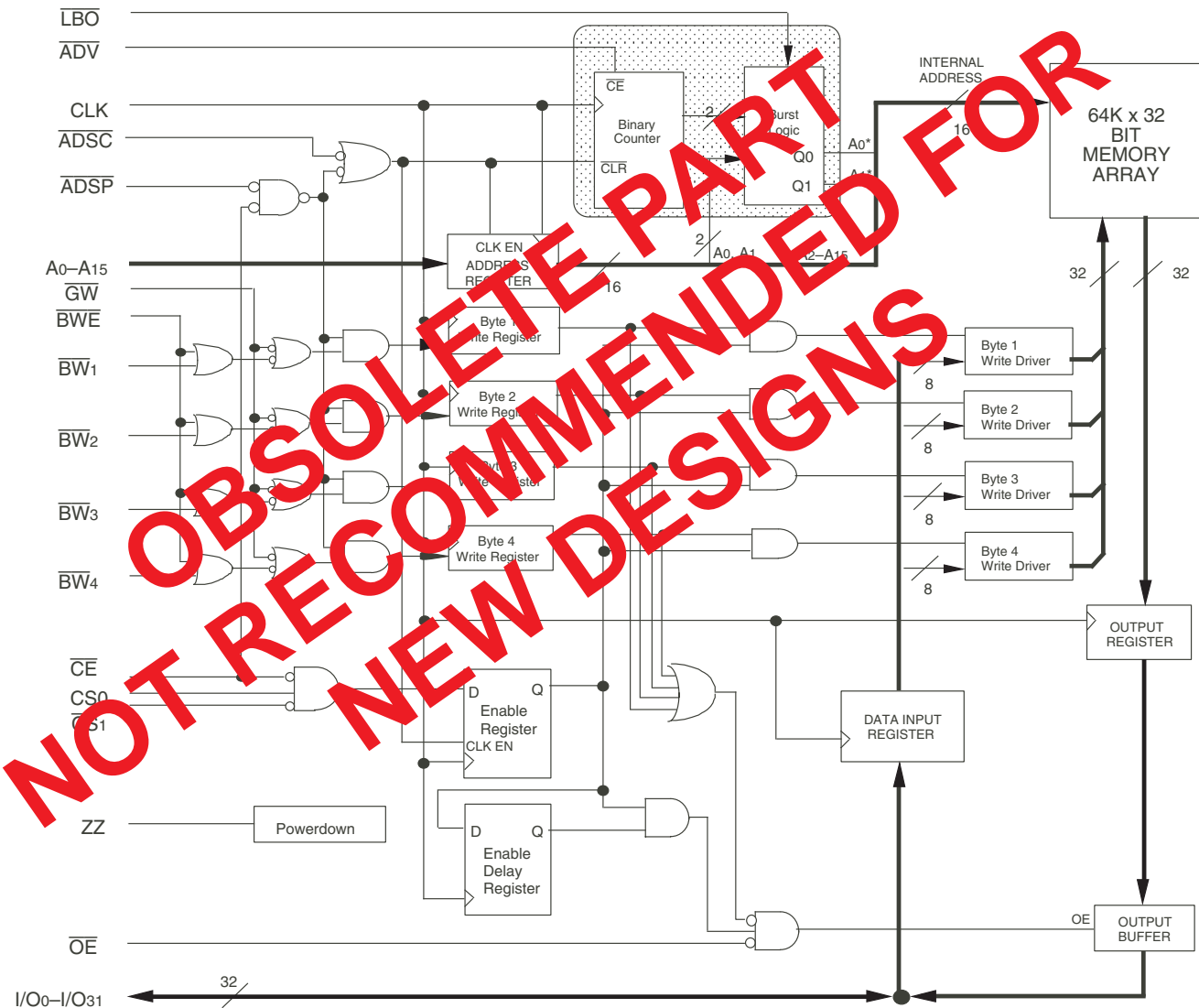
**THE DATASHEET OF
71V632S7PFG8**



Features

- ◆ 64K x 32 memory configuration
- ◆ Supports high system speed:
Commercial and Industrial:
 - 5 5ns clock access time (100 MHz)
 - 6 6ns clock access time (83 MHz)
 - 7 7ns clock access time (66 MHz)
- ◆ Single-cycle deselect functionality
- ◆ LBO input selects interleaved or linear burst mode
- ◆ Self-timed write cycle with global write control (\overline{GW}), byte write enable (\overline{BWE}), and byte writes (\overline{BWx})
- ◆ Power down controlled by ZZ input
- ◆ Operates with a single 3.3V power supply (+10/-5%)
- ◆ Packaged in a JEDEC Standard 100-pin rectangular plastic thin quad flatpack (TQFP)
- ◆ Green parts available, see ordering information

Functional Block Diagram



3619 drw 01

Description

The IDT71V632 is a 3.3V high-speed SRAM organized as 64K x 32 with full support of the Pentium™ and PowerPC™ processor interfaces. The pipelined burst architecture provides cost-effective 3-1-1-1 secondary cache performance for processors up to 100MHz.

The IDT71V632 SRAM contains write, data, address, and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V632 can provide four cycles of data for

a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected (\overline{ADV} =LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses will be defined by the internal burst counter and the \overline{LBO} input pin.

The IDT71V632 SRAM utilizes a high-performance, high-volume 3.3V CMOS process, and is packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) for optimum board density in both desktop and notebook applications.

Pin Description Summary

| | | | |
|---|-----------------------------------|-------|--------------|
| A ₀ -A ₁₅ | Address Inputs | Input | Synchronous |
| \overline{CE} | Chip Enable | Input | Synchronous |
| CS ₀ , \overline{CS}_1 | Chips Selects | Input | Synchronous |
| \overline{OE} | Output Enable | Input | Asynchronous |
| \overline{GW} | Global Write Enable | Input | Synchronous |
| \overline{BWE} | Byte Write Enable | Input | Synchronous |
| \overline{BW}_1 , \overline{BW}_2 , \overline{BW}_3 , \overline{BW}_4 | Individual Byte Write Selects | Input | Synchronous |
| CLK | Clock | Input | N/A |
| \overline{ADV} | Burst Address Advance | Input | Synchronous |
| \overline{ADSC} | Address Status (Cache Controller) | Input | Synchronous |
| \overline{ADSP} | Address Status (Processor) | Input | Synchronous |
| \overline{LBO} | Linear / Interleaved Burst Order | Input | DC |
| ZZ | Sleep Mode | Input | Asynchronous |
| I/O ₀ -I/O ₃₁ | Data Input/Output | I/O | Synchronous |
| V _{DD} , V _{DD0} | 3.3V | Power | N/A |
| V _{SS} , V _{SS0} | Array Ground, I/O Ground | Power | N/A |

3619 tbl 01

Pin Definitions⁽¹⁾

| Symbol | Pin Function | I/O | Active | Description |
|---|-----------------------------------|-----|--------|--|
| A0–A15 | Address Inputs | I | N/A | Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{\text{ADSC}}$ Low or $\overline{\text{ADSP}}$ Low and $\overline{\text{CE}}$ Low. |
| $\overline{\text{ADSC}}$ | Address Status (Cache Controller) | I | LOW | Synchronous Address Status from Cache Controller. $\overline{\text{ADSC}}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{\text{ADSC}}$ is NOT GATED by $\overline{\text{CE}}$. |
| $\overline{\text{ADSP}}$ | Address Status (Processor) | I | LOW | Synchronous Address Status from Processor. $\overline{\text{ADSP}}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{\text{ADSP}}$ is gated by $\overline{\text{CE}}$. |
| $\overline{\text{ADV}}$ | Burst Address Advance | I | LOW | Synchronous Address Advance. $\overline{\text{ADV}}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When this input is HIGH the burst counter is not incremented; that is, there is no address advance. |
| $\overline{\text{BWE}}$ | Byte Write Enable | I | LOW | Synchronous byte write enable gates the byte write inputs $\overline{\text{BW1}}\text{--}\overline{\text{BW4}}$. If $\overline{\text{BWE}}$ is LOW at the rising edge of CLK then $\overline{\text{BWx}}$ inputs are passed to the next stage in the circuit. A byte write can still be blocked if $\overline{\text{ADSP}}$ is LOW at the rising edge of CLK. If $\overline{\text{ADSP}}$ is HIGH and $\overline{\text{BWx}}$ is LOW at the rising edge of CLK then data will be written to the SRAM. If $\overline{\text{BWE}}$ is HIGH then the byte write inputs are blocked and only $\overline{\text{GW}}$ can initiate a write cycle. |
| $\overline{\text{BW1}}\text{--}\overline{\text{BW4}}$ | Individual Byte Write Enables | I | LOW | Synchronous byte write enables. $\overline{\text{BW1}}$ controls I/O(7:0), $\overline{\text{BW2}}$ controls I/O(15:8), etc. Any active byte write causes all outputs to be disabled. $\overline{\text{ADSP}}$ LOW disables all byte writes. $\overline{\text{BW1}}\text{--}\overline{\text{BW4}}$ must meet specified setup and hold times with respect to CLK. |
| $\overline{\text{CE}}$ | Chip Enable | I | LOW | Synchronous chip enable. $\overline{\text{CE}}$ is used with CS_0 and $\overline{\text{CS}}_1$ to enable the IDT71V632. $\overline{\text{CE}}$ also gates $\overline{\text{ADSP}}$. |
| CLK | Clock | I | N/A | This is the clock input. All timing references for the device are made with respect to this input. |
| CS_0 | Chip Select 0 | I | HIGH | Synchronous active HIGH chip select. CS_0 is used with $\overline{\text{CE}}$ and $\overline{\text{CS}}_1$ to enable the chip. |
| $\overline{\text{CS}}_1$ | Chip Select 1 | I | LOW | Synchronous active LOW chip select. $\overline{\text{CS}}_1$ is used with $\overline{\text{CE}}$ and CS_0 to enable the chip. |
| $\overline{\text{GW}}$ | Global Write Enable | I | LOW | Synchronous global write enable. This input will write all four 8-bit data bytes when LOW on the rising edge of CLK. $\overline{\text{GW}}$ supercedes individual byte write enables. |
| I/O ₀ –I/O ₃₁ | Data Input/Output | I/O | N/A | Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK. |
| $\overline{\text{LBO}}$ | Linear Burst Order | I | LOW | Asynchronous burst order selection DC input. When $\overline{\text{LBO}}$ is HIGH the Interleaved (Intel) burst sequence is selected. When $\overline{\text{LBO}}$ is LOW the Linear (PowerPC) burst sequence is selected. $\overline{\text{LBO}}$ is a static DC input and must not change state while the device is operating. |
| $\overline{\text{OE}}$ | Output Enable | I | LOW | Asynchronous output enable. When $\overline{\text{OE}}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{\text{OE}}$ is HIGH the I/O pins are in a high-impedance state. |
| V _{DD} | Power Supply | N/A | N/A | 3.3V core power supply inputs. |
| V _{DDQ} | Power Supply | N/A | N/A | 3.3V I/O power supply inputs. |
| V _{SS} | Ground | N/A | N/A | Core ground pins. |
| V _{SSQ} | Ground | N/A | N/A | I/O ground pins. |
| NC | No Connect | N/A | N/A | NC pins are not electrically connected to the chip. |
| ZZ | Sleep Mode | I | HIGH | Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V632 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. |

NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

3619 tbl 02

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Value | Unit |
|----------------------------------|--------------------------------------|------------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| V _{TERM} ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to V _{DD} +0.5 | V |
| T _A | Operating Temperature | 0 to +70 | °C |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | °C |
| P _T | Power Dissipation | 1.0 | W |
| I _{OUT} | DC Output Current | 50 | mA |

3619 tbl 05

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{DD}, V_{DDQ} and Input terminals only.
- I/O terminals.

Capacitance

(T_A = +25°C, f = 1.0MHz, TQFP package)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 6 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

3619 tbl 06

NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | V _{SS} | V _{DD} | V _{DDQ} |
|------------|----------------|-----------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 0V | 3.3V+10/-5% | 3.3V+10/-5% |
| Industrial | -40°C to +85°C | 0V | 3.3V+10/-5% | 3.3V+10/-5% |

3619 tbl 03

Recommended DC Operating Conditions

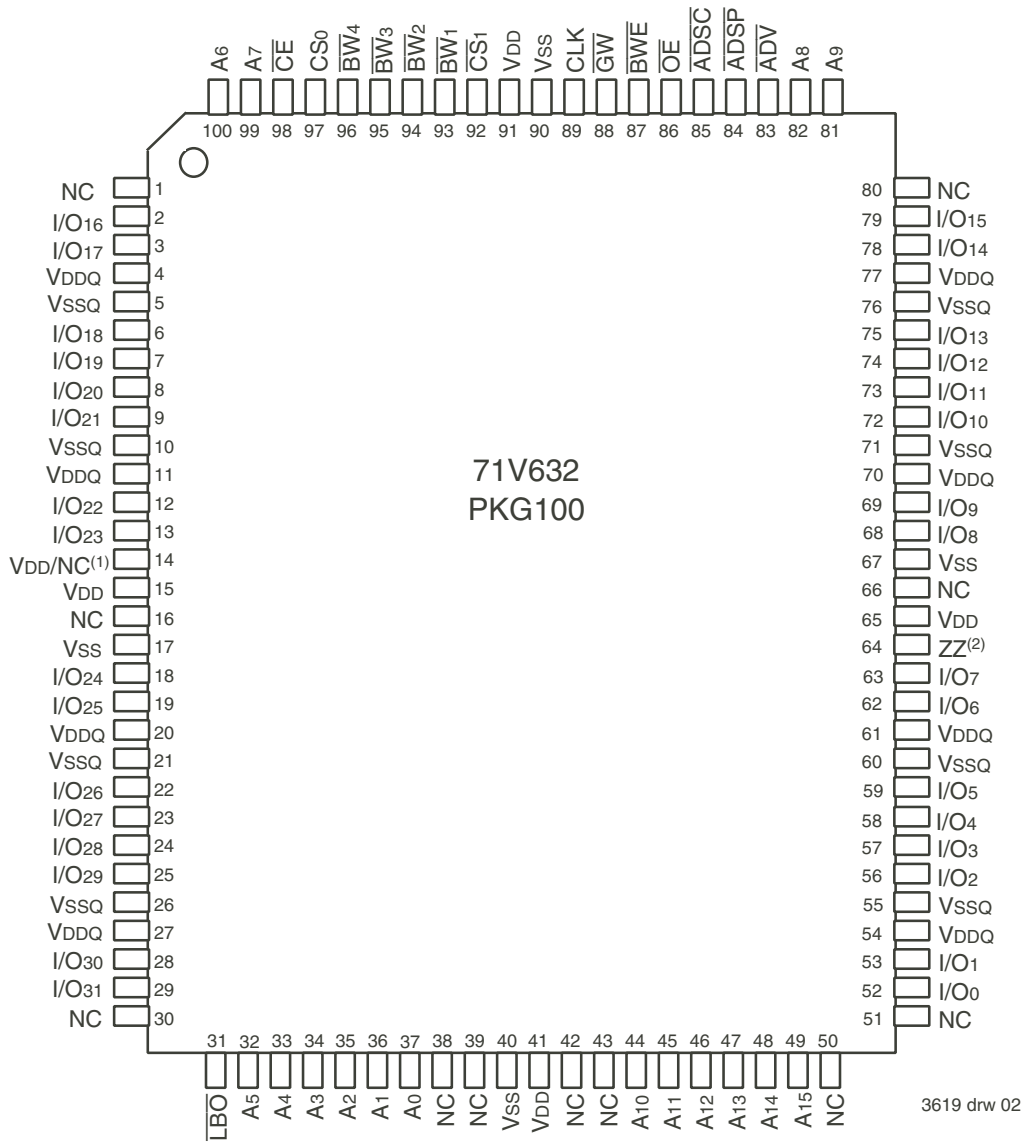
| Symbol | Parameter | Min. | Max. | Unit |
|------------------------------------|-----------------------------|---------------------|--------------------------------------|------|
| V _{DD} | Core Supply Voltage | 3.135 | 3.63 | V |
| V _{DDQ} | I/O Supply Voltage | 3.135 | 3.63 | V |
| V _{SS} , V _{SSQ} | Ground | 0 | 0 | V |
| V _{IH} | Input High Voltage — Inputs | 2.0 | 5.0 ⁽¹⁾ | V |
| V _{IH} | Input High Voltage — I/O | 2.0 | V _{DDQ} +0.3 ⁽²⁾ | V |
| V _{IL} | Input Low Voltage | -0.3 ⁽³⁾ | 0.8 | V |

3619 tbl 04

NOTES:

- V_{IH} (max) = 6.0V for pulse width less than t_{cy}/2, once per cycle.
- V_{IH} (max) = V_{DDQ} + 1.0V for pulse width less than t_{cy}/2, once per cycle.
- V_{IL} (min) = -1.0V for pulse width less than t_{cy}/2, once per cycle.

Pin Configuration



Top View TQFP

NOTES:

1. Pin 14 can either be directly connected to VDD or not connected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

Synchronous Truth Table^(1,2)

| Operation | Address Used | \overline{CE} | CS ₀ | \overline{CS}_1 | \overline{ADSP} | \overline{ADSC} | \overline{ADV} | \overline{GW} | \overline{BWE} | \overline{BW}_x | $\overline{OE}^{(3)}$ | CLK | I/O |
|------------------------------|--------------|-----------------|-----------------|-------------------|-------------------|-------------------|------------------|-----------------|------------------|-------------------|-----------------------|-----|------|
| Deselected Cycle, Power Down | None | H | X | X | X | L | X | X | X | X | X | ↑ | Hi-Z |
| Deselected Cycle, Power Down | None | L | X | H | L | X | X | X | X | X | X | ↑ | Hi-Z |
| Deselected Cycle, Power Down | None | L | L | X | L | X | X | X | X | X | X | ↑ | Hi-Z |
| Deselected Cycle, Power Down | None | L | X | H | X | L | X | X | X | X | X | ↑ | Hi-Z |
| Deselected Cycle, Power Down | None | L | L | X | X | L | X | X | X | X | X | ↑ | Hi-Z |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | X | L | ↑ | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | X | H | ↑ | Hi-Z |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | H | X | L | ↑ | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | H | L | ↑ | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | H | H | ↑ | Hi-Z |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | L | X | ↑ | DIN |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | L | X | X | X | ↑ | DIN |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | X | L | ↑ | DOUT |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | X | H | ↑ | Hi-Z |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | X | H | L | ↑ | DOUT |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | X | H | H | ↑ | Hi-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | X | L | ↑ | DOUT |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | X | H | ↑ | Hi-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | L | ↑ | DOUT |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | H | ↑ | Hi-Z |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | H | L | L | X | ↑ | DIN |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | L | X | X | X | ↑ | DIN |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | H | L | L | X | ↑ | DIN |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | L | X | X | X | ↑ | DIN |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | X | L | ↑ | DOUT |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | X | H | ↑ | Hi-Z |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | X | H | L | ↑ | DOUT |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | X | H | H | ↑ | Hi-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | X | L | ↑ | DOUT |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | X | H | ↑ | Hi-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | X | H | L | ↑ | DOUT |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | X | H | H | ↑ | Hi-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | L | L | X | ↑ | DIN |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | L | X | X | X | ↑ | DIN |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | L | L | X | ↑ | DIN |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | L | X | X | X | ↑ | DIN |

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. ZZ = LOW for this table.
3. \overline{OE} is an asynchronous input.

3619 tbl 07

Synchronous Write Function Truth Table⁽¹⁾

| Operation | \overline{GW} | \overline{BWE} | \overline{BW}_1 | \overline{BW}_2 | \overline{BW}_3 | \overline{BW}_4 |
|-----------------------------|-----------------|------------------|-------------------|-------------------|-------------------|-------------------|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write all Bytes | L | X | X | X | X | X |
| Write all Bytes | H | L | L | L | L | L |
| Write Byte 1 ⁽²⁾ | H | L | L | H | H | H |
| Write Byte 2 ⁽²⁾ | H | L | H | L | H | H |
| Write Byte 3 ⁽²⁾ | H | L | H | H | L | H |
| Write Byte 4 ⁽²⁾ | H | L | H | H | H | L |

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. Multiple bytes may be selected during the same cycle.

3619 tbl 08

Asynchronous Truth Table⁽¹⁾

| Operation ⁽²⁾ | \overline{OE} | ZZ | I/O Status | Power |
|--------------------------|-----------------|----|--|---------|
| Read | L | L | Data Out (I/O ₀ - I/O ₃₁) | Active |
| Read | H | L | High-Z | Active |
| Write | X | L | High-Z — Data In (I/O ₀ - I/O ₃₁) | Active |
| Deselected | X | L | High-Z | Standby |
| Sleep | X | H | High-Z | Sleep |

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

3619 tbl 09

Interleaved Burst Sequence Table ($\overline{LBO} = V_{DD}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address ⁽¹⁾ | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

3619 tbl 10

Linear Burst Sequence Table ($\overline{LBO} = V_{SS}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address ⁽¹⁾ | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

3619 tbl 11

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3V \pm 10/-5\%$)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|--|---|------|------|---------|
| $ I_{LI} $ | Input Leakage Current | $V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$ | — | 5 | μA |
| $ I_{LZZ} $ | ZZ and $\overline{LB0}$ Input Leakage Current ⁽¹⁾ | $V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$ | — | 30 | μA |
| $ I_{LO} $ | Output Leakage Current | $\overline{CE} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}, V_{OUT} = 0V \text{ to } V_{DD}, V_{DD} = \text{Max.}$ | — | 5 | μA |
| $V_{OL} (3.3V)$ | Output Low Voltage | $I_{OL} = 5mA, V_{DD} = \text{Min.}$ | — | 0.4 | V |
| $V_{OH} (3.3V)$ | Output High Voltage | $I_{OH} = -5mA, V_{DD} = \text{Min.}$ | 2.4 | — | V |

NOTE:

3619 tbl 12

- The $\overline{LB0}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾ ($V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V$)

| Symbol | Parameter | Test Conditions | SA4 ^(3,4) | | S5 | | S6 | | S7 | | Unit |
|-----------|--------------------------------------|---|----------------------|------|--------|------|--------|------|--------|------|------|
| | | | Com'l. | Ind. | Com'l. | Ind. | Com'l. | Ind. | Com'l. | Ind. | |
| I_{DD} | Operating Power Supply Current | Device Selected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{IH}$ or $\leq V_{IL}, f = f_{MAX}^{(2)}$ | 220 | — | 200 | 200 | 180 | 180 | 160 | 160 | mA |
| I_{SB} | Standby Power Supply Current | Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{IH}$ or $\leq V_{IL}, f = f_{MAX}^{(2)}$ | 70 | — | 65 | 65 | 60 | 60 | 55 | 55 | mA |
| I_{SB1} | Full Standby Power Supply Current | Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{HD}$ or $\leq V_{LD}, f = 0^{(2)}$ | 15 | — | 15 | 15 | 15 | 15 | 15 | 15 | mA |
| I_{ZZ} | Full Sleep Mode Power Supply Current | $ZZ \geq V_{HD}, V_{DD} = \text{Max.}$ | 10 | — | 10 | 10 | 10 | 10 | 10 | 10 | mA |

3619 tbl 13

NOTES:

- All values are maximum guaranteed values.
- At $f = f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of $1/t_{cvc}$ while $\overline{ADSC} = \text{LOW}$; $f=0$ means no input lines are changing.
- SA4 speed grade corresponds to a t_{CD} of 4.5 ns.
- 0°C to +70°C temperature range only.

AC Test Loads

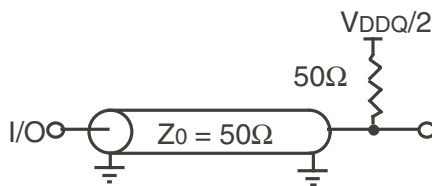
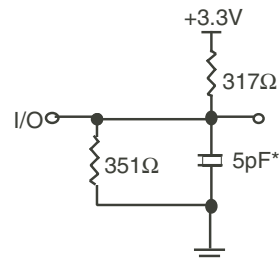


Figure 1. AC Test Load

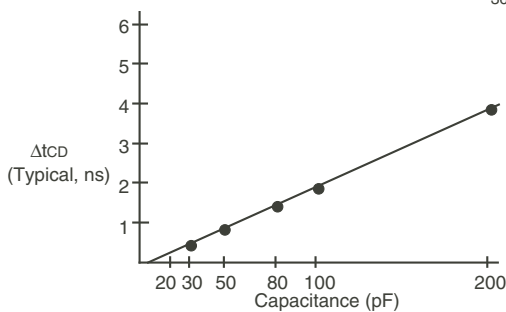
3619 drw 03



3619 drw 04

* Including scope and jig capacitance.

Figure 2. High-Impedance Test Load (for $t_{OHZ}, t_{CHZ}, t_{OLZ},$ and t_{DC1})



3619 drw 05

Figure 3. Lumped Capacitive Load, Typical Derating

AC Test Conditions

| | |
|--------------------------------|---------------------|
| Input Pulse Levels | 0 to 3.0V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| AC Test Load | See Figures 1 and 2 |

3619 tbl 14

AC Electrical Characteristics

(VDD, VDDQ = 3.3V +10/-5%, Commercial and Industrial Temperature Ranges)

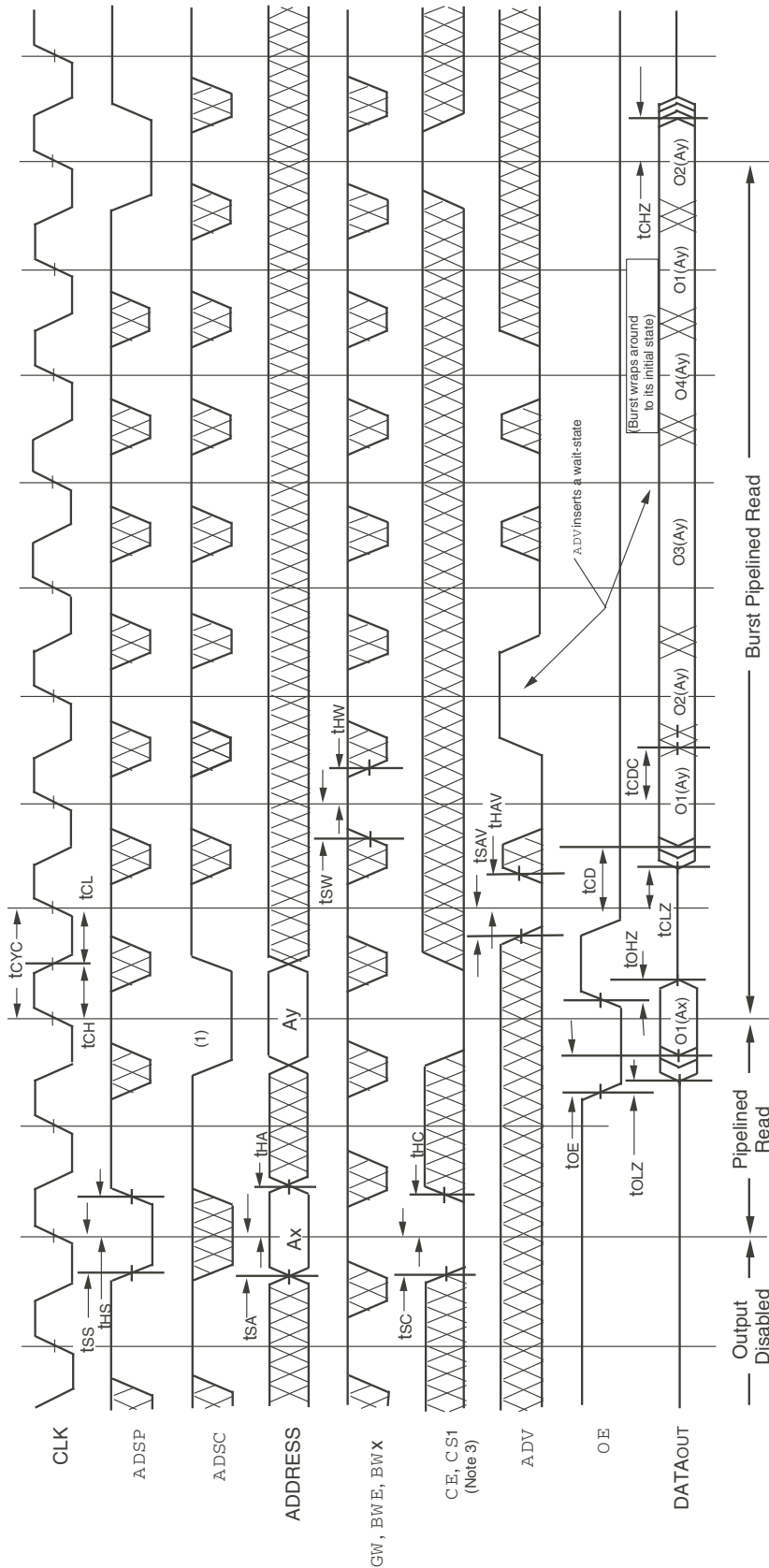
| Symbol | Parameter | 71V632SA4 ^(5,6) | | 71V632S5 | | 71V632S6 | | 71V632S7 | | Unit |
|--|-----------------------------------|----------------------------|------|----------|------|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| CLOCK PARAMETERS | | | | | | | | | | |
| t _{CC} | Clock Cycle Time | 8.5 | — | 10 | — | 12 | — | 15 | — | ns |
| t _{CH} ⁽¹⁾ | Clock High Pulse Width | 3.5 | — | 4 | — | 4.5 | — | 5 | — | ns |
| t _{CL} ⁽¹⁾ | Clock Low Pulse Width | 3.5 | — | 4 | — | 4.5 | — | 5 | — | ns |
| OUTPUT PARAMETERS | | | | | | | | | | |
| t _{CD} | Clock High to Valid Data | — | 4.5 | — | 5 | — | 6 | — | 7 | ns |
| t _{CD} | Clock High to Data Change | 1.5 | — | 1.5 | — | 2 | — | 2 | — | ns |
| t _{CLZ} ⁽²⁾ | Clock High to Output Active | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{CHZ} ⁽²⁾ | Clock High to Data High-Z | 1.5 | 4 | 1.5 | 5 | 2 | 5 | 2 | 6 | ns |
| t _{OE} | Output Enable Access Time | — | 4 | — | 5 | — | 5 | — | 6 | ns |
| t _{OLZ} ⁽²⁾ | Output Enable Low to Data Active | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{OHZ} ⁽²⁾ | Output Enable High to Data High-Z | — | 4 | — | 4 | — | 5 | — | 6 | ns |
| SETUP TIMES | | | | | | | | | | |
| t _{SA} | Address Setup Time | 2.2 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| t _{SS} | Address Status Setup Time | 2.2 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| t _{SD} | Data in Setup Time | 2.2 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| t _{SW} | Write Setup Time | 2.2 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| t _{SAV} | Address Advance Setup Time | 2.2 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| t _{SC} | Chip Enable/Select Setup Time | 2.2 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| HOLD TIMES | | | | | | | | | | |
| t _{HA} | Address Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HS} | Address Status Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HD} | Data In Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HW} | Write Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HAV} | Address Advance Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| t _{HC} | Chip Enable/Select Hold Time | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| SLEEP MODE AND CONFIGURATION PARAMETERS | | | | | | | | | | |
| t _{ZZPW} | ZZ Pulse Width | 100 | — | 100 | — | 100 | — | 100 | — | ns |
| t _{ZZR} ⁽³⁾ | ZZ Recovery Time | 100 | — | 100 | — | 100 | — | 100 | — | ns |
| t _{CFG} ⁽⁴⁾ | Configuration Set-up Time | 34 | — | 40 | — | 50 | — | 50 | — | ns |

3619 tbl 15

NOTES:

1. Measured as HIGH above 2.0V and LOW below 0.8V.
2. Transition is measured ± 200 mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{\text{LBO}}$ input. $\overline{\text{LBO}}$ is a static input and must not change during normal operation.
5. The 71V632SA4 speed grade corresponds to a t_{CD} of 4.5ns.
6. 0°C to +70°C temperature range only.

Timing Waveform of Pipelined Read Cycle^(1,2)

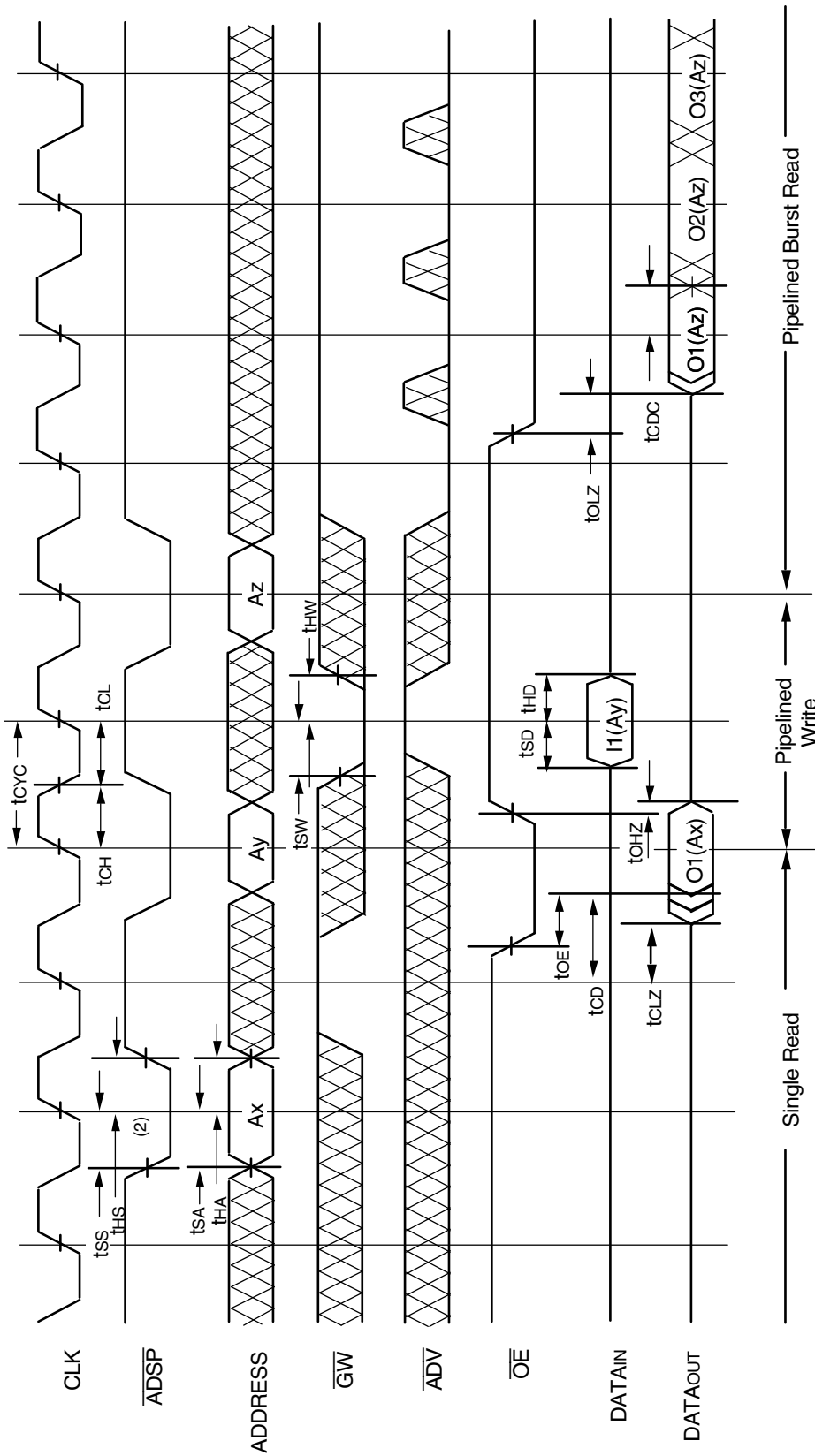


3619 drw 06

NOTES:

1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay. O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. Z \bar{Z} input is LOW and LBO is Don't Care for this cycle.
3. CS0 limiting transitions are identical but inverted to the $\bar{C}\bar{E}$ and $\bar{C}\bar{S}1$ signals. For example, when $\bar{C}\bar{E}$ and $\bar{C}\bar{S}1$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Combined Pipelined Read and Write Cycles^(1,2,3)

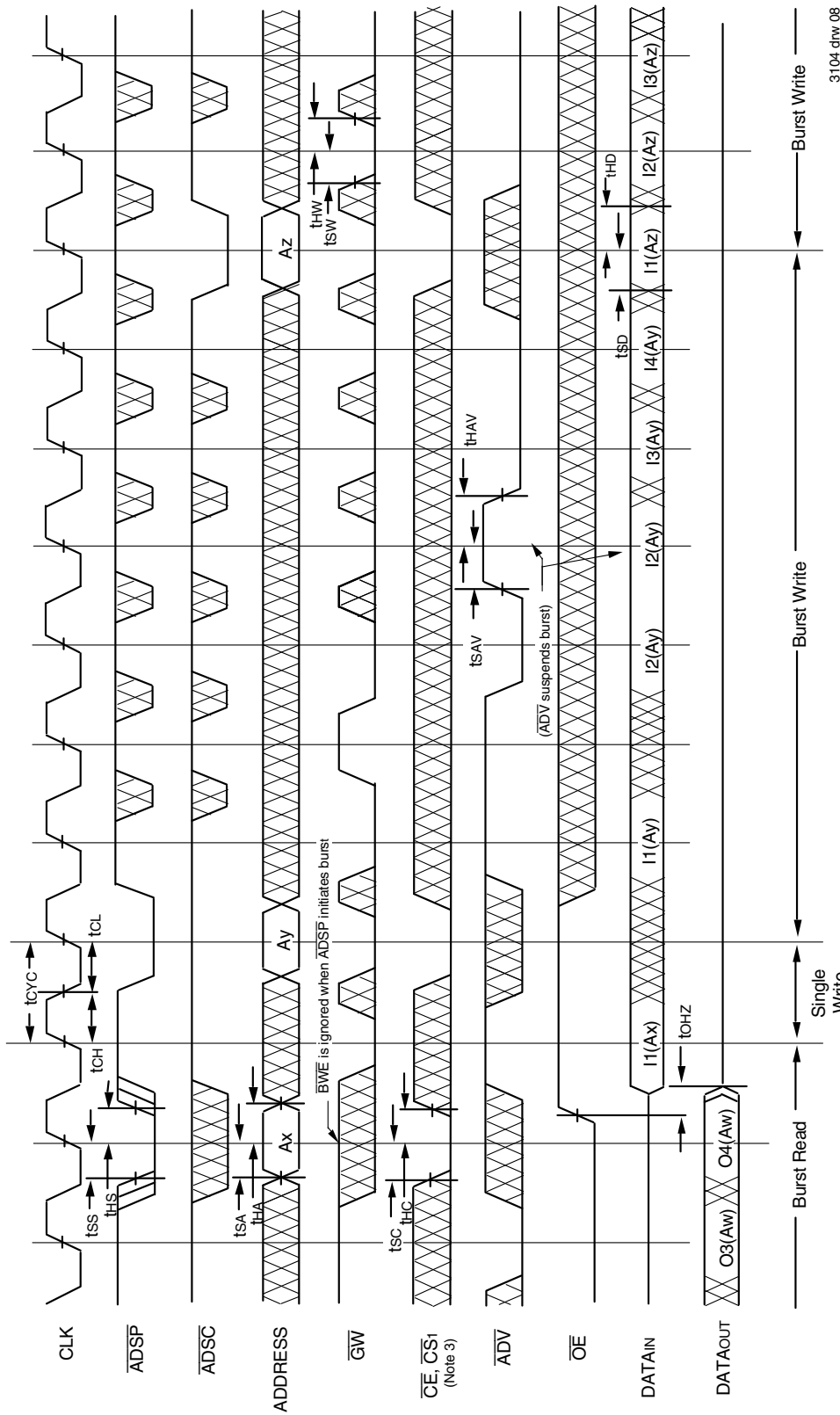


3619 d1w 07

NOTES:

1. Device is selected through entire cycle: \overline{CE} and $\overline{CS1}$ are LOW, $\overline{CS0}$ is HIGH.
2. ZZ input is LOW and LBO is Don't Care for this cycle.
3. O1(Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay. O1 (Az) represents the first output from the external addresses Az; O2(Az) represents the next output data in the burst sequence of the base address Az, etc. where Ao and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.

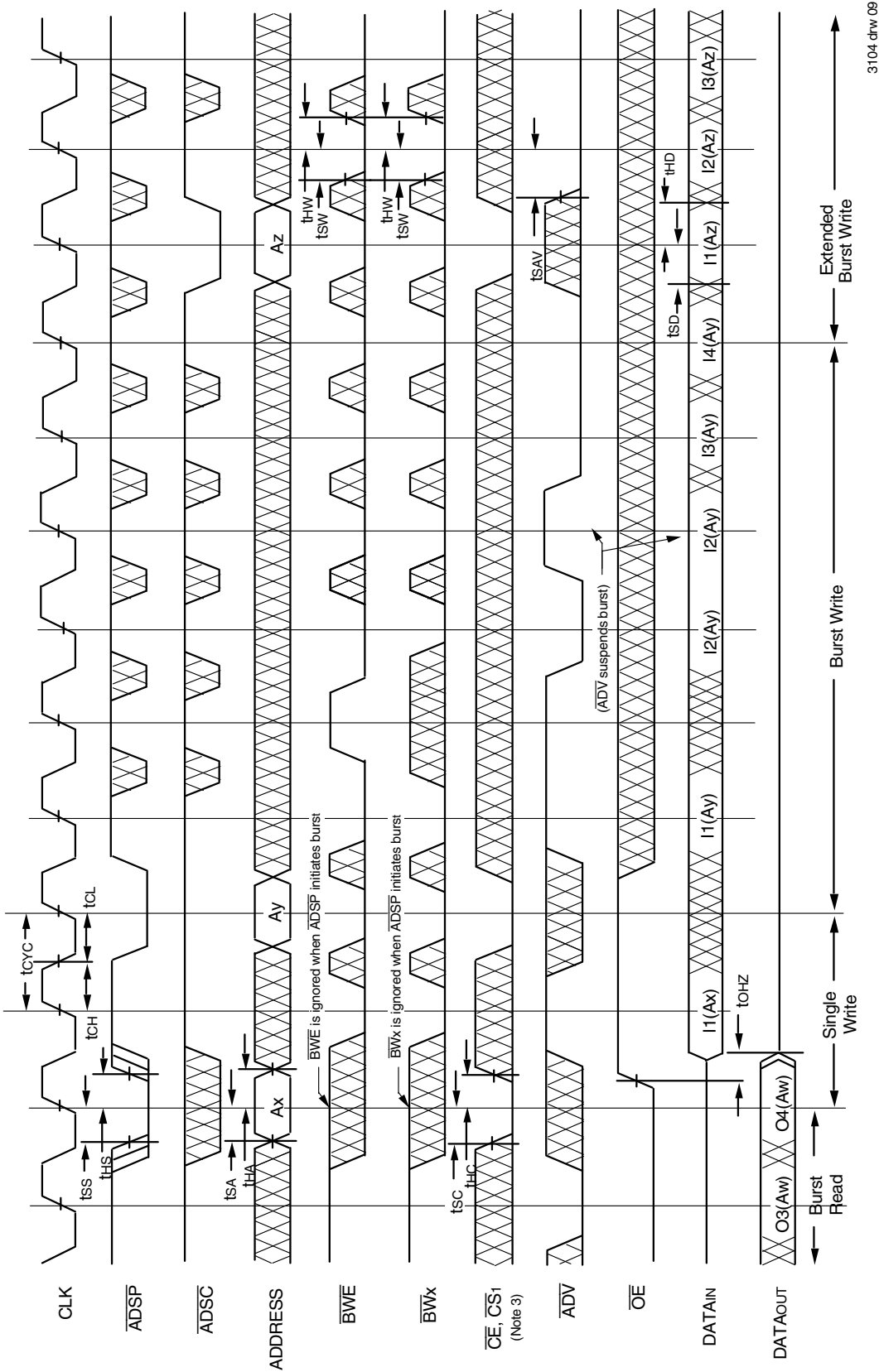
Timing Waveform of Write Cycle No. 1 — **GW** Controlled^(1,2,3)



NOTES:

1. Z \bar{Z} input is LOW, \overline{BWE} is HIGH, and \overline{LBO} is Don't Care for this cycle.
2. $O4(Aw)$ represents the final output data in the burst sequence of the base address Aw . $I1(Ax)$ represents the first input from the external address Ax . $I1(Ay)$ represents the first input from the external address Ay . $I1(Ay)$ and $A1$ are advancing in the sequence defined by the state of the \overline{LBO} input. In the case of input $I2(Ay)$ this data is valid for two cycles because \overline{ADV} is high and has suspended the burst.
3. $\overline{CS0}$ timing transitions are identical but inverted to the \overline{CE} and $\overline{CS1}$ signals. For example, when \overline{CE} and $\overline{CS1}$ are LOW on this waveform, $\overline{CS0}$ is HIGH.

Timing Waveform of Write Cycle No. 2 — Byte Controlled^(1,2,3)

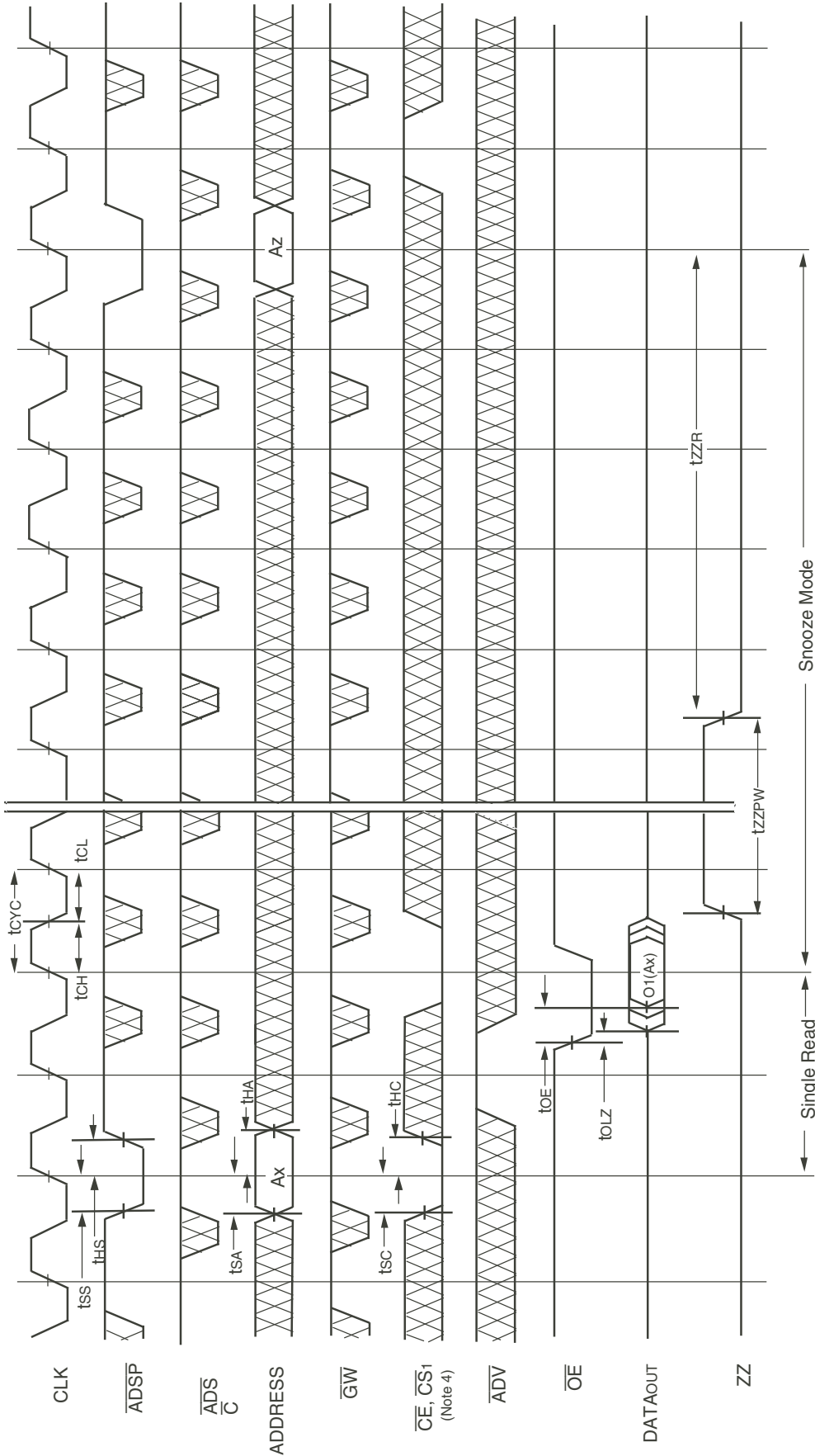


3104 drw 09

NOTES:

1. Z \bar{Z} input is LOW, $\overline{G\bar{W}}$ is HIGH, and \overline{LBO} is Don't Care for this cycle.
2. O4(Aw) represents the final output data in the burst sequence of the base address Aw. I1(Ax) represents the first input from the external address Ay. I2(Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the \overline{LBO} input. In the case of input I2(Ay) this data is valid for two cycles because ADV is high and has suspended the burst.
3. CS0 limiting transitions are identical but inverted to the \overline{CE} and $\overline{CS1}$ signals. For example, when \overline{CE} and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Sleep (ZZ) and Power-Down Modes^(1,2,3)

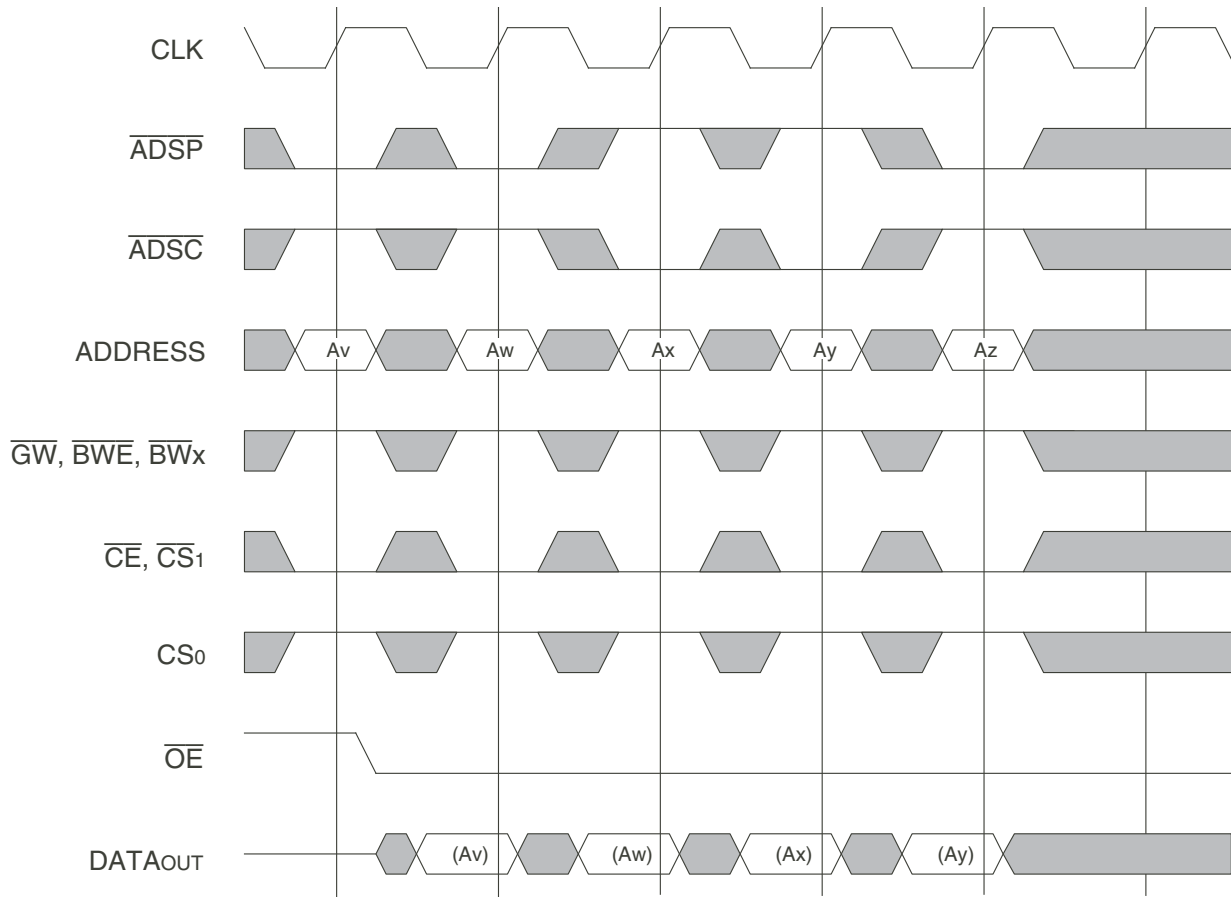


3104 drw 10

NOTES:

1. Device must power up in deselected Mode.
2. LBO input is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS0 limiting transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Non-Burst Read Cycle Timing Waveform

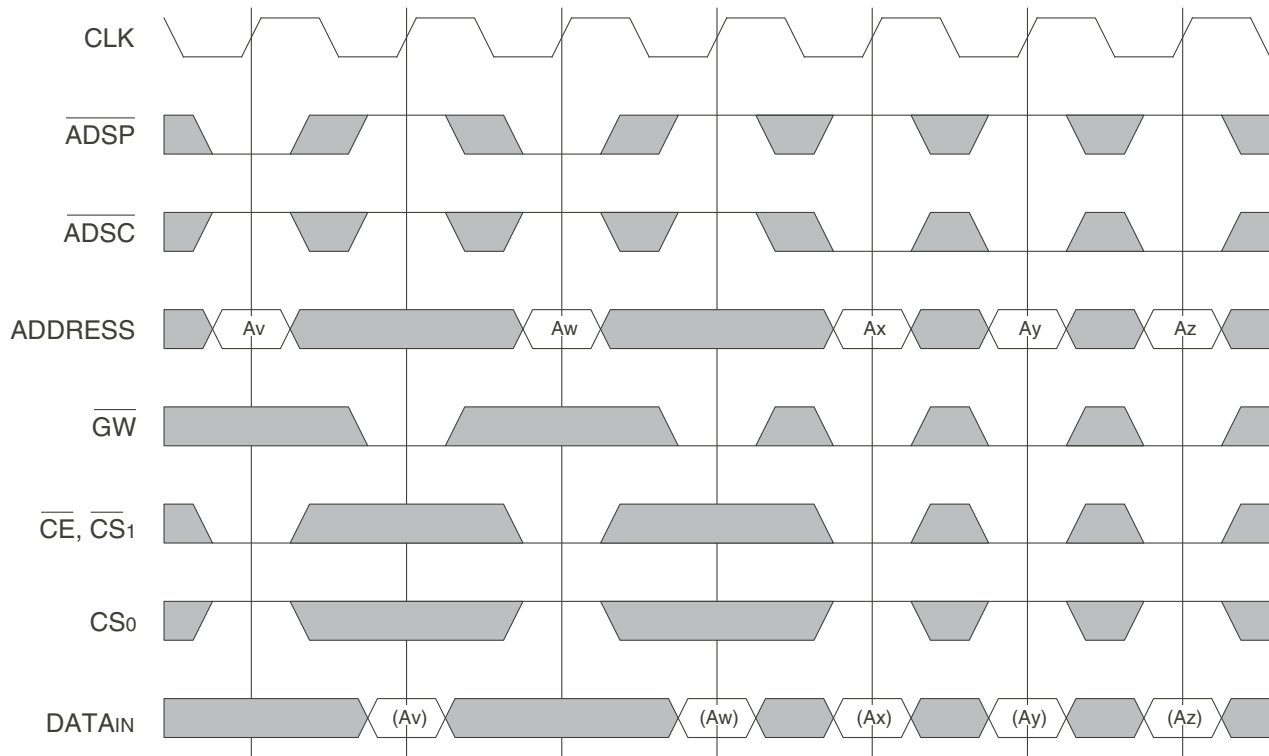


3619 drw 11

NOTES:

1. \overline{ZZ} input is LOW, \overline{ADV} is HIGH and \overline{LBO} is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, \overline{ADSP} and \overline{ADSC} function identically and are therefore interchangeable.

Non-Burst Write Cycle Timing Waveform

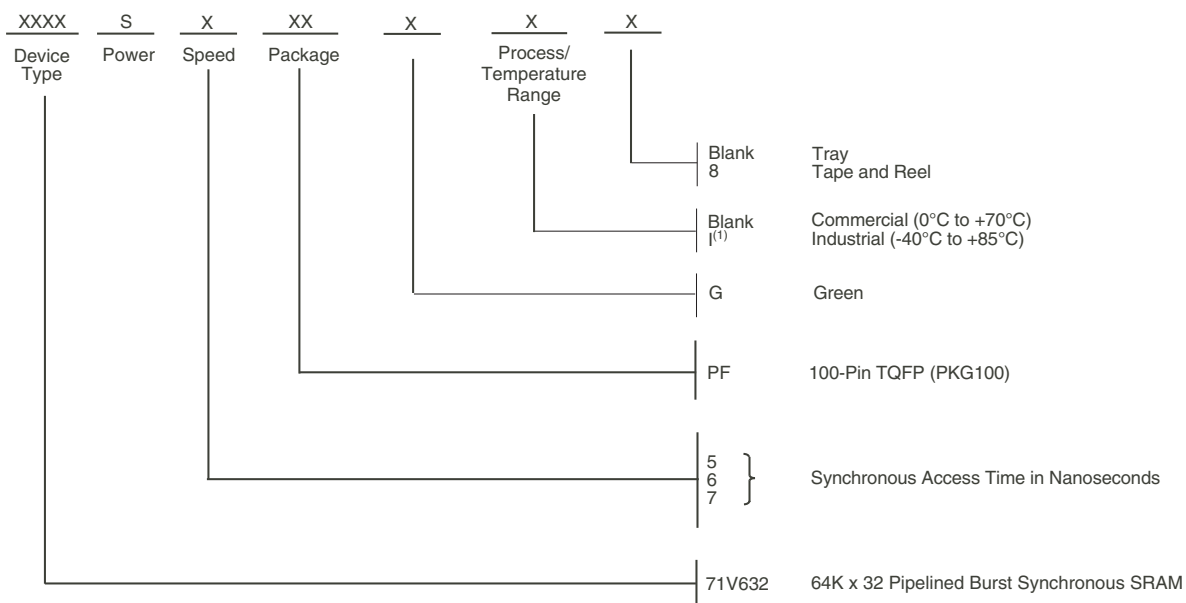


3619 drw 12

NOTES:

1. ZZ input is LOW, \overline{ADV} and \overline{OE} are HIGH, and $\overline{LB0}$ is Don't Care for this cycle.
2. (A_x) represents the data for address A_x , etc.
3. Although only \overline{GW} writes are shown, the functionality of \overline{BWE} and \overline{BWx} together is the same as \overline{GW} .
4. For write cycles, \overline{ADSP} and \overline{ADSC} have different limitations.

Ordering Information



3619 drw 13

NOTES:

- Contact your local sales office for industrial temp range for other speeds, packages and powers.

| Part Number | Speed in Megahertz | t _{cd} Parameter | Clock Cycle Time |
|-------------|--------------------|---------------------------|------------------|
| 71V632S5PF | 100 MHz | 5 ns | 10 ns |
| 71V632S6PF | 83 MHz | 6 ns | 12 ns |
| 71V632S7PF | 66 MHz | 7 ns | 15 ns |

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Orderable Part Information

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| 5 | 71V632S5PFGI | PKG100 | TQFP | I |
| | 71V632S5PFGI8 | PKG100 | TQFP | I |
| 6 | 71V632S6PFGI | PKG100 | TQFP | I |
| | 71V632S6PFGI8 | PKG100 | TQFP | I |
| 7 | 71V632S7PFG | PKG100 | TQFP | C |
| | 71V632S7PFG8 | PKG100 | TQFP | C |
| | 71V632S7PFGI | PKG100 | TQFP | I |
| | 71V632S7PFGI8 | PKG100 | TQFP | I |

Datasheet Document History

| | | |
|----------|--------------------|---|
| 09/09/99 | | Updated to new format |
| | Pg. 1, 8, 9, 17 | Revised speed offerings to 66–117MHz |
| | Pg. 15, 16 | Added non-burst read and write cycle timing diagrams |
| | Pg. 18 | Added Datasheet Document History |
| 09/30/99 | Pg. 1, 4, 8, 9, 17 | Added industrial temperature range offerings |
| 04/04/00 | Pg. 17 | Added 100pinTQFP package Diagram Outline |
| 08/09/00 | | Not recommended for new designs |
| 08/17/01 | | Removed "Not recommended for new designs" from the background on the datasheet |
| 02/28/07 | Pg. 18 | Added Z generation die step to data sheet ordering information. |
| 10/16/08 | Pg. 18 | Removed "IDT" from orderable part number. |
| 05/27/10 | Pg. 17 | Added "Restricted hazardous substance device" to the ordering information |
| 02/24/17 | Pg. 1 | Removed Z from device part number |
| | | Added green availability to features |
| | Pg. 5 | Update PK100-1 to package code PKG100 and restore overbars |
| | Pg. 14 | Restored Sleep (ZZ) Timing Waveform |
| | Pg. 16 | Restored Non-Burst Write Cycle Timing Waveform |
| | | Removed PSC Package Diagram |
| | Pg. 17 | Restored Ordering Information: Added Green, Tape & Reel, Tray and footnote indicators |
| | | Removed Z Die Stepping indicator in Ordering Information |
| 03/09/20 | Pg. 1 - 19 | Rebranded as Renesas datasheet |
| | Pg. 1 - 2 | Corrected typos |
| | Pg. 1 & 17 | Deleted obsolete A4 speed grade |
| | Pg. 17 | Added Orderable Part Information table |
| 03/04/22 | | 71V632 Datasheet changed to Obsolete Status |

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