



## DS26LV31T 3V Enhanced CMOS Quad Differential Line Driver

Check for Samples: [DS26LV31T](#)

### FEATURES

- Industrial Product Meets TIA/EIA-422-B (RS-422) and ITU-T V.11 Recommendation
- Military Product Conforms to TIA/EIA-422-B (RS-422)
- Interoperable with Existing 5V RS-422 Networks
- Industrial and Military temperature Range
- Guaranteed  $V_{OD}$  of 2V min Over Operating Conditions
- Balanced Output Crossover for Low EMI (Typical Within 40 mV of 50% Voltage Level)
- Low Power Design (330  $\mu$ W @ 3.3V static)
- ESD  $\geq$  7 kV on Cable I/O Pins (HBM)
- Guaranteed AC Parameter:
  - Maximum Driver Skew: 2 ns
  - Maximum Transition Time: 10 ns
- Pin Compatible with DS26C31
- Available in SOIC and CLGA Packaging

- Standard Microcircuit Drawing (SMD) 5962-98584

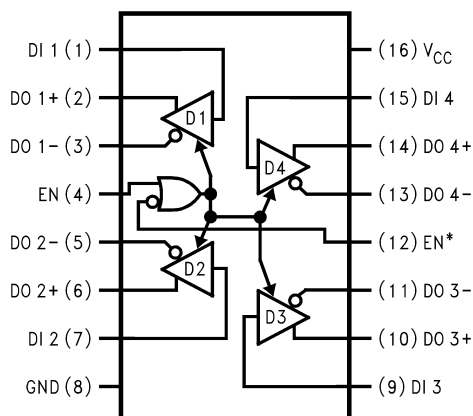
### DESCRIPTION

The DS26LV31T is a high-speed quad differential CMOS driver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS26LV31T features low static  $I_{CC}$  of 100  $\mu$ A MAX which makes it ideal for battery powered and power conscious applications.

Differential outputs have the same  $V_{OD}$  guarantee ( $\geq$ 2V) as the 5V version.

The EN and EN\* inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. Protection diodes protect all the driver inputs against electrostatic discharge. Outputs have enhanced ESD protection providing greater than 7 kV tolerance. The driver and enable inputs (DI, EN, EN\*) are compatible with low voltage LVTTTL and LVCMOS devices.

### Connection Diagram



**Figure 1. Dual-In-Line Package  
Top View  
See Package D (R-PDSO-G16)**



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Truth Table<sup>(1)</sup>

Enables		Input	Outputs	
EN	EN*	DI	DO+	DO-
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

- (1) L = Low logic state  
 X = Irrelevant  
 H = High logic state  
 Z = TRI-STATE



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

Supply Voltage ( $V_{CC}$ )	-0.5V to +7V
Enable Input Voltage (EN, EN*)	-0.5V to $V_{CC} + 0.5V$
Driver Input Voltage (DI)	-0.5V to $V_{CC} + 0.5V$
Clamp Diode Current	±20 mA
DC Output Current, per pin	±150 mA
Driver Output Voltage	
(Power Off: DO+, DO-)	-0.5V to +7V
Maximum Package Power Dissipation @+25°C	
D0016A Package	1226 mW
NAD0016A Package	1119 mW
Derate D0016A Package 9.8 mW/°C above +25°C	
Derate NAD0016A Package 7.5 mW/°C above +25°C	
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
ESD Ratings (HBM, 1.5 kΩ, 100 pF)	
Driver Outputs	≥7 kV
Other Pins	≥2.5 kV

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The [Electrical Characteristics](#) specifies conditions of device operation.  
 (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

### Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC}$ )	3.0	3.3	3.6	V
Operating Free Air Temperature Range ( $T_A$ )				
DS26LV31T	-40	+25	+85	°C
DS26LV31W	-55	+25	+125	°C
Input Rise and Fall Time			500	ns

**Electrical Characteristics<sup>(1) (2)</sup>**

Over supply voltage and operating temperature ranges, unless otherwise specified

Parameter		Test Conditions		Pin	Min	Typ	Max	Units
V <sub>OD1</sub>	Output Differential Voltage	R <sub>L</sub> = ∞ (No Load)		DO+, DO-		3.3	4	V
V <sub>OD2</sub>	Output Differential Voltage	R <sub>L</sub> = 100Ω (Figure 2)			2	2.6		V
ΔV <sub>OD2</sub>	Change in Magnitude of Output Differential Voltage	I <sub>O</sub> ≥ 20 mA			-400	7	400	mV
V <sub>OD3</sub>	Output Differential Voltage	R <sub>L</sub> = 3900Ω (V.11) Figure 2 and <sup>(3)</sup>				3.2	3.6	V
V <sub>OC</sub>	Common Mode Voltage	R <sub>L</sub> = 100Ω (Figure 2)				1.5	2	V
ΔV <sub>OC</sub>	Change in Magnitude of Common Mode Voltage				-400	6	400	mV
I <sub>OZ</sub>	TRI-STATE Leakage Current	V <sub>OUT</sub> = V <sub>CC</sub> or GND Drivers Disabled				±0.5	±20	μA
I <sub>SC</sub>	Output Short Circuit Current	V <sub>OUT</sub> = 0V V <sub>IN</sub> = V <sub>CC</sub> or GND <sup>(4)</sup>	T <sub>A</sub> = -40°C to +85°C		-40	-70	-150	mA
			T <sub>A</sub> = -55°C to +125°C <sup>(5)</sup>		-30		-160	mA
I <sub>OFF</sub>	Output Leakage Current	V <sub>CC</sub> = 0V, V <sub>OUT</sub> = 3V or 6V				0.03	100	μA
		V <sub>CC</sub> = 0V, V <sub>OUT</sub> = -0.25V	T <sub>A</sub> = -40°C to +85°C			-0.08	-100	μA
			T <sub>A</sub> = -55°C to +125°C				-200	μA
V <sub>IH</sub>	High Level Input Voltage			DI, EN, EN*	2.0		V <sub>CC</sub>	V
V <sub>IL</sub>	Low Level Input Voltage				GND		0.8	V
I <sub>IH</sub>	High Level Input Current	V <sub>IN</sub> = V <sub>CC</sub>					10	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>IN</sub> = GND			-10			μA
V <sub>CL</sub>	Input Clamp Voltage	I <sub>IN</sub> = -18 mA					-1.5	V
I <sub>CC</sub>	Power Supply Current	No Load, V <sub>IN</sub> (all) = V <sub>CC</sub> or GND			T <sub>A</sub> = -40°C to +85°C	V <sub>CC</sub>		100
				T <sub>A</sub> = -55°C to +125°C				125

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages V<sub>OD1</sub>, V<sub>OD2</sub>, V<sub>OD3</sub>.
- (2) All typicals are given for V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C.
- (3) This specification limit is for compliance with TIA/EIA-422-B and ITU-T V.11.
- (4) Only one output shorted at a time. The output (true or complement) is configured High.
- (5) This parameter does not meet the TIA/EIA-422-B specification.

**Switching Characteristics - Industrial<sup>(1) (2)</sup>**

Over supply voltage and -40°C to +85°C operating temperature range, unless otherwise specified

Parameter		Test Conditions		Min	Typ	Max	Units
t <sub>PHLD</sub>	Differential Propagation Delay High to Low	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 50 pF (Figure 3 and Figure 4)		6	10.5	16	ns
t <sub>PLHD</sub>	Differential Propagation Delay Low to High			6	11	16	ns
t <sub>SKD</sub>	Differential Skew (same channel)  t <sub>PHLD</sub> - t <sub>PLHD</sub>				0.5	2.0	ns
t <sub>SK1</sub>	Skew, Pin to Pin (same device)				1.0	2.0	ns
t <sub>SK2</sub>	Skew, Part to Part <sup>(3)</sup>				3.0	5.0	ns
t <sub>TLH</sub>	Differential Transition Time Low to High (20% to 80%)				4.2	10	ns
t <sub>THL</sub>	Differential Transition Time High to Low (80% to 20%)				4.7	10	ns
t <sub>PHZ</sub>	Disable Time High to Z			(Figure 5 Figure 6)			12
t <sub>PLZ</sub>	Disable Time Low to Z				9	20	ns

- (1) f = 1 MHz, t<sub>r</sub> and t<sub>f</sub> ≤ 6 ns, 10% to 90%.
- (2) See TIA/EIA-422-B specifications for exact test conditions.
- (3) Devices are at the same V<sub>CC</sub> and within 5°C within the operating temperature range

### Switching Characteristics - Industrial <sup>(1)</sup> <sup>(2)</sup> (continued)

Over supply voltage and -40°C to +85°C operating temperature range, unless otherwise specified

Parameter		Test Conditions	Min	Typ	Max	Units
t <sub>PZH</sub>	Enable Time Z to High			22	32	ns
t <sub>PZL</sub>	Enable Time Z to Low			22	32	ns
f <sub>max</sub>	Maximum Operating Frequency <sup>(4)</sup>		32			MHz

(4) All channels switching, output duty cycle criteria is 40%/60% measured at 50%. This parameter is guaranteed by design and characterization.

### Switching Characteristics - Military <sup>(1)</sup> <sup>(2)</sup>

Over supply voltage and -55°C to +125°C operating temperature range, unless otherwise specified

Parameter		Test Conditions	Min	Max	Units
t <sub>PHLD</sub>	Differential Propagation Delay High to Low	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 50 pF (Figure 3 Figure 4)  (Figure 5 Figure 6)	5	25	ns
t <sub>PLHD</sub>	Differential Propagation Delay Low to High		5	25	ns
t <sub>SKD</sub>	Differential Skew (same channel)  t <sub>PHLD</sub> - t <sub>PLHD</sub>			5.0	ns
t <sub>SK1</sub>	Skew, Pin to Pin (same device)			5.0	ns
t <sub>PHZ</sub>	Disable Time High to Z			35	ns
t <sub>PLZ</sub>	Disable Time Low to Z			35	ns
t <sub>PZH</sub>	Enable Time Z to High			40	ns
t <sub>PZL</sub>	Enable Time Z to Low			40	ns

(1) f = 1 MHz, t<sub>r</sub> and t<sub>f</sub> ≤ 6 ns, 10% to 90%.

(2) See TIA/EIA-422-B specifications for exact test conditions.

PARAMETER MEASUREMENT INFORMATION

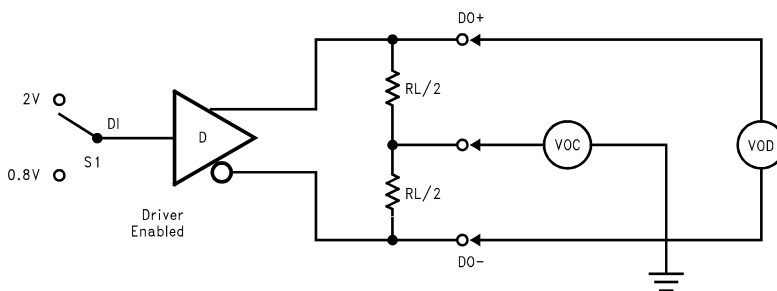


Figure 2. Differential Driver DC Test Circuit

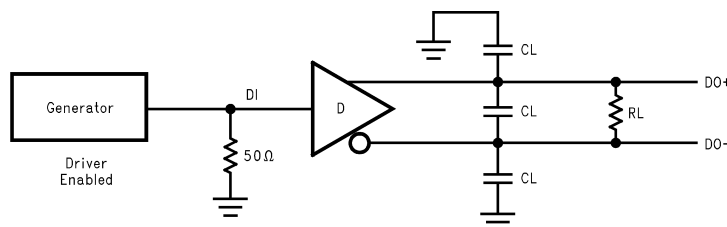
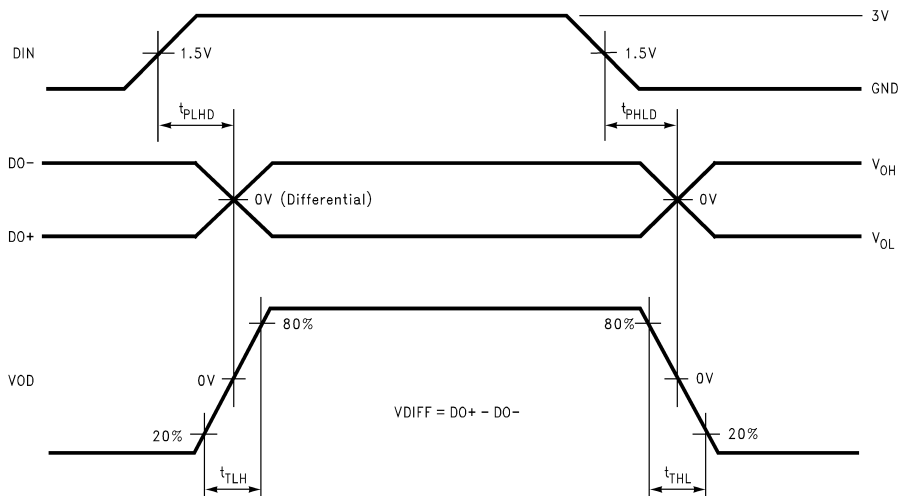
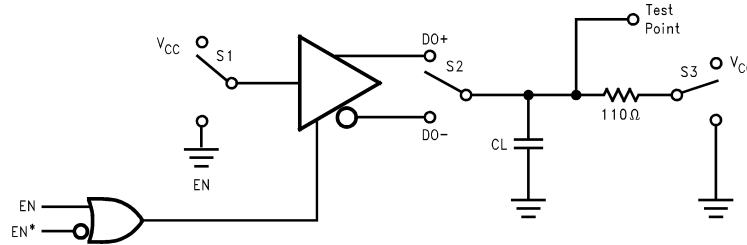


Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit



- A. Generator waveform for all tests unless otherwise specified:  $f = 1 \text{ MHz}$ , Duty Cycle = 50%  $Z_0 = 50\Omega$ ,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10$ .
- B.  $C_L$  includes probe and fixture capacitance.

Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms



If EN is the input, then EN\* = High  
 If EN\* is the input, then EN = Low

Figure 5. Driver Single-Ended TRI-STATE Test Circuit

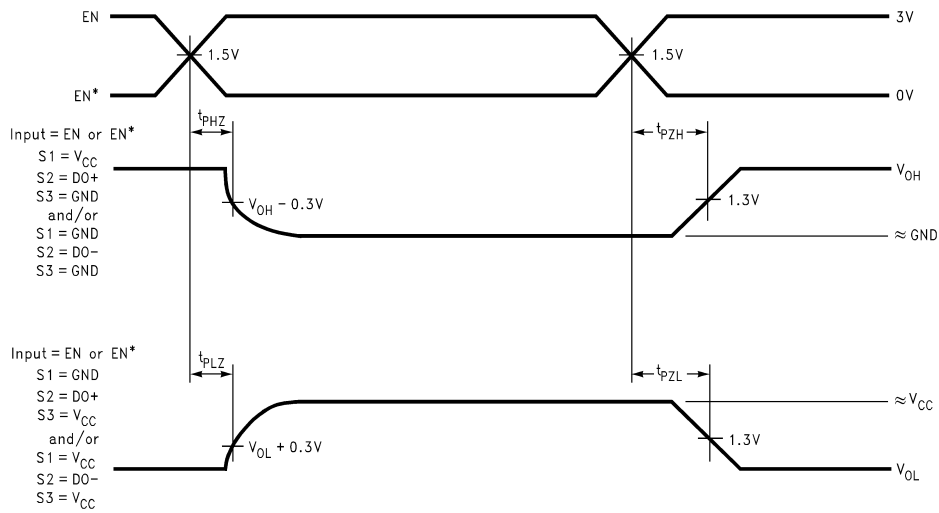


Figure 6. Driver Single-Ended TRI-STATE Waveforms

## Typical Application Information

General application guidelines and hints for differential drivers and receivers may be found in the following application notes:

- AN-214
- AN-457
- AN-805
- AN-847
- AN-903
- AN-912
- AN-916

### Power Decoupling Recommendations:

Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1  $\mu$ F in parallel with 0.01  $\mu$ F at the power supply pin. A 10  $\mu$ F or greater solid tantalum or electrolytic should be connected at the power entry point on the printed circuit board.

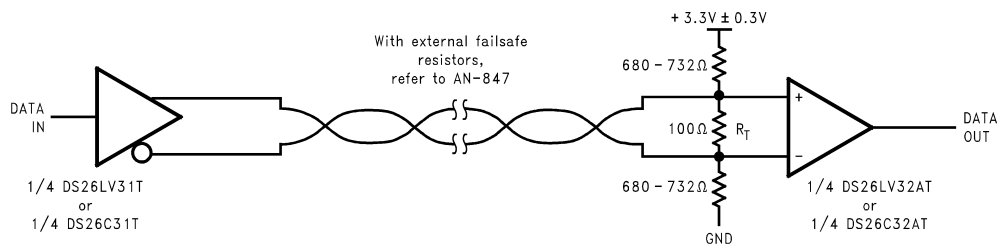
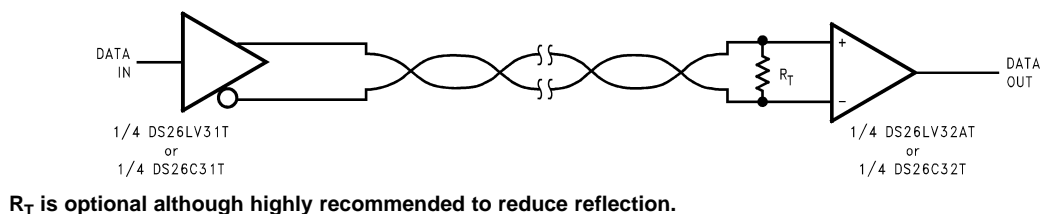


Figure 7. Typical Driver Connection

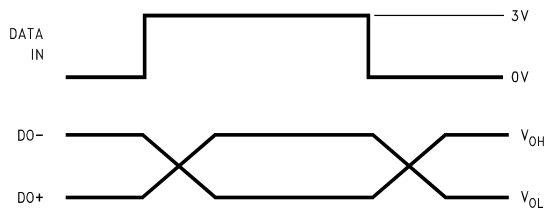


Figure 8. Typical Driver Output Waveforms

## REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">7</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS26LV31TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26LV31 TM	<a href="#">Samples</a>
DS26LV31TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26LV31 TM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26LV31TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS26LV31TMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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