THE DATASHEET OF

DS26401NA2+

www.win-source.net 0086-755-83957316

DS26401
Octal T1/E1/J1 Framer

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26401 is an octal, software-selectable T1, E1 or J1 framer. It is composed of eight framer/formatters and a system (backplane) interface. Each framer has an HDLC controller that can be mapped to any DS0 or FDL (T1)/Sa (E1) bit. The DS26401 also includes a full-feature BERT device, which can be used with any of the eight T1/E1 ports, and an internal clock adapter useful for creating synchronous, high frequency backplane timing. The DS26401 is controlled through an 8-bit parallel port that can be configured for nonmultiplexed Intel or Motorola operation.

APPLICATIONS

Line Cards
Add-Drop Multiplexers
DSLAMs
Timing Systems
PBXs
Switches
Central Office Equipment
Routers
IMA
ATM
WAN Interface
Customer-Premise Equipment

Go to www.maxim-ic.com/telecom for a complete list of Telecommunications data sheets, evaluation kits, application notes, and software downloads.

FEATURES

- 8 Independent, Full-Featured T1/E1/J1 Framers/Formatters
- Independent Transmit and Receive Paths
- Flexible Signaling Extraction and Insertion
- Alarm Detection and Insertion
- Transmit Synchronizer
- AMI, B8ZS, HDB3, NRZ Line Coding
- Performance Monitor Counters
- BOC Message Controller (T1)
- Two-Frame Elastic Store Buffers for Each Transmitter and Receiver
- One HDLC Controller per Framer
- RAI-CI and AIS-CI Support
- Full-Feature BERT can be Mapped to Any Port
- Flexible TDM Backplane Supports Bus Rates from 1.544MHz to 16.384MHz
- Internal Clock Generator (CLAD) Supplies 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz
- JTAG Test Port
- Single 3.3V Supply with 5V Tolerant Inputs
- 17mm x 17mm, 256-Pin BGA (1.00mm Pitch)

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS26401	0°C to +70°C	256 BGA
DS26401N	-40°C to +85°C	256 BGA

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1. APPLICABLE STANDARDS

The DS26401 conforms to the applicable parts of the following standards.

SPECIFICATION	TITLE
ANSI	
T1.102-1993	*Digital Hierarchy—Electrical Interfaces*
T1.107-1995	*Digital Hierarchy—Formats Specification*
T1.231-1997	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.403-1999	*Network and Customer Installation Interfaces—DS1 Electrical Interface*
AT&T	
TR54016	*Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Superframe Format*
TR62411	*High Capacity Digital Service Channel Interface Specification*
ITU	
G.704, 1995	*Synchronous Frame Structures used at 1544, 6312, 2048, 8488, and 44,736 kbit/s Hierarchical Levels*
G.706, 1991	*Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704*
G.732, 1993	*Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s*
G.736, 1993	*Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s*
G.775, 1994	*Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria*
G.823, 1993	*The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048kbps Hierarchy*
I.431, 1993	*Primary Rate User-Network Interface—Layer 1 Specification*
O.151, 1992	*Error Performance Measuring Equipment Operating at the Primary Rate and Above*
O.161, 1988	*In-service code violation monitors for digital systems*
ETSI	
ETS 300 011, 1998	*Integrated Services Digital Network (ISDN); Primary rate User-Network Interface (UNI); Part 1: Layer 1 specification*
ETS 300 166, 1993	*Transmission and multiplexing; Physical/electrical characteristics of hierarchical digital interfaces for equipment using the 2048 kbit/s-based plesiochronous or synchronous digital hierarchies*
ETS 300 233, 1994	*Integrated Services Digital Network (ISDN); Access digital section for ISDN primary rate*
CTR 4, 1995	*Integrated Services Digital Network (ISDN); Attachment requirements for terminal equipment to connect to an ISDN using ISDN primary rate access*
I.432, 1993	*B-ISDN User-Network Interface—Physical Layer Specification–ITU-T*
CTR 12, 1993	*Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2048 kbit/s digital unstructured leased lines (D2048U) attachment requirements for terminal equipment interface*
CTR 13, 1996	*Business Telecommunications (BTC); 2048 kbit/s digital structured leased lines (D2048S); Attachment requirements for terminal equipment interface*
TTC	
JT-G.704, 1995	*Frame Structures on Primary and Secondary Hierarchical Digital Interfaces*
JTI.431, 1995	*ISDN Primary Rate User-Network Interface Layer 1 Specification*

2. FEATURES

2.1 Framer/Formatter

- Fully Independent Transmit and Receive Functionality
- Full Receive and Transmit Path Transparency
- T1 Framing Formats D4 and ESF per T1.403, and Expanded SLC-96 Support (TR-TSY-008)
- E1 FAS Framing and CRC-4 Multiframe per G.704/G.706 and G.732 CAS Multiframe
- Detailed Alarm and Status Reporting with Optional Interrupt Support
- Large Path and Line Error Counters for
  - T1: BPV, CV, CRC6, and Framing Bit Errors
  - E1: BPV, CV, CRC4, E-Bit, and Frame Alignment Errors
  - Timed or Manual Update Modes
- DS1 Idle Code Generation on a Per-Channel Basis in Both Transmit and Receive Paths
  - User-Defined
  - Digital Milliwatt
- ANSI T1.403-1998 Support
- G.965 V5.2 Link Detect
- Ability to Monitor One DS0 Channel in Both the Transmit and Receive Paths
- In-Band Repeating Pattern Generators and Detectors
  - Three Independent Detectors
  - Patterns from 1 to 8 bits or 16 bits in Length
- Bit Oriented Code (BOC) Support
- Flexible Signaling Support
  - Software- or Hardware-Based
  - Interrupt Generated on Change of Signaling Data
  - Signaling Debounce
  - Optional Receive Signaling Freeze on Loss of Frame (LOF), Loss of Signal (LOS), or Change-of-Frame Alignment
- Hardware Pins Provided to Indicate Loss of Frame, Loss of Signal, Loss-of-Transmit Clock (LOTC), or Signaling Freeze Condition
- Automatic RAI Generation to ETS 300 011 Specifications
- RAI-CI and AIS-CI Support
- Expanded Access to Sa and Si Bits
- Option to Extend Carrier Loss Criteria to a 1ms Period as per ETS 300 233
- Japanese J1 Support
  - Ability to Calculate and Check CRC6 According to the Japanese Standard
  - Ability to Generate Yellow Alarm According to the Japanese Standard

2.2 System Interface

- Independent Two-Frame Receive and Transmit Elastic Stores
  - Independent Control and Clocking
  - Controlled Slip Capability with Status
  - Minimum Delay Mode Supported
- Maximum Backplane Rate of 16.384MHz in IBO Mode
- Supports T1 to E1 Conversion
- Programmable Output Clocks for Fractional T1, E1, H0, and H12 Applications
- Interleaving PCM Bus Operation (IBO)
- Hardware Signaling Capability
  - Receive Signaling Reinsertion to a Backplane Multiframe Sync
  - Availability of Signaling in a Separate PCM Data Stream
  - Signaling Freezing
- Ability to Pass the T1 F-Bit Position Through the Elastic Stores in the 2.048MHz Backplane Mode
- User-Selectable Synthesized Clock Output

2.3 HDLC Controllers

- HDLC Engine (One per Framer):
  - Independent 64-byte Rx and Tx Buffers with Interrupt Support
  - Access FDL, Sa, or Single DS0 Channel
  - Compatible with Polled or Interrupt Driven Environments

2.4 Test and Diagnostics

- Global, Full-Feature BERT
  - Any Pseudo-Random Pattern Up to $2^{32} - 1$
  - Up to 32 Taps can be Used Simultaneously
  - User-Defined Repetitive Patterns Up to 512 Bytes in Length
  - Large, 48-Bit Error and Bit Counters
  - Map to Any Framer/DS0/FDL (T1) or Sa Bits (E1)
  - Programmable Error Insertion
- BPV Insertion
- F-Bit Corruption for Line Testing
- Loopbacks
  - Remote
  - Local
  - Per-Channel
- IEEE 1149.1 Support

2.5 Control Port

- 8-Bit Parallel Control Port
- Intel or Motorola Nonmultiplexed Support
- Flexible Status Registers Support Polled, Interrupt, or Hybrid Program Environments
- Software Reset Supported
- Hardware Reset Pin

3. BLOCK DIAGRAMS

Figure 3-1. Block Diagram

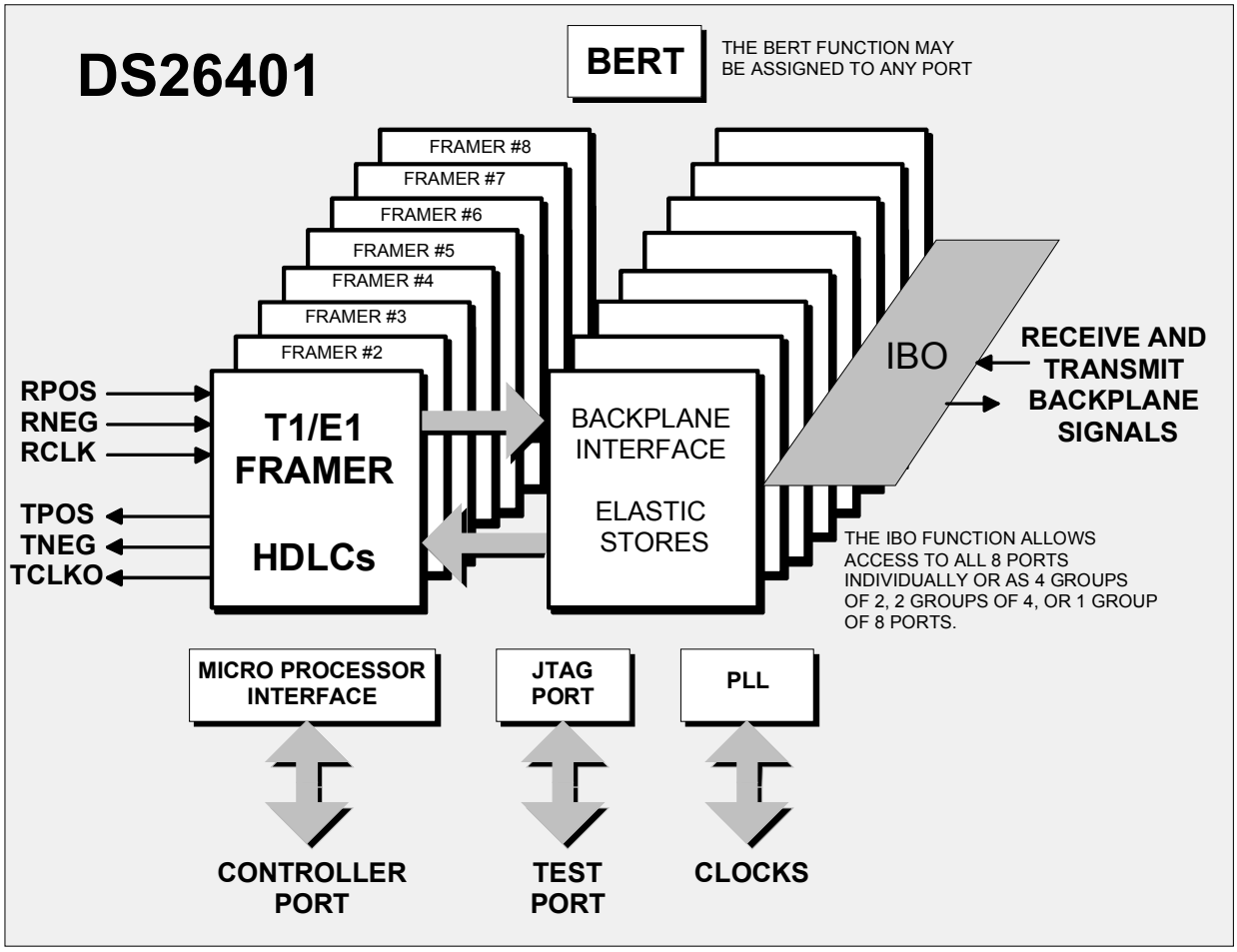


Figure 3-2. Typical PLL Connection

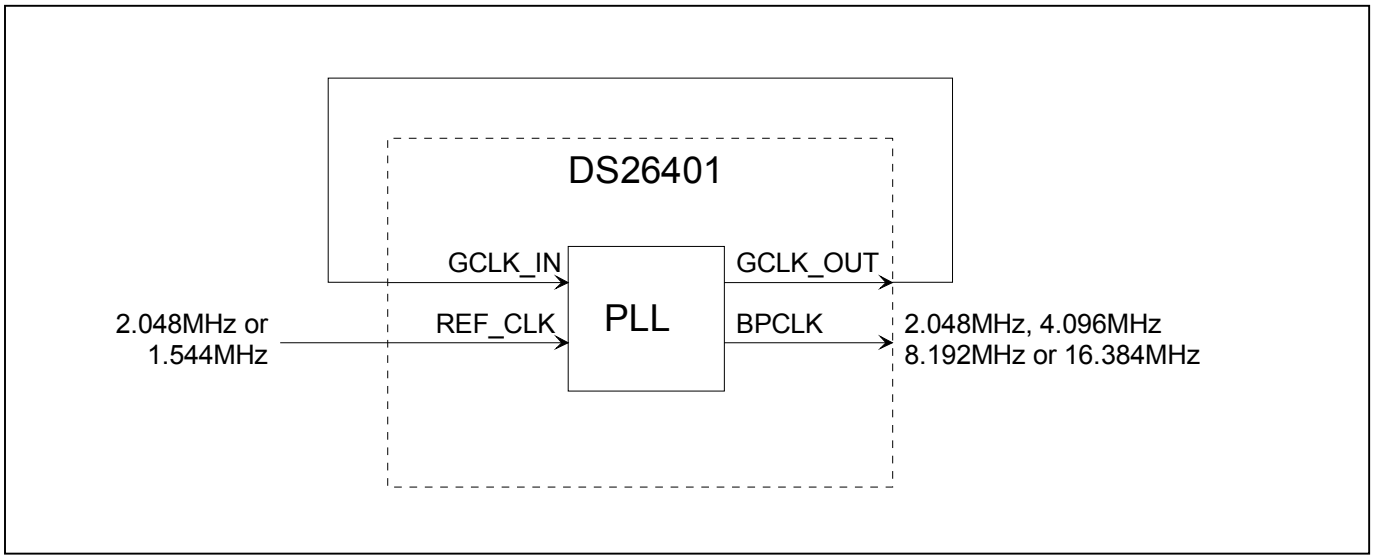


Figure 3-3. Typical Bipolar Network-Side Interface to Framers

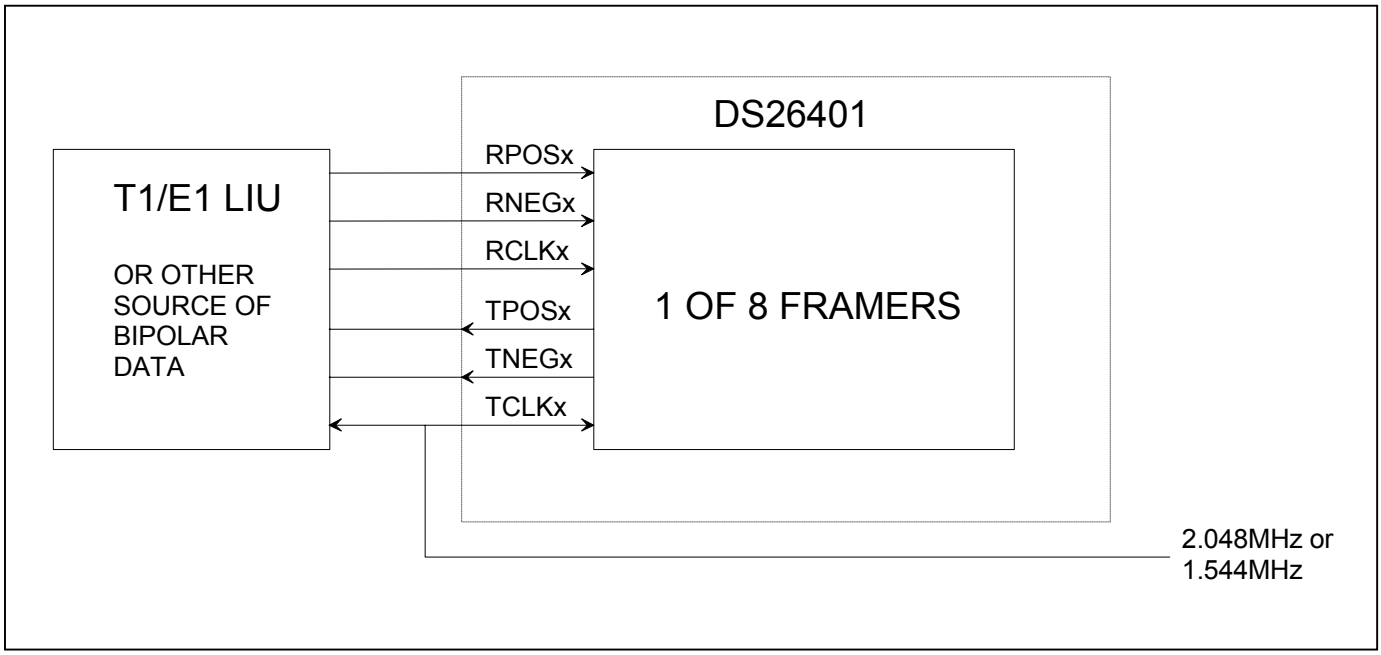
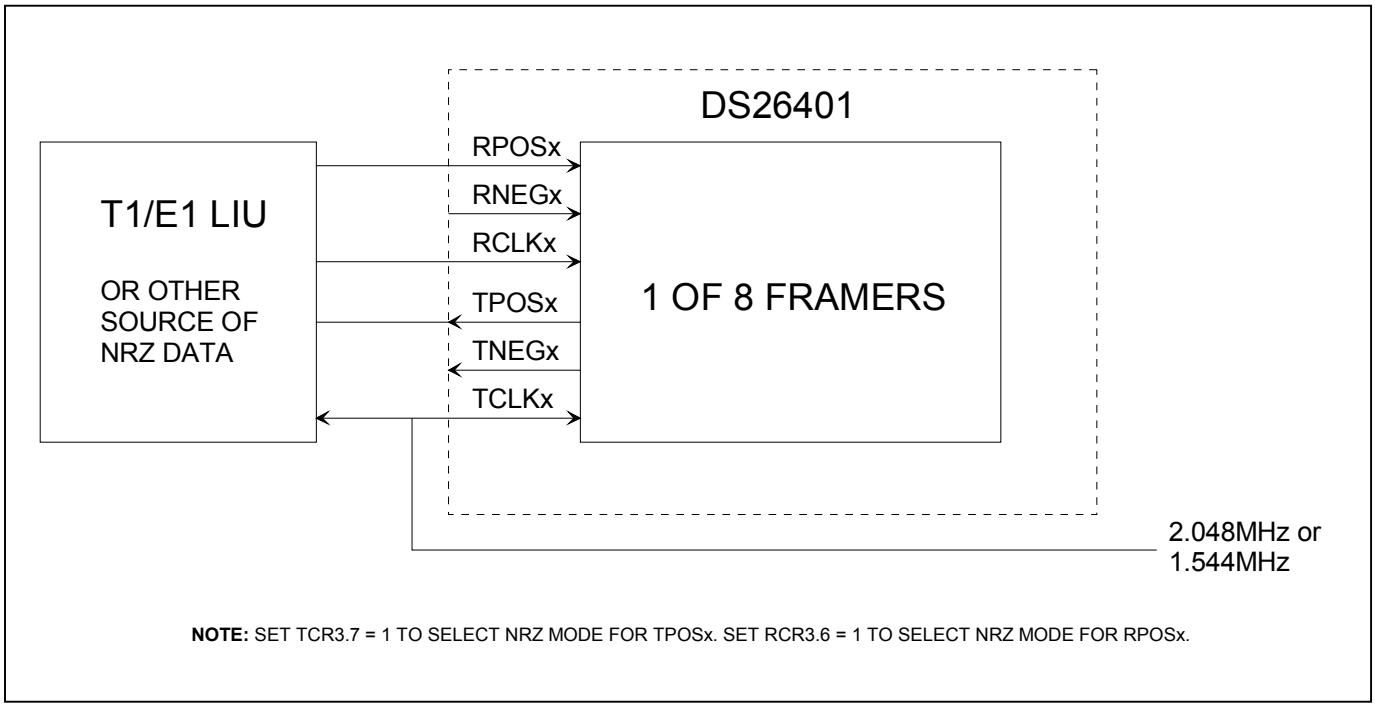


Figure 3-4. Typical NRZ Network-Side Interface to Framers



NOTE: SET TCR3.7 = 1 TO SELECT NRZ MODE FOR TPOSx. SET RCR3.6 = 1 TO SELECT NRZ MODE FOR RPOSx.

4. SIGNAL LIST (SORTED BY SIGNAL NAME)

PIN	NAME	TYPE	FUNCTION
B5	ADDR0	I	µP Address Bus Bit 0
A5	ADDR1	I	µP Address Bus Bit 1
C6	ADDR2	I	µP Address Bus Bit 2
E8	ADDR3	I	µP Address Bus Bit 3
A6	ADDR4	I	µP Address Bus Bit 4
B6	ADDR5	I	µP Address Bus Bit 5
D7	ADDR6	I	µP Address Bus Bit 6
C7	ADDR7	I	µP Address Bus Bit 7
A7	ADDR8	I	µP Address Bus Bit 8
D8	ADDR9	I	µP Address Bus Bit 9
C8	ADDR10	I	µP Address Bus Bit 10
A8	ADDR11	I	µP Address Bus Bit 11
F16	BPCLK	O	Programmable Backplane Clock
B2	BTS	I	Motorola or Intel Bus Type Select
B4	$\overline{CS}$	I	Chip Select (Active Low)
A1	DATA0	I/O	µP Data Bus Bit 0
C4	DATA1	I/O	µP Data Bus Bit 1
A2	DATA2	I/O	µP Data Bus Bit 2
B3	DATA3	I/O	µP Data Bus Bit 3
D5	DATA4	I/O	µP Data Bus Bit 4
A3	DATA5	I/O	µP Data Bus Bit 5
D6	DATA6	I/O	µP Data Bus Bit 6
A4	DATA7	I/O	µP Data Bus Bit 7
G16	GCLK_IN	I	Global Clock Input
G13	GCLK_OUT	O	Global Clock Output
R12	HIZE	I	High-Z Enable
E9	$\overline{INT}$	O	Interrupt (Active Low)
N10	JTCLK	I	JTAG Clock
T11	JTDI	I	JTAG Data Input
P11	JTDO	O	JTAG Data Output
T10	JTMS	I	JTAG Test Mode Select
R11	JTRST	I	JTAG Reset
B7, B13, D2, D15, E6, E14, F2, G14, J16, M9, N15, P2, P8, R5	N.C.		No Connect
B1	RCHBLK/CLK1	O	Rx Channel Block/Clock for Framer 1
H1	RCHBLK/CLK2	O	Rx Channel Block/Clock for Framer 2
L5	RCHBLK/CLK3	O	Rx Channel Block/Clock for Framer 3
P6	RCHBLK/CLK4	O	Rx Channel Block/Clock for Framer 4
N11	RCHBLK/CLK5	O	Rx Channel Block/Clock for Framer 5
M15	RCHBLK/CLK6	O	Rx Channel Block/Clock for Framer 6
E15	RCHBLK/CLK7	O	Rx Channel Block/Clock for Framer 7
A13	RCHBLK/CLK8	O	Rx Channel Block/Clock for Framer 8
C2	RCLK1	I	Rx Clock for Framer 1
H4	RCLK2	I	Rx Clock for Framer 2
L4	RCLK3	I	Rx Clock for Framer 3
N6	RCLK4	I	Rx Clock for Framer 4
M11	RCLK5	I	Rx Clock for Framer 5
L14	RCLK6	I	Rx Clock for Framer 6
E16	RCLK7	I	Rx Clock for Framer 7
C12	RCLK8	I	Rx Clock for Framer 8
E7	$\overline{RD}$ ($\overline{DS}$)	I	Read Strobe (Active Low)
F15	REF_CLK	I	Reference Clock (1.544MHz/2.048MHz)
T12	$\overline{RESET}$	I	Global Reset (Active Low)
E5	RF/RMSYNC1	O	Rx Frame/MF Sync for Framer 1
H3	RF/RMSYNC2	O	Rx Frame/MF Sync for Framer 2
N1	RF/RMSYNC3	O	Rx Frame/MF Sync for Framer 3
T5	RF/RMSYNC4	O	Rx Frame/MF Sync for Framer 4
T13	RF/RMSYNC5	O	Rx Frame/MF Sync for Framer 5

PIN	NAME	TYPE	FUNCTION
M16	RF/RMSYNC6	O	Rx Frame/MF Sync for Framer 6
F14	RF/RMSYNC7	O	Rx Frame/MF Sync for Framer 7
C13	RF/RMSYNC8	O	Rx Frame/MF Sync for Framer 8
D1	RLOF/LOTC1	O	RLOF or LOTC for Framer 1
K2	RLOF/LOTC2	O	RLOF or LOTC for Framer 2
T1	RLOF/LOTC3	O	RLOF or LOTC for Framer 3
P7	RLOF/LOTC4	O	RLOF or LOTC for Framer 4
P13	RLOF/LOTC5	O	RLOF or LOTC for Framer 5
K14	RLOF/LOTC6	O	RLOF or LOTC for Framer 6
C15	RLOF/LOTC7	O	RLOF or LOTC for Framer 7
D11	RLOF/LOTC8	O	RLOF or LOTC for Framer 8
F5	RLOS/RSIGF1	O	RLOS for Framer 1
J4	RLOS/RSIGF2	O	RLOS for Framer 2
R2	RLOS/RSIGF3	O	RLOS for Framer 3
T7	RLOS/RSIGF4	O	RLOS for Framer 4
T16	RLOS/RSIGF5	O	RLOS for Framer 5
K13	RLOS/RSIGF6	O	RLOS for Framer 6
C16	RLOS/RSIGF7	O	RLOS for Framer 7
A11	RLOS/RSIGF8	O	RLOS for Framer 8
C1	RNEG1	I	Rx Negative Data for Framer 1
H5	RNEG2	I	Rx Negative Data for Framer 2
M4	RNEG3	I	Rx Negative Data for Framer 3
R6	RNEG4	I	Rx Negative Data for Framer 4
N12	RNEG5	I	Rx Negative Data for Framer 5
L16	RNEG6	I	Rx Negative Data for Framer 6
D16	RNEG7	I	Rx Negative Data for Framer 7
B12	RNEG8	I	Rx Negative Data for Framer 8
D4	RPOS1	I	Rx Positive Data for Framer 1
J2	RPOS2	I	Rx Positive Data for Framer 2
P1	RPOS3	I	Rx Positive Data for Framer 3
T6	RPOS4	I	Rx Positive Data for Framer 4
T14	RPOS5	I	Rx Positive Data for Framer 5
L13	RPOS6	I	Rx Positive Data for Framer 6
G12	RPOS7	I	Rx Positive Data for Framer 7
E11	RPOS8	I	Rx Positive Data for Framer 8
E4	RSER1	O	Receive Serial Data for Framer 1
J1	RSER2	O	Receive Serial Data for Framer 2
R1	RSER3	O	Receive Serial Data for Framer 3
M7	RSER4	O	Receive Serial Data for Framer 4
R14	RSER5	O	Receive Serial Data for Framer 5
L15	RSER6	O	Receive Serial Data for Framer 6
F12	RSER7	O	Receive Serial Data for Framer 7
A12	RSER8	O	Receive Serial Data for Framer 8
D3	RSIG1	O	Receive Signaling Data for Framer 1
J3	RSIG2	O	Receive Signaling Data for Framer 2
N3	RSIG3	O	Receive Signaling Data for Framer 3
N7	RSIG4	O	Receive Signaling Data for Framer 4
T15	RSIG5	O	Receive Signaling Data for Framer 5
K12	RSIG6	O	Receive Signaling Data for Framer 6
F13	RSIG7	O	Receive Signaling Data for Framer 7
C11	RSIG8	O	Receive Signaling Data for Framer 8
E3	RSYNC1	I/O	Rx Frame/MF Sync for Framer 1
K1	RSYNC2	I/O	Rx Frame/MF Sync for Framer 2
M5	RSYNC3	I/O	Rx Frame/MF Sync for Framer 3
R7	RSYNC4	I/O	Rx Frame/MF Sync for Framer 4
R15	RSYNC5	I/O	Rx Frame/MF Sync for Framer 5
K16	RSYNC6	I/O	Rx Frame/MF Sync for Framer 6
E13	RSYNC7	I/O	Rx Frame/MF Sync for Framer 7
B11	RSYNC8	I/O	Rx Frame/MF Sync for Framer 8
C3	RSYSCLK1	I	Receive System Clock for Framer 1
H2	RSYSCLK2	I	Receive System Clock for Framer 2
N2	RSYSCLK3	I	Receive System Clock for Framer 3
M6	RSYSCLK4	I	Receive System Clock for Framer 4
R13	RSYSCLK5	I	Receive System Clock for Framer 5

PIN	NAME	TYPE	FUNCTION
L12	RSYSCLK6	I	Receive System Clock for Framer 6
H12	RSYSCLK7	I	Receive System Clock for Framer 7
D12	RSYSCLK8	I	Receive System Clock for Framer 8
F3	TCHBLK/CLK1	O	Tx Channel Block/Clock for Framer 1
L2	TCHBLK/CLK2	O	Tx Channel Block/Clock for Framer 2
R3	TCHBLK/CLK3	O	Tx Channel Block/Clock for Framer 3
N8	TCHBLK/CLK4	O	Tx Channel Block/Clock for Framer 4
P14	TCHBLK/CLK5	O	Tx Channel Block/Clock for Framer 5
J15	TCHBLK/CLK6	O	Tx Channel Block/Clock for Framer 6
A16	TCHBLK/CLK7	O	Tx Channel Block/Clock for Framer 7
C10	TCHBLK/CLK8	O	Tx Channel Block/Clock for Framer 8
F4	TCLK1	I	Tx Clock for Framer 1
L1	TCLK2	I	Tx Clock for Framer 2
T3	TCLK3	I	Tx Clock for Framer 3
R9	TCLK4	I	Tx Clock for Framer 4
P15	TCLK5	I	Tx Clock for Framer 5
J13	TCLK6	I	Tx Clock for Framer 6
B15	TCLK7	I	Tx Clock for Framer 7
B10	TCLK8	I	Tx Clock for Framer 8
G1	TCLKO1	O	Tx Clock Output for Framer 1
M3	TCLKO2	O	Tx Clock Output for Framer 2
P5	TCLKO3	O	Tx Clock Output for Framer 3
P10	TCLKO4	O	Tx Clock Output for Framer 4
M14	TCLKO5	O	Tx Clock Output for Framer 5
H13	TCLKO6	O	Tx Clock Output for Framer 6
D13	TCLKO7	O	Tx Clock Output for Framer 7
B8	TCLKO8	O	Tx Clock Output for Framer 8
P12	TESTPIN1	I	Used for factory tests (Note 1)
M10	TESTPIN2	I	Used for factory tests (Note 1)
G5	TNEG1	O	Tx Negative Data for Framer 1
L3	TNEG2	O	Tx Negative Data for Framer 2
P4	TNEG3	O	Tx Negative Data for Framer 3
T9	TNEG4	O	Tx Negative Data for Framer 4
P16	TNEG5	O	Tx Negative Data for Framer 5
H15	TNEG6	O	Tx Negative Data for Framer 6
A15	TNEG7	O	Tx Negative Data for Framer 7
B9	TNEG8	O	Tx Negative Data for Framer 8
F1	TPOS1	O	Tx Positive Data for Framer 1
J5	TPOS2	O	Tx Positive Data for Framer 2
N4	TPOS3	O	Tx Positive Data for Framer 3
M8	TPOS4	O	Tx Positive Data for Framer 4
N13	TPOS5	O	Tx Positive Data for Framer 5
J12	TPOS6	O	Tx Positive Data for Framer 6
E12	TPOS7	O	Tx Positive Data for Framer 7
A10	TPOS8	O	Tx Positive Data for Framer 8
G4	TSER1	I	Transmit Serial Data for Framer 1
M1	TSER2	I	Transmit Serial Data for Framer 2
N5	TSER3	I	Transmit Serial Data for Framer 3
P9	TSER4	I	Transmit Serial Data for Framer 4
N14	TSER5	I	Transmit Serial Data for Framer 5
H16	TSER6	I	Transmit Serial Data for Framer 6
B14	TSER7	I	Transmit Serial Data for Framer 7
C9	TSER8	I	Transmit Serial Data for Framer 8
G3	TSIG1	I	Transmit Signaling Data for Framer 1
M2	TSIG2	I	Transmit Signaling Data for Framer 2
T4	TSIG3	I	Transmit Signaling Data for Framer 3
R10	TSIG4	I	Transmit Signaling Data for Framer 4
M13	TSIG5	I	Transmit Signaling Data for Framer 5
H14	TSIG6	I	Transmit Signaling Data for Framer 6
C14	TSIG7	I	Transmit Signaling Data for Framer 7
A9	TSIG8	I	Transmit Signaling Data for Framer 8
E1	TSSYNC1	I	Transmit System Sync for Framer 1
K4	TSSYNC2	I	Transmit System Sync for Framer 2
T2	TSSYNC3	I	Transmit System Sync for Framer 3

PIN	NAME	TYPE	FUNCTION
T8	TSSYNC4	I	Transmit System Sync for Framer 4
R16	TSSYNC5	I	Transmit System Sync for Framer 5
J14	TSSYNC6	I	Transmit System Sync for Framer 6
D14	TSSYNC7	I	Transmit System Sync for Framer 7
D10	TSSYNC8	I	Transmit System Sync for Framer 8
G2	TSYNC1	I/O	Tx Frame/MF Sync for Framer 1
K5	TSYNC2	I/O	Tx Frame/MF Sync for Framer 2
R4	TSYNC3	I/O	Tx Frame/MF Sync for Framer 3
N9	TSYNC4	I/O	Tx Frame/MF Sync for Framer 4
N16	TSYNC5	I/O	Tx Frame/MF Sync for Framer 5
G15	TSYNC6	I/O	Tx Frame/MF Sync for Framer 6
A14	TSYNC7	I/O	Tx Frame/MF Sync for Framer 7
D9	TSYNC8	I/O	Tx Frame/MF Sync for Framer 8
E2	TSYSCLK1	I	Transmit System Clock for Framer 1
K3	TSYSCLK2	I	Transmit System Clock for Framer 2
P3	TSYSCLK3	I	Transmit System Clock for Framer 3
R8	TSYSCLK4	I	Transmit System Clock for Framer 4
M12	TSYSCLK5	I	Transmit System Clock for Framer 5
K15	TSYSCLK6	I	Transmit System Clock for Framer 6
B16	TSYSCLK7	I	Transmit System Clock for Framer 7
E10	TSYSCLK8	I	Transmit System Clock for Framer 8
F8, F9, G8, G9, H6, H7 H10, H11, J6, J7, J10, J11, K8, K9, L8, L9	V_{DD}	—	
F6, F7, F10, F11, G6, G7, G10, G11, H8, H9, J8, J9, K6, K7, K10, K11, L6, L7, L10, L11	V_{SS}	—	Signal
C5	WR (R/$\overline{W}$)	I	Write Strobe (Active Low)

Note 1: Connect to V_{SS}.

5. SIGNAL DESCRIPTIONS

5.1 Receive Framer Signals

Signal Name: **RPOS (1–8)**
Signal Description: **Receive Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLK for bipolar data to be clocked through the receive side framer. Data on RPOS and RNEG will typically be AMI, B8ZS, or HDB3 format bipolar data. RPOS can be used for unipolar (NRZ) data if enabled by the Input Data Format bit (IDF) at RCR3.7.

Signal Name: **RNEG (1–8)**
Signal Description: **Receive Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLK for bipolar data to be clocked through the receive side framer. Data on RPOS and RNEG will typically be AMI, B8ZS, or HDB3 format bipolar data. The RNEG input should be grounded when the DS26401 is set to receive unipolar (NRZ) data, enabled by the Input Data Format bit (IDF) at RCR3.7.

Signal Name: **RCLK (1–8)**
Signal Description: **Receive Clock**
Signal Type: **Input**
A 1.544MHz (T1) or 2.048MHz (E1) clock that is used to clock data through the receive side framer.

Signal Name: **RSER (1–8)**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Signal Name: **RSIG (1–8)**
Signal Description: **Receive Signaling Output**
Signal Type: **Output**
Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Signal Name: **RSYNC (1–8)**
Signal Description: **Receive Sync**
Signal Type: **Input/Output**
An extracted pulse, one RCLK wide that identifies either frame or multiframe boundaries. If set to output frame boundaries then RSYNC can be programmed to output doublewide pulses on signaling frames in T1 mode.

Signal Name: **RSYSCLK (1–8)**
Signal Description: **Receive System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, or 8.192MHz, or 16.384MHz receive backplane clock. Only used when the receive-side elastic store function is enabled. Should be tied low in applications that do not use the receive-side elastic store.

Signal Name: **RCHBLK/CLK (1–8)**
Signal Description: **Receive Channel Block/Clock**
Signal Type: **Output**
Pin can be configured to output either RCHBLK or RCHCLK. RCHBLK is a user programmable output that can be forced high or low during any of the 24 T1 or 32 E1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as fractional service, 384kbps, service, 768kbps, or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning.

RCHCLK is a 192 kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. Can also be programmed to output a gated bit clock useful for fractional services. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

Signal Name: **RLOF/LOTC (1–8)**
Signal Description: **Receive Loss of Frame/Loss of Transmit Clock**
Signal Type: **Output**
A dual function output that is controlled by the GCR1.5 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for approximately three clock periods.

Signal Name: **RLOS/RSIGF (1–8)**
Signal Description: **Receive Loss of Signal/Receive Signaling Freeze**
Signal Type: **Output**
A dual function output that is controlled by the GCR2.3 control bit. This pin can be programmed to toggle high when the framer detects a loss of signal condition, or when the signaling data is frozen via either automatic or manual intervention. Used to alert downstream equipment of the condition.

Signal Name: **RF/RMSYNC (1–8)**
Signal Description: **Receive Frame Sync/Receive Multiframe Sync**
Signal Type: **Output**
A dual function output controlled by the GCR2.2 control bit. RFSYNC is an extracted 8kHz pulse, one RCLK wide that identifies frame boundaries. RMSYNC is an extracted pulse, one RCLK wide (elastic store disabled) or one RSYSCLK wide (elastic store enabled), which identifies multiframe boundaries. When the receive elastic store is enabled, the RMSYNC signal indicates the multiframe sync on the system (backplane) side of the e-store. In E1 mode, will indicate either the CRC4 or CAS multiframe as determined by the RSMS2 control bit at RIOCR.1

5.2 Transmit Framer Signals

Signal Name: **TPOS (1–8)**
Signal Description: **Transmit Positive Data Output**
Signal Type: **Output**
Update on the rising edge of TCLK with the bipolar data out of the transmit side formatter. Can be programmed to source NRZ data via the output data format (TCR3.7) control bit.

Signal Name: **TNEG (1–8)**
Signal Description: **Transmit Negative Data Output**
Signal Type: **Output**
Update on the rising edge of TCLK with the bipolar data out of the transmit side formatter.

Signal Name: **TCLK (1–8)**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 1.544MHz or a 2.048MHz primary clock. Used to clock data through the transmit side formatter.

Signal Name: **TCLKO (1–8)**
Signal Description: **Transmit Clock Output**
Signal Type: **Output**
This clock is provided to simplify interface to a line interface unit (LIU). This signal is used to register the TPOS and TNEG outputs and is typically synchronous with the TCLK input. However, in framer and payload loopback applications this signal becomes synchronous with RCLK.

Signal Name: **TSER (1–8)**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Signal Name: **TSIG (1–8)**
Signal Description: **Transmit Signaling Input**
Signal Type: **Input**
When enabled, this input will sample signaling bits for insertion into outgoing PCM data stream. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.

Signal Name: **TSYNC (1–8)**
Signal Description: **Transmit Sync**
Signal Type: **Input / Output**
A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. This signal can also be programmed to output either a frame or multiframe pulse. If this pin is set to output pulses at frame boundaries, it can also be set to output doublewide pulses at signaling frames in T1 mode.

Signal Name: **TSSYNC (1–8)**
Signal Description: **Transmit System Sync**
Signal Type: **Input**
Only used when the transmit-side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit-side elastic store.

Signal Name: **TSYSCLK (1–8)**
Signal Description: **Transmit System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. Only used when the transmit-side elastic store function is enabled. Should be tied low in applications that do not use the transmit-side elastic store.

Signal Name: **TCHBLK/CLK (1–8)**
Signal Description: **Transmit Channel Block**
Signal Type: **Output**
A dual function pin. TCHBLK is a user programmable output that can be forced high or low during any of the channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as Fractional T1, Fractional E1, 384kbps (H0), 768kbps, or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning.

TCHCLK is a 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. Can also be programmed to output a gated bit clock useful for fractional services. Synchronous with TCLK when the transmit-side elastic store is disabled. Synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

5.3 Parallel Control Port

Signal Name: **ADDR[11:0]**
Signal Description: **Microprocessor Address Bus**
Signal Type: **Input**
This bus selects a specific register in the DS26401 during read/write access. ADDR11 is the MSB and ADDR0 is the LSB.

Signal Name: **DATA[7:0]**
Signal Description: **Microprocessor Data Bus**
Signal Type: **Input/Output**
This 8-bit, bidirectional data bus is used for read/write access of the DS26401 information and control registers. DATA7 is the MSB and DATA0 is the LSB.

Signal Name: $\overline{CS}$
Signal Description: **Chip Select**
Signal Type: **Input**
This active-low signal is used to qualify register read/write accesses. The $\overline{RD}$ and $\overline{WR}$ signals are qualified with $\overline{CS}$.

Signal Name: $\overline{RD}$ **(**$\overline{DS}$**)**
Signal Description: **Read Enable**
Signal Type: **Input**
This active-low signal along with $\overline{CS}$ qualifies read access to one of the DS26401 registers. The DS26401 drives the DATA bus with the contents of the addressed register while $\overline{RD}$ and $\overline{CS}$ are both low.

Signal Name: $\overline{WR}$ **(R/**$\overline{W}$**)**
Signal Description: **Write Enable**
Signal Type: **Input**
This active-low signal along with $\overline{CS}$ qualifies write access to one of the DS26401 registers. Data at DATA[7:0] is written into the addressed register at the rising edge of $\overline{WR}$ while $\overline{CS}$ is low.

Signal Name: $\overline{INT}$
Signal Description: **Interrupt**
Signal Type: **Output**
This active-low, open-drain output is asserted when an unmasked interrupt event is detected. $\overline{INT}$ is deasserted when all interrupts have been acknowledged and serviced.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Set high to select Motorola bus timing, low to select Intel bus timing. This pin controls the function of the $\overline{RD}$ ($\overline{DS}$), and $\overline{WR}$ (R/$\overline{W}$) pins. If BTS = 1, these pins assume the function listed in parentheses ().

5.4 System Interface

Signal Name: **REF_CLK**
Signal Description: **Reference Clock**
Signal Type: **Input**
A continuous T1 (1.544MHz) or E1 (2.048MHz) clock used to create GCLK_OUT and BPCLK.

Signal Name: **GCLK_OUT**
Signal Description: **Global Clock Output**
Signal Type: **Output**
This output clock is generated from the REF_CLK input and is a 45MHz clock. This pin is usually connected to GCLK_IN.

Signal Name: **GCLK_IN**
Signal Description: **Global Clock Input**
Signal Type: **Input**
Primary clock for internal state machines. Can be connected to GCLK_OUT, or provided by the user. The GCLK_IN frequency must be between 43MHz and 49MHz for proper operation.

Signal Name: **BPCLK**
Signal Description: **Backplane Clock**
Signal Type: **Output**
Programmable clock output created from REFCLK. Can be set to 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz.

Signal Name: $\overline{RESET}$
Signal Description: **System Reset**
Signal Type: **Input**
Active-low reset. Forcing this input low sets all internal registers to their default value.

Signal Name: **HIZE**
Signal Description: **High-Z Enable**
Signal Type: **Input**
Active high. Forcing this input high when the $\overline{RESET}$ and JTRST pins are low will hold all outputs in high-impedance mode.

5.5 Test

Signal Name: **JTRST**
Signal Description: **IEEE 1149.1 Test Reset**
Signal Type: **Input**
JTRST is used to asynchronously reset the test access port controller. After power-up, JTRST must be toggled from low to high. This action will set the device into the JTAG DEVICE ID mode. Pulling JTRST low restores normal device operation. JTRST is pulled high internally through a 10kΩ resistor operation. If boundary scan is not used, this pin should be held low.

Signal Name: **JTMS**
Signal Description: **IEEE 1149.1 Test Mode Select**
Signal Type: **Input**
This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10kΩ pullup resistor.

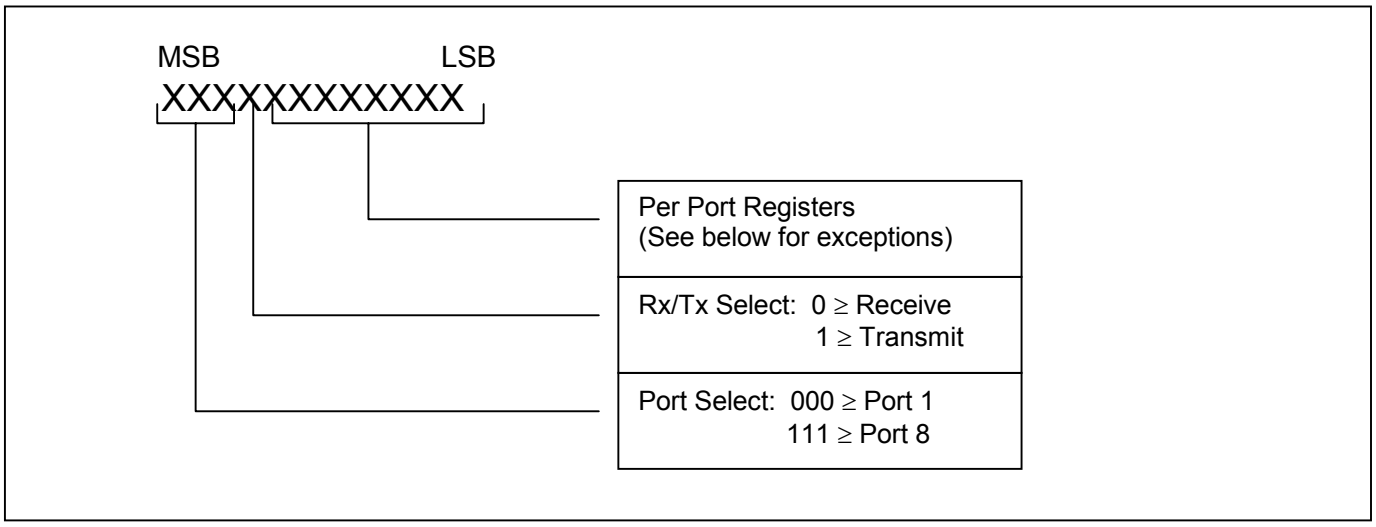
Signal Name: **JTCLK**
Signal Description: **IEEE 1149.1 Test Clock Signal**
Signal Type: **Input**
This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge.

Signal Name: **JTDI**
Signal Description: **IEEE 1149.1 Test Data Input**
Signal Type: **Input**
Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10kΩ pullup resistor.

Signal Name: **JTDO**
Signal Description: **IEEE 1149.1 Test Data Output**
Signal Type: **Output**
Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected.

6. REGISTER MAP

The DS26401 has an 8-bit μP control bus with 12 address bits. The address bits are structured as follows:



7. GLOBAL FUNCTIONS

7.1 Global Registers

ADDRESS	NAME	TYPE	FUNCTION	PAGE
0F0	GCR1	R/W	Global Control Register 1	25
0F1	GCR2	R/W	Global Control Register 2	26
0F2	—	—	Unused, must be set = 0 for proper operation	—
0F3	—	—	Unused, must be set = 0 for proper operation	—
0F4	—	—	Unused, must be set = 0 for proper operation	—
0F5	—	—	Unused, must be set = 0 for proper operation	—
0F6	—	—	Unused, must be set = 0 for proper operation	—
0F7	—	—	Unused, must be set = 0 for proper operation	—
0F8	IDR	R	Device ID Register	35
0F9	GSR1	R	Global Status Register 1	36
0FA	GSR2	R	Global Status Register 2	37
0FB	—	—	Unused, must be set = 0 for proper operation	—
0FC	—	—	Unused, must be set = 0 for proper operation	—
0FD	—	—	Unused, must be set = 0 for proper operation	—
0FE	—	—	Unused, must be set = 0 for proper operation	—
0FF	—	—	Unused, must be set = 0 for proper operation	—

7.2 Global Register Description and Operation

Register Name: **GCR1**
Register Description: **Global Control Register 1**
Register Address: **0F0h**

Bit #	7	6	5	4	3	2	1	0
Name	BBEDIM	BLOSIM	RLOFLTS	GIBO	REFCLKS	BWE	GCLE	GIPI
Default	0	0	0	0	0	0	0	0

Bit 0 / Global Interrupt Pin Inhibit (GIPI)
0 = Normal operation (interrupt pin ($\overline{INT}$) toggles low on an unmasked interrupt condition)
1 = Interrupt inhibit (interrupt pin ($\overline{INT}$) is forced high (inactive) when this bit is set)

Bit 1 / Global Counter Latch Enable (GCLE). A low-to-high transition on this bit, when enabled, latches the framer performance-monitor counters and the internal BERT counters. Each framer can be independently enabled to accept this input, as well as the BERT. This bit must be cleared and set again to perform another counter latch.

Bit 2 / Bulk Write Enable (BWE). When this bit is set, a port write to one of the octal ports is mapped into all 8 ports. This bit is useful for device initialization. It must be cleared before performing a read operation.
0 = Normal operation
1 = Bulk write is enabled

Bit 3 / Reference Clock-Frequency Select (REFCLKS). This bit sets the divider ratio of the internal clock generator depending on the frequency of the reference clock input.
0 = REF_CLK is 1.544MHz
1 = REF_CLK is 2.048MHz

Bit 4 / Ganged IBO Enable (GIBO). This bit is used to select either the internal mux for IBO operation or externally wire-OR operation. Normally this bit should be set = 0 and the internal mux is used.
0 = Use internal IBO mux
1 = Externally wire-OR TSERs and RSERs for IBO operation

Bit 5 / Receive Loss-of-Frame/Loss-of-Transmit Clock-Indication Select (RLOFLTS)
0 = RLOF/LOTCx pins indicate receive loss-of-frame
1 = RLOF/LOTCx pins indicate loss-of-transmit clock

Bit 6 / BERT Loss-of-Sync Interrupt Mask (BLOSIM)
0 = DS26401 does not generate an interrupt on $\overline{INT}$ for a BERT LOS
1 = DS26401 generates an interrupt on $\overline{INT}$ for a BERT LOS

Bit 7 / BERT Bit-Error-Detect Interrupt Mask (BBEDIM)
0 = DS26401 does not generate an interrupt on $\overline{INT}$ for a BERT bit-error detect
1 = DS26401 generates an interrupt on $\overline{INT}$ for a BERT bit-error detect

Register Name: **GCR2**
Register Description: **Global Control Register 2**
Register Address: **0F1h**

Bit #	7	6	5	4	3	2	1	0
Name	IBOMS1	IBOMS0	BPCLK1	BPCLK0	RLOSSFS	RFMSS	TCBCS	RCBCS
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive-Channel Block/Clock Select (RCBCS). This bit controls the function of all eight RCHBLK/CLK pins.

0 = RCHBLK/CLK pins output RCHBLK (1–8) (receive-channel block)
1 = RCHBLK/CLK pins output RCHCLK (1–8) (receive-channel clock)

Bit 1 / Transmit-Channel Block/Clock Select (TCBCS). This bit controls the function of all eight TCHBLK/CLK pins.

0 = TCHBLK/CLK pins output TCHBLK (1–8) (transmit-channel block)
1 = TCHBLK/CLK pins output TCHCLK (1–8) (transmit-channel block)

Bit 2 / Receive-Frame/Multiframe Sync Select (RFMSS). This bit controls the function of all eight RF/RMSYNC pins.

0 = RF/RMSYNC pins output RFSYNC (1–8) (receive-frame sync)
1 = RF/RMSYNC pins output RMSYNC (1–8) (receive-multiframe sync)

Bit 3 / Receive Loss-of-Signal/Signaling Freeze Select (RLOSSFS). This bit controls the function of all eight RLOS/RSIGF pins.

0 = RLOS/RSIGF pins output RLOS (1–8) (receive loss-of-signal)
1 = RLOS/RSIGF pins output RSIGF (1–8) (receive-signaling freeze)

Bits 4, 5 / Backplane Clock Select 0–1 (BPCLK0/1). These bits determine the clock frequency output on the BPCLK pin.

BPCLK1	BPCLK0	BPCLK Frequency (MHz)
0	0	2.048
0	1	4.096
1	0	8.192
1	1	16.384

Bits 6, 7 / Interleave Bus Operation Mode Select 0–1 (IBOMS0/1). These bits determine the configuration of the IBO (interleaved bus) multiplexer. These bits should be used with the Rx and Tx IBO control registers within each of the framer units. Additional information concerning the IBO mux is given in Section 7.3.

IBOMS1	IBOMS0	IBO Mode
0	0	IBO Mux Disabled
0	1	4.096MHz (2 per)
1	0	8.192MHz (4 per)
1	1	16.384MHz (8 per)

7.3 IBO Multiplexer

The IBO multiplexer is used with the IBO function located within each framer/formatter block (controlled by the RIBOC and TIBOC registers). When enabled, the IBO multiplexer simplifies user interface by connecting TDM bus signals internally. The IBO multiplexer eliminates the need for ganged external wiring and tri-state output drivers on the RSER and RSIG pins.

The DS26401 also supports the traditional mode of IBO operation by allowing complete access to individual framers and tri-stating the RSER and RSIG pins at the appropriate times for external bus wiring. This operation mode is enabled per framer in the associated RIBOC and TIBOC registers, while leaving the IBO multiplexer disabled (IBOMS0 = 0 and IBOMS1 = 0).

Figure 7-1, Figure 7-2, and Figure 7-3 show the equivalent internal circuit for each IBO mode. Table 7-1 describes the pin function changes for each mode of the IBO multiplexer.

The transmit and receive IBO functions are described in Sections 8.21 (T1 XMIT), 9.20 (T1 REC), 10.17 (E1 XMIT), and 11.19 (E1 REC).

Figure 7-1. Internal IBO Multiplexer Equivalent Circuit—4.096MHz

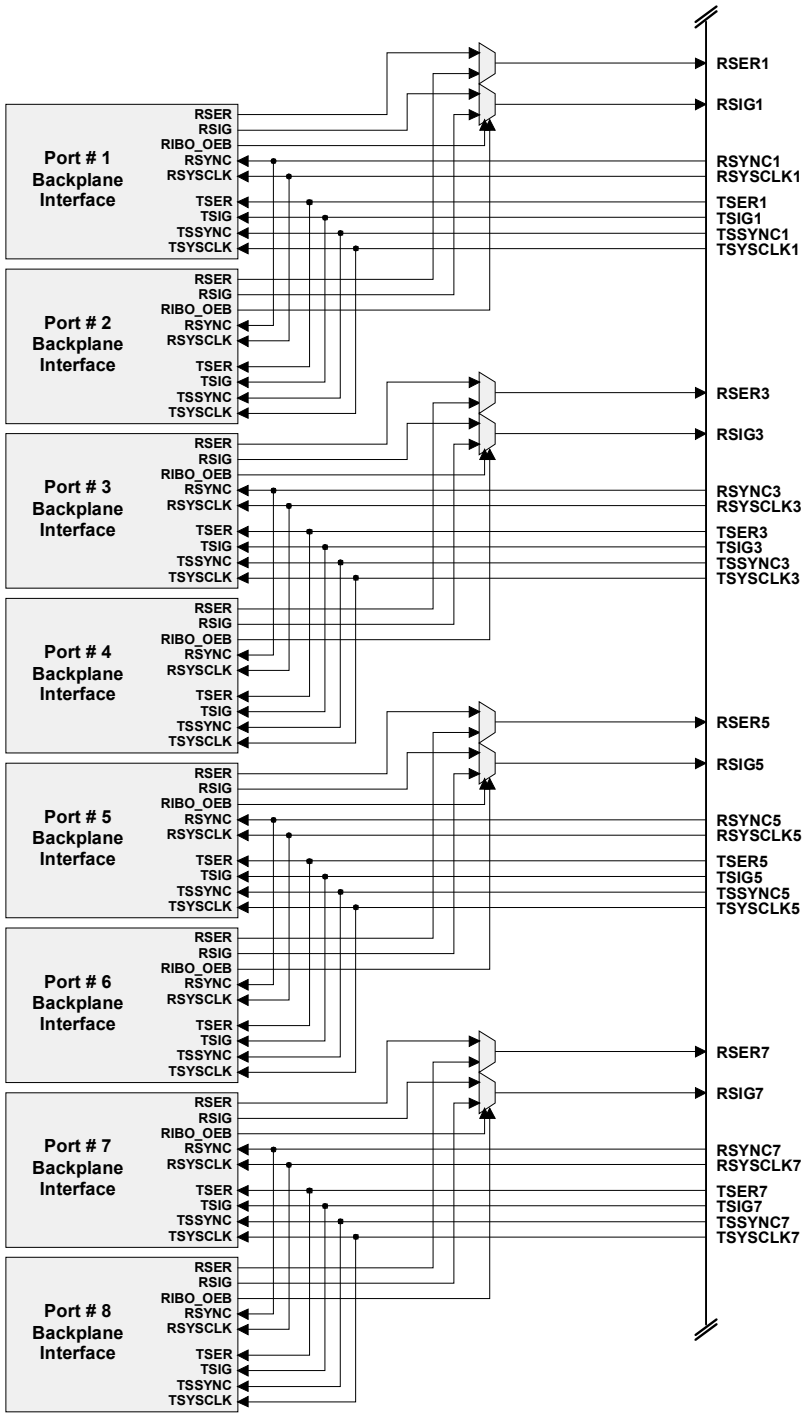


Figure 7-2. Internal IBO Multiplexer Equivalent Circuit—8.192MHz

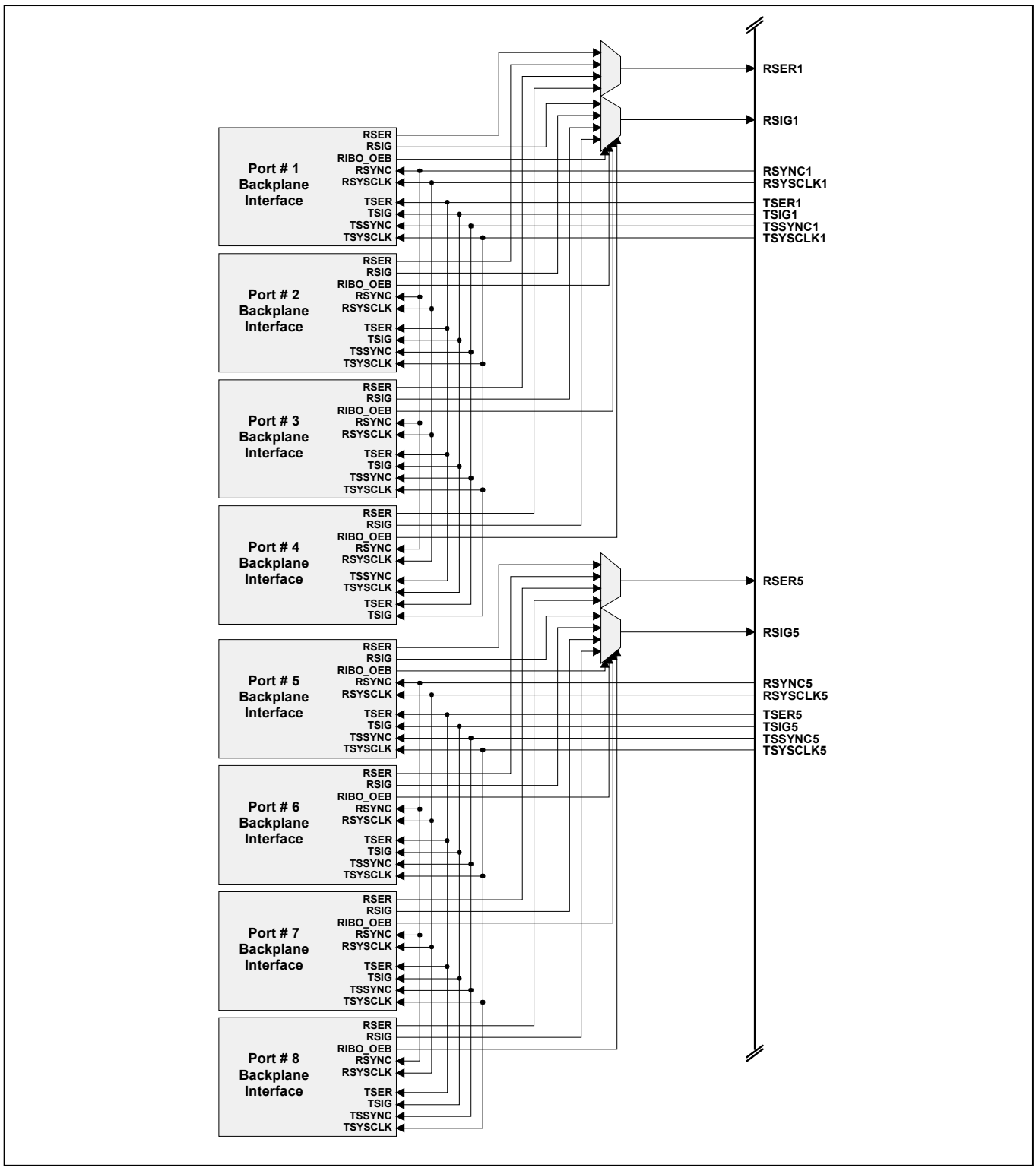


Figure 7-3. Internal IBO Multiplexer Equivalent Circuit—16.394MHz

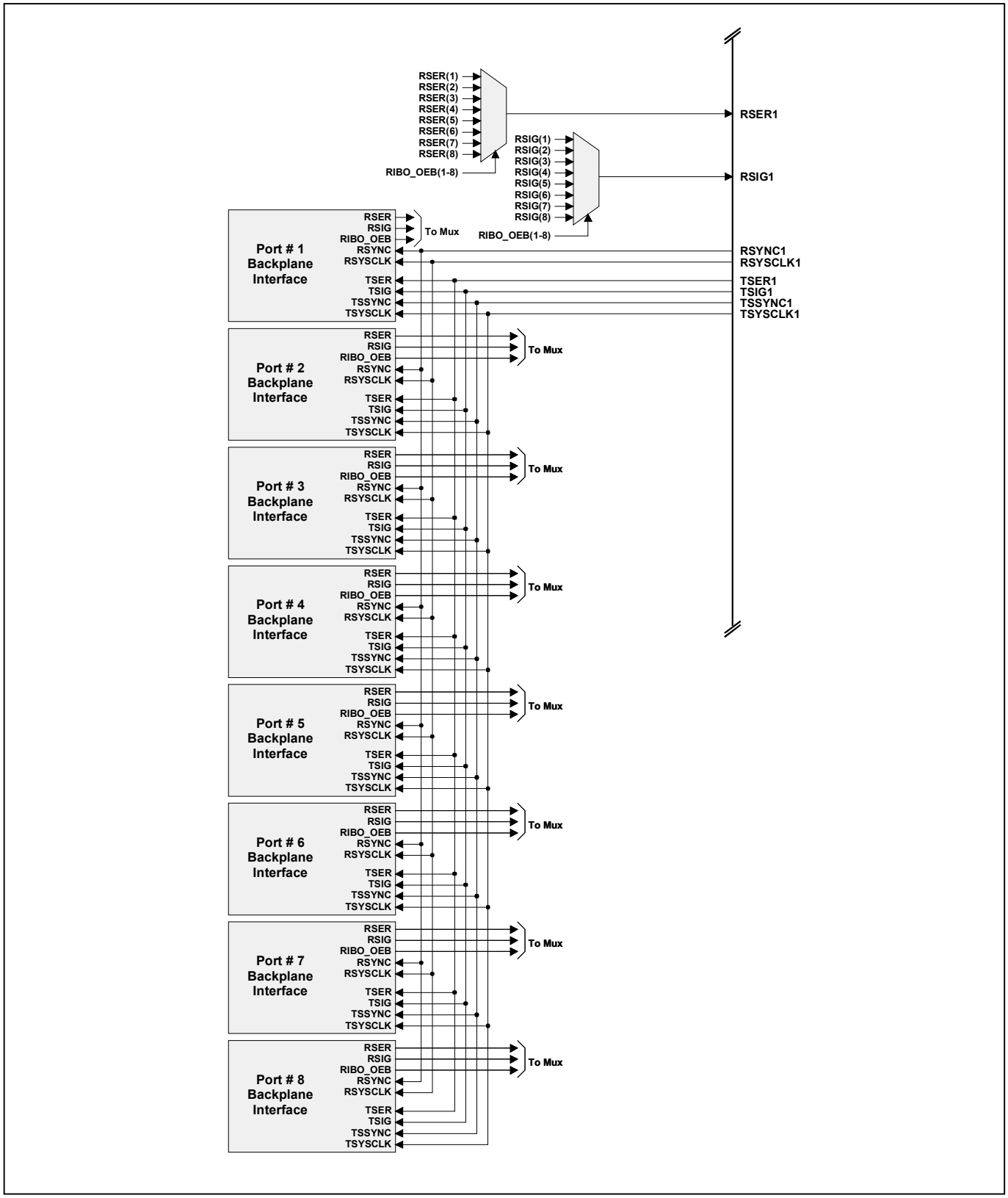


Table 7-1. Pin Functions with IBO Mux Enabled

RSER Output Pin Definitions

NAME	NORMAL USE	4.096MHz IBO	8.192MHz IBO	16.384MHz IBO
RSER1	Rx Serial Data for Port # 1	Combined Rx Serial Data for Ports 1 & 2	Combined Rx Serial Data for Ports 1–4	Rx Serial Data for Ports 1–8
RSER2	Rx Serial Data for Port # 2	Unused	Unused	Unused
RSER3	Rx Serial Data for Port # 3	Combined Rx Serial Data for Ports 3 & 4	Unused	Unused
RSER4	Rx Serial Data for Port # 4	Unused	Unused	Unused
RSER5	Rx Serial Data for Port # 5	Combined Rx Serial Data for Ports 5 & 6	Combined Rx Serial Data for Ports 5–8	Unused
RSER6	Rx Serial Data for Port # 6	Unused	Unused	Unused
RSER7	Rx Serial Data for Port # 7	Combined Rx Serial Data for Ports 7 & 8	Unused	Unused
RSER8	Rx Serial Data for Port # 8	Unused	Unused	Unused

RSIG Output Pin Definitions

NAME	NORMAL USE	4.096MHz IBO	8.192MHz IBO	16.384MHz IBO
RSIG1	Rx Signaling Data for Port # 1	Combined Rx Signaling Data for Ports 1 & 2	Combined Rx Signaling Data for Ports 1–4	Rx Signaling Data for Ports 1–8
RSIG2	Rx Signaling Data for Port # 2	Unused	Unused	Unused
RSIG3	Rx Signaling Data for Port # 3	Combined Rx Signaling Data for Ports 3 & 4	Unused	Unused
RSIG4	Rx Signaling Data for Port # 4	Unused	Unused	Unused
RSIG5	Rx Signaling Data for Port # 5	Combined Rx Signaling Data for Ports 5 & 6	Combined Rx Signaling Data for Ports 5–8	Unused
RSIG6	Rx Signaling Data for Port # 6	Unused	Unused	Unused
RSIG7	Rx Signaling Data for Port # 7	Combined Rx Signaling Data for Ports 7 & 8	Unused	Unused
RSIG8	Rx Signaling Data for Port # 8	Unused	Unused	Unused

Table 7-1. Pin Functions with IBO Mux Enabled (continued)

TSER Input Pin Definitions

NAME	NORMAL USE	4.096MHz IBO	8.192MHz IBO	16.384MHz IBO
TSER1	Tx Serial Data for Port # 1	Combined Tx Serial Data for Ports 1 & 2	Combined Tx Serial Data for Ports 1–4	Tx Serial Data for Ports 1–8
TSER2	Tx Serial Data for Port # 2	Unused	Unused	Unused
TSER3	Tx Serial Data for Port # 3	Combined Tx Serial Data for Ports 3 & 4	Unused	Unused
TSER4	Tx Serial Data for Port # 4	Unused	Unused	Unused
TSER5	Tx Serial Data for Port # 5	Combined Tx Serial Data for Ports 5 & 6	Combined Tx Serial Data for Ports 5–8	Unused
TSER6	Tx Serial Data for Port # 6	Unused	Unused	Unused
TSER7	Tx Serial Data for Port # 7	Combined Tx Serial Data for Ports 7 & 8	Unused	Unused
TSER8	Tx Serial Data for Port # 8	Unused	Unused	Unused

TSIG Input Pin Definitions

NAME	NORMAL USE	4.096MHz IBO	8.192MHz IBO	16.384MHz IBO
TSIG1	Tx Signaling Data for Port # 1	Combined Tx Signaling Data for Ports 1 & 2	Combined Tx Signaling Data for Ports 1–4	Tx Signaling Data for Ports 1–8
TSIG2	Tx Signaling Data for Port # 2	Unused	Unused	Unused
TSIG3	Tx Signaling Data for Port # 3	Combined Tx Signaling Data for Ports 3 & 4	Unused	Unused
TSIG4	Tx Signaling Data for Port # 4	Unused	Unused	Unused
TSIG5	Tx Signaling Data for Port # 5	Combined Tx Signaling Data for Ports 5 & 6	Combined Tx Signaling Data for Ports 5–8	Unused
TSIG6	Tx Signaling Data for Port # 6	Unused	Unused	Unused
TSIG7	Tx Signaling Data for Port # 7	Combined Tx Signaling Data for Ports 7 & 8	Unused	Unused
TSIG8	Tx Signaling Data for Port # 8	Unused	Unused	Unused

Table 7-1. Pin Functions with IBO Mux Enabled (continued)

RSYNC Input Pin Definitions

NAME	NORMAL USE	4.096MHz IBO	8.192MHz IBO	16.384MHz IBO
RSYNC1	Rx Frame Pulse for port # 1	Rx Frame Pulse for Ports 1 & 2	Rx Frame Pulse for Ports 1–4	Rx Frame Pulse for Ports 1–8
RSYNC2	Rx Frame Pulse for port # 2	Unused	Unused	Unused
RSYNC3	Rx Frame Pulse for port # 3	Rx Frame Pulse for Ports 3 & 4	Unused	Unused
RSYNC4	Rx Frame Pulse for port # 4	Unused	Unused	Unused
RSYNC5	Rx Frame Pulse for port # 5	Rx Frame Pulse for Ports 5 & 6	Rx Frame Pulse for Ports 5–8	Unused
RSYNC6	Rx Frame Pulse for port # 6	Unused	Unused	Unused
RSYNC7	Rx Frame Pulse for port # 7	Rx Frame Pulse for Ports 7 & 8	Unused	Unused
RSYNC8	Rx Frame Pulse for port # 8	Unused	Unused	Unused

TSSYNC Input Pin Definitions

NAME	NORMAL USE	4.096MHz IBO	8.192MHz IBO	16.384MHz IBO
TSSYNC1	Tx Frame Pulse for Port # 1	Tx Frame Pulse for Ports 1 & 2	Tx Frame Pulse for Ports 1– 4	Tx Frame Pulse for Ports 1–8
TSSYNC2	Tx Frame Pulse for Port # 2	Unused	Unused	Unused
TSSYNC3	Tx Frame Pulse for Port # 3	Tx Frame Pulse for Ports 3 & 4	Unused	Unused
TSSYNC4	Tx Frame Pulse for Port # 4	Unused	Unused	Unused
TSSYNC5	Tx Frame Pulse for Port # 5	Tx Frame Pulse for Ports 5 & 6	Tx Frame Pulse for Ports 5–8	Unused
TSSYNC6	Tx Frame Pulse for Port # 6	Unused	Unused	Unused
TSSYNC7	Tx Frame Pulse for Port # 7	Tx Frame Pulse for Ports 7 & 8	Unused	Unused
TSSYNC8	Tx Frame Pulse for Port # 8	Unused	Unused	Unused

Table 7-1. Pin Functions with IBO Mux Enabled (continued)

RSYSCLK Input Pin Definitions

NAME	NORMAL USE	4.096MHz IBO	8.192MHz IBO	16.384MHz IBO
RSYSCLK1	Rx System Clock for port # 1	Rx System Clock for Ports 1 & 2	Rx System Clock for Ports 1– 4	Rx System Clock for Ports 1– 8
RSYSCLK2	Rx System Clock for port # 2	Unused	Unused	Unused
RSYSCLK3	Rx System Clock for port # 3	Rx System Clock for Ports 3 & 4	Unused	Unused
RSYSCLK4	Rx System Clock for port # 4	Unused	Unused	Unused
RSYSCLK5	Rx System Clock for port # 5	Rx System Clock for Ports 5 & 6	Rx System Clock for Ports 5–8	Unused
RSYSCLK6	Rx System Clock for port # 6	Unused	Unused	Unused
RSYSCLK7	Rx System Clock for port # 7	Rx System Clock for Ports 7 & 8	Unused	Unused
RSYSCLK8	Rx System Clock for port # 8	Unused	Unused	Unused

TSYSCLK Input Pin Definitions

NAME	NORMAL USE	4.096MHz IBO	8.192MHz IBO	16.384MHz IBO
TSYSCLK1	Tx System Clock for Port # 1	Tx System Clock for Ports 1 & 2	Tx System Clock for Ports 1–4	Tx System Clock for Ports 1– 8
TSYSCLK2	Tx System Clock for Port # 2	Unused	Unused	Unused
TSYSCLK3	Tx System Clock for Port # 3	Tx System Clock for Ports 3 & 4	Unused	Unused
TSYSCLK4	Tx System Clock for Port # 4	Unused	Unused	Unused
TSYSCLK5	Tx System Clock for Port # 5	Tx System Clock for Ports 5 & 6	Tx System Clock for Ports 5–8	Unused
TSYSCLK6	Tx System Clock for Port # 6	Unused	Unused	Unused
TSYSCLK7	Tx System Clock for Port # 7	Tx System Clock for Ports 7 & 8	Unused	Unused
TSYSCLK8	Tx System Clock for Port # 8	Unused	Unused	Unused

Register Name: **IDR**
Register Description: **Device Identification Register**
Register Address: **0F8h**

Bit #	7	6	5	4	3	2	1	0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Default	0	0	0	0	0	0	0	0

Bits 0 to 3/Chip Revision Bits (ID0 to ID3). The lower four bits of the IDR are used to display the die revision of the chip. IDO is the LSB of a decimal code that represents the chip revision.

Bits 4 to 7/Device ID (ID4 to ID7). The upper four bits of the IDR are used to display the DS26401 ID.

DEVICE	ID (ID4 to ID7)
DS26401	8h

Register Name: **GSR1**
Register Description: **Global Status Register 1**
Register Address: **0F9h**

Bit #	7	6	5	4	3	2	1	0
Name	FIS8	FIS7	FIS6	FIS5	FIS4	FIS3	FIS2	FIS1
Default	0	0	0	0	0	0	0	0

Note: *The GSR1 register reports the framer interrupt status for each of the 8 T1/E1 framers. A logic 1 in the associated bit location indicates a framer has set (active low) its interrupt signal.*

Bit 0 / Framer Interrupt Status 1 (FIS1)
0 = Framer 1 has not issued an interrupt
1 = Framer 1 has issued an interrupt

Bit 1 / Framer Interrupt Status 2 (FIS2)
0 = Framer 2 has not issued an interrupt
1 = Framer 2 has issued an interrupt

Bit 2 / Framer Interrupt Status 3 (FIS3)
0 = Framer 3 has not issued an interrupt
1 = Framer 3 has issued an interrupt

Bit 3 / Framer Interrupt Status 4 (FIS4)
0 = Framer 4 has not issued an interrupt
1 = Framer 4 has issued an interrupt

Bit 4 / Framer Interrupt Status 5 (FIS5)
0 = Framer 5 has not issued an interrupt
1 = Framer 5 has issued an interrupt

Bit 5 / Framer Interrupt Status 6 (FIS6)
0 = Framer 6 has not issued an interrupt
1 = Framer 6 has issued an interrupt

Bit 6 / Framer Interrupt Status 7 (FIS7)
0 = Framer 7 has not issued an interrupt
1 = Framer 7 has issued an interrupt

Bit 7 / Framer Interrupt Status 8 (FIS8)
0 = Framer 8 has not issued an interrupt
1 = Framer 8 has issued an interrupt

Register Name: **GSR2**
Register Description: **Global Status Register 2**
Register Address: **0FAh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	BBED	BLOS
Default	0	0	0	0	0	0	0	0

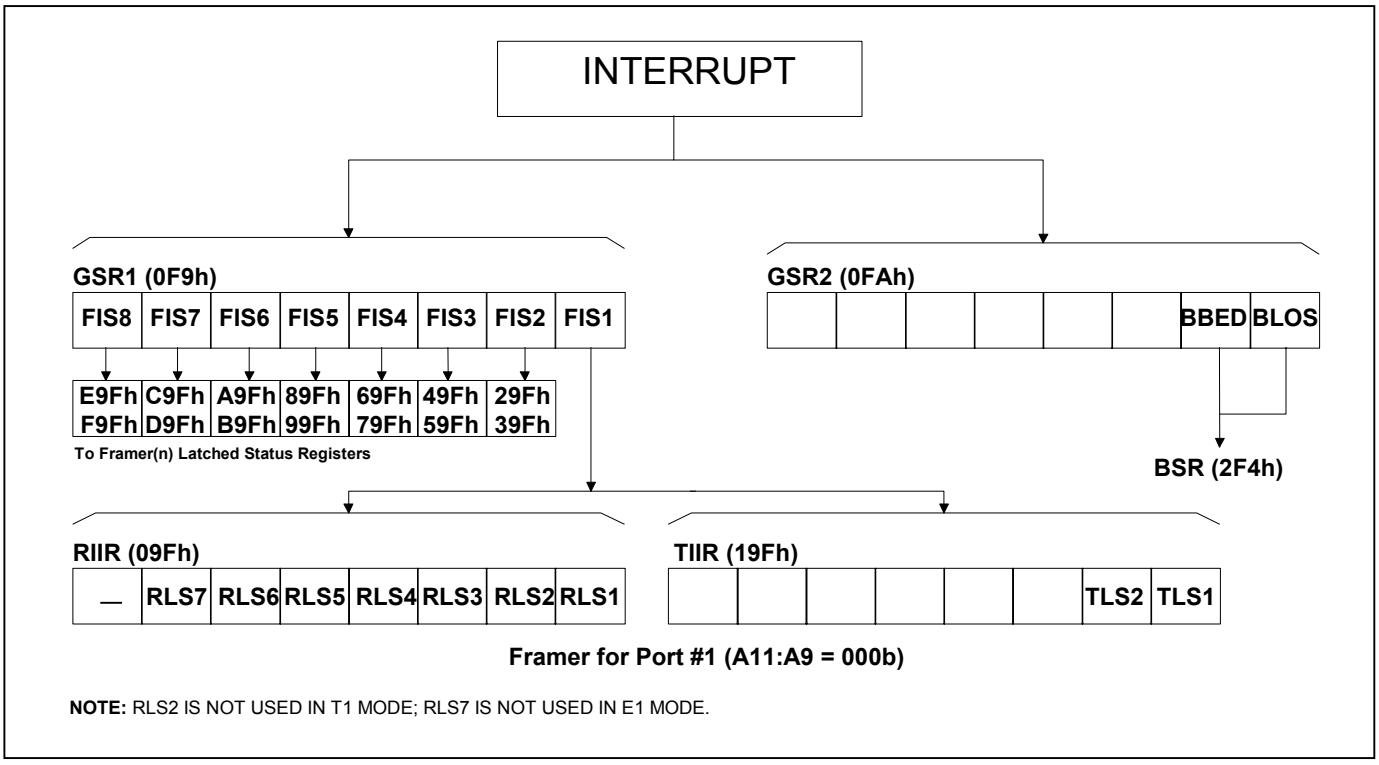
Bit 0 / BERT Loss-of-Sync Interrupt Status (BLOS)
0 = The BERT has not issued an interrupt for LOS
1 = The BERT has issued an interrupt for LOS (only possible when BLOSIM in GCR1 is set)

Bit 1 / BERT Bit-Error-Detect Interrupt Status (BBED)
0 = The BERT has not issued an interrupt for BED
1 = The BERT has issued an interrupt for BED (only possible when BBEDIM in GCR1 is set)

Bits 2–7 / Unused

7.4 Interrupt Tree

When the host processor detects an interrupt, the user can first read the GSR1 and GSR2 registers to narrow down the potential source of the interrupt event. Bit locations set in the GSR1 register direct the user to one or more framers, from where the appropriate status register(s) can be discerned with RIIR and TIIR.



NOTE: RLS2 IS NOT USED IN T1 MODE; RLS7 IS NOT USED IN E1 MODE.

8. T1 RECEIVER

8.1 T1 Receiver Register Map

ADDRESS	R/W	FUNCTION	NAME	PAGE
000	—	Unused (See note)	—	—
001	—	Unused	—	—
002	—	Unused	—	—
003	—	Unused	—	—
004	—	Unused	—	—
005	—	Unused	—	—
006	—	Unused	—	—
007	—	Unused	—	—
008	—	Unused	—	—
009	—	Unused	—	—
00A	—	Unused	—	—
00B	—	Unused	—	—
00C	—	Unused	—	—
00D	—	Unused	—	—
00E	—	Unused	—	—
00F	—	Unused	—	—
010	R/W	Rx HDLC Control	RHC	200
011	R/W	Rx HDLC Bit Suppress	RHBSE	200
012	R/W	Rx DS0 Monitor Select	RDS0SEL	181
013	R/W	Rx Signaling Control	RSIGC	184
014	R/W	Rx Control 2	RCR2	159
015	R/W	Rx BOC Control	RBOCC	83
016	—	Unused	—	—
017	—	Unused	—	—
018	—	Unused	—	—
019	—	Unused	—	—
01A	—	Unused	—	—
01B	—	Unused	—	—
01C	R/W	Rx Test Register 1	RTEST1	—
01D	R/W	Rx Test Register 2	RTEST2	—
01E	R/W	Rx Test Register 3	RTEST3	—
01F	R/W	Rx Test Register 4	RTEST4	—
020	R/W	Rx Idle Definition 1	RIDR1	187
021	R/W	Rx Idle Definition 2	RIDR2	187
022	R/W	Rx Idle Definition 3	RIDR3	187
023	R/W	Rx Idle Definition 4	RIDR4	187
024	R/W	Rx Idle Definition 5	RIDR5	187
025	R/W	Rx Idle Definition 6	RIDR6	187
026	R/W	Rx Idle Definition 7	RIDR7	187
027	R/W	Rx Idle Definition 8	RIDR8	187
028	R/W	Rx Idle Definition 9	RIDR9	187
029	R/W	Rx Idle Definition 10	RIDR10	187
02A	R/W	Rx Idle Definition 11	RIDR11	187
02B	R/W	Rx Idle Definition 12	RIDR12	187
02C	R/W	Rx Idle Definition 13	RIDR13	187
02D	R/W	Rx Idle Definition 14	RIDR14	187
02E	R/W	Rx Idle Definition 15	RIDR15	187
02F	R/W	Rx Idle Definition 16	RIDR16	187
030	R/W	Rx Idle Definition 17	RIDR17	187
031	R/W	Rx Idle Definition 18	RIDR18	187
032	R/W	Rx Idle Definition 19	RIDR19	187
033	R/W	Rx Idle Definition 20	RIDR20	187
034	R/W	Rx Idle Definition 21	RIDR21	187
035	R/W	Rx Idle Definition 22	RIDR22	187
036	R/W	Rx Idle Definition 23	RIDR23	187

ADDRESS	R/W	FUNCTION	NAME	PAGE
037	R/W	Rx Idle Definition 24	RIDR24	187
038	R/W	Rx Sig All Ones Insertion 1	RSAOI1	75
039	R/W	Rx Sig All Ones Insertion 2	RSAOI2	75
03A	R/W	Rx Sig All Ones Insertion 3	RSAOI3	75
03B	—	Unused	—	—
03C	R/W	Rx Digital Milliwatt Enable 1	RDMWE1	63
03D	R/W	Rx Digital Milliwatt Enable 2	RDMWE2	63
03E	R/W	Rx Digital Milliwatt Enable 3	RDMWE3	63
03F	—	Unused	—	—
040	R	Rx Signaling 1	RS1	185
041	R	Rx Signaling 2	RS2	185
042	R	Rx Signaling 3	RS3	185
043	R	Rx Signaling 4	RS4	185
044	R	Rx Signaling 5	RS5	185
045	R	Rx Signaling 6	RS6	185
046	R	Rx Signaling 7	RS7	185
047	R	Rx Signaling 8	RS8	185
048	R	Rx Signaling 9	RS9	185
049	R	Rx Signaling 10	RS10	185
04A	R	Rx Signaling 11	RS11	185
04B	R	Rx Signaling 12	RS12	185
04C	—	Unused	—	—
04D	—	Unused	—	—
04E	—	Unused	—	—
04F	—	Unused	—	—
050	R	Rx Line-Code Violation Counter 1	LCVCR1	66
051	R	Rx Line-Code Violation Counter 2	LCVCR2	66
052	R	Rx Path-Code Violation Count 1	PCVCR1	67
053	R	Rx Path-Code Violation Count 2	PCVCR2	67
054	R	Rx Frames Out-of-Sync Counter 1	FOSCR1	68
055	R	Rx Frames Out-of-Sync Counter 2	FOSCR2	68
056	—	Unused	—	—
057	—	Unused	—	—
058	—	Unused	—	—
059	—	Unused	—	—
05A	—	Unused	—	—
05B	—	Unused	—	—
05C	—	Unused	—	—
05D	—	Unused	—	—
05E	—	Unused	—	—
05F	—	Unused	—	—
060	R	Rx DS0 Monitor	RDS0M	181
061	—	Unused	—	—
062	R	Rx FDL	RFDL	86
063	R	Rx BOC	RBOC	84
064	R	Rx SLC96 Data Link 1	RSLC1	85
065	R	Rx SLC96 Data Link 2	RSLC2	85
066	R	Rx SLC96 Data Link 3	RSLC3	85
067	—	Unused	—	—
068	—	Unused	—	—
069	—	Unused	—	—
06A	—	Unused	—	—
06B	—	Unused	—	—
06C	—	Unused	—	—
06D	—	Unused	—	—
06E	—	Unused	—	—
06F	—	Unused	—	—
070	—	Unused	—	—
071	—	Unused	—	—
072	—	Unused	—	—
073	—	Unused	—	—

ADDRESS	R/W	FUNCTION	NAME	PAGE
074	—	Unused	—	—
075	—	Unused	—	—
076	—	Unused	—	—
077	—	Unused	—	—
078	—	Unused	—	—
079	—	Unused	—	—
07A	—	Unused	—	—
07B	—	Unused	—	—
07C	—	Unused	—	—
07D	—	Unused	—	—
07E	—	Unused	—	—
07F	—	Unused	—	—
080	R/W	Rx Master Mode	RMMR	156
081	R/W	Rx Control 1	RCR1	158
082	R/W	Rx In-Band Code Control	RIBCC	87
083	R/W	Rx Control 3	RCR3	160
084	R/W	Rx I/O Configuration	RIOCR	161
085	R/W	Rx Elastic Store Control	RESCR	190
086	R/W	Rx Error Count Configuration	ERCNT	65
087	R/W	Rx HDLC FIFO Control	RHFC	201
088	R/W	Rx Interleave Bus Op Control	RIBOC	209
089	R/W	Rx Spare Code Control	RSCC	90
08A	R/W	Rx BERT Interface Control	RBICR	210
08B	R/W	Rx BERT Bit Suppress En	RBBS	211
08C	—	Unused	—	—
08D	—	Unused	—	—
08E	R/W	Rx Test Register 5	RTEST5	—
08F	R/W	Rx Test Register 6	RTEST6	—
090	R/W	Rx Latched Status 1	RLS1	166
091	R/W	Rx Latched Status 2	RLS2	168
092	R/W	Rx Latched Status 3	RLS3	170
093	R/W	Rx Latched Status 4	RLS4	173
094	R/W	Rx Latched Status 5	RLS5	205
095	—	Unused	—	—
096	R/W	Rx Latched Status 7	RLS7	
097	—	Unused	—	—
098	R/W	Rx Signaling CoS Status 1	RSS1	74
099	R/W	Rx Signaling CoS Status 2	RSS2	74
09A	R/W	Rx Signaling CoS Status 3	RSS3	74
09B	—	Unused	—	—
09C	R/W	Rx Spare Code Definition 1	RSPCD1	87
09D	R/W	Rx Spare Code Definition 2	RSPCD2	87
09E	—	Unused	—	—
09F	R/W	Rx Interrupt Information Reg	RIIR	157
0A0	R/W	Rx Interrupt Mask Reg 1	RIM1	167
0A1	—	Unused	—	—
0A2	R/W	Rx Interrupt Mask Reg 3	RIM3	171
0A3	R/W	Rx Interrupt Mask Reg 4	RIM4	174
0A4	R/W	Rx Interrupt Mask Reg 5	RIM5	206
0A5	—	Unused	—	—
0A6	R/W	Rx Interrupt Mask Reg 7	RIM7	
0A7	—	Unused	—	—
0A8	R/W	Rx Sig CoS Interrupt Enable 1	RSCSE1	186
0A9	R/W	Rx Sig CoS Interrupt Enable 2	RSCSE2	186
0AA	R/W	Rx Sig CoS Interrupt Enable 3	RSCSE3	186
0AB	—	Unused	—	—
0AC	R/W	Rx Up-Code Definition 1	RUPCD1	88
0AD	R/W	Rx Up-Code Definition 2	RUPCD2	88
0AE	R/W	Rx Down-Code Definition 1	RDNCD1	89
0AF	R/W	Rx Down-Code Definition 2	RDNCD2	89
0B0	R	Rx Real-Time Status 1	RRTS1	165

ADDRESS	R/W	FUNCTION	NAME	PAGE
0B1	—	Unused	—	—
0B2	R	Rx Real-Time Status 3	RRTS3	169
0B3	—	Unused	—	—
0B4	R	Rx Real-Time Status 5 (HDLC)	RRTS5	204
0B5	R	Rx HDLC Packet Bytes Available	RHPBA	202
0B6	R	Rx HDLC FIFO	RHF	203
0B7	—	Unused	—	—
0B8	—	Unused	—	—
0B9	—	Unused	—	—
0BA	—	Unused	—	—
0BB	—	Unused	—	—
0BC	—	Unused	—	—
0BD	—	Unused	—	—
0BE	—	Unused	—	—
0BF	—	Unused	—	—
0C0	R/W	Rx Blank Channel Select 1	RBCS1	191
0C1	R/W	Rx Blank Channel Select 2	RBCS2	191
0C2	R/W	Rx Blank Channel Select 3	RBCS3	191
0C3	R/W	Rx Blank Channel Select 4	RBCS4	191
0C4	R/W	Rx Channel Blocking 1	RCBR1	188
0C5	R/W	Rx Channel Blocking 2	RCBR2	188
0C6	R/W	Rx Channel Blocking 3	RCBR3	188
0C7	R/W	Rx Channel Blocking 4	RCBR4	188
0C8	R/W	Rx Signaling Insertion 1	RSI1	186
0C9	R/W	Rx Signaling Insertion 2	RSI2	186
0CA	R/W	Rx Signaling Insertion 3	RSI3	186
0CB	R/W	Rx Signaling Insertion 4	RSI4	186
0CC	R/W	Rx Gapped Clock Channel Select 1	RGCCS1	193
0CD	R/W	Rx Gapped Clock Channel Select 2	RGCCS2	193
0CE	R/W	Rx Gapped Clock Channel Select 3	RGCCS3	193
0CF	R/W	Rx Gapped Clock Channel Select 4	RGCCS4	193
0D0	R/W	Rx Channel Idle Code Enable 1	RCICE1	187
0D1	R/W	Rx Channel Idle Code Enable 2	RCICE2	187
0D2	R/W	Rx Channel Idle Code Enable 3	RCICE3	187
0D3	—	Unused	—	—
0D4	R/W	Rx BERT Channel Select 1	RBCS1	191
0D5	R/W	Rx BERT Channel Select 2	RBCS2	191
0D6	R/W	Rx BERT Channel Select 3	RBCS3	191
0D7	—	Unused	—	—
0D8	—	Unused	—	—
0D9	—	Unused	—	—
0DA	—	Unused	—	—
0DB	—	Unused	—	—
0DC	—	Unused	—	—
0DD	—	Unused	—	—
0DE	—	Unused	—	—
0DF	—	Unused	—	—
0E0	—	Unused	—	—
0E1	—	Unused	—	—
0E2	—	Unused	—	—
0E3	—	Unused	—	—
0E4	—	Unused	—	—
0E5	—	Unused	—	—
0E6	—	Unused	—	—
0E7	—	Unused	—	—
0E8	—	Unused	—	—
0E9	—	Unused	—	—
0EA	—	Unused	—	—
0EB	—	Unused	—	—
0EC	—	Unused	—	—
0ED	—	Unused	—	—

ADDRESS	R/W	FUNCTION	NAME	PAGE
0EE	—	Unused	—	—
0EF	—	Unused	—	—
0F0	—	Used by Global Functions	—	—
0F1	—	Used by Global Functions	—	—
0F2	—	Unused	—	—
0F3	—	Unused	—	—
0F4	—	Unused	—	—
0F5	—	Unused	—	—
0F6	—	Unused	—	—
0F7	—	Unused	—	—
0F8	—	Used by Global Functions	—	—
0F9	—	Used by Global Functions	—	—
0FA	—	Used by Global Functions	—	—
0FB	—	Unused	—	—
0FC	—	Unused	—	—
0FD	—	Unused	—	—
0FE	—	Unused	—	—
0FF	—	Unused	—	—

Note: All unused addresses should be set to 0.

8.2 T1 Receive Framer Description and Operation

The DS26401 includes eight fully independent DS1/E1 framers. The framers are designed to interface seamlessly to the line side through an external LIU. Each framer can be individually programmed to accept AMI, B8ZS, HDB3, or NRZ data. In T1 mode, each framer supports D4 (SF), ESF, and SLC-96 frame formats, and detects/reports common alarms such as AIS, RAI, LOS, and OOF, as well as AIS-CI and RAI-CI. Performance monitor counters are maintained for each port, which report bipolar/line-code violations, F-bit/CRC errors, and number of out-of-sync multiframes.

Each framer has an HDLC controller that can be mapped into a single time slot, or Sa4 to Sa8 bits (E1 mode), or the FDL (T1 mode), and has 64-byte FIFO buffers in both the transmit and receive paths.

The HDLC controllers perform the necessary overhead for generating and receiving performance report messages (PRM) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controllers automatically generate and detect flags; generate and check the CRC checksum; generate and detect abort sequences and stuff and destuff zeros; and byte align to the data stream. The FIFO buffers are large enough to allow a full PRM to be received or transmitted without host intervention.

Other features contained within each framer include a BOC detector with programmable code integration and three independent 16-bit loop-code detectors. Host interface is simplified with status registers optimized for either interrupt driven or polled environments. In many cases, status bits are reported in both real-time and latched on change-of-state with separate bits for each state change. Most latched bits can be mapped to generate an external interrupt on the $\overline{INT}$ pin.

Backplane interface is simplified with the inclusion of two-frame elastic-store memories in each of the receive and transmit paths. These buffers can be used to control slips in asynchronous environments, or rate-adapt from 1.544MHz to 2.048MHz. The DS26401 also supports an interleaved backplane operating at 4.096MHz, 8.192MHz, or 16.384MHz.

Additional details about the operation of the DS1 framer are included in the register descriptions in this section.

8.3 Receive Master-Mode Register

The receive master-mode register (RMMR) controls the initialization of the receive-side framer. The FRM_EN bit can be left low if the framer for that particular port is not going to be used, putting the circuit in a low-power (sleep) state.

Register Name: **RMMR**
Register Description: **Receive Master Mode Register**
Register Address: **080h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	FRM_EN	INIT_DONE	—	—	—	—	SFTRST	T1/E1
Default	0	0	0	0	0	0	0	0

Bit 0 / Receiver T1/E1 Mode Select (T1/E1). This bit sets the operating mode for receiver only! This bit must be set to the desired state before writing INIT_DONE.
0 = T1 operation
1 = E1 operation

Bit 1 / Soft Reset (SFTRST). Level-sensitive processor reset. Should be taken high, then low to reset and initialize the internal processor.
0 = Normal operation
1 = Hold the internal RISC in reset. This bit only affects the receive-side processor.

Bits 2–5 / Unused. Must be set = 0 for proper operation.

Bit 6 / Initialization Done (INIT_DONE). The host (user) must set this bit once the configuration registers have been written. The host is required to write or clear all RAM based registers (addresses 00H to 7FH) prior to setting this bit. Once INIT_DONE is set, the internal processor will check the FRM_EN bit. If enabled, the internal processor continues executing based on the initial configuration.

Bit 7 / Framer Enable (FRM_EN). This bit must be written with the desired value prior to setting INIT_DONE.
0 = Framer disabled (held in low-power state)
1 = Framer enabled (all features active)

8.4 Interrupt Information Register

The interrupt information registers provide an indication of which DS26401 status registers are generating an interrupt. When an interrupt occurs, the host can read RIIR to quickly identify which of the seven T1 receive status registers is causing the interrupt(s). The interrupt information register bits clear once the appropriate interrupt has been serviced and cleared, as long as no other interrupt condition is present in the associated status register. Status bits that have been masked through the receive-interrupt mask (RIMx) registers are also masked from the RIIR register.

Register Name: **RIIR**
Register Description: **Receive Interrupt Information Register**
Register Address: **9Fh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	RLS7	RLS6	RLS5	RLS4	RLS3	RLS2*	RLS1
Default	0	0	0	0	0	0	0	0

**RLS2 does not create an interrupt, therefore this bit is not used in T1 mode.*

8.5 T1 Receive Control Registers

These registers provide the primary setup and control of the receive framers.

Register Name: **RCR1**
Register Description: **Receive Control Register 1**
Register Address: **081h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	SYNCT	RB8ZS	RFM	ARC	SYNCC	RJC	SYNCE	RESYNC
Default	0	0	0	0	0	0	0	0

Bit 0 / Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the receive-side framer is initiated. Must be cleared and set again for a subsequent resync.

Bit 1 / Sync Enable (SYNCE)
0 = auto resync enabled
1 = auto resync disabled

Bit 2 / Receive Japanese CRC6 Enable (RJC)
0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation)
1 = use Japanese standard JT-G704 CRC6 calculation

Bit 3 / Sync Criteria (SYNCC)
In D4 Framing Mode:
0 = search for Ft pattern, then search for Fs pattern
1 = cross couple Ft and Fs pattern
In ESF Framing Mode:
0 = search for FPS pattern only
1 = search for FPS and verify with CRC6

Bit 4 / Auto Resync Criteria (ARC)
0 = Resync on OOF or LOS event
1 = Resync on OOF only

Bit 5 / Receive Frame Mode Select (RFM)
0 = ESF framing mode
1 = D4 framing mode

Bit 6 / Receive B8ZS Enable (RB8ZS)
0 = B8ZS disabled
1 = B8ZS enabled

Bit 7 / Sync Time (SYNCT)
0 = qualify 10 bits
1 = qualify 24 bits

Register Name: **RCR2**
Register Description: **Receive Control Register 2**
Register Address: **014h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	RSLC96	OOF2	OOF1	RAIIE	RD4RM
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive-Side D4 Remote Alarm Select (RD4RM)

0 = zeros in bit 2 of all channels
1 = a one in the S-bit position of frame 12 (J1 Yellow Alarm Mode)

Bit 1 / Receive RAI Integration Enable (RAIIE). The ESF RAI indication can be interrupted for a period not to exceed 100ms per interruption (T1.403). In ESF mode, setting RAIIE causes the RAI status from the DS26401 to be integrated for 200ms.

0 = RAI detects when 16 consecutive patterns of 00FF appear in the FDL.
RAI clears when 14 or less patterns of 00FF hex out of 16 possible appear in the FDL.
1 = RAI detects when the condition has been present for greater than 200ms.
RAI clears when the condition has been absent for greater than 200ms.

Bits 2, 3 / Out-of-Frame Select Bits (OOF2, OOF1)

OOF2	OOF1	OUT OF FRAME CRITERIA
0	0	2/4 frame bits in error
0	1	2/5 frame bits in error
1	0	2/6 frame bits in error
1	1	2/6 frame bits in error

Bit 4 / Receive SLC-96 Synchronizer Enable (RSLC96). See Section 8.17.

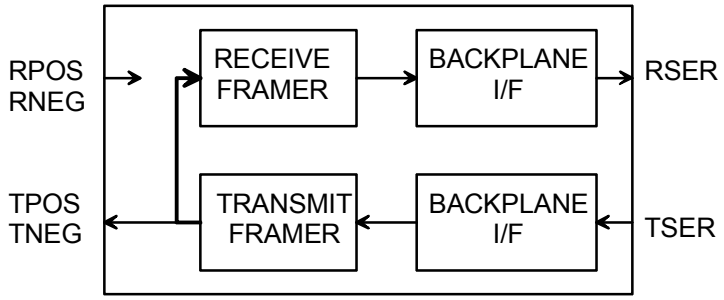
0 = the SLC-96 synchronizer is disabled
1 = the SLC-96 synchronizer is enable

Bits 5–7 / Unused. Must be set = 0 for proper operation.

Register Name: **RCR3**
Register Description: **Receive Control Register 3**
Register Address: **083h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	IDF	—	RSERC	—	—	RLB	PLB	FLB
Default	0	0	0	0	0	0	0	0

Bit 0 / Framer Loopback (FLB)
0 = loopback disabled
1 = loopback enabled

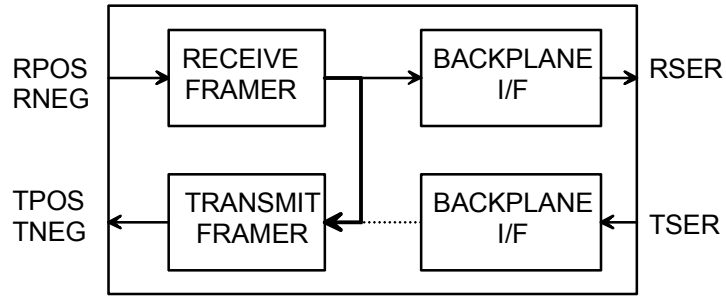


FRAMER LOOPBACK

This loopback is useful in testing and debugging applications. In FLB, the DS26401 loops data from the transmit side back to the receive side. When FLB is enabled, the following occurs:

1) (T1 mode) An unframed all-ones code is transmitted at TPOS and TNEG.
   (E1 mode) Normal data is transmitted at TPOS and TNEG.
2) Data at RPOS and RNEG is ignored.
3) All receive-side signals take on timing synchronous with TCLK instead of RCLK.

Bit 1 / Payload Loopback (PLB)
0 = loopback disabled
1 = loopback enabled



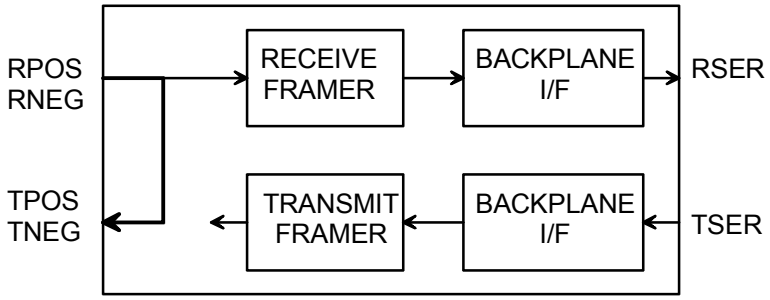
PAYLOAD LOOPBACK
(CAN BE DONE ON A PER-CHANNEL BASIS)

When PLB is enabled, the following occurs:
1) Data is transmitted from the TPOS and TNEG pins synchronous with RCLK instead of TCLK.
2) All the receive-side signals continue to operate normally.
3) The TCHCLK and TCHBLK signals are forced low.
4) Data at the TSER, TDATA, and TSIG pins is ignored.
5) The TLCLK signal becomes synchronous with RCLK instead of TCLK.

Normally, this loopback is only enabled when ESF framing is being performed, but it can also be enabled in D4 framing applications. In a PLB situation, the DS26401 loops the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, they are reinserted by the DS26401.

Bit 2 / Remote Loopback (RLB)

0 = loopback disabled
1 = loopback enabled



REMOTE LOOPBACK

In this loopback, data input through the RPOS and RNEG pins is transmitted back to the TPOS and TNEG pins. Data continues to pass through the DS26401's receive-side framer as it would normally, and the data from the transmit-side formatter is ignored.

Bits 3, 4, 6 / Unused. Must be set = 0 for proper operation.

Bit 5 / RSER Control (RSERC)

0 = Allow RSER to output data as received under all conditions (normal operation)
1 = Force RSER to one under loss-of-frame alignment conditions

Bit 7 / Input Data Format (IDF)

0 = Bipolar data is expected at RPOS and RNEG (either AMI or B8ZS).
1 = NRZ data is expected at RPOS. The BPV counter is disabled and RNEG is ignored by the DS26401.

Register Name: **RIOCR**
Register Description: **Receive I/O Configuration Register**
Register Address: **084h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RCLKINV	RSYNCINV	H100EN	RSCLKM	RSMS	RSIO	RSMS2	RSMS1
Default	0	0	0	0	0	0	0	0

Bit 0 / RSYNC Mode Select 1 (RSMS1). Selects frame or multiframe pulse when RSYNC pin is in output mode. In input mode (elastic store must be enabled) multiframe mode is only useful when receive signaling reinsertion is enabled.
0 = frame mode
1 = multiframe mode

Bit 1 / RSYNC Mode Select 2 (RSMS2)
T1: RSYNC pin must be programmed in the output frame mode
0 = do not pulse double wide in signaling frames
1 = do pulse double wide in signaling frames
E1: RSYNC pin must be programmed in the output multiframe mode
0 = RSYNC outputs CAS multiframe boundaries
1 = RSYNC outputs CRC4 multiframe boundaries

Bit 2 / RSYNC I/O Select (RSIO). (Note: This bit must be set to zero when elastic store is disabled)
0 = RSYNC is an output
1 = RSYNC is an input (only valid if elastic store enabled)

Bit 3 / RSYNC Multiframe Skip Control (RSMS). This bit is useful in framing format conversions from D4 to ESF. This function is not available when the receive-side elastic store is enabled. RSYNC must be set to output multiframe pulses.
0 = RSYNC outputs a pulse at every multiframe.
1 = RSYNC outputs a pulse at every other multiframe.

Bit 4 / RSYSCLK Mode Select (RSCLKM)
0 = if RSYSCLK is 1.544MHz
1 = if RSYSCLK is 2.048MHz or IBO enabled

Bit 5 / H.100 SYNC Mode (H100EN). See additional details in Section 8.6.
0 = Normal operation
1 = RSYNC and TSSYNC signals are shifted.

Bit 6 / RSYNC Invert (RSYNCINV)
0 = No inversion
1 = Invert RSYNC output

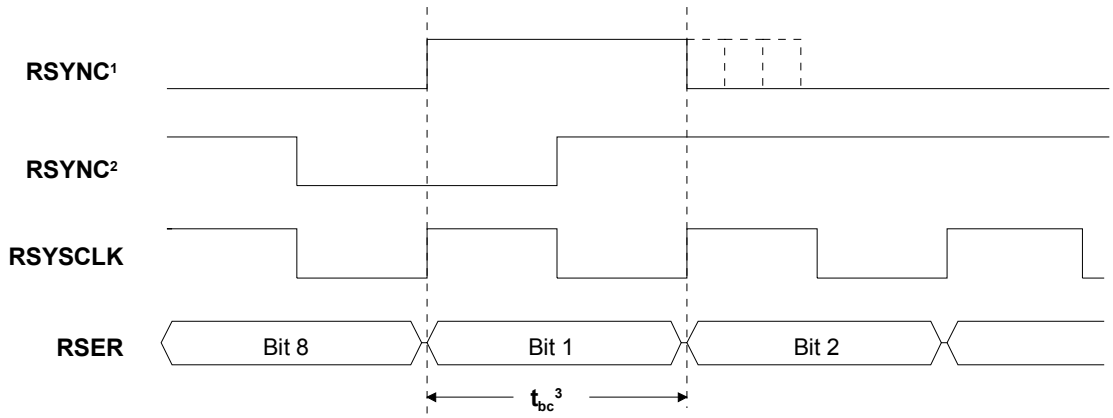
Bit 7 / RCLK Invert (RCLKINV)
0 = No inversion
1 = Invert RCLK as input

8.6 H.100 (CT Bus) Compatibility

The H.100 (or CT Bus) is a synchronous, bit-serial, TDM transport bus operating at 8.192MHz. The H.100 standard also allows compatibility modes to operate at 2.048MHz, 4.096MHz, or 8.192MHz. The control bit H100EN (RIOCR.5), when combined with RSYNCINV and TSSYNCINV, allows the DS26401 to accept a CT-Bus-compatible frame-sync signal ($\overline{\text{CT_FRAME}}$) at the RSYNC and TSSYNC inputs. The following rules apply to the H100EN control bit:

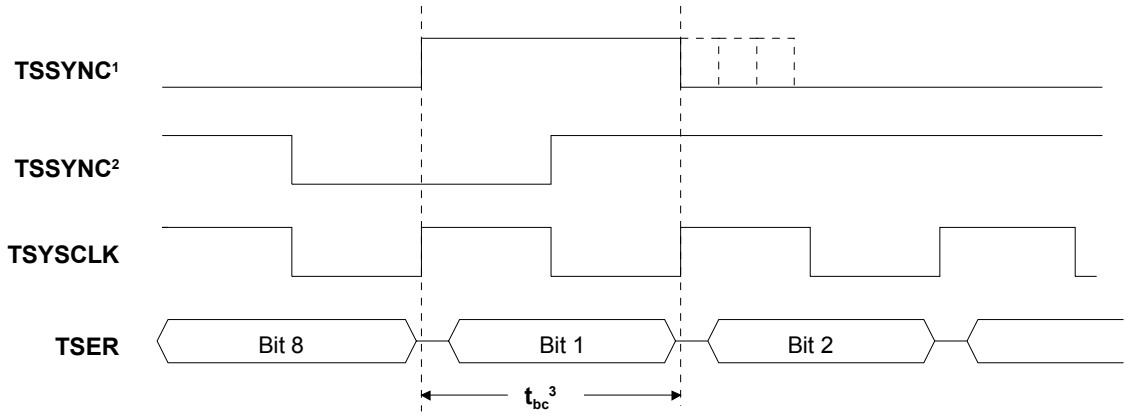
1) The H100EN bit controls the sampling point for the RSYNC (input mode) and TSSYNC only. (The RSYNC output and other sync signals are not affected.)
2) The H100EN bit is always used with the receive and transmit elastic store buffers.
3) The H100EN bit is typically used with 8.192MHz IBO mode (Section 8.21), but can also be used with 4.096MHz IBO mode or 2.048MHz backplane operation.
4) The H100EN bit in RIOCR controls both RSYNC and TSSYNC (i.e., there is no separate control bit for the TSSYNC).
5) The H100EN bit does **not** invert the expected signal; RSYNCINV (RIOCR) and TSSYNCINV (TIOCR) must be set high to invert the inbound sync signals.

Figure 8-1. RSYNC Input in H.100 (CT Bus) Mode



NOTE 1: RSYNC INPUT MODE, IN NORMAL OPERATION
NOTE 2: RSYNC INPUT MODE, H100EN = 1 AND RSYNCINV = 1.
NOTE 3: t_{bc} (BIT CELL TIME) = 122ns (typ). t_{bc} = 244ns OR 488ns ALSO ACCEPTABLE.

Figure 8-2. TSSYNC Input in H.100 (CT Bus) Mode



NOTE 1: TSSYNC IN NORMAL OPERATION.
NOTE 2. TSSYNC WITH H100EN = 1 AND TSSYNCINV = 1.
NOTE 3: t_{bc} (BIT CELL TIME) = 122ns (typ). t_{bc} = 244ns OR 488ns ALSO ACCEPTABLE.

8.7 T1 Receive Status and Information

When a particular event has occurred (or is occurring), the appropriate bit in one of these registers is set to 1. Status bits can operate in either a latched or real-time fashion. Some latched bits can be enabled to generate a hardware interrupt through the $\overline{INT}$ signal.

Real-Time Bits

Some status bits operate in a real-time fashion. These bits are read-only and indicate the present state of an alarm or a condition. Real-time bits remain stable and valid during the host read operation. The current value of the internal status signals can be read at any time from the real-time status registers without changing any of the latched status register bits.

Latched Bits

When an event or an alarm occurs and a latched bit is set to 1, it remains set until the user clears it. These bits typically respond on a change-of-state for an alarm, condition, or event, and operate in a read-then-write fashion. The user should read the value of the desired status bit and then write a 1 to that particular bit location to clear the latched value (write a zero to locations not to be cleared). Once the bit is cleared, it is not set again until the event has occurred again.

Mask Bits

Some of the alarms and events can be either masked or unmasked from the interrupt pin through the interrupt mask registers (RIMx). When unmasked, the $\overline{INT}$ signal is forced low when the enabled event or condition occurs. The $\overline{INT}$ pin is allowed to return high (if no other unmasked interrupts are present) when the user reads, then clears (with a write) the alarm bit that caused the interrupt to occur. Note that the latched status bit and the $\overline{INT}$ pin clear even if the alarm is still present.

Note that some conditions can have multiple status indications. For example, receive loss-of-frame (RLOF) provides the following indications:

RRTS1.0 (RLOF)	Real-time indication that the receiver is not synchronized with incoming data stream. Read-only bit that remains high as long as the condition is present.
RLS1.0 (RLOFD)	Latched indication that the receiver has lost synchronization since the bit was last cleared. Bit will clear when written by the user, even if the condition is still present (rising edge detect of RRTS1.0).
RLS1.4 (RLOFC)	Latched indication that the receiver has reacquired synchronization since the bit was last cleared. Bit will clear when written by the user, even if the condition is still present (falling edge detect of RRTS1.0).

Table 8-1. T1 Alarm Criteria

ALARM	SET CRITERIA	CLEAR CRITERIA
AIS (Blue Alarm) (Note 1)	When over a 3ms window, 5 or fewer zeros are received	When over a 3ms window, 6 or more zeros are received
RAI (Yellow Alarm) 1) D4 Bit 2 Mode (RCR2.0 = 0)	When bit 2 of 256 consecutive channels is set to zero for at least 254 occurrences	When bit 2 of 256 consecutive channels is set to zero for less than 254 occurrences
2) D4 12th F-Bit Mode (RCR2.0 = 1; also referred to as the Japanese Yellow Alarm)	When the 12th framing bit is set to one for two consecutive occurrences	When the 12th framing bit is set to zero for two consecutive occurrences
3) ESF Mode	When 16 consecutive patterns of 00FF appear in the FDL	When 14 or less patterns of 00FF hex out of 16 possible appear in the FDL
LOS (also referred to as Receive Carrier Loss (RCL))	When 192 consecutive zeros are received	When 14 or more ones out of 112 possible bit positions are received starting with the first one received

Note 1: The definition of the Alarm Indication Signal (Blue Alarm) is an unframed all-ones signal. AIS detectors should be able to operate properly in the presence of a 10E-3 error rate, and they should not falsely trigger on a framed all-ones signal. The AIS alarm criteria in the DS26401 has been set to achieve this performance. It is recommended that the RAIS bit be qualified with the RLOF bit.

Note 2: The following terms are equivalent:
RAIS = Blue Alarm
RLOS = RCL
RLOF = Loss of Frame
RRAI = Yellow Alarm

Register Name: **RRTS1**
Register Description: **Receive Real-Time Status Register 1**
Register Address: **0B0h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	RRAI	RAIS	RLOS	RLOF
Default	0	0	0	0	0	0	0	0

All bits in this register are real-time (not latched).

Bit 0 / Receive Loss-of-Frame Condition (RLOF). Set when the DS26401 is not synchronized to the received data stream.

Bit 1 / Receive Loss-of-Signal Condition (RLOS). Set when 192 consecutive zeros have been detected at RPOS and RNEG.

Bit 2 / Receive Alarm Indication Signal Condition (RAIS). Set when an unframed all-ones code is received at RPOS and RNEG.

Bit 3 / Receive Remote Alarm Indication Condition (RRAI). Set when a remote alarm is received at RPOS and RNEG.

Bits 4 to 7 / Unused

Register Name: **RLS1**
Register Description: **Receive Latched Status Register 1**
Register Address: **090h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RRAIC	RAISC	RLOSC	RLOFC	RRAID	RAISD	FLOSD	RLOFD
Default	0	0	0	0	0	0	0	0

All bits in this register are latched and can create interrupts.

Bit 0 / Receive Loss-of-Frame Condition Detect (RLOFD). Rising edge detect of RLOF. Set when the DS26401 has lost synchronized to the received data stream.

Bit 1 / Receive Loss-of-Signal Condition Detect (RLOSD). Rising edge detect of RLOS. Set when 192 consecutive zeros have been detected at RPOS and RNEG.

Bit 2 / Receive Alarm Indication Signal Condition Detect (RAISD). Rising edge detect of RAIS. Set when an unframed all-ones code is received at RPOS and RNEG.

Bit 3 / Receive Remote Alarm Indication Condition Detect (RRAID). Rising edge detect of RRAI. Set when a remote alarm is received at RPOS and RNEG.

Bit 4 / Receive Loss-of-Frame Condition Clear (RLOFC). Falling edge detect of RLOF. Set when an RLOF condition has cleared.

Bit 5 / Receive Loss-of-Signal Condition Clear (RLOSC). Falling edge detect of RLOS. Set when an RLOS condition has cleared.

Bit 6 / Receive Alarm Indication Signal Condition Clear (RAISC). Falling edge detect of RAIS. Set when a RAIS condition has cleared.

Bit 7 / Receive Remote Alarm Indication Condition Clear (RRAIC). Falling edge detect of RRAI. Set when a RRAI condition has cleared.

Register Name: **RIM1**
Register Description: **Receive Interrupt Mask Register 1**
Register Address: **0A0h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RRAIC	RAISC	RLOSC	RLOFC	RRAID	RAISD	RLOSD	RLOFD
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Loss-of-Frame Condition Detect (RLOFD)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Receive Loss-of-Signal Condition Detect (RLOSD)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Receive Alarm Indication Signal Condition Detect (RAISD)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Receive Remote Alarm Indication Condition Detect (RRAID)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Receive Loss-of-Frame Condition Clear (RLOFC)
0 = interrupt masked
1 = interrupt enabled

Bit 5 / Receive Loss-of-Signal Condition Clear (RLOSC)
0 = interrupt masked
1 = interrupt enabled

Bit 6 / Receive Alarm Indication Signal Condition Clear (RAISC)
0 = interrupt masked
1 = interrupt enabled

Bit 7 / Receive Remote Alarm Indication Condition Clear (RRAIC)
0 = interrupt masked
1 = interrupt enabled

Register Name: **RLS2**
Register Description: **Receive Latched Status Register 2**
Register Address: **091h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RPDV	—	COFA	8ZD	16ZD	SEFE	B8ZS	FBE
Default	0	0	0	0	0	0	0	0

All bits in this register are latched. This register does not create interrupts.

Bit 0 / Frame Bit Error Event (FBE). Set when an Ft (D4) or FPS (ESF) framing bit is received in error.

Bit 1 / B8ZS Codeword Detect Event (B8ZS). Set when a B8ZS codeword is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not. This bit is useful for automatically setting the line coding.

Bit 2 / Severely Errored Framing Event (SEFE). Set when 2 out of 6 framing bits (Ft or FPS) are received in error.

Bit 3 / Sixteen Zero Detect Event (16ZD). Set when a string of at least 16 consecutive zeros (regardless of the length of the string) have been received at RPOS and RNEG.

Bit 4 / Eight Zero Detect Event (8ZD). Set when a string of at least eight consecutive zeros (regardless of the length of the string) have been received at RPOS and RNEG.

Bit 5 / Change-of-Frame Alignment Event (COFA). Set when the last resync resulted in a change of frame or multiframe alignment.

Bit 6 / Unused

Bit 7 / Receive Pulse Density Violation Event (RPDV). Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.

Register Name: **RRTS3**
Register Description: **Receive Real-Time Status Register 3**
Register Address: **0B2h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	LORC	LSP	LDN	LUP
Default	0	0	0	0	0	0	0	0

All bits in this register are real-time (not latched).

Bit 0 / Loop-Up Code Detected Condition (LUP). Set when the loop-up code as defined in the RUPCD1/2 register is being received.

Bit 1 / Loop-Down Code Detected Condition (LDN). Set when the loop-down code as defined in the RDNCD1/2 register is being received.

Bit 2 / Spare Code Detected Condition (LSP). Set when the spare code as defined in the RSCD1/2 registers is being received.

Bit 3 / Loss-of-Receive Clock Condition (LORC). Set when the RCLK pin has not transitioned for one channel time.

Bits 4 to 7 / Unused

Register Name: **RLS3**
Register Description: **Receive Latched Status Register 3**
Register Address: **092h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	LORCC	LSPC	LDNC	LUPC	LORCD	LSPD	LDND	LUPD
Default	0	0	0	0	0	0	0	0

All bits in this register are latched and can create interrupts.

Bit 0 / Loop-Up Code Detected Condition Detect (LUPD). Rising edge detect of LUP. Set when the loop-up code as defined in the RUPCD1/2 register is being received.

Bit 1 / Loop-Down Code Detected Condition Detect (LDND). Rising edge detect of LDN. Set when the loop-down code as defined in the RDNCD1/2 register is being received.

Bit 2 / Spare Code Detected Condition Detect (LSPD). Rising edge detect of LSP. Set when the spare code as defined in the RSCD1/2 registers is being received.

Bit 3 / Loss of Receive Clock Condition Detect (LORCD). Rising edge detect of LORC. Set when the RCLK pin has not transitioned for one channel time.

Bit 4 / Loop-Up Code Detected Condition Clear (LUPC). Falling edge detect of LUP. Set when a loop-up condition was detected and then removed.

Bit 5 / Loop-Down Code Detected Condition Clear (LDNC). Falling edge detect of LDN. Set when a loop-down condition was detected and then removed.

Bit 6 / Spare Code Detected Condition Clear (LSPC). Falling edge detect of LSP. Set when a spare-code match condition was detected and then removed.

Bit 7 / Loss-of-Receive Clock Condition Clear (LORCC). Falling edge detect of LORC. Set when a LORC condition was detected and then removed.

Register Name: **RIM3**
Register Description: **Receive Interrupt Mask Register 3**
Register Address: **0A2h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	LORCC	LSPC	LDNC	LUPC	LORCD	LSPD	LDND	LUPD
Default	0	0	0	0	0	0	0	0

Bit 0 / Loop-Up Code Detected Condition Detect (LUPD)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Loop-Down Code Detected Condition Detect (LDND)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Spare Code Detected Condition Detect (LSPD)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Loss-of-Receive Clock Condition Detect (LORCD)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Loop-Up Code Detected Condition Clear (LUPC)
0 = interrupt masked
1 = interrupt enabled

Bit 5 / Loop-Down Code Detected Condition Clear (LDNC)
0 = interrupt masked
1 = interrupt enabled

Bit 6 / Spare Code Detected Condition Clear (LSPC)
0 = interrupt masked
1 = interrupt enabled

Bit 7 / Loss-of-Receive Clock Condition Clear (LORCC)
0 = interrupt masked
1 = interrupt enabled

Register Name: **RLS4**
Register Description: **Receive Latched Status Register 4**
Register Address: **093h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RESF	RESEM	RSLIP	—	RSCOS	1SEC	TIMER	RMF
Default	0	0	0	0	0	0	0	0

All bits in this register are latched and can create interrupts.

Bit 0 / Receive Multiframe Event (RMF). Set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries.

Bit 1 / Timer Event (TIMER). Follows the error counter update interval as determined by the ECUS bit in the error counter configuration register (ERCNT).

T1: Set on increments of 1 second or 42ms based on RCLK.
E1: Set on increments of 1 second or 62.5ms based on RCLK.

Bit 2 / One-Second Timer (1SEC). Set on every one-second interval based on RCLK.

Bit 3 / Receive Signaling Change-of-State Event (RSCOS). Set when any channel selected by the receive signaling change-of-state interrupt-enable registers (RSCSE1 through RSCSE3), changes signaling state.

Bit 4 / Unused

Bit 5 / Receive Elastic Store Slip Occurrence Event (RSLIP). Set when the receive-elastic store has either repeated or deleted a frame.

Bit 6 / Receive Elastic Store Empty Event (RESEM). Set when the receive-elastic store buffer empties and a frame is repeated.

Bit 7 / Receive Elastic Store Full Event (RESF). Set when the receive-elastic store buffer fills and a frame is deleted.

Register Name: **RIM4**
Register Description: **Receive Interrupt Mask Register 4**
Register Address: **0A3h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RESF	RESEM	RSLIP	—	RSCOS	1SEC	TIMER	RMF
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Multiframe Event (RMF)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Timer Event (TIMER)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / One-Second Timer (1SEC)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Receive Signaling Change-of-State Event (RSCOS)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Unused. Must be set = 0 for proper operation.

Bit 5 / Receive Elastic Store Slip Occurrence Event (RSLIP)
0 = interrupt masked
1 = interrupt enabled

Bit 6 / Receive Elastic Store Empty Event (RESEM)
0 = interrupt masked
1 = interrupt enabled

Bit 7 / Receive Elastic Store Full Event (RESF)
0 = interrupt masked
1 = interrupt enabled

Register Name: **RLS7**
Register Description: **Receive Latched Status Register 7**
Register Address: **096h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RRAI-CI	RAIS-CI	RSLC96	RFDLF	BC	BD
Default	0	0	0	0	0	0	0	0

All bits in this register are latched and can create interrupts.

Bit 0 / BOC Detect Event (BD). Set when a valid BOC has been detected (with the BOC filter applied) (Section 11.11)

Bit 1 / BOC Clear Event (BC). Set when a valid BOC is no longer detected (with the disintegration filter applied). (Section 11.11)

Bit 2 / Receive FDL Register Full Event (RFDLF). Set when the 8-bit RFDL register is full. Useful for SLC-96 operation, or manual extraction of FDL data bits (Sections 11.12 and 11.13).

Bit 3 / Receive SLC-96 Alignment Event (RSLC96). Set when a valid SLC-96 alignment pattern is detected in the fs-bit stream, and the RSLCx registers have data available for retrieval (Section 11.12).

Bit 4 / Receive AIS-CI Detect (RAIS-CI). Set when an AIS-CI pattern has been detected by the receiver (see Section 11.5.1). This bit is set only if an AIS condition is being detected (RRTS1.2). This is a latched bit that must be cleared by the host, and sets again each time the AIS-CI pattern is detected (approximately every 1.2 seconds).

Bit 5 / Receive RAI-CI Detect (RRAI-CI). Set when an RAI-CI pattern has been detected by the receiver (see Section 11.5.1). This bit is active in ESF-framing mode only, and sets only if an RAI condition is being detected (RRTS1.3). When the host reads (and clears) this bit, it will set again each time the RAI-CI pattern is detected (approximately every 1.1 seconds).

Bits 6, 7 / Unused

Register Name: **RIM7**
Register Description: **Receive Interrupt Mask Register 7 (BOC/FDL)**
Register Address: **A6h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RRAI-CI	RAIS-CI	RSLC96	RFDLF	BC	BD
Default	0	0	0	0	0	0	0	0

Bit 0 / BOC Detect Event (BD)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / BOC Clear Event (BC)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Receive FDL Register Full (RFDLF)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Receive SLC-96 (RSLC96)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Receive AIS-CI (RAIS-CI)
0 = interrupt masked
1 = interrupt enabled

Bit 5 / Receive RAI-CI (RRAI-CI)
0 = interrupt masked
1 = interrupt enabled

Bits 6, 7 / Unused. Must be set = 0 for proper operation.

8.7.1 Receive AIS-CI and RAI-CI Detection

AIS-CI is a repetitive pattern of 1.26 seconds. It consists of 1.11 seconds of an unframed all ones pattern and 0.15 seconds of all ones modified by the AIS-CI signature. The AIS-CI signature is a repetitive pattern 6176 bits in length in which, if the first bit is numbered bit 0, bits 3088, 3474 and 5790 are logical zeros and all other bits in the pattern are logical ones (T1.403). AIS-CI is an unframed pattern and therefore is defined for all T1 framing formats. The RAIS-CI bit is set when the AIS-CI pattern has been detected and RAIS (RRTS1.2) is set. RAIS-CI is a latched bit and should be cleared by the host when read. RAIS-CI will continue to set approximately every 1.2 seconds that the condition is present. The host will need to 'poll' the bit, in conjunction with the normal AIS indicators to determine when the condition has cleared.

RAI-CI is a repetitive pattern within the ESF data link with a period of 1.08 seconds. It consists of sequentially interleaving 0.99 seconds of "00000000 11111111" (right-to-left) with 90ms of "00111110 11111111". The RRAI-CI bit is set when a bit-oriented code of "00111110 11111111" is detected while RRAI (RRTS1.3) is set. The RRAI-CI detector uses the receive BOC filter bits (RBF0 & RBF1) located in RBOCC to determine the integration time for RAI-CI detection. Like RAIS-CI, the RRAI-CI bit is latched and should be cleared by the host when read. RRAI-CI will continue to set approximately every 1.1 seconds that the condition is present. The host will need to 'poll' the bit, in conjunction with the normal RAI indicators to determine when the condition has cleared. It may be useful to enable the 200ms ESF RAI integration time with the RAIIE control bit (RCR2.1) in networks that use RAI-CI.

8.8 T1 Receive-Side Digital Milliwatt Code Generation

Receive-side digital milliwatt code generation involves using the receive-digital milliwatt registers (T1RDMR1/2/3) to determine which of the 24 T1 channels of the T1 line going to the backplane should be overwritten with a digital milliwatt pattern. The digital milliwatt code is an 8-byte repeating pattern that represents a 1kHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). Each bit in the T1RDMRx registers, represents a particular channel. If a bit is set to 1, then the receive data in that channel is replaced with the digital milliwatt code. If a bit is set to zero, no replacement occurs.

Register Name: **RDMWE1, RDMWE2, RDMWE3**
Register Description: **T1 Receive-Digital Milliwatt-Enable Registers**
Register Address: **03Ch, 03Dh, 03Eh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RDMWE1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RDMWE2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RDMWE3**

Bits 0 to 7 / Receive-Digital Milliwatt Enable for Channels 1 to 24 (CH1 to CH24)

0 = Do not affect the receive data associated with this channel.
1 = Replace the receive data associated with this channel with digital milliwatt code.

8.9 T1 Error Count Registers

The DS26401 contains three T1 performance counters that are used to accumulate line coding errors, path errors, and synchronization errors. Counter update options include one-second boundaries, 42ms (T1 mode only), 62.5ms (E1 mode only), or manually. See the *Error Counter Configuration Register* (ERCNT) section. When updated automatically, the user can use the interrupt from the timer to determine when to read these registers. The line-code violation count register has the potential to saturate, but the bit error would have to exceed 10E-2 before this would occur. All other counters roll over.

Several options are available for latching the performance counters:

1) Each framer's counters are latched independently based on independent one-second interval timers.
2) Each framer's counters are latched independently based on independent 42ms interval timers.
3) Each framer's counters are latched independently with a low-to-high transition on the respective MECU control bit.
4) Counters from selected framers are latched synchronously at the one-second interval supplied by Framer #1.
5) Counters from selected framers are synchronously latched manually with the global counter latch-enable (GCLE) bit in GCR1.

The following table shows control bit settings in the ERCNT register to support each of the five modes discussed above.

Control Bit	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
EAMS	0	0	1	0	1
ECUS	0	1	X	0	0
MECU	0	0	0 to 1	0	0
MCUS	0	0	0	0	1
1SECS	0	0	0	1	0

Register Name: **ERCNT**
Register Description: **Error Counter Configuration Register**
Register Address: **086h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	1SECS	MCUS	MECU	ECUS	EAMS	FSBE	MOSCRF	LCVCRF
Default	0	0	0	0	0	0	0	0

Bit 0 / T1 Line-Code Violation Count Register Function Select (LCVCRF)
0 = do not count excessive zeros
1 = count excessive zeros

Bit 1 / Multiframe Out-of-Sync Count Register Function Select (MOSCRF)
0 = count errors in the framing bit position
1 = count the number of out-of-sync multiframes

Bit 2 / PCVCR Fs-Bit Error Report Enable (FSBE)
0 = do not report bit errors in Fs-bit position; only Ft bit position
1 = report bit errors in Fs-bit position as well as Ft bit position

Bit 3 / Error Accumulation Mode Select (EAMS)
0 = ERCNT.4 determines accumulation time (timed update)
1 = ERCNT.5 determines accumulation time (manual update)

Bit 4 / Error Counter Update Select (ECUS)
T1 mode:
0 = Update error counters once a second
1 = Update error counters every 42ms (336 frames)
E1 mode:
0 = Update error counters once a second
1 = Update error counters every 62.5ms (500 frames)

Bit 5 / Manual Error Counter Update (MECU). When enabled by ERCNT.3, the changing of this bit from 0 to 1 allows the next clock cycle to load the error counter registers with the latest counts and reset the counters. The user must wait a minimum of 250μs before reading the error count registers to allow for proper update.

Bit 6 / Manual Counter Update Select (MCUS). When manual update mode is enabled with EAMS, this bit can be used to allow the GLCE bit in GCR1 to latch all counters. Useful for synchronously latching counters of multiple framers.
0 = MECU is used to manually latch counters.
1 = GLCE is used to manually latch counters.

Bit 7 / One-Second Select (1SECS). When timed update is enabled by EAMS, setting this bit for a specific framer allows that framer's counters to latch on the one-second reference from Framer #1.
0 = Use internally generated one-second timer.
1 = Use one-second timer from Framer #1.

8.9.1 T1 Line-Code Violation Count Register (LCVCR)

T1 code violations are defined as bipolar violations (BPVs) or excessive zeros. If the B8ZS mode is set for the receive side, then B8ZS codewords are not counted. This counter is always enabled; it is not disabled during receive loss-of-synchronization (RLOF = 1) conditions. See Table 8-2 for details of exactly what the LCVCRs count.

Table 8-2. T1 Line-Code Violation Counting Options

COUNT EXCESSIVE ZEROS? (ERCNT.0)	B8ZS ENABLED? (RCR1.6)	WHAT IS COUNTED IN THE LCVCRs
No	No	BPVs
Yes	No	BPVs + 16 consecutive zeros
No	Yes	BPVs (B8ZS codewords not counted)
Yes	Yes	BPVs + 8 consecutive zeros

Register Name: **LCVCR1**
Register Description: **Line-Code Violation Count Register 1**
Register Address: **050h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	LCVC15	LCVC14	LCVC13	LCVC12	LCVC11	LCVC10	LCVC9	LCCV8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Line-Code Violation Counter Bits 8 to 15 (LCVC8 to LCVC15). LCV15 is the MSB of the 16-bit code violation count.

Register Name: **LCVCR2**
Register Description: **Line-Code Violation Count Register 2**
Register Address: **051h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	LCVC7	LCVC6	LCVC5	LCVC4	LCVC3	LCVC2	LCVC1	LCVC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Line-Code Violation Counter Bits 0 to 7 (LCVC0 to LCVC7). LCV0 is the LSB of the 16-bit code violation count

8.9.2 T1 Path-Code Violation Count Register (PCVCR)

The path-code violation count register records either Ft, Fs, or CRC6 errors in T1 frames. When the receive side of a framer is set to operate in the T1 ESF framing mode, PCVCR records errors in the CRC6 codewords. When set to operate in the T1 D4 framing mode, PCVCR counts errors in the Ft framing bit position. Through the ERCNT.2 bit, a framer can be programmed to also report errors in the Fs framing bit position. The PCVCR is disabled during receive loss-of-synchronization (RLOF = 1) conditions. See Table 8-3 for a detailed description of exactly what errors the PCVCR counts.

Table 8-3. T1 Path-Code Violation Counting Arrangements

FRAMING MODE	COUNT Fs ERRORS?	WHAT IS COUNTED IN THE PCVCRs
D4	No	Errors in the Ft pattern
D4	Yes	Errors in both the Ft & Fs patterns
ESF	Don't Care	Errors in the CRC6 codewords

Register Name: **PCVCR1**
Register Description: **Path-Code Violation Count Register 1**
Register Address: **052h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	PCVC15	PCVC14	PCVC13	PCVC12	PCVC11	PCVC10	PCVC9	PCVC8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Path-Code Violation Counter Bits 8 to 15 (PCVC8 to PCVC15). PCVC15 is the MSB of the 16-bit path-code violation count

Register Name: **PCVCR2**
Register Description: **Path-Code Violation Count Register 2**
Register Address: **053h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	PCVC7	PCVC6	PCVC5	PCVC4	PCVC3	PCVC2	PCVC1	PCVC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Path-Code Violation Counter Bits 0 to 7 (PCVC0 to PCVC7). PCVC0 is the LSB of the 16-bit path-code violation count.

8.9.3 T1 Frames Out-of-Sync Count Register (FOSCR)

The FOSCR is used to count the number of multiframes that the receive synchronizer is out of sync. This number is useful in ESF applications needing to measure the parameters loss-of-frame count (LOFC) and ESF error events as described in AT&T publication TR54016. When the FOSCR is operated in this mode, it is not disabled during receive loss of synchronization (RLOF = 1) conditions. The FOSCR has alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the FOSCR is operated in this mode, it is disabled during receive loss-of-synchronization (RLOF = 1) conditions. See Table 8-4 for a detailed description of what the FOSCR is capable of counting.

Table 8-4. T1 Frames Out-of-Sync Counting Arrangements

FRAMING MODE (RCR1.5)	COUNT MOS OR F–BIT ERRORS (ERCNT.1)	WHAT IS COUNTED IN THE FOSCRs
D4	MOS	Number of multiframes out of sync
D4	F-Bit	Errors in the Ft pattern
ESF	MOS	Number of multiframes out of sync
ESF	F-Bit	Errors in the FPS pattern

Register Name: **FOSCR1**
Register Description: **Frames Out-of-Sync Count Register 1**
Register Address: **054h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	FOS15	FOS14	FOS13	FOS12	FOS11	FOS10	FOS9	FOS8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Frames Out-of-Sync Counter Bits 8 to 15 (FOS8 to FOS15). FOS15 is the MSB of the 16-bit frames out-of-sync count.

Register Name: **FOSCR2**
Register Description: **Frames Out-of-Sync Count Register 2**
Register Address: **055h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	FOS7	FOS6	FOS5	FOS4	FOS3	FOS2	FOS1	FOS0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Frames Out-of-Sync Counter Bits 0 to 7 (FOS0 to FOS7). FOS0 is the LSB of the 16-bit frames out-of-sync count.

8.10 DS0 Monitoring Function

The DS26401 can monitor one DS0 (64kbps) channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the receive direction, the RCM0 to RCM4 bits in the RDS0SEL register need to be properly set and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the receive DS0 (RDS0M) register. The RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate T1 channel. T1 channels 1 through 24 map to register values 0 through 23. For example, if DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into RDS0SEL:

RCM4 = 0
RCM3 = 1
RCM2 = 1
RCM1 = 1
RCM0 = 0

Register Name: **RDS0SEL**
Register Description: **Receive-Channel Monitor Select**
Register Address: **012h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	RCM4	RCM3	RCM2	RCM1	RCM0
Default	0	0	0	0	0	0	0	0

Bits 0 to 4 / Receive-Channel Monitor Bits (RCM0 to RCM4). RCM0 is the LSB of a 5-bit channel select that determines which receive-DS0 channel data appears in the RDS0M register.

Bits 5–7 / Unused. Must be set = 0 for proper operation.

Register Name: **RDS0M**
Register Description: **Receive-DS0 Monitor Register**
Register Address: **060h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	B1	B2	B3	B4	B5	B6	B7	B8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Receive-DS0 Channel Bits (B1 to B8). Receive-channel data that has been selected by the receive-channel monitor select register. B8 is the LSB of the DS0 channel (last bit to be received).

8.11 T1 Receive Signaling Operation

There are two methods to access receive-signaling data: through processor-based (i.e., software-based) signaling or hardware-based signaling. Processor-based refers to access through the receive-signaling registers, RS1–RS12. Hardware-based refers to the RSIG pin. Both methods can be used simultaneously.

8.11.1 Processor-Based Signaling

The robbed-bit signalingis sampled in the receive data stream and copied into the receive-signaling registers, RS1 through RS12. The signaling information in these registers is always updated on multiframe boundaries. This function is always enabled.

8.11.2 Change of State

To avoid constant monitoring of the receive-signaling registers, the DS26401 can be programmed to alert the host when any specific channel or channels undergo a change of their signaling state. For T1, RSCSE1 through RSCSE3 are used to select which channels can cause a change-of-state indication. The change of state is indicated in latched status register 4 (RLS4.3). If signaling integration is enabled, the new signaling state must be constant for three multiframes before a change-of-state indication is indicated. The user can enable the $\overline{INT}$ pin to toggle low upon detection of a change in signaling by setting the interrupt mask bit RIM4.3. The signaling integration mode is global and cannot be enabled on a channel-by-channel basis.

The user can identify which channels have undergone a signaling change of state by reading the receive-signaling status (RSS1–RSS3) registers. The information from these registers tells the user which RSx register to read for the new signaling data. All changes are indicated in the RSS1–RSS3 registers regardless of the RSCSE1–RSCSE3 registers.

8.11.3 Hardware-Based Receive Signaling

In hardware-based signaling, the signaling data can be obtained from the RSER pin or the RSIG pin. RSIG is a signaling-PCM stream output on a channel-by-channel basis from the signaling buffer. The T1 robbed-bit signaling data is still present in the original data stream at RSER. The signaling buffer provides signaling data to the RSIG pin and also allows signaling data to be reinserted into the original data stream in a different alignment that is determined by a multiframe signal from the RSYNC pin. In this mode, the receive-elastic store can be enabled or disabled. If the receive-elastic store is enabled, then the backplane clock (RSYSCLK) can be either 1.544MHz or 2.048MHz. If IBO mode is enabled, then RSYSCLK can also be 4.096MHz, 8.192MHz, or 16.384MHz. In the ESF-framing mode, the ABCD signaling bits are output on RSIG in the lower nibble of each channel. The RSIG data is updated once a multiframe (3ms) unless a freeze is in effect. In the D4 framing mode, the AB signaling bits are output twice on RSIG in the lower nibble of each channel. Hence, bits 5 and 6 contain the same data as bits 7 and 8, respectively, in each channel. The RSIG data is updated once a multiframe (1.5ms) unless a freeze is in effect.

8.11.4 Signaling Debounce

When signaling integration is enabled, the signaling data at RSIG is automatically debounced. Signaling must be constant for three multiframes before being updated at RSIG. Signaling debounce is enabled on a global basis.

8.11.5 Receive-Signaling Reinsertion at RSER

In this mode, the user provides a multiframe sync at the RSYNC pin, and the signaling data is reinserted based on this alignment. In T1 mode, this results in two copies of the signaling data in the RSER data stream. The original signaling data is based on the Fs/ESF frame positions and the realigned data is based on the user-supplied multiframe sync applied at RSYNC. In voice channels, this extra copy of signaling data is of little consequence. Reinsertion can be avoided in data channels since this feature is activated on a per-channel basis. For reinsertion, the elastic store must be enabled, however, the backplane clock can be either 1.544MHz or 2.048MHz.

Signaling reinsertion mode is enabled on a per-channel basis by setting the receive-signaling reinsertion channel-select bit high in the RSIx registers. The channels that are to have signaling reinserted are selected by writing to the RSI1–RSI3 registers for T1.

8.11.6 Force Receive-Signaling All Ones

In T1 mode, the user can, on a per-channel basis, force the robbed-bit signaling bit positions to 1. This is done by using the RSAOI registers. The user sets the channel-select bit in the RSAOI1–RSAOI3 registers to select the channels that are to have the signaling forced to 1.

8.11.7 Receive-Signaling Freeze

The signaling data in the four-multiframe signaling buffer is frozen in a known good state upon either a loss-of-synchronization (OOF event), carrier loss, or change-of-frame alignment. This action meets the requirements of BellCore TR-TSY-000170 for signaling freezing. To allow this freeze action to occur, the RSFE control bit (RSIGC.1) should be set high. The user can force a freeze by setting the RSFF control bit (RSIGC.2) high. The RSIGF output pin provides a hardware indication that a freeze is in effect. The four-multiframe buffer provides a three-multiframe delay in the signaling bits provided at the RSIG pin (and at the RSER pin if receive-signaling reinsertion is enabled). When freezing is enabled (RSFE = 1), the signaling data is held in the last known good state until the corrupting error condition subsides. When the error condition subsides, the signaling data is held in the old state for at least an additional 9ms (or 4.5ms in D4 framing mode) before being allowed to be updated with new signaling data.

Register Name: **RSIGC**
Register Description: **Receive Signaling Control Register**
Register Address: **013h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	RFSA1	—	RSFF	RSFE	RSIE
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive-Signaling Integration Enable (RSIE)
0 = signaling changes of state reported on any change in selected channels
1 = signaling must be stable for three multiframes for a change of state to be reported

Bit 1 / Receive-Signaling Freeze Enable (RSFE)
0 = no freezing of receive-signaling data occurs
1 = allow freezing of receive-signaling data at RSIG (and RSER if receive-signaling reinsertion is enabled)

Bit 2 / Receive-Signaling Force Freeze (RSFF). Freezes receive-side signaling at RSIG (and RSER if receive-signaling reinsertion is enabled); overrides receive-freeze enable (RFE).
0 = do not force a freeze event
1 = force a freeze event

Bits 3, 5–7 / Unused. Must be set = 0 for proper operation.

Bit 4 / Receive-Force Signaling All Ones (RFSA1)
0 = do not force robbed bit signaling to all ones
1 = force signaling bits to all ones on a per-channel basis according to the RSAOI1–RSAOI3 registers

Register Name: **RS1 to RS12**
Register Description: **Receive Signaling Registers**
Register Address: **040h to 04Bh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only two signaling bits per channel (A and B). In the D4 framing mode, the framer repeats the A and B signaling data in the C and D bit locations. Therefore, when the framer is operated in D4 framing mode, the user needs to retrieve the signaling bits every 1.5ms as opposed to 3ms for ESF mode. The receive-signaling registers are frozen and not updated during a loss-of-sync condition. They contain the most recent signaling information before the OOF occurred.

(MSB)							**(LSB)**	
CH1-A	CH1-B	CH1-C	CH1-D	CH13-A	CH13-B	CH13-C	CH13-D	**RS1**
CH2-A	CH2-B	CH2-C	CH2-D	CH14-A	CH14-B	CH14-C	CH14-D	**RS2**
CH3-A	CH3-B	CH3-C	CH3-D	CH15-A	CH15-B	CH15-C	CH15-D	**RS3**
CH4-A	CH4-B	CH4-C	CH4-D	CH16-A	CH16-B	CH16-C	CH16-D	**RS4**
CH5-A	CH5-B	CH5-C	CH5-D	CH17-A	CH17-B	CH17-C	CH17-D	**RS5**
CH6-A	CH6-B	CH6-C	CH6-D	CH18-A	CH18-B	CH18-C	CH18-D	**RS6**
CH7-A	CH7-B	CH7-C	CH7-D	CH19-A	CH19-B	CH19-C	CH19-D	**RS7**
CH8-A	CH8-B	CH8-C	CH8-D	CH20-A	CH20-B	CH20-C	CH20-D	**RS8**
CH9-A	CH9-B	CH9-C	CH9-D	CH21-A	CH21-B	CH21-C	CH21-D	**RS9**
CH10-A	CH10-B	CH10-C	CH10-D	CH22-A	CH22-B	CH22-C	CH22-D	**RS10**
CH11-A	CH11-B	CH11-C	CH11-D	CH23-A	CH23-B	CH23-C	CH23-D	**RS11**
CH12-A	CH12-B	CH12-C	CH12-D	CH24-A	CH24-B	CH24-C	CH24-D	**RS12**

Register Name: **RSS1, RSS2, RSS3**
Register Description: **Receive Signaling Status Registers**
Register Address: **098h, 099h, 09Ah [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

When a channel's signaling data changes state, the respective bit in registers RSS1–RSS3 is set and latched. The RSCOS bit (RLSR4.3) is set if the channel was also enabled by setting the appropriate bit in RSCSE1–3. The $\overline{INT}$ signal goes low if enabled by the interrupt mask bit RIM4.3.

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RSS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RSS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RSS3**

Note: *Status bits in this register are latched.*

Register Name: **RSCSE1, RSCSE2, RSCSE3**
Register Description: **Receive-Signaling Change-of-State Enable**
Register Address: **0A8h, 0A9h, 0AAh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Setting any of the CH1 through CH24 bits in the RSS1 through RSS3 registers cause RSCOS (RLSR4.3) to be set when that channel's signaling data changes state.

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RSCSE1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RSCSE2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RSCSE3**

Register Name: **RSI1, RSI2, RSI3, RSI4**
Register Description: **Receive-Signaling Reinsertion Enable Registers**
Register Address: **0C8h, 0C9h, 0CAh, 0CBh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Setting any of the CH1 through CH24 bits in the RSI1 through RSI3 registers causes signaling data to be reinserted for the associated channel. RSI4 is used for 2.048MHz backplane operation.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RSI1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RSI2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RSI3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**RSI4***

Register Name: **RSAOI1, RSAOI2, RSAOI3,**
Register Description: **Receive-Signaling All-Ones Insertion Registers**
Register Address: **038h, 039h, 03Ah [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Setting any of the CH1 through CH24 bits in the RSAOI1 through RSAOI3 registers causes signaling data to be replaced with logic ones as received at the backplane.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RSAOI1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RSAOI2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RSAOI3**

8.12 T1 Receive Per-Channel Idle Code Insertion

Channel data can be replaced by an idle code on a per-channel basis in the transmit and receive directions. Twenty-four receive idle definition registers (RIDR1–RIDR24) are provided to set the 8-bit idle code for each channel. The receive-channel idle code-enable registers (RCICE1–3) are used to enable idle code replacement on a per-channel basis.

Register Name: **RIDR1 to RIDR24**
Register Description: **Receive Idle-Code Definition Registers 1 to 24**
Register Address: **020h to 037h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Per-Channel Idle Code Bits (C0 to C7). C0 is the LSB of the code (this bit is transmitted last). Address 20H is for channel 1; address 37H is for channel 24.

Register Name: **RCICE1, RCICE2, RCICE3**
Register Description: **Receive-Channel Idle Code-Enable Registers**
Register Address: **0D0h, 0D1h, 0D2h [+ (200h * n) : where n = 0 to 7, for Ports 1 to 8]**

The receive-channel idle code-enable registers (RCICE1/2/3) are used to determine which of the 24 T1 channels from the T1 line to the backplane should be overwritten with the code placed in the receive idle-code definition register.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RCICE1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RCICE2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RCICE3**

Bits 0 to 7 / Receive Channels 1 to 24 Code Insertion Control Bits (CH1 to CH24)
0 = do not insert data from the idle code array into the receive data stream
1 = insert data from the idle code array into the receive data stream

8.13 Receive-Channel Blocking Operation

The receive-channel blocking registers (RCBR1/RCBR2/RCBR3/RCBR4) and the transmit-channel blocking registers (TCBR1/TCBR2/TCBR3/TCBR4) control the RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHBLK pins are user-programmable outputs that can be forced high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN-PRI applications. When the appropriate bits are set to 1, the RCHBLK and TCHBLK pin is held high during the entire corresponding channel time. When used in T1 mode, only RCBR1 to RCBR3 and the LSB of RCBR4 are used.

Register Name: **RCBR1, RCBR2, RCBR3, RCBR4**
Register Description: **Receive-Channel Blocking Registers**
Register Address: **0C4h, 0C5h, 0C6h, 0C7h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RCBR1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RCBR2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RCBR3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25/Fbit	**RCBR4***

Bits 0 to 7 / Receive Channels 1 to 32 Channel Blocking Control Bits (CH1 to CH32).

0 = force the RCHBLK pin to remain low during this channel time
1 = force the RCHBLK pin high during this channel time

In T1 mode, the LSB of RCBR4 determines whether or not the RCHBLK signal pulses high during the F-bit time:

RCBR4.0 = 0, do not pulse RCHBLK during the F-bit
RCBR4.0 = 1, pulse RCHBLK during the F-bit

In this mode RCBR4.1 to RCBR4.7 should be set to 0.

8.14 Receive Elastic Stores Operation

The DS26401 contains dual, two-frame elastic stores—one for the receive direction and one for the transmit direction. Both elastic stores are fully independent. The transmit- and receive-side elastic stores can be enabled/disabled independent of each other. Also, each elastic store can interface to either a 1.544MHz or 2.048MHz/4.096MHz/8.192MHz/16.384MHz backplane without regard to the backplane rate for the other elastic store.

The elastic stores have two main purposes. First, they can be used for rate conversion. When the DS26401 is in the T1 mode, the elastic stores can rate-convert the T1 data stream to a 2.048MHz backplane. In E1 mode, the elastic store can rate-convert the E1 data stream to a 1.544MHz backplane. Secondly, they can be used to absorb the differences in frequency and phase between the T1 or E1 data stream and an asynchronous (i.e., not locked) backplane clock (which can be 1.544MHz or 2.048MHz). In this mode, the elastic stores manage the rate difference and perform controlled slips, deleting or repeating frames of data in order to manage the difference between the network and the backplane.

The elastic stores can also be used to multiplex T1 or E1 data streams into higher backplane rates. This is the interleave bus option (IBO), which is discussed in Section 8.21.

Note that the receive-elastic-store status bits are contained in RLS4 with the associated interrupt bits located in RIM4. These bits indicate a receive slip event, or when the e-store FIFO is in a full or empty condition. See the register definition for RLS4 for additional information.

Register Name: **RESCR**
Register Description: **Receive Elastic Store Control Register**
Register Address: **085h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RDATFMT	RGCLKEN	—	RSZS	RESALGN	RESR	RESMDM	RESE
Default	0	0	0	0	0	0	0	0

Note: *RGPCKEN and RDATFMT are not associated with the elastic store and are explained in the fractional support section.*

Bit 0 / Receive-Elastic-Store Enable (RESE)
0 = elastic store is bypassed
1 = elastic store is enabled

Bit 1 / Receive-Elastic Store Minimum Delay Mode (RESMDM)
0 = elastic stores operate at full two-frame depth
1 = elastic stores operate at 32-bit depth

Bit 2 / Receive-Elastic Store Reset (RESR). Setting this bit from zero to 1 forces the read pointer into the same frame that the write pointer is exiting, minimizing the delay through the elastic store. If this command should place the pointers within the slip zone (see bit 4), then an immediate slip occurs and the pointers move back to opposite frames. Should be toggled after RSYSCLK has been applied and is stable. Do not leave this bit set HIGH.

Bit 3 / Receive-Elastic Store Align (RESALGN). Setting this bit from zero to 1 forces the receive-elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command will be executed and the data will be disrupted. Should be toggled after RSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align.

Bit 4 / Receive Slip Zone Select (RSZS). This bit determines the minimum distance allowed between the elastic store read and write pointers before forcing a controlled slip. This bit is only applies during T1 to E1 or E1 to T1 conversion applications.
0 = force a slip at 9 bytes or less of separation (used for clustered blank channels)
1 = force a slip at 2 bytes or less of separation (used for distributed blank channels)

Bit 5 / Unused. Must be set = 0 for proper operation.

Bit 6 / Receive Gapped Clock Enable (RGCLKEN)
0 = RCHCLK functions normally
1 = Enable gapped bit clock output on RCHCLK

Bit 7 / Receive-Channel Data Format (RDATFMT)
0 = 64kbps (data contained in all 8 bits)
1 = 56kbps (data contained in 7 out of the 8 bits)

8.14.1 Mapping T1 Channels Onto a 2.048MHz Backplane

Setting the RSCLKM bit in RIOCR.4 enables the receive-elastic store to operate with a 2.048MHz backplane (32 time slots/frame). In this mode, the user can choose which of the backplane channels on RSER receive the T1 data by programming the receive-blank channel-select registers (RBCS1–4). A logic 1 in the associated bit location forces RSER high for that backplane channel. Typically, the user wants to program 8 channels to be "blanked." The default (power-up) configuration blanks channels 25 to 32, so that the 24 T1 channels are mapped into the first 24 channels of the 2.048MHz backplane. If the user chooses to blank channel 1 (TS0) by setting RBCS1.0 = 1, then the F-bit is passed into the MSB of TS0 on RSER.

For example, if:

RBCS1 = 01h
RBCS2 = 00h
RBCS3 = 01h
RBCS4 = FCh

Then on RSER:

Channel 1 (MSB) = F-bit
Channel 1 (bits 1–7) = all ones
Channels 2–16 = T1 channels 1–15
Channel 17 = all ones
Channels 18–26 = T1 channels 16–24
Channels 27–32 = all ones

Register Name: **RBCS1, RBCS2, RBCS3, RBCS4**
Register Description: **Receive Blank Channel Select Registers**
Register Address: **0C0h, 0C1h, 0C2h, 0C3h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Note that when two or more sequential channels are chosen to be blanked, the receive-slip zone-select bit (RSZS) should be set to zero. If the blank channels are distributed (such as 1, 5, 9, 13, 17, 21, 25, 29), then the RSZS bit can be set to 1, which may provide a lower occurrence of slips in certain applications.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RBCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RBCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RBCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**RBCS4**

Bits 0–7 / Receive Blank Channel Select for Channels 1 to 32 (RBCS1-32).

0 = do not blank this channel (channel data is available on RSER)
1 = RSER is forced to all ones for this channel

8.14.2 Additional Receive-Elastic-Store Information

If the receive-side elastic store is enabled, then the user must provide either a 1.544MHz or 2.048MHz clock at the RSYSCLK pin. For higher rate system clock applications, see the *Interleaved PCM Bus Option* in Section 8.21. The user has the option of either providing a frame/multiframe sync at the RSYNC pin or having the RSYNC pin provide a pulse on frame/multiframe boundaries. If signaling reinsertion is enabled, the robbed-bit signaling data is realigned to the multiframe-sync input on RSYNC. Otherwise, a multiframe-sync input on RSYNC is treated as a simple frame boundary by the elastic store. The framer always indicated frame boundaries on the network side of the elastic store through the RFSYNC output, whether the elastic store is enabled or not. Multiframe boundaries are always indicated through the RMSYNC output. If the elastic store is enabled, RMSYNC outputs the multiframe boundary on the backplane side of the elastic store. When the device is receiving T1, and the backplane is enabled for 2.048MHz operation, the RMSYNC signal outputs the T1 multiframe boundaries as delayed through the elastic store.

If the user selects to apply a 2.048MHz clock to the RSYSCLK pin, then the backplane blank-channel-select registers (RBCS1–4) can be used to determine which channels have the data output at RSER forced to all ones. If the user chooses to blank time slot 0, then the F-bit is passed into the MSB of TS0. If the two-frame elastic buffer either fills or empties, a controlled slip occurs. If the buffer empties, a full frame of data is repeated at RSER, and the RLS4.5 and RLS4.6 bits are set to 1. If the buffer fills, a full frame of data is deleted, and the RLS4.5 and RLS4.7 bits are set to 1.

8.14.2.1 Elastic Store Initialization

There are two elastic-store initializations that can be used to improve performance in certain applications—the elastic-store reset and elastic-store align. Both of these involve the manipulation of the elastic store's read and write pointers, and are useful primarily in synchronous applications (RSYSCLK/TSYSCLK are locked to RCLK/TCLK respectively). The elastic-store reset is used to minimize the delay through the elastic store. The elastic-store align bit is used to center the read/write pointers to the extent possible.

Elastic Store Delay After Initialization

INITIALIZATION	REGISTER BIT	DELAY
Receive-Elastic-Store Reset	RESCR.2	N bytes < Delay < 1 Frame + N bytes
Transmit-Elastic-Store Reset	TESCR.2	N bytes < Delay < 1 Frame + N bytes
Receive-Elastic-Store Align	RESCR.3	1/2 Frame < Delay < 1 ½ Frames
Transmit-Elastic-Store Align	TESCR.3	1/2 Frame < Delay < 1 ½ Frames

N = 9 for RSZS = 0
N = 2 for RSZS = 1

8.14.2.2 Minimum-Delay Mode

Elastic-store minimum-delay mode can be used when the elastic store's system clock is locked to its network clock (i.e., RCLK locked to RSYSCLK for the receive side and TCLK locked to TSYSCLK for the transmit side). RESCR.1 enables the receive-elastic-store minimum-delay mode. When enabled, the elastic stores are forced to a maximum depth of 32 bits instead of the normal two-frame depth. This feature is useful primarily in applications that interface to a 2.048MHz bus. Certain restrictions apply when minimum-delay mode is used. In addition to the restriction mentioned above, RSYNC must be configured as an output when the receive-elastic store is in minimum-delay mode and TSYNC must be configured as an output when transmit-minimum-delay mode is enabled. In a typical application, RSYSCLK and TSYSCLK are locked to RCLK, and RSYNC (frame-output mode) is connected to TSSYNC (frame-input mode). All the slip contention logic in the framer is disabled (since slips cannot occur). On power-up, after the RSYSCLK and TSYSCLK signals have locked to their respective network clock signals, the elastic-store-reset bit (RESCR.2) should be toggled from zero to 1 to ensure proper operation.

8.15 Fractional T1 Support (Gapped-Clock Mode)

The DS26401 can be programmed to output gapped clocks for selected channels in the receive and transmit paths to simplify connections into a USART or LAPD controller in Fractional T1/E1 or ISDN-PRI applications. When the gapped-clock feature is enabled, a gated clock is output on the RCHCLK signal. The channel selection is controlled through the receive-gapped-clock channel-select registers (RGCCS1–RGCCS4). The receive path is enabled for gapped-clock mode with the RGCLKEN bit (RESCR.6). Both 56kbps and 64kbps channel formats are supported as determined by RESCR.7. When 56kbps mode is selected, the clock corresponding to the data/control bit in the channel is omitted (only the seven most significant bits of the channel have clocks).

Register Name: **RGCCS1, RGCCS2, RGCCS3, RGCCS4**
Register Description: **Receive-Gapped-Clock Channel-Select Registers**
Register Address: **0CCh, 0CDh, 0CEh, 0CFh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RGCCS 1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RGCCS 2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RGCCS 3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25/F-Bit	**RGCCS 4***

Bits 0 to 7 / Receive Channels 1 to 32 Gapped-Clock Channel Select Bits (CH1 to CH32)

0 = no clock is present on RCHCLK during this channel time
1 = force a clock on RCHCLK during this channel time. The clock will be synchronous with RCLK if the elastic store is disabled, and synchronous with RSYSCLK if the elastic store is enabled.

***Note that RGCCS4 has two functions:**
When 2.048MHz backplane mode is selected, this register allows the user to enable the gapped clock on RCHCLK for any of the 32 possible backplane channels.

When 1.544MHz backplane mode is selected, the LSB of this register determines whether or not a clock is generated on RCHCLK during the F-bit time:

RGCCS4.0 = 0: do not generate a clock during the F-bit
RGCCS4.0 = 1: generate a clock during the F-bit

In this mode, RGCCS4.1—RGCCS4.7 should be set to 0.

8.16 T1 Bit-Oriented Code (BOC) Controller

The DS26401 contains a BOC generator on the transmit side and a BOC detector on the receive side. The BOC function is available only in T1 mode.

In ESF mode, the DS26401 continuously monitors the receive message bits for a valid BOC message. The BOC-detect (BD) status bit at RLS7.0 is set once a valid message has been detected for time determined by the receive-BOC-filter bits RBF0 and RBF1 in the RBOCC register. The 6-bit BOC message is available in the RBOC register. Once the user has cleared the BD bit, it remains clear until a new BOC is detected (or the same BOC is detected following a BOC-clear event). The BOC-clear (BC) bit at RLS7.1 is set when a valid BOC is no longer being detected for a time determined by the receive-BOC-disintegration bits RBD0 and RBD1 in the RBOCC register.

The BD and BC status bits can create a hardware interrupt on the $\overline{INT}$ signal as enabled by the associated interrupt mask bits in the RIM7 register.

Register Name: **RBOCC**
Register Description: **Receive BOC Control Register**
Register Address: **015h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RBR	—	RBD1	RBD0	—	RBF1	RBF0	—
Default	0	0	0	0	0	0	0	0

Bits 0, 3, 6 / Unused. Must be set = 0 for proper operation.

Bits 1 to 2 / Receive-BOC-Filter Bits (RBF0, RBF1). The BOC filter sets the number of consecutive patterns that must be received without error prior to an indication of a valid message.

RBF1	RBF0	Consecutive BOC Codes for Valid Sequence Identification
0	0	None
0	1	3
1	0	5
1	1	7 (Note 1)

Bits 4 to 5 / Receive-BOC-Disintegration Bits (RBD0, RBD1). The BOC Disintegration filter sets the number of message bits that must be received without a valid BOC in order to set the BC bit indicating that a valid BOC is no longer being received.

RBD1	RBD0	Consecutive Message Bits for BOC Clear Identification
0	0	16
0	1	32
1	0	48
1	1	64 (Note 1)

Bit 7 / Receive-BOC Reset (RBR). A 0-to-1 transition resets the BOC circuitry. Must be cleared and set again for a subsequent reset. Modifications to the RBF0, RBF1, RBD0, and RBD1 bits are not applied to the BOC controller until a BOC reset has been completed.

Note 1: The DS26401's BOC controller does not integrate and disintegrate concurrently. Therefore, if the maximum integration time and the maximum disintegration time are used together, BOC messages that repeat fewer than 11 times may not be detected.

Register Name: **RBOC**
Register Description: **Receive BOC Register**
Register Address: **63h + (200h * n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RBOC5	RBOC4	RBOC3	RBOC2	RBOC1	RBOC0
Default	0	0	0	0	0	0	0	0

The RBOC Register always contains the last valid BOC received.

Bit 0 / BOC Bit 0 (RBOC0)

Bit 1 / BOC Bit 1 (RBOC1)

Bit 2 / BOC Bit 2 (RBOC2)

Bit 3 / BOC Bit 3 (RBOC3)

Bit 4 / BOC Bit 4 (RBOC4)

Bit 5 / BOC Bit 5 (RBOC5)

Bits 6, 7 / Unused

8.17 Receive SLC-96 Operation

In an SLC-96-based transmission scheme, the standard Fs-bit pattern is robbed to make room for a set of message fields. The SLC-96 multiframe is made up of six D4 superframes, hence it is 72 frames long. In the 72-frame SLC-96 multiframe, 36 of the framing bits are the normal Ft pattern and the other 36 bits are divided into alarm, maintenance, spoiler, and concentrator bits, as well as 12 bits of the normal Fs pattern. Additional SLC-96 information can be found in BellCore document TR–TSY–000008.

To enable the DS26401 to synchronize onto an SLC-96 pattern, the following configuration should be used:

- Set to D4 framing mode (RCR1.5 = 1)
- Set to cross-couple Ft and Fs bits (RCR1.3 = 1)
- Enable SLC-96 synchronizer (RCR2.4 = 1)
- Set to minimum sync time (RCR1.7 = 0)

The status bit RSLC96 located at RLS7.3 is useful for retrieving SLC-96 message data. The RSLC96 bit indicates when the framer has received the 12-bit Fs-alignment pattern and updated the data-link registers RSLC1–RSLC3 with the latest message data from the incoming data stream. Once the RSLC96 bit is set, the user has 2ms to retrieve the most recent message data from the RSLC1/2/3 registers. Note that RSLC96 is not set if the DS26401 is unable to detect the 12-bit SLC-96 alignment pattern.

Register Name: **RSLC1, RSLC2, RSLC3**
Register Description: **Receive SLC96 Data Link Registers**
Register Address: **064h, 065h, 066h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							**(LSB)**	
C8	C7	C6	C5	C4	C3	C2	C1	**RSLC1**
M2	M1	S = 0	S = 1	S = 0	C11	C10	C9	**RSLC2**
S = 1	S4	S3	S2	S1	A2	A1	M3	**RSLC3**

8.18 Receive FDL

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the receive FDL register (RFDL). Since the RFDL is 8 bits in length, it fills up every 2ms (8 x 250µs). The framer signals an external microcontroller that the buffer has filled through the RLS7.2 bit. If enabled through RIM7.2, the $\overline{INT}$ pin toggles low, indicating that the buffer has filled and needs to be read. The user has 2ms to read this data before it is lost. Note that no zero destuffing is applied for the data provided through the RFDL register.

Register Name: **RFDL**
Register Description: **Receive FDL Register**
Register Address: **062h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0
Default	0	0	0	0	0	0	0	0

The receive FDL register (RFDL) reports the incoming facility data link (FDL) or the incoming Fs bits. The LSB is received first. In D4 framing mode, RFDL updates on multiframe boundaries and reports the six Fs bits in RFDL0–RFDL5.

Bit 0 / Receive FDL Bit 0 (RFDL0). LSB of the received FDL code.

Bit 1 / Receive FDL Bit 1 (RFDL1)

Bit 2 / Receive FDL Bit 2 (RFDL2)

Bit 3 / Receive FDL Bit 3 (RFDL3)

Bit 4 / Receive FDL Bit 4 (RFDL4)

Bit 5 / Receive FDL Bit 5 (RFDL5)

Bit 6 / Receive FDL Bit 6 (RFDL6)

Bit 7 / Receive FDL Bit 7 (RFDL7). MSB of the received FDL code.

8.19 Programmable In-Band Loop-Code Detection

The DS26401 can generate and detect a repeating bit pattern from 1 to 8 bits or 16 bits in length. This function is available only in T1 mode. The framer has three programmable pattern detectors. Typically, two of the detectors are used for loop-up and loop-down code detection. The user programs the codes to be detected in the receive-up-code definition (RUPCD1 and RUPCD2) registers and the receive-down-code definition (RDNCD1 and RDNCD2) registers, and the length of each pattern is selected through the RIBCC register. A third detector (spare) is defined and controlled through the RSPCD1/RSPCD2 and RSCC registers. When detecting a 16-bit pattern, both receive-code-definition registers are used together to form a 16-bit register. For 8-bit patterns, both receive-code-definition registers are filled with the same value. Detection of a 1-, 2-, 3-, 4-, 5-, 6-, and 7-bit pattern only requires the first receive-code-definition register to be filled. The framer detects repeating pattern codes in framed and unframed circumstances with bit-error rates as high as 10E-2. The detectors can handle F-bit-inserted and F-bit-overwrite patterns. Writing the least significant byte of the receive-code-definition register resets the integration period for that detector. The code detector has a nominal integration period of 36ms. Therefore, after about 36ms of receiving a valid code, the proper status bit (LUP, LDN, and LSP) is set to 1. Note that real-time status bits, as well as latched set and clear bits, are available for LUP, LDN, and LSP (RRTS3 and RLS3). Normally codes are sent for 5 seconds. It is recommended that the software poll the framer every 50ms to 1000ms until 5 seconds has elapsed to ensure the code is continuously present.

Register Name: **RIBCC**
Register Description: **Receive In-Band Code Control Register**
Register Address: **082h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RUP2	RUP1	RUP0	RDN2	RDN1	RDN0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2 / Receive-Down-Code Length Definition Bits (RDN0 to RDN2)

RDN2	RDN1	RDN0	Length Selected (bits)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8 / 16

Bits 3 to 5 / Receive-Up-Code Length Definition Bits (RUP0 to RUP2)

RUP2	RUP1	RUP0	Length Selected (bits)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8 / 16

Register Name: **RUPCD1**
Register Description: **Receive-Up Code-Definition Register 1**
Register Address: **0ACh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Note: *Writing this register resets the detector's integration period.*

Bit 0 / Receive-Up Code-Definition Bit 0 (C0). A don't care if a 1- to 7-bit length is selected.
Bit 1 / Receive-Up Code-Definition Bit 1 (C1). A don't care if a 1- to 6-bit length is selected.
Bit 2 / Receive-Up Code-Definition Bit 2 (C2). A don't care if a 1- to 5-bit length is selected.
Bit 3 / Receive-Up Code-Definition Bit 3 (C3). A don't care if a 1- to 4-bit length is selected.
Bit 4 / Receive-Up Code-Definition Bit 4 (C4). A don't care if a 1- to 3-bit length is selected.
Bit 5 / Receive-Up Code-Definition Bit 5 (C5). A don't care if a 1- or 2-bit length is selected.
Bit 6 / Receive-Up Code-Definition Bit 6 (C6). A don't care if a 1-bit length is selected.
Bit 7 / Receive-Up Code-Definition Bit 7 (C7). First bit of the repeating pattern.

Register Name: **RUPCD2**
Register Description: **Receive-Up Code-Definition Register 2**
Register Address: **0ADh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive-Up Code-Definition Bit 0 (C0). A don't care if a 1- to 7-bit length is selected.
Bit 1 / Receive-Up Code-Definition Bit 1 (C1). A don't care if a 1- to 7-bit length is selected.
Bit 2 / Receive-Up Code-Definition Bit 2 (C2). A don't care if a 1- to 7-bit length is selected.
Bit 3 / Receive-Up Code-Definition Bit 3 (C3). A don't care if a 1- to 7-bit length is selected.
Bit 4 / Receive-Up Code-Definition Bit 4 (C4). A don't care if a 1- to 7-bit length is selected.
Bit 5 / Receive-Up Code-Definition Bit 5 (C5). A don't care if a 1- to 7-bit length is selected.
Bit 6 / Receive-Up Code-Definition Bit 6 (C6). A don't care if a 1- to 7-bit length is selected.
Bit 7 / Receive-Up Code-Definition Bit 7 (C7). A don't care if a 1- to 7-bit length is selected.

Register Name: **RDNCD1**
Register Description: **Receive-Down Code-Definition Register 1**
Register Address: **0AEh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Note: *Writing this register resets the detector's integration period.*

Bit 0 / Receive-Down Code-Definition Bit 0 (C0). A don't care if a 1- to 7-bit length is selected.
Bit 1 / Receive-Down Code-Definition Bit 1 (C1). A don't care if a 1- to 6-bit length is selected.
Bit 2 / Receive-Down Code-Definition Bit 2 (C2). A don't care if a 1- to 5-bit length is selected.
Bit 3 / Receive-Down Code-Definition Bit 3 (C3). A don't care if a 1- to 4-bit length is selected.
Bit 4 / Receive-Down Code-Definition Bit 4 (C4). A don't care if a 1- to 3-bit length is selected.
Bit 5 / Receive-Down Code-Definition Bit 5 (C5). A don't care if a 1- or 2-bit length is selected.
Bit 6 / Receive-Down Code-Definition Bit 6 (C6). A don't care if a 1-bit length is selected.
Bit 7 / Receive-Down Code-Definition Bit 7 (C7). First bit of the repeating pattern.

Register Name: **RDNCD2**
Register Description: **Receive-Down Code-Definition Register 2**
Register Address: **0AFh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive-Down Code Definition Bit 0 (C0). A don't care if a 1- to 7-bit length is selected.
Bit 1 / Receive-Down Code-Definition Bit 1 (C1). A don't care if a 1- to 7-bit length is selected.
Bit 2 / Receive-Down Code-Definition Bit 2 (C2). A don't care if a 1- to 7-bit length is selected.
Bit 3 / Receive-Down Code-Definition Bit 3 (C3). A don't care if a 1- to 7-bit length is selected.
Bit 4 / Receive-Down Code-Definition Bit 4 (C4). A don't care if a 1- to 7-bit length is selected.
Bit 5 / Receive-Down Code-Definition Bit 5 (C5). A don't care if a 1- to 7-bit length is selected.
Bit 6 / Receive-Down Code-Definition Bit 6 (C6). A don't care if a 1- to 7-bit length is selected.
Bit 7 / Receive-Down Code-Definition Bit 7 (C7). A don't care if a 1- to 7-bit length is selected.

Register Name: **RSCC**
Register Description: **In-Band Receive-Spare Control Register**
Register Address: **089h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	RSC2	RSC1	RSC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2 / Receive-Spare Code-Length Definition Bits (RSC0 to RSC2)

RSC2	RSC1	RSC0	Length Selected (bits)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8 / 16

Bits 3–7 / Unused. Must be set = 0 for proper operation.

Register Name: **RSCD1**
Register Description: **Receive-Spare Code-Definition Register 1**
Register Address: **09Ch + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Note: *Writing this register resets the detector's integration period.*

Bit 0 / Receive-Spare Code-Definition Bit 0 (C0). A don't care if a 1- to 7-bit length is selected.
Bit 1 / Receive-Spare Code-Definition Bit 1 (C1). A don't care if a 1- to 6-bit length is selected.
Bit 2 / Receive-Spare Code-Definition Bit 2 (C2). A don't care if a 1- to 5-bit length is selected.
Bit 3 / Receive-Spare Code-Definition Bit 3 (C3). A don't care if a 1- to 4-bit length is selected.
Bit 4 / Receive-Spare Code-Definition Bit 4 (C4). A don't care if a 1- to 3-bit length is selected.
Bit 5 / Receive-Spare Code-Definition Bit 5 (C5). A don't care if a 1- or 2-bit length is selected.
Bit 6 / Receive-Spare Code-Definition Bit 6 (C6). A don't care if a 1-bit length is selected.
Bit 7 / Receive-Spare Code-Definition Bit 7 (C7). First bit of the repeating pattern.

Register Name: **RSCD2**
Register Description: **Receive-Spare Code-Definition Register 2**
Register Address: **09Dh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive-Spare Code-Definition Bit 0 (C0). A don't care if a 1- to 7-bit length is selected.
Bit 1 / Receive-Spare Code-Definition Bit 1 (C1). A don't care if a 1- to 7-bit length is selected.
Bit 2 / Receive-Spare Code-Definition Bit 2 (C2). A don't care if a 1- to 7-bit length is selected.
Bit 3 / Receive-Spare Code-Definition Bit 3 (C3). A don't care if a 1- to 7-bit length is selected.
Bit 4 / Receive-Spare Code-Definition Bit 4 (C4). A don't care if a 1- to 7-bit length is selected.
Bit 5 / Receive-Spare Code-Definition Bit 5 (C5). A don't care if a 1- to 7-bit length is selected.
Bit 6 / Receive-Spare Code-Definition Bit 6 (C6). A don't care if a 1- to 7-bit length is selected.
Bit 7 / Receive-Spare Code-Definition Bit 7 (C7). A don't care if a 1- to 7-bit length is selected.

8.20 Receive HDLC Controller

The HDLC controller can be mapped into a single time slot, or Sa4 to Sa8 bits (E1 mode), or the FDL (T1 mode). The HDLC controller has a 64-byte FIFO buffer in the transmit and receive paths. The user can select any specific bits within the time slot(s) to assign to the HDLC controller, as well as specific Sa bits (E1 mode).

The HDLC controller performs the necessary overhead for generating and receiving performance report messages (PRM) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controller automatically generates and detects flags; generates and checks the CRC checksum; generates and detects abort sequences and stuffs and destuffs zeros; and byte aligns to the data stream. The 64-byte buffers in the HDLC controller are large enough to allow a full PRM to be received or transmitted without host intervention.

Register Name: **RHC**
Register Description: **Receive HDLC Control Register**
Register Address: **010h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RCRCD	RHR	RHMS	RHCS4	RHCS3	RHCS2	RHCS1	RHCS0
Default	0	0	0	0	0	0	0	0

Bit 0 to Bit 4 / Receive HDLC Channel Select (RHCSx). These bits determine which DS0 is mapped to the HDLC controller when enabled with RHMS = 0. RHCS0 to RHCS4 = all zeros selects channel 1, RHCS0 to RHCS4 = all ones selects channel 32 (E1)

Bit 5 / Receive HDLC Mapping Select (RHMS)
0 = Receive HDLC assigned to channels
1 = Receive HDLC assigned to FDL (T1 mode), Sa bits (E1 mode)

Bit 6 / Receive HDLC Reset (RHR). Resets the receive-HDLC controller and flushes the receive FIFO. Must be cleared and set again for a subsequent reset.
0 = Normal operation
1 = Reset receive HDLC controller and flush the receive FIFO

Bit 7 / Receive CRC16 Display (RCRCD)
0 = Do not write received CRC16 code to FIFO
1= Write received CRC16 code to FIFO after last octet of packet

Register Name: **RHBSE**
Register Description: **Receive HDLC Bit Suppress Register**
Register Address: **011h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	BSE8	BSE7	BSE6	BSE5	BSE4	BSE3	BSE2	BSE1
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Channel Bit 1 Suppress (BSE1). LSB of the channel. Set to one to stop this bit from being used.

Bit 1 / Receive Channel Bit 2 Suppress (BSE2). Set to one to stop this bit from being used

Bit 2 / Receive Channel Bit 3 Suppress (BSE3). Set to one to stop this bit from being used

Bit 3 / Receive Channel Bit 4 Suppress (BSE4). Set to one to stop this bit from being used

Bit 4 / Receive Channel Bit 5 Suppress (BSE5). Set to one to stop this bit from being used

Bit 5 / Receive Channel Bit 6 Suppress (BSE6). Set to one to stop this bit from being used.

Bit 6 / Receive Channel Bit 7 Suppress (BSE7). Set to one to stop this bit from being used.

Bit 7 / Receive Channel Bit 8 Suppress (BSE8). MSB of the channel. Set to one to stop this bit from being used.

8.20.1 HDLC FIFO Control

Control of the receive FIFO is accomplished through the receive-HDLC FIFO control (RHFC). The FIFO control register sets the watermarks for the receive FIFO.

When the receive FIFO fills above the high watermark, the RHWM bit (RRTS5.1) is set. RHWM is a real-time bit and remains set as long as the receive FIFO's write pointer is above the watermark. If enabled, this condition can also cause an interrupt through the $\overline{INT}$ pin.

Register Name: **RHFC**
Register Description: **Receive HDLC FIFO Control Register**
Register Address: **087h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	RFHWM1	RFHWM0
Default	0	0	0	0	0	0	0	0

Bits 0 to 1 / Receive FIFO High Watermark Select (RFHWM0 to RFHWM1)

RFHWM1	RFHWM0	Receive FIFO Watermark (bytes)
0	0	4
0	1	16
1	0	32
1	1	48

Bits 2–7 / Unused. Must be set = 0 for proper operation.

8.20.2 Receive-Packet-Bytes Available

The lower 6 bits of the receive-packet-bytes-available register indicates the number of bytes (0 through 64) that can be read from the receive FIFO. The value indicated by this register informs the host as to how many bytes can be read from the receive FIFO without going past the end of a message. This value refers to one of four possibilities: the first part of a packet, the continuation of a packet, the last part of a packet, or a complete packet. After reading the number of bytes indicated by this register, the host then checks the HDLC status registers for detailed message status.

If the value in the RHPBA register refers to the beginning portion of a message or continuation of a message, then the MSB of the RHPBA register returns a 1. This indicates that the host may safely read the number of bytes returned by the lower 6 bits of the RHPBA register, but there is no need to check the information register since the packet has not yet terminated (successfully or otherwise).

Register Name: **RHPBA**
Register Description: **Receive HDLC Packet Bytes Available Register**
Register Address: **0B5h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	MS	RPBA6	RPBA5	RPBA4	RPBA3	RPBA2	RPBA1	RPBA0
Default	0	0	0	0	0	0	0	0

Bits 0–6 / Receive FIFO Packet Bytes Available Count (RPBA0 to RPBA6). RPBA0 is the LSB.

Bit 7 / Message Status (MS)

0 = Bytes indicated by RPBA0 through RPBA6 are the end of a message. Host must check the HDLC Status register for details.
1 = Bytes indicated by RPBA0 through RPBA6 are the beginning or continuation of a message. The host does not need to check the HDLC status.

Register Name: **RHF**
Register Description: **Receive HDLC FIFO Register**
Register Address: **0B6h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RHD7	RHD6	RHD5	RHD4	RHD3	RHD2	RHD1	RHD0
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive HDLC Data Bit 0 (RHD0). LSB of a HDLC packet data byte.

Bit 1 / Receive HDLC Data Bit 1 (RHD1)

Bit 2 / Receive HDLC Data Bit 2 (RHD2)

Bit 3 / Receive HDLC Data Bit 3 (RHD3)

Bit 4 / Receive HDLC Data Bit 4 (RHD4)

Bit 5 / Receive HDLC Data Bit 5 (RHD5)

Bit 6 / Receive HDLC Data Bit 6 (RHD6)

Bit 7 / Receive HDLC Data Bit 7 (RHD7). MSB of a HDLC packet data byte.

8.20.3 HDLC Status and Information

RRTS5 and RLS5 provide status information for the receive HDLC controller. When a particular event has occurred (or is occurring), the appropriate bit in one of these registers is set to 1. With the latched bits, when an event occurs and a bit is set to 1, it remains set until the user reads that bit. The bit is cleared when it is read and it is not set again until the event has occurred again. The real-time bits report the current instantaneous conditions that are occurring and the history of these bits is not latched.

Like the other latched-status registers, the user follows a read of the status bit with a write. The byte written to the register informs the device which of the latched bits the user wishes to clear (the real-time bits are not affected by writing to the status register). The user writes a byte to one of these registers, with a 1 in the bit positions the user wishes to clear and a zero in the bit positions the user wishes not to clear.

The HDLC status register RLS5 can initiate a hardware interrupt through the $\overline{INT}$ output signal. Each of the events in this register can be either masked or unmasked from the interrupt pin through the receive-HDLC interrupt-mask register (RIM5). Interrupts force the $\overline{INT}$ signal low when the event occurs. The $\overline{INT}$ pin is allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

Register Name: **RRTS5**
Register Description: **Receive Real-Time Status Register 5 (HDLC)**
Register Address: **0B4h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	PS2	PS1	PS0	—	—	RHWM	RNE
Default	0	0	0	0	0	0	0	0

Note: *All bits in this register are real-time.*

Bit 0 / Receive-FIFO Not Empty Condition (RNE). Set when the receive 64-byte FIFO has at least one byte available for a read. This is a real-time bit.

Bit 1 / Receive-FIFO Above High-Watermark Condition (RHWM). Set when the receive 64-byte FIFO fills beyond the high watermark as defined by the receive-HDLC FIFO control register (RHFC).This is a real-time bit.

Bits 2, 3, 7 / Unused

Bits 4 to 6 / Receive Packet Status (PS0 to PS2). These are real-time bits indicating the status as of the last read of the receive FIFO.

PS2	PS1	PS0	PACKET STATUS
0	0	0	**In Progress:** End of message has not yet been reached.
0	0	1	**Packet OK:** Packet ended with correct CRC codeword.
0	1	0	**CRC Error:** A closing flag was detected, preceded by a corrupt CRC codeword.
0	1	1	**Abort:** Packet ended because an abort signal was detected (seven or more ones in a row).
1	0	0	**Overrun:** HDLC controller terminated reception of packet because receive FIFO is full.

Register Name: **RLS5**
Register Description: **Receive Latched Status Register 5 (HDLC)**
Register Address: **094h + (200h x n) : where n = 0 to 7, or Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	ROVR	RHOBT	RPE	RPS	RHWMS	RNES
Default	0	0	0	0	0	0	0	0

Note: *All bits in this register are latched and can cause interrupts.*

Bit 0 / Receive-FIFO Not Empty Set Event (RNES). Set when the receive FIFO has transitioned from ‘empty’ to ‘not-empty’ (at least one byte has been put into the FIFO). Rising edge detect of RNE.

Bit 1 / Receive-FIFO Above High-Watermark Set Event (RHWMS). Set when the receive-64-byte FIFO crosses the high watermark as defined by the receive HDLC FIFO control register (RHFC). Rising edge detect of RHWM.

Bit 2 / Receive Packet Start Event (RPS). Set when the HDLC controller detects an opening byte. This is a latched bit and will be cleared when read.

Bit 3 / Receive Packet End Event (RPE). Set when the HDLC controller detects either the finish of a valid message (i.e., CRC check complete) or when the controller has experienced a message fault such as a CRC checking error, or an overrun condition, or an abort has been seen. This is a latched bit and is cleared when read.

Bit 4 / Receive HDLC Opening Byte Event (RHOBT). Set when the next byte available in the receive FIFO is the first byte of a message.

Bit 5 / Receive FIFO Overrun (ROVR). Set when the receive HDLC controller has terminated packet reception because the FIFO buffer is full.

Bits 6, 7 / Unused

Register Name: **RIM5**
Register Description: **Receive Interrupt Mask 5 (HDLC)**
Register Address: **0A4h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	ROVR	RHOBT	RPE	RPS	RHWMS	RNES
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive-FIFO Not Empty Set Event (RNES)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Receive-FIFO Above High-Watermark Set Event (RHWMS)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Receive-Packet-Start Event (RPS)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Receive-Packet-End Event (RPE)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Receive-HDLC Opening-Byte Event (RHOBT)
0 = interrupt masked
1 = interrupt enabled

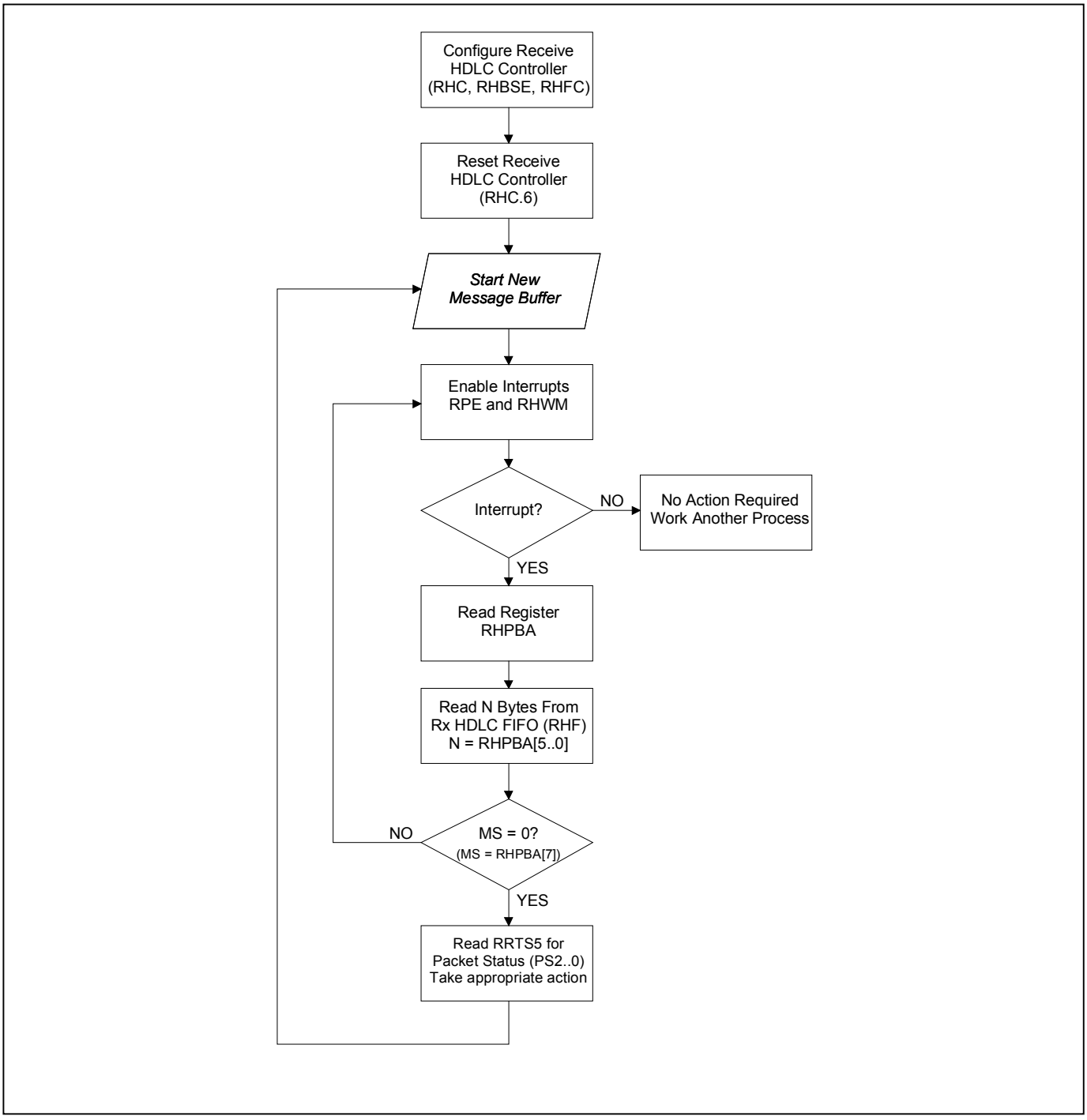
Bit 5 / Receive-FIFO Overrun (ROVR)
0 = interrupt masked
1 = interrupt enabled

Bits 6, 7 / Unused. Must be set = 0 for proper operation.

8.20.4 HDLC Receive Example

The HDLC status registers in the DS26401 allow for flexible software interface to meet the user's preferences. When receiving HDLC messages, the host can choose to be interrupt-driven, or to poll to desired status registers, or a combination of polling and interrupt processes can be used. Figure 8-3 shows an example routine for using the DS26401 HDLC receiver.

Figure 8-3. Receive HDLC Example



8.21 Interleaved PCM Bus Operation (IBO)

In many architectures, the PCM outputs of individual framers are combined into higher-speed PCM buses to simplify transport across the system backplane. The DS26401 can be configured to allow PCM data to be multiplexed into higher-speed buses, eliminating external hardware, and saving board space and cost. The DS26401 can be configured for channel or frame interleave.

The interleaved PCM bus option (IBO) supports three bus speeds. The 4.096MHz bus speed allows two PCM data streams to share a common bus. The 8.192MHz bus speed allows four PCM data streams to share a common bus. The 16.384MHz bus speed allows eight PCM data streams to share a common bus. The receive-elastic stores of each transceiver must be enabled. Through the IBO register, the user can configure each framer for a specific bus position. For all IBO bus configurations, each framer is assigned an exclusive position in the high-speed PCM bus. The 8kHz frame sync can be generated from the system backplane or from the first device on the bus. All other devices on the bus must have their frame syncs configured as inputs. Relative to this common frame sync, the devices await their turn to drive or sample the bus according to the settings of the DA0, DA1, and DA2 bits of the RIBOC register.

8.21.1 Channel Interleave

In channel-interleave mode, data is output to the PCM data-out bus one channel at a time from each of the connected DS26401s until all channels of frame n from each framer has been placed on the bus. This mode can be used even when the DS26401s are operating asynchronous to each other. The elastic stores manage slip conditions. The DS26401 provides an active-low signal (RIBO_OEB) during bus active times. RIBO_OEB can be used to control a bus multiplexer or tri-state buffer control. Functional timing is given in Figure 13-6.

8.21.2 Frame Interleave

In frame-interleave mode, data is output to the PCM data bus one frame at a time from each of the framers. This mode is used only when all connected DS26401s are operating in a synchronous fashion (all inbound T1 or E1 lines are synchronous) and are synchronous with the system clock (system clock derived from T1 or E1 line). In this mode, slip conditions are not allowed. Functional timing is given in Figure 13-7.

Register Name: **RIBOC**
Register Description: **Receive Interleave Bus Operation Control Register**
Register Address: **088h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	IBS1	IBS0	IBOSEL	IBOEN	DA2	DA1	DA0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2 / Device Assignment Bits (DA0 to DA2)

DA2	DA1	DA0	Device Position
0	0	0	1st device on bus
0	0	1	2nd device on bus
0	1	0	3rd device on bus
0	1	1	4th device on bus
1	0	0	5th device on bus
1	0	1	6th device on bus
1	1	0	7th device on bus
1	1	1	8th device on bus

Bit 3 / Interleave Bus Operation Enable (IBOEN)
0 = Interleave Bus Operation disabled.
1 = Interleave Bus Operation enabled.

Bit 4 / Interleave Bus Operation Select (IBOSEL). This bit selects channel or frame interleave mode.
0 = Channel Interleave
1 = Frame Interleave

Bits 5 to 6 / IBO Bus Size bit 1 (IBS0 to IBS1). Indicates how many devices on the bus.

IBS1	IBS0	Bus Size
0	0	2 Devices on bus (4.096MHz)
0	1	4 Devices on bus (8.192MHz)
1	0	8 Devices on bus (16.384MHz)
1	1	Reserved for future use

Bit 7 / Unused. Must be set = 0 for proper operation.

8.22 Interfacing the T1 Rx Framer to the BERT

Data from the DS26401 receive framer can be ported to the on-chip BERT by using the registers described below. Either framed or unframed data can be provided to the BERT, controlled by the RBFUS bit in the RBICR. Any single DS0 or combination of DS0s can be extracted from the data stream up to the entire T1 payload, as controlled by the RBCS registers.

Note that one BERT resource is shared among all 8 framers. Therefore, the RBEN bit should be set for only one framer at a time. If multiple framers have the RBEN bit set, the lower number framer is assigned the resource. Details concerning the on-chip BERT can be found in Section 12.

Register Name: **RBICR**
Register Description: **Receive BERT Interface Control Register**
Register Address: **08Ah + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	RBDC	RBFUS	RBEN
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive BERT Enable (RBEN)
0 = Receive BERT is not assigned to this framer.
1 = Receive BERT is assigned to this framer.

Bit 1 / Receive BERT Framed/Unframed Select (RBFUS)
0 = The framer does **not** provide data from the F-bit position (framed).
1 = The framer clocks data from the F-bit position (unframed).

Bit 2 / Receive BERT Direction Control (RBDC)
0 = Receive Path: The BERT receives data from the network side via RPOS and RNEG.
1 = Backplane: The BERT receives data from the system backplane via the TSER pin.

Bits 3–7 / Unused. Must be set = 0 for proper operation.

Register Name: **RBCS1, RBCS2, RBCS3**
Register Description: **Receive BERT Channel Select Registers**
Register Address: **0D4h, 0D5h, 0D6h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Setting any of the CH1 through CH24 bits in the RBCS1 through RBCS3 registers maps data from those channels to the on-board BERT. RBEN must be set to 1 for these registers to function. Multiple or all channels can be selected simultaneously. These registers affect the receive-side framer only.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RBCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RBCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RBCS3**

Register Name: **RBBS**
Register Description: **Receive BERT Bit Suppress Register**
Register Address: **08Bh**

Bit #	7	6	5	4	3	2	1	0
Name	BSE8	BSE7	BSE6	BSE5	BSE4	BSE3	BSE2	BSE1
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Channel Bit 1 Suppress (BSE1). LSB of the channel. Set to one to stop this bit from being used.
Bit 1 / Receive Channel Bit 2 Suppress (BSE2). Set to one to stop this bit from being used.
Bit 2 / Receive Channel Bit 3 Suppress (BSE3). Set to one to stop this bit from being used.
Bit 3 / Receive Channel Bit 4 Suppress (BSE4). Set to one to stop this bit from being used.
Bit 4 / Receive Channel Bit 5 Suppress (BSE5). Set to one to stop this bit from being used
Bit 5 / Receive Channel Bit 6 Suppress (BSE6). Set to one to stop this bit from being used.
Bit 6 / Receive Channel Bit 7 Suppress (BSE7). Set to one to stop this bit from being used.
Bit 7 / Receive Channel Bit 8 Suppress (BSE8). MSB of the channel. Set to one to stop this bit from being used.

9. T1 TRANSMIT

9.1 T1 Transmit Register Map

ADDRESS	TYPE	FUNCTION	NAME	PAGE
100	—	Unused	—	—
101	—	Unused	—	—
102	—	Unused	—	—
103	—	Unused	—	—
104	—	Unused	—	—
105	—	Unused	—	—
106	—	Unused	—	—
107	—	Unused	—	—
108	—	Unused	—	—
109	—	Unused	—	—
10A	—	Unused	—	—
10B	—	Unused	—	—
10C	—	Unused	—	—
10D	—	Unused	—	—
10E	—	Unused	—	—
10F	—	Unused	—	—
110	R/W	Tx HDLC Control 1	THC1	248
111	R/W	Tx HDLC Bit Suppress	THBSE	249
112	—	Unused	—	—
113	R/W	Tx HDLC Control 2	THC2	249
114	—	Unused	—	—
115	—	Unused	—	—
116	—	Unused	—	—
117	—	Unused	—	—
118	R/W	Tx Software Signaling Insertion Enable 1	SSIE1	121
119	R/W	Tx Software Signaling Insertion Enable 2	SSIE2	121
11A	R/W	Tx Software Signaling Insertion Enable 3	SSIE3	121
11B	—	Unused	—	—
11C	R/W	Tx Test Register 1	TTEST1	—
11D	R/W	Tx Test Register 2	TTEST2	—
11E	R/W	Tx Test Register 3	TTEST3	—
11F	R/W	Tx Test Register 4	TTEST4	—
120	R/W	Tx Idle Definition 1	TIDR1	233
121	R/W	Tx Idle Definition 2	TIDR2	233
122	R/W	Tx Idle Definition 3	TIDR3	233
123	R/W	Tx Idle Definition 4	TIDR4	233
124	R/W	Tx Idle Definition 5	TIDR5	233
125	R/W	Tx Idle Definition 6	TIDR6	233
126	R/W	Tx Idle Definition 7	TIDR7	233
127	R/W	Tx Idle Definition 8	TIDR8	233
128	R/W	Tx Idle Definition 9	TIDR9	233
129	R/W	Tx Idle Definition 10	TIDR10	233
12A	R/W	Tx Idle Definition 11	TIDR11	233
12B	R/W	Tx Idle Definition 12	TIDR12	233
12C	R/W	Tx Idle Definition 13	TIDR13	233
12D	R/W	Tx Idle Definition 14	TIDR14	233
12E	R/W	Tx Idle Definition 15	TIDR15	233
12F	R/W	Tx Idle Definition 16	TIDR16	233
130	R/W	Tx Idle Definition 17	TIDR17	233
131	R/W	Tx Idle Definition 18	TIDR18	233
132	R/W	Tx Idle Definition 19	TIDR19	233
133	R/W	Tx Idle Definition 20	TIDR20	233
134	R/W	Tx Idle Definition 21	TIDR21	233
135	R/W	Tx Idle Definition 22	TIDR22	233
136	R/W	Tx Idle Definition 23	TIDR23	233

ADDRESS	TYPE	FUNCTION	NAME	PAGE
137	R/W	Tx Idle Definition 24	TIDR24	233
138	—	Unused	—	—
139	—	Unused	—	—
13A	—	Unused	—	—
13B	—	Unused	—	—
13C	—	Unused	—	—
13D	—	Unused	—	—
13E	—	Unused	—	—
13F	—	Unused	—	—
140	R/W	Tx Signaling 1	TS1	231
141	R/W	Tx Signaling 2	TS2	231
142	R/W	Tx Signaling 3	TS3	231
143	R/W	Tx Signaling 4	TS4	231
144	R/W	Tx Signaling 5	TS5	231
145	R/W	Tx Signaling 6	TS6	231
146	R/W	Tx Signaling 7	TS7	231
147	R/W	Tx Signaling 8	TS8	231
148	R/W	Tx Signaling 9	TS9	231
149	R/W	Tx Signaling 10	TS10	231
14A	R/W	Tx Signaling 11	TS11	231
14B	R/W	Tx Signaling 12	TS12	231
14C	—	Unused	—	—
14D	—	Unused	—	—
14E	—	Unused	—	—
14F	—	Unused	—	—
150	R/W	Tx Channel Idle Code Enable 1	TCICE1	233
151	R/W	Tx Channel Idle Code Enable 2	TCICE2	233
152	R/W	Tx Channel Idle Code Enable 3	TCICE3	233
153	—	Unused	—	—
154	—	Unused	—	—
155	—	Unused	—	—
156	—	Unused	—	—
157	—	Unused	—	—
158	—	Unused	—	—
159	—	Unused	—	—
15A	—	Unused	—	—
15B	—	Unused	—	—
15C	—	Unused	—	—
15D	—	Unused	—	—
15E	—	Unused	—	—
15F	—	Unused	—	—
160	—	Unused	—	—
161	—	Unused	—	—
162	R/W	Tx FDL	TFDL	131
163	R/W	Tx BOC	TBOC	130
164	R/W	Tx SLC96 Data Link 1	TSLC1	132
165	R/W	Tx SLC96 Data Link 2	TSLC2	132
166	R/W	Tx SLC96 Data Link 3	TSLC3	132
167	—	Unused	—	—
168	—	Unused	—	—
169	—	Unused	—	—
16A	—	Unused	—	—
16B	—	Unused	—	—
16C	—	Unused	—	—
16D	—	Unused	—	—
16E	—	Unused	—	—
16F	—	Unused	—	—
170	—	Unused	—	—
171	—	Unused	—	—
172	—	Unused	—	—
173	—	Unused	—	—

ADDRESS	TYPE	FUNCTION	NAME	PAGE
174	—	Unused	—	—
175	—	Unused	—	—
176	—	Unused	—	—
177	—	Unused	—	—
178	—	Unused	—	—
179	—	Unused	—	—
17A	—	Unused	—	—
17B	—	Unused	—	—
17C	—	Unused	—	—
17D	—	Unused	—	—
17E	—	Unused	—	—
17F	—	Unused	—	—
180	R/W	Tx Master Mode	TMMR	217
181	R/W	Tx Control 1	TCR1	219
182	R/W	Tx Control 2	TCR2	220
183	R/W	Tx Control 3	TCR3	222
184	R/W	Tx I/O Configuration	TIOCR	224
185	R/W	Tx Elastic Store Control	TESCR	237
186	R/W	Tx Control 4	TCR4	113
187	R/W	Tx HDLC FIFO Control	THFC	250
188	R/W	Tx Interleave Bus Op Control	TIBOC	257
189	R/W	Tx DS0 Monitor Select	TDS0SEL	229
18A	R/W	Tx BERT Interface Control	TBICR	146
18B	R/W	Tx BERT Bit Suppress Enable	TBBS	—
18C	—	Unused	—	—
18D	—	Unused	—	—
18E	R/W	Tx Synchronizer Control	TSYNCC	260
18F	R/W	Tx Test Register 5	TTEST5	—
190	R/W	Tx Latched Status 1	TLS1	226
191	R/W	Tx Latched Status 2 (HDLC)	TLS2	252
192	R/W	Tx Latched Status 3 (SYNC)	TLS3	261
193	—	Unused	—	—
194	—	Unused	—	—
195	—	Unused	—	—
196	—	Unused	—	—
197	—	Unused	—	—
198	—	Unused	—	—
199	—	Unused	—	—
19A	—	Unused	—	—
19B	—	Unused	—	—
19C	—	Unused	—	—
19D	—	Unused	—	—
19E	—	Unused	—	—
19F	R/W	Tx Interrupt Information Register	TIIR	218
1A0	R/W	Tx Interrupt Mask Register 1	TIM1	227
1A1	R/W	Tx Interrupt Mask Register 2 (HDLC)	TIM2	253
1A2	R/W	Tx Interrupt Mask Register 3 (SYNC)	TIM3	261
1A3	—	Unused	—	
1A4	—	Unused	—	
1A5	—	Unused	—	
1A6	—	Unused	—	
1A7	—	Unused	—	
1A8	—	Unused	—	
1A9	—	Unused	—	
1AA	—	Unused	—	
1AB	—	Unused	—	
1AC	R/W	Tx Code Definition 1	TCD1	143
1AD	R/W	Tx Code Definition 2	TCD2	143
1AE	—	Unused	—	
1AF	—	Unused	—	
1B0	—	Unused	—	

ADDRESS	TYPE	FUNCTION	NAME	PAGE
1B1	R	Tx Real-Time Status Register 2 (HDLC)	TRTS2	251
1B2	—	Unused	—	
1B3	R	Tx HDLC FIFO Buffer Available	TFBA	140
1B4	W	Tx HDLC FIFO	THF	140
1B5	—	Unused	—	
1B6	—	Unused	—	
1B7	—	Unused	—	
1B8	—	Unused	—	
1B9	—	Unused	—	
1BA	—	Unused	—	
1BB	R	Tx DS0 Monitor	TDS0M	119
1BC	—	Unused	—	
1BD	—	Unused	—	
1BE	—	Unused	—	
1BF	—	Unused	—	
1C0	R/W	Tx Blank Channel Select 1	TBCS1	238
1C1	R/W	Tx Blank Channel Select 2	TBCS2	238
1C2	R/W	Tx Blank Channel Select 3	TBCS3	238
1C3	R/W	Tx Blank Channel Select 4	TBCS4	238
1C4	R/W	Tx Channel Blocking 1	TCBR1	234
1C5	R/W	Tx Channel Blocking 2	TCBR2	234
1C6	R/W	Tx Channel Blocking 3	TCBR3	234
1C7	R/W	Tx Channel Blocking 4	TCBR4	234
1C8	R/W	Tx Hardware Signaling Channel Select 1	THSCS1	232
1C9	R/W	Tx Hardware Signaling Channel Select 2	THSCS2	232
1CA	R/W	Tx Hardware Signaling Channel Select 3	THSCS3	232
1CB	R/W	Tx Hardware Signaling Channel Select 4	THSCS4	232
1CC	R/W	Tx Gapped Clock Channel Select 1	TGCCS1	239
1CD	R/W	Tx Gapped Clock Channel Select 2	TGCCS2	239
1CE	R/W	Tx Gapped Clock Channel Select 3	TGCCS3	239
1CF	R/W	Tx Gapped Clock Channel Select 4	TGCCS4	239
1D0	R/W	Per-Channel Loopback Enable 1	PCL1	118
1D1	R/W	Per-Channel Loopback Enable 2	PCL2	118
1D2	R/W	Per-Channel Loopback Enable 3	PCL3	118
1D3	—	Unused	—	
1D4	R/W	Tx BERT Channel Select 1	TBPCS1	
1D5	R/W	Tx BERT Channel Select 2	TBPCS2	
1D6	R/W	Tx BERT Channel Select 3	TBPCS3	
1D7	—	Unused	—	
1D8	—	Unused	—	
1D9	—	Unused	—	
1DA	—	Unused	—	
1DB	—	Unused	—	
1DC	—	Unused	—	
1DD	—	Unused	—	
1DE	—	Unused	—	
1DF	—	Unused	—	
1E0–1FF	—	Unused	—	

Note: The register addresses are 9-bits wide (shown here in hexadecimal). Addresses with the MSB clear (0xxH) are used for the DS26401 receiver; addresses with the MSB set (1xxH) are used for the DS26401 transmitter.

9.2 T1 Transmit Formatter Description and Operation

Eight fully independent DS1/E1 transmit formatters are included within the DS26401. The formatters are designed to interface seamlessly to the line via an external LIU. Each port can be individually programmed to transmit AMI, B8ZS, HDB3, or NRZ data. In T1 mode each formatter supports D4 (SF), ESF, and SLC-96 frame formats, and transmits common alarms such as AIS, RAI, AIS-CI, and RAI-CI.

Each framer also has an HDLC controller which can be mapped into a single time slot, or Sa4 to Sa8 bits (E1 Mode) or the FDL (T1 Mode) and has 64 byte FIFO buffers in both the transmit and receive paths. The user can select any specific bits within the time slot(s) to assign to the HDLC controllers, as well as specific Sa bits (E1 Mode).

The HDLC controllers perform all the necessary overhead for generating and receiving Performance Report Messages (PRM) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The controllers automatically generate and detects flags, generate and check the CRC check sum, generate and detect abort sequences, stuff and de-stuff zeros, and byte align to the data stream. The large FIFO buffers allow a full PRM to be received or transmitted without host intervention.

Other features contained within each framer include a BOC generator and a 16-bit loop code generator. Host interface is simplified with status registers optimized for either interrupt driven or polled environments. In many cases, status bits are reported both real-time and latched on change-of-state with separate bits for each state change. Most latched bits can be enabled to generate an external interrupt on the $\overline{INT}$ pin.

Additional details concerning the operation of the DS1 formatter are included within the register descriptions within this section.

9.3 Transmit-Master Mode Register

The transmit-master mode register (TMMR) controls the initialization of the transmit-side formatter. The FRM_EN bit may be left 'low' if the formatter for that particular port is not going to be used, putting the circuit in a low-power (sleep) state.

Register Name: **TMMR**
Register Description: **Transmit Master Mode Register**
Register Address: **180h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	FRM_EN	INIT_DONE	—	—	—	—	SFTRST	T1/E1
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmitter T1/E1 Mode Select (T1/E1). Sets operating mode for transmitter only! This bit must be written with the desired value prior to setting INIT_DONE.
0 = T1 operation
1 = E1 operation

Bit 1 / Soft Reset (SFTRST). Level-sensitive processor reset. Should be taken high then low to reset and initialize the internal processor.
0 = Normal operation
1 = Hold the internal RISC in reset. This bit only affects the transmit-side processor.

Bits 2–5 / Unused. Must be set = 0 for proper operation.

Bit 6 / Initialization Done (INIT_DONE). The host (user) must set this bit once he/she has written the configuration registers. The host is required to write or clear all RAM based registers (addresses 100H to 17FH) prior to setting this bit. Once INIT_DONE is set, the internal processor will check the FRM_EN bit. If enabled, the internal processor continues executing based on the initial configuration.

Bit 7 / Framer Enable (FRM_EN). This bit must be written with the desired value prior to setting INIT_DONE.
0 = Framer disabled (held in low-power state)
1 = Framer enabled (all features active)

9.4 Interrupt Information Registers

The interrupt information registers provide an indication of which DS26401 status registers are generating an interrupt. When an interrupt occurs, the host can read TIIR to quickly identify which of the transmit status registers are causing the interrupt(s). These are real-time registers in that the bits will clear once the appropriate interrupt has been serviced and cleared.

Register Name: **TIIR**
Register Description: **Transmit Interrupt Information Register**
Register Address: **19Fh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	TLS3	TLS2	TLS1
Default	0	0	0	0	0	0	0	0

9.5 T1 Transmit Control Registers

Register Name: **TCR1**
Register Description: **Transmit Control Register 1**
Register Address: **181h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TJC	TFPT	TCPT	TSSE	GB7S	TB8ZS	TAIS	TRAI
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Remote Alarm Indication (TRAI)
0 = do not transmit remote alarm
1 = transmit remote alarm

Bit 1 / Transmit Alarm Indication Signal (TAIS)
0 = transmit data normally
1 = transmit an unframed all-ones code at TPOS and TNEG

Bit 2 / Transmit B8ZS Enable (TB8ZS)
0 = B8ZS disabled
1 = B8ZS enabled

Bit 3 / Global Bit 7 Stuffing (GB7S)
0 = allow the SSIEx registers to determine which channels containing all zeros are to be bit 7 stuffed
1 = force bit 7 stuffing in all-zero byte channels regardless of how the SSIEx registers are programmed

Bit 4 / Transmit-Software Signaling Enable (TSSE)
0 = do not source signaling data from the TSx registers regardless of the SSIEx registers. The SSIEx registers still define which channels are to have B7 stuffing performed.
1 = source signaling data as enabled by the SSIEx registers.

Bit 5 / Transmit CRC Pass-Through (TCPT)
0 = source CRC6 bits internally
1 = CRC6 bits sampled at TSER during F-bit time

Bit 6 / Transmit F-Bit Pass-Through (TFPT)
0 = F bits sourced internally
1 = F bits sampled at TSER

Bit 7 / Transmit Japanese CRC6 Enable (TJC)
0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation)
1 = use Japanese standard JT–G704 CRC6 calculation

Register Name: **TCR2**
Register Description: **Transmit Control Register 2**
Register Address: **182h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TFDLS	TSLC96	—	FBCT2	FBCT1	TD4RM	PDE	TB7ZS
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Side Bit 7 Zero Suppression Enable (TB7ZS)
0 = no stuffing occurs
1 = force bit 7 to a one as determined by the GB7S bit at TCR1.3

Bit 1 / Pulse Density Enforcer Enable (PDE). The framer always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403: no more than 15 consecutive zeros and at least N ones in each and every time window of 8 x (N +1) bits where N = 1 through 23. Violations for the transmit and receive data streams are reported in the TLS1.3 and RLS2.7 bits respectively. When this bit is set to one, the DS26401 will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, this bit should be set to zero since B8ZS encoded data streams cannot violate the pulse density requirements.
0 = disable transmit pulse density enforcer
1 = enable transmit pulse density enforcer

Bit 2 / Transmit D4 RAI Select (TD4RM)
0 = zeros in bit 2 of all channels
1 = a one in the S-bit position of frame 12

Bit 3 / F Bit Corruption Type 1. (FBCT1). A low-to-high transition of this bit causes the next three consecutive Ft (D4 framing mode) or FPS (ESF framing mode) bits to be corrupted causing the remote end to experience a loss of synchronization.

Bit 4 / F Bit Corruption Type 2. (FBCT2). Setting this bit high enables the corruption of one Ft (D4 framing mode) or FPS (ESF framing mode) bit in every 128 Ft or FPS bits as long as the bit remains set.

Bit 5 / Unused. Must be set = 0 for proper operation.

Bit 6 / Transmit SLC–96 (TSLC96). Set this bit to a one in SLC-96 framing applications. Must be set to source the SLC-96 alignment pattern and data from the TSLC1-3 registers. See Section 8.12 for details.
0 = SLC–96 insertion disabled
1 = SLC–96 insertion enabled

Bit 7 / TFDL Register Select (TFDLS)
0 = source FDL or Fs bits from the internal TFDL register or the SLC-96 data formatter (TCR2.6)
1 = source FDL or Fs bits from the internal HDLC controller

Register Name: **TCR3**
Register Description: **Transmit Control Register 3**
Register Address: **183h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	ODF	ODM	TCSS1	TCSS0	MFRS	TFM	IBVD	TLOOP
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Loop-Code Enable (TLOOP). See Section 8.13 for details.
0 = transmit data normally
1 = replace normal transmitted data with repeating code as defined in registers TCD1 and TCD2

Bit 1 / Insert BPV (IBPV). A 0-to-1 transition on this bit will cause a single BiPolar Violation (BPV) to be inserted into the transmit data stream. Once this bit has been toggled from a 0 to a 1, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted.

Bit 2 / Transmit Frame Mode Select (TFM)
0 = ESF framing mode
1 = D4 framing mode

Bit 3 / Multiframe Reference Select (MFRS). This bit selects the source for the transmit formatter multiframe boundary.
0 = Normal Operation. Transmit multiframe boundary is determined by 'line-side' counters referenced to TSYNC when TSYNC is an input. Free running when TSYNC is an output.
1 = Pass-Forward Operation. Tx multiframe boundary determined by 'system-side' counters referenced to TSSYNC input, which is then 'passed forward' to the line side clock domain. This mode can only be used when the transmit elastic store is enabled with a synchronous backplane (i.e., no frame slips allowed). This mode must be used to allow Tx hardware signaling insertion while the Tx elastic store is enabled.

Bit 4 / Transmit Clock Source Select Bit 0 (TCSS0)

Bit 5 / Transmit Clock Source Select Bit 1 (TCSS1)

TCSS1	TCSS0	Transmit Clock Source
0	0	The TCLK pin is always the source of Transmit Clock.
0	1	Switch to the clock present at RCLK when the signal at the TCLK pin fails to transition after 1 channel time.
1	0	For Future Use
1	1	Use the signal present at RCLK as the Transmit Clock. The TCLK pin is ignored.

Bit 6 / Output Data Mode (ODM)
0 = pulses at TPOS and TNEG are one full TCLK period wide
1 = pulses at TPOS and TNEG are 1/2 TCLK period wide

Bit 7 / Output Data Format (ODF)
0 = bipolar data at TPOS and TNEG
1 = NRZ data at TPOS; TNEG = 0

Register Name: **TCR4**
Register Description: **Transmit Control Register 4**
Register Address: **186h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TRAIM	TAISM	TC1	TC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 1 / Transmit Code Length Definition Bits (TC0 to TC1)

TC1	TC0	Length Selected (bits)
0	0	5
0	1	6 / 3
1	0	7
1	1	16 / 8 / 4 / 2 / 1

Bit 2 / Transmit AIS Mode (TAISM). Determines the pattern sent when TAIS (TCR1.1) is activated.
0 = transmit normal AIS (unframed all ones) upon activation with TCR1.1
1 = transmit AIS-CI (T1.403) upon activation with TCR1.1

Bit 3 / Transmit RAI Mode (TRAIM). Determines the pattern sent when TRAI (TCR1.0) is activated in ESF frame mode only.
0 = transmit normal RAI upon activation with TCR1.0
1 = transmit RAI-CI (T1.403) upon activation with TCR1.0

Bits 4–7 / Unused. Must be set = 0 for proper operation.

Register Name: **TIOCR**
Register Description: **Transmit I/O Configuration Register**
Register Address: **184h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TCLKINV	TSYNCINV	TSSYNCINV	TSCLKM	TSSM	TSIO	TSDW	TSM
Default	0	0	0	0	0	0	0	0

Bit 0 / TSYNC Mode Select (TSM). Selects frame or multiframe mode for the TSYNC pin.
0 = frame mode
1 = multiframe mode

Bit 1 / TSYNC Doublewide (TSDW). (Note: This bit must be set to zero when TSM = 1 or when TSIO = 0.)
0 = do not pulse double wide in signaling frames
1 = do pulse double wide in signaling frames

Bit 2 / TSYNC I/O Select (TSIO)
0 = TSYNC is an input
1 = TSYNC is an output

Bit 3 / TSSYNC Mode Select (TSSM). Selects frame or multiframe mode for the TSSYNC pin.
0 = frame mode
1 = multiframe mode

Bit 4 / TSYSCLK Mode Select (TSCLKM)
0 = if TSYSCLK is 1.544MHz
1 = if TSYSCLK is 2.048/4.096/8.192/16.384MHz or IBO enabled (see Section 9.20 for details on IBO function)

Bit 5 / TSSYNC Invert (TSSYNCINV)
0 = No inversion
1 = Invert

Bit 6 / TSYNC Invert (TSYNCINV)
0 = No inversion
1 = Invert

Bit 7 / TCLK Invert (TCLKINV)
0 = No inversion
1 = Invert

9.6 T1 Transmit Status and Information

When a particular event has occurred (or is occurring), the appropriate bit in one of these registers will be set to a one. Status bits may operate in either a latched or real-time fashion. Some latched bits may be enabled to generate a hardware interrupt via the $\overline{INT}$ signal.

Real-Time Bits

Some status bits operate in a real-time fashion. These bits are read-only and indicate the present state of an alarm or a condition. Real time bits will remain stable, and valid during the host read operation. The current value of the internal status signals can be read at any time from the real time status registers without changing any the latched status register bits

Latched Bits

When an event or an alarm occurs and a latched bit is set to a one, it will remain set until cleared by the user. These bits typically respond on a 'change-of-state' for an alarm, condition, or event; and operate in a read-then-write fashion. The user should read the value of the desired status bit, and then write a '1' to that particular bit location in order to clear the latched value (write a '0' to locations not to be cleared). Once the bit is cleared, it will not be set again until the event has occurred again.

Mask Bits

Some of the alarms and events can be either masked or unmasked from the interrupt pin via the Interrupt Mask Registers (TIMx). When unmasked, the $\overline{INT}$ signal will be forced low when the enabled event or condition occurs. The $\overline{INT}$ pin will be allowed to return high (if no other unmasked interrupts are present) when the user reads then clears (with a write) the alarm bit that caused the interrupt to occur. Note that the latched status bit and the $\overline{INT}$ pin will clear even if the alarm is still present.

Register Name: **TLS1**
Register Description: **Transmit Latched Status Register 1**
Register Address: **190h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TESF	TESEM	TSLIP	TSLC96	TPDV	TMF	LOTCC	LOTC
Default	0	0	0	0	0	0	0	0

All bits in this register are latched and can cause interrupts.

Bit 0 / Loss of Transmit Clock Condition (LOTC). Set when the TCLK pin has not transitioned for approximately 3 clock periods. Will force the LOTC pin high if enabled. This bit can be cleared by the host even if the condition is still present. The LOTC pin will remain high while the condition exists, even if the host has cleared the status bit.

If enabled by TIM1.0, the $\overline{INT}$ pin will transition low when this bit is set, and transition high when this bit is cleared (if no other unmasked interrupt conditions exist).

Bit 1 / Loss of Transmit Clock Condition Clear (LOTCC). Set when the LOTC condition has cleared (a clock has been sensed at the TCLK pin).

Bit 2 / Transmit Multiframe Event (TMF). Set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries.

Bit 3 / Transmit Pulse Density Violation Event (TPDV). Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.

Bit 4 / Transmit SLC96 Multiframe Event (TSLC96). When enabled by TCR2.6, this bit will set once per SLC96 multiframe (72 frames) to alert the host that new data may be written to the TSLC1-TSLC3 registers. See section 9.16.

Bit 5 / Transmit Elastic Store Slip Occurrence Event (TSLIP). Set when the transmit elastic store has either repeated or deleted a frame.

Bit 6 / Transmit Elastic Store Empty Event (TESEM). Set when the transmit elastic store buffer empties and a frame is repeated.

Bit 7 / Transmit Elastic Store Full Event (TESF). Set when the transmit elastic store buffer fills and a frame is deleted.

Register Name: **TIM1**
Register Description: **Transmit Interrupt Mask Register 1**
Register Address: **1A0h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TESF	TESEM	TSLIP	TSLC96	TPDV	TMF	LOTCC	LOTC
Default	0	0	0	0	0	0	0	0

Bit 0 / Loss of Transmit Clock Condition (LOTC)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Loss of Transmit Clock Clear Condition (LOTCC)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Transmit Multiframe Event (TMF)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Transmit Pulse Density Violation Event (TPDV)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Transmit SLC96 Multiframe Event (TSLC96)
0 = interrupt masked
1 = interrupt enabled

Bit 5 / Transmit Elastic Store Slip Occurrence Event (TSLIP)
0 = interrupt masked
1 = interrupt enabled

Bit 6 / Transmit Elastic Store Empty Event (TESEM)
0 = interrupt masked
1 = interrupt enabled

Bit 7 / Transmit Elastic Store Full Event (TESF)
0 = interrupt masked
1 = interrupt enabled

9.7 T1 Per-Channel Loopback

The Per-Channel Loopback Registers (PCLRs) determine which channels (if any) from the backplane should be replaced with the data from the receive side or in other words, off of the T1 or E1 line. If this loopback is enabled, then transmit and receive clocks and frame syncs must be synchronized. One method to accomplish this would be to tie RCLK to TCLK and RFSYNC to TSYNC. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

Each of the bit position in the Per-Channel Loopback Registers (PCLR1/PCLR2/PCLR3) represent a DS0 channel in the outgoing frame. When these bits are set to a one, data from the corresponding receive channel will replace the data on TSER for that channel.

Register Name: **PCL1, PCL2, PCL3**
Register Description: **Per-Channel Loopback Enable Registers**
Register Address: **1D0h, 1D1h, 1D2h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**PCL1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**PCL2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**PCL3**

Bits 0 to 7 / Per-Channel Loopback Enable for Channels 1 to 24 (CH1 to CH24)

0 = Loopback disabled
1 = Enable Loopback. Source data from the corresponding receive channel

9.8 T1 Transmit DS0 Monitoring Function

The DS26401 has the ability to monitor one DS0 (64kbps) channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction the user will determine which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the TDS0SEL register. In the receive direction, the RCM0 to RCM4 bits in the RDS0SEL register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits will appear in the Transmit DS0 Monitor (TDS0M) register and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the Receive DS0 (RDS0M) register. The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate T1or E1 channel. T1 channels 1 through 24 map to register values 0 through 23. E1 channels 1 through 32 map to register values 0 through 31. For example, if DS0 channel 6 in the transmit direction and DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into TDS0SEL and RDS0SEL:

TCM4 = 0	RCM4 = 0
TCM3 = 0	RCM3 = 1
TCM2 = 1	RCM2 = 1
TCM1 = 0	RCM1 = 1
TCM0 = 1	RCM0 = 0

Register Name: **TDS0SEL**
Register Description: **Transmit DS0 Channel Monitor Select**
Register Address: **189h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	TCM4	TCM3	TCM2	TCM1	TCM0
Default	0	0	0	0	0	0	0	0

Bits 0 to 4 / Transmit Channel Monitor Bits (TCM0 to TCM4). TCM0 is the LSB of a 5 bit channel select that determines which transmit channel data will appear in the TDS0M register.

Bits 5 to 7 / Unused. Must be set = 0 for proper operation.

Register Name: **TDS0M**
Register Description: **Transmit DS0 Monitor Register**
Register Address: **1BBh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	B1	B2	B3	B4	B5	B6	B7	B8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Transmit DS0 Channel Bits (B1 to B8). Transmit channel data that has been selected by the Transmit Channel Monitor Select Register. B8 is the LSB of the DS0 channel (last bit to be transmitted).

9.9 T1 Transmit Signaling Operation

There are two methods to provide transmit signaling data—processor-based (i.e., software-based) or hardware-based. Processor-based refers to access through the transmit-signaling registers, TS1-TS12, while hardware-based refers to using the TSIG pins. Both methods can be used simultaneously.

9.9.1 Processor-Based Mode

In Processor Based mode, signaling data is loaded into the Transmit Signaling registers (TS1 – TS12) via the host interface. On multiframe boundaries, the contents of these registers is loaded into a shift register for placement in the appropriate bit position in the outgoing data stream. The user can utilize the Transmit Multiframe Interrupt in Latched Status Register 1 (TLS1.2) to know when to update the signaling bits. The user need not update any transmit signaling register for which there is no change of state for that register.

Each Transmit Signaling Register contains the Robbed Bit signaling for each time slots that will be inserted into the outgoing stream if enabled to do so via TCR1.4.

Signaling data can be sourced from the TS registers on a per-channel basis by utilizing the Software Signaling Insertion Enable registers, SSIE1 through SSIE3.

In T1 ESF framing mode, there are four signaling bits per channel (A, B, C, and D). TS1 – TS12 contain a full multiframe of signaling data. In T1 D4 framing mode, there are only two signaling bits per channel (A and B). In T1 D4 framing mode, the framer uses A and B bit positions for the next multiframe. The C and D bit positions become ‘don’t care’ in D4 mode.

9.9.2 Hardware-Based Mode

In hardware-based mode, signaling data is input via the TSIG pin. This signaling PCM stream is buffered and inserted to the data stream being input at the TSER pin.

Signaling data may be input via the Transmit Hardware Signaling Channel Select (THSCS) function, the framer can be set up to take the signaling data presented at the TSIG pin and insert the signaling data into the PCM data stream that is being input at the TSER pin. The user can control which channels are to have signaling data from the TSIG pin inserted into them on a per-channel basis. The signaling insertion capabilities of the framer are available whether the transmit side elastic store is enabled or disabled. If the elastic store is enabled, the backplane clock (TSYSCLK) can be either 1.544MHz or 2.048MHz. If IBO mode is enabled, then TSYSCLK may also be 4.096MHz, 8.192MHz, or 16.384MHz.

Register Name: **TS1 TO TS12**
Register Description: **Transmit Signaling Registers (T1 MODE)**
Register Address: **140h – 14Bh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH1-A	CH1-B	CH1-C	CH1-D	CH13-A	CH13-B	CH13-C	CH13-D	TS1
CH2-A	CH2-B	CH2-C	CH2-D	CH14-A	CH14-B	CH14-C	CH14-D	TS2
CH3-A	CH3-B	CH3-C	CH3-D	CH15-A	CH15-B	CH15-C	CH15-D	TS3
CH4-A	CH4-B	CH4-C	CH4-D	CH16-A	CH16-B	CH16-C	CH16-D	TS4
CH5-A	CH5-B	CH5-C	CH5-D	CH17-A	CH17-B	CH17-C	CH17-D	TS5
CH6-A	CH6-B	CH6-C	CH6-D	CH18-A	CH18-B	CH18-C	CH18-D	TS6
CH7-A	CH7-B	CH7-C	CH7-D	CH19-A	CH19-B	CH19-C	CH19-D	TS7
CH8-A	CH8-B	CH8-C	CH8-D	CH20-A	CH20-B	CH20-C	CH20-D	TS8
CH9-A	CH9-B	CH9-C	CH9-D	CH21-A	CH21-B	CH21-C	CH21-D	TS9
CH10-A	CH10-B	CH10-C	CH10-D	CH22-A	CH22-B	CH22-C	CH22-D	TS10
CH11-A	CH11-B	CH11-C	CH11-D	CH23-A	CH23-B	CH23-C	CH23-D	TS11
CH12-A	CH12-B	CH12-C	CH12-D	CH24-A	CH24-B	CH24-C	CH24-D	TS12

Note: *In D4 framing mode, the C and D bits are not used.*

Register Name: **SSIE1, SSIE2, SSIE3**
Register Description: **Software Signaling Insertion Enable Registers**
Register Address: **118h, 119h, 11Ah [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**SSIE1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**SSIE2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**SSIE3**

Bits 0 to 7 / Software Signaling Insertion Enable for Channels 1 to 24 (SSIEx). These bits determine which channels are to have signaling inserted form the Transmit Signaling registers.

0 = do not source signaling data from the TS registers for this channel
1 = source signaling data from the TS registers for this channel

Register Name: **THSCS1, THSCS2, THSCS3, THSCS4**
Register Description: **Transmit Hardware Signaling Channel Select Registers**
Register Address: **1C8h, 1C9h, 1CAh, 1CBh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**THSCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**THSCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**THSCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**THSCS4***

Bits 0 to 7 / Transmit Hardware Signaling Channel Select for Channels 1 to 32 (THSCS1-4). These bits determine which channels have signaling data inserted from the TSIG pin into the TSER PCM data.

0 = do not source signaling data from the TSIG pin for this channel
1 = source signaling data from the TSIG pin for this channel

** Note that THSCS4 is only used in 2.048MHz backplane applications.*

9.10 T1 Transmit Per-Channel Idle Code Insertion

Channel data can be replaced by an idle code on a per-channel basis in the transmit and receive directions. Twenty-four Transmit Idle Definition Registers (TIDR1-TIDR24) are provided to set the 8-bit idle code for each channel. The Transmit Channel Idle Code Enable registers (TCICE1-3) are used to enable idle code replacement on a per channel basis.

Register Name: **TIDR1 to TIDR24**
Register Description: **Transmit Idle Code Definition Registers 1 to 24**
Register Address: **120h to 137h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Per-Channel Idle Code Bits (C0 to C7). C0 is the LSB of the Code (this bit is transmitted last). Address 120H is for channel 1, address 137H is for channel 24.

The Transmit Channel Idle Code Enable Registers (TCICE1/2/3) are used to determine which of the 24 T1 channels from the backplane should be overwritten with the code placed in the Transmit Idle Code Definition Register.

Register Name: **TCICE1, TCICE2, TCICE3**
Register Description: **Transmit Channel Idle Code Enable Registers**
Register Address: **150h, 151h, 152h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**TCICE1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**TCICE2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**TCICE3**

Bits 0 to 7 / Transmit Channels 1 to 24 Code Insertion Control Bits (CH1 to CH24)
0 = do not insert data from the Idle Code Array into the transmit data stream
1 = insert data from the Idle Code Array into the transmit data stream

9.11 T1 Transmit Channel Blocking Registers

The Receive Channel blocking Registers (RCBR1 / RCBR2 / RCBR3 / RCBR4) and the Transmit Channel Blocking Registers (TCBR1 / TCBR2 / TCBR3 / TCHR4) control RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHBLK pins are user programmable outputs that can be forced either high or low during individual channels. When the appropriate bits are set to a one, the RCHBLK and TCHBLK pin will be held high during the entire corresponding channel time.

Register Name: **TCBR1, TCBR2, TCBR3, TCBR4**
Register Description: **Transmit Channel Blocking Registers**
Register Address: **1C4h, 1C5h, 1C6h, 1C7h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**TCBR1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**TCBR2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**TCBR3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25/Fbit	**TCBR4***

Bits 0 to 7 / Transmit Channels 1 to 32 Channel Blocking Control Bits (CH1 to CH32)

0 = force the TCHBLK pin to remain low during this channel time
1 = force the TCHBLK pin high during this channel time
In T1 mode, the LSB of TCBR4 determines whether or not the TCHBLK signal will pulse high during the F-Bit time:

TCBR4.0 = 0, do not pulse TCHBLK during the F-Bit
TCBR4.0 = 1, pulse TCHBLK during the F-Bit

In this mode, TCBR4.1 to TCBR4.7 should be set to 0.

9.12 T1 Transmit Elastic Stores Operation

The DS26401 contains dual two-frame elastic stores, one for the receive direction and one for the transmit direction. Both elastic stores are fully independent. The transmit- and receive-side elastic stores can be enabled/disabled independent of each other. Also, each elastic store can interface to either a 1.544MHz or 2.048/4.096/8.192/16.384MHz backplane without regard to the backplane rate of the other elastic store.

The elastic stores have two main purposes. First, they can be used for rate conversion. When the DS26401 is in the T1 mode, the elastic stores can rate convert the T1 data stream to a 2.048MHz backplane. In E1 mode, the elastic store can rate convert the E1 data stream to a 1.544MHz backplane. Secondly, they can be used to absorb the differences in frequency and phase between the T1 or E1 data stream and an asynchronous (i.e., not locked) backplane clock (which can be 1.544MHz or 2.048MHz). In this mode, the elastic stores will manage the rate difference and perform controlled slips, deleting or repeating frames of data in order to manage the difference between the network and the backplane.

The elastic stores can also be used to multiplex T1 or E1 data streams into higher backplane rates. This is the Interleave Bus Option (IBO) which is discussed in Section 9.20.

Note that the receive elastic store status bits are contained in TLS1 with the associated interrupt bits located in TIM1. These bits indicate a receive slip event, or when the e-store FIFO is in a ‘full’ or ‘empty’ condition. See the register definition for TLS1 for additional information.

The operation of the transmit elastic store is very similar to the receive side. If the transmit side elastic store is enabled a 1.544MHz or 2.048MHz clock can be applied to the TSYSCLK input. For higher rate system clock applications, see the Interleave Bus Option section. Controlled slips in the transmit elastic store are reported in the TLS1.5 bit and the direction of the slip is reported in the TLS1.6 and TLS1.7 bits.

If the user selects to apply a 2.048MHz clock to the TSYSCLK pin, then the data input at TSER will be ignored on the channels marked by the TBCS registers. The user can supply frame or multiframe sync pulse to the TSSYNC input. Note that the user may find it useful to program the TCHBLK output as a method to mark backplane channels that will be ignored during T1 to E1 conversion.

9.12.1 Elastic Stores Initialization

There are two elastic store initializations that may be used to improve performance in certain applications, Elastic Store Reset and Elastic Store Align. Both of these involve the manipulation of the elastic store's read and write pointers and are useful primarily in synchronous applications (RSYSCLK/TSYSCLK are locked to RCLK/TCLK, respectively). The elastic store reset is used to minimize the delay through the elastic store. The elastic store align bit is used to center the read/write pointers to the extent possible.

Elastic Store Delay After Initialization

INITIALIZATION	REGISTER BIT	DELAY
Receive Elastic Store Reset	RESCR.2	N bytes < Delay < 1 Frame + N bytes
Transmit Elastic Store Reset	TESCR.2	N bytes < Delay < 1 Frame + N bytes
Receive Elastic Store Align	RESCR.3	1/2 Frame < Delay < 1 ½ Frames
Transmit Elastic Store Align	TESCR.3	1/2 Frame < Delay < 1 ½ Frames

N = 9 for TSZS = 0

N = 2 for TSZS = 1

9.12.2 Minimum Delay Mode

Elastic store minimum delay mode may be used when the elastic store's system clock is locked to its network clock (i.e., RCLK locked to RSYSCLK for the receive side and TCLK locked to TSYSCLK for the transmit side). TESCR.1 and RESCR.1 enable the transmit and receive elastic store minimum delay modes. When enabled the elastic stores will be forced to a maximum depth of 32 bits instead of the normal two-frame depth. This feature is useful primarily in applications that interface to a 2.048MHz bus. Certain restrictions apply when minimum delay mode is used. In addition to the restriction mentioned above, RSYNC must be configured as an output when the receive elastic store is in minimum delay mode and TSYNC must be configured as an output when transmit minimum delay mode is enabled. The RSYNC and TSYNC outputs are registered on the rising edge of RSYSCLK and TSYSCLK respectfully. In a typical application RSYSCLK and TSYSCLK are locked to RCLK, and RSYNC (frame output mode) is connected to TSSYNC (frame input mode). All the slip contention logic in the framer is disabled (since slips cannot occur). On power-up after the RSYSCLK and TSYSCLK signals have locked to their respective network clock signals, the elastic store reset bits (TESCR.2 and RESCR.2) should be toggled from a zero to a one to ensure proper operation.

Register Name: **TESCR**
Register Description: **Transmit Elastic Store Control Register**
Register Address: **185h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TDATFMT	TGCLKEN	—	TSZS	TESALGN	TESR	TESMDM	TESE
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Elastic Store Enable (TESE)
0 = elastic store is bypassed
1 = elastic store is enabled

Bit 1 / Transmit Elastic Store Minimum Delay Mode (TESMDM)
0 = elastic stores operate at full two frame depth
1 = elastic stores operate at 32-bit depth

Bit 2 / Transmit Elastic Store Reset (TESR). Setting this bit from a zero to a one will force the read pointer into the same frame that the write pointer is exiting, minimizing the delay through the elastic store. If this command should place the pointers within the slip zone (see bit 4), then an immediate slip will occur and the pointers will move back to opposite frames. Should be toggled after TSYSCLK has been applied and is stable. Do not leave this bit set HIGH.

Bit 3 / Transmit Elastic Store Align (TESALGN). Setting this bit from a zero to a one will force the transmit elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command will be executed and the data will be disrupted. Should be toggled after TSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align.

Bit 4 / Transmit Slip Zone Select (TSZS). This bit determines the minimum distance allowed between the elastic store read and write pointers before forcing a controlled slip. This bit is only applies during T1 to E1 or E1 to T1 conversion applications.
0 = force a slip at 9 bytes or less of separation (used for clustered blank channels)
1 = force a slip at 2 bytes or less of separation (used for distributed blank channels)

Bit 5 / Unused. Must be set = 0 for proper operation.

Bit 6 / Transmit Gapped Clock Enable (TGPCKEN)
0 = TCHCLK functions normally
1 = Enable gapped bit clock output on TCHCLK

Bit 7 / Transmit Channel Data Format (TDATFMT)
0 = 64KBps (data contained in all 8 bits)
1 = 56KBps (data contained in 7 out of the 8 bits)

Note: Bits 6 and 7 for fractional backplane support. See Section 9.13.

9.12.3 Mapping T1 Channels from a 2.048MHz Backplane

Setting the TSCLKM bit in TIOCR.4 will enable the transmit elastic store to operate with a 2.048MHz backplane (32 time slots/frame). In this mode, the user can chose which of the backplane channels on TSER will be mapped into the T1 data stream by programming the Transmit Blank Channel Select registers (TBCS1–4). A logic 1 in the associated bit location will force the transmit elastic store to ignore backplane data for that channel. Typically, the user will want to program eight channels to be ignored. The default (power-up) configuration will ignore channels 25 to 32, so that the first 24 backplane channels are mapped into the T1 transmit data stream.

For example, if the user desired to transmit data from the 2.048MHz backplane channels 2–16 and 18–26, the TBCS registers should be programmed as follows:

TBCS1 = 01h // ignore backplane channel 1 //
TBCS2 = 00h
TBCS3 = 01h // ignore backplane channel 17 //
TBCS4 = FCh // ignore backplane channels 27-32 //

Register Name: **TBCS1, TBCS2, TBCS3, TBCS4**
Register Description: **Transmit Blank Channel Select Registers**
Register Address: **1C0h, 1C1h, 1C2h, 1C3h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**TBCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**TBCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**TBCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**TBCS4**

Bits 0 to 7 / Transmit Blank Channel Select for Channels 1 to 32 (TBCS1 to 32)

0 = transmit TSER data from this channel
1 = ignore TSER data from this channel

Note that when two or more sequential channels are chosen to be ignored, the receive slip zone select bit should be set to zero. If the ignore channels are distributed (such as 1, 5, 9, 13, 17, 21, 25, 29) then the RSZS bit can be set to one, which may provide a lower occurrence of slips in certain applications.

9.13 Fractional T1 Support (Gapped Clock Mode)

The DS26401 can be programmed to output gapped clocks for selected channels in the receive and transmit paths to simplify connections into a USART or LAPD controller in Fractional T1/E1 or ISDN–PRI applications. When the gapped clock feature is enabled, a gated clock is output on the TCHCLK signal. The channel selection is controlled via the transmit gapped clock channel select registers (TGCCS1-TGCCS4). The transmit path is enabled for gapped clock mode with the TGCLKEN bit (TESCR.6). Both 56kbps and 64kbps channel formats are supported as determined by TESCR.7. When 56kbps mode is selected, the clock corresponding to the Data/Control bit in the channel is omitted (only the seven most significant bits of the channel have clocks).

Register Name: **TGCCS1, TGCCS2, TGCCS3, TGCCS4**
Register Description: **Transmit Gapped Clock Channel Select Registers**
Register Address: **1CCh, 1CDh, 1CEh, 1CFh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**TGCCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**TGCCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**TGCCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25/Fbit	**TGCCS4***

Bits 0 to 7 / Transmit Channels 1 to 32 Gapped Clock Channel Select Bits (CH1 to CH32)

0 = no clock is present on TCHCLK during this channel time
1 = force a clock on TCHCLK during this channel time. The clock will be synchronous with TCLK if the elastic store is disabled, and synchronous with TSYSCLK if the elastic store is enabled.

*** Note that TGCCS4 has two functions:**

When 2.048MHz backplane mode is selected, this register allows the user to enable the 'gapped' clock on TCHCLK for any of the 32 possible backplane channels.

When 1.544MHz backplane mode is selected, the LSB of this register determines whether or not a clock is generated on TCHCLK during the F-Bit time:

TGCCS4.0 = 0, do not generate a clock during the F-Bit
TGCCS4.0 = 1, generate a clock during the F-Bit

In this mode, TGCCS4.1 to TGCCS4.7 should be set to 0.

9.14 T1 Transmit Bit Oriented Code (BOC) Controller

The DS26401 contains a BOC generator on the transmit side and a BOC detector on the receive side. The BOC function is available only in T1 mode.

Bits 0 through 5 in the TBOC register contain the BOC message to be transmitted. Setting SBOC = 1 (THC2.6) causes the transmit BOC controller to immediately begin inserting the BOC sequence into the FDL bit position. The transmit BOC controller automatically provides the abort sequence. BOC messages will be transmitted as long as SBOC is set. Note that the TFPT (TCR1.6) control bit must be set to 'zero' for the BOC message to overwrite F-bit information being sampled on TSER.

To Transmit a BOC

1) Write 6-bit code into the TBOC register.
2) Set SBOC bit in THC2 = 1.

Register Name: **TBOC**
Register Description: **Transmit BOC Register**
Register Address: **163h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—-	—	TBOC5	TBOC4	TBOC3	TBOC2	TBOC1	TBOC0
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit BOC Bit 0 (TBOC0). LSB of the Transmit BOC Code.

Bit 1 / Transmit BOC Bit 1 (TBOC1)

Bit 2 / Transmit BOC Bit 2 (TBOC2)

Bit 3 / Transmit BOC Bit 3 (TBOC3)

Bit 4 / Transmit BOC Bit 4 (TBOC4)

Bit 5 / Transmit BOC Bit 5 (TBOC5). MSB of the Transmit BOC Code.

Bits 6, 7 / Unused

9.15 T1 Transmit FDL

When enabled with TCR2.7, the transmit section will shift out into the T1 data stream, either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL register (TFDL). When a new value is written to the TFDL, it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full eight bits has been shifted out, the framer will signal the host microcontroller that the buffer is empty and that more data is needed by setting the TLS2.4 bit to a one. The $\overline{INT}$ will also toggle low if enabled via TIM2.4. The user has 2ms to update the TFDL with a new value. If the TFDL is not updated, the old value in the TFDL will be transmitted once again. Note that in this mode, no zero stuffing will be applied to the FDL data.

In the D4 framing mode, the framer uses the TFDL register to insert the Fs framing pattern. To allow the device to properly insert the Fs framing pattern, the TFDL register must be programmed to 1Ch and the following bits must be programmed as shown: TCR2.7 = 0 (source Fs data from the TFDL register) TCR2.6 = 1 (allow the TFDL register to load on multiframe boundaries).

Register Name: **TFDL**
Register Description: **Transmit FDL Register**
Register Address: **162h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TFDL7	TFDL6	TFDL5	TFDL4	TFDL3	TFDL2	TFDL1	TFDL0
Default	0	0	0	1	1	1	0	0

Note: *Also used to insert Fs framing pattern in D4 framing mode.*

The Transmit FDL Register (TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first. In D4 mode, only the lower six bits are used.

Bit 0 / Transmit FDL Bit 0 (TFDL0). LSB of the Transmit FDL Code.

Bit 1 / Transmit FDL Bit 1 (TFDL1)

Bit 2 / Transmit FDL Bit 2 (TFDL2)

Bit 3 / Transmit FDL Bit 3 (TFDL3)

Bit 4 / Transmit FDL Bit 4 (TFDL4)

Bit 5 / Transmit FDL Bit 5 (TFDL5)

Bit 6 / Transmit FDL Bit 6 (TFDL6)

Bit 7 / Transmit FDL Bit 7 (TFDL7). MSB of the Transmit FDL Code.

9.16 Transmit SLC–96 Operation

In a SLC–96 based transmission scheme, the standard Fs bit pattern is robbed to make room for a set of message fields. The SLC–96 multiframe is made up of six D4 superframes, hence it is 72 frames long. In the 72-frame SLC–96 multiframe, 36 of the framing bits are the normal Ft pattern and the other 36 bits are divided into alarm, maintenance, spoiler, and concentrator bits as well as 12 bits of the normal Fs pattern. Additional SLC-96 information can be found in BellCore document TR–TSY–000008.

To insert the SLC-96 message fields, the user has the option to either use the external TLINK pin or the use the onboard TFDL register. Use of the TLINK pin will require additional circuitry, and to enable this option the TCR2.7 bit should be set to one. To insert the SLC-96 message using the TFDL register, the user should configure the DS26401 as shown below:

TCR2.6 (TSLC96) = 1	Enable Transmit SLC-96
TCR2.7 (TFDLS) = 0	Source FS bits via TFDL or SLC96 formatter
TCR3.2 (TFM) = 1	D4 framing Mode
TCR1.6 (TFPT) = 0	Do not 'pass through' TSER F-bits.

The DS26401 will automatically insert the 12-bit alignment pattern in the Fs bits for the SLC96 data link frame. Data from the TSLC1–TSLC3 will be inserted into the remaining Fs bit locations of the SLC96 multiframe. The status bit TSLC96 located at TLS1.4 will set to indicate that the SLC96 data link buffer has been transmitted and that the user should write new message data into TSLC1–TSLC3. The host will have 2.5ms after the assertion of TLS1.4 to write the registers TSLC1–TSLC3. If no new data is provided in these registers, the previous values will be retransmitted.

Register Name: **TSLC1, TSLC2, TSLC3**
Register Description: **Transmit SLC96 Data Link Registers**
Register Address: **164h, 165h, 166h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
C8	C7	C6	C5	C4	C3	C2	C1	**TSLC1**
M2	M1	S = 0	S = 1	S = 0	C11	C10	C9	**TSLC2**
S = 1	S4	S3	S2	S1	A2	A1	M3	**TSLC3**

9.17 Transmit HDLC Controller

The HDLC controller can be mapped into a single time slot, or Sa4 to Sa8 bits (E1 Mode) or the FDL (T1 Mode). The HDLC controller has a 64-byte FIFO buffer in both the transmit and receive paths. The user can select any specific bits within the time slot(s) to assign to the HDLC controller, as well as specific Sa bits (E1 Mode).

The HDLC controller performs all the necessary overhead for generating and receiving Performance Report Messages (PRM) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controller automatically generates and detects flags, generates and checks the CRC check sum, generates and detects abort sequences, stuffs and de-stuffs zeros, and byte aligns to the data stream.

Register Name: **THC1**
Register Description: **Transmit HDLC Control Register 1**
Register Address: **110h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	NOFS	TEOML	THR	THMS	TFS	TEOM	TZSD	TCRCD
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit CRC Defeat (TCRCD). A 2-byte CRC code is automatically appended to the outbound message. This bit can be used to disable the CRC function.
0 = enable CRC generation (normal operation)
1 = disable CRC generation

Bit 1 / Transmit Zero Stuffer Defeat (TZSD). The Zero Stuffer function automatically inserts a zero in the message field (between the flags) after 5 consecutive ones to prevent the emulation of a flag or abort sequence by the data pattern. The receiver automatically removes (de-stuffs) any zero after 5 ones in the message field.
0 = enable the zero stuffer (normal operation)
1 = disable the zero stuffer

Bit 2 / Transmit End of Message (TEOM). Should be set to a one just before the last data byte of an HDLC packet is written into the transmit FIFO at THF. If not disabled via TCRCD, the transmitter will automatically append a 2-byte CRC code to the end of the message.

Bit 3 / Transmit Flag/Idle Select (TFS). This bit selects the inter-message fill character after the closing and before the opening flags (7Eh).
0 = 7Eh
1 = FFh

Bit 4 / Transmit HDLC Mapping Select (THMS)
0 = Transmit HDLC assigned to channels
1 = Transmit HDLC assigned to FDL(T1 mode), Sa Bits(E1 mode)

Bit 5 / Transmit HDLC Reset (THR). Will reset the transmit HDLC controller and flush the transmit FIFO. An abort followed by 7Eh or FFh flags/idle will be transmitted until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent reset.
0 = Normal operation
1 = Reset transmit HDLC controller and flush the transmit FIFO

Bit 6 / Transmit End of Message and Loop (TEOML). To loop on a message, should be set to a one just before the last data byte of an HDLC packet is written into the transmit FIFO. The message will repeat until the user clears this bit or a new message is written to the transmit FIFO. If the host clears the bit, the looping message will complete then flags will be transmitted until new message is written to the FIFO. If the host terminates the loop by writing a new message to the FIFO the loop will terminate, one or two flags will be transmitted and the new message will start. If not disabled via TCRCD, the transmitter will automatically append a 2-byte CRC code to the end of all messages.

Bit 7 / Number of Flags Select (NOFS)
0 = send one flag between consecutive messages
1 = send two flags between consecutive messages

Register Name: **THC2**
Register Description: **Transmit HDLC Control Register 2**
Register Address: **113h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TABT	SBOC	THCEN	THCS4	THCS3	THCS2	THCS1	THCS0
Default	0	0	0	0	0	0	0	0

Bits 0 to 4 / Transmit HDLC Channel Select (THCS0 to 4). Determines which DSO channel will carry the HDLC message if enabled.

Bit 5 / Transmit HDLC Controller Enable (THCEN)
0 = Transmit HDLC Controller is not enabled
1 = Transmit HDLC Controller is enabled

Bit 6 / Send BOC (SBOC). Set = 1 to transmit the BOC code placed in bits 0 to 5 of the TBOC register.

Bit 7 / Transmit Abort (TABT). A 0-to-1 transition will cause the FIFO contents to be dumped and one FEh abort to be sent followed by 7Eh or FFh flags/idle until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent abort to be sent.

Register Name: **THBSE**
Register Description: **Transmit HDLC Bit Suppress**
Register Address: **111h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TBSE8	TBSE7	TBSE6	TBSE5	TBSE4	TBSE3	TBSE2	TBSE1
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Bit 1 Suppress (TBSE1). LSB of the channel. Set to one to stop this bit from being used.

Bit 1 / Transmit Bit 2 Suppress (TBSE2). Set to one to stop this bit from being used.

Bit 2 / Transmit Bit 3 Suppress (TBSE3). Set to one to stop this bit from being used.

Bit 3 / Transmit Bit 4 Suppress (TBSE4). Set to one to stop this bit from being used.

Bit 4 / Transmit Bit 5 Suppress (TBSE5). Set to one to stop this bit from being used.

Bit 5 / Transmit Bit 6 Suppress (TBSE6). Set to one to stop this bit from being used.

Bit 6 / Transmit Bit 7 Suppress (TBSE7). Set to one to stop this bit from being used.

Bit 7 / Transmit Bit 8 Suppress (TBSE8). MSB of the channel. Set to one to stop this bit from being used.

9.17.1 Transmit HDLC FIFO Control

Control of the transmit FIFO is accomplished via the Transmit HDLC FIFO Control (THFC). The FIFO Control register sets the watermarks for the receive FIFO.

When the transmit FIFO empties below the low watermark, the TLWM bit in the appropriate HDLC status register will be set. TLWM is a real-time bit and remains set as long as the transmit FIFO's write pointer is below the watermark. If enabled, this condition can also cause an interrupt via the $\overline{INT}$ pin.

Register Name: **THFC**
Register Description: **Transmit HDLC FIFO Control Register**
Register Address: **187h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	TFLWM1	TFLWM0
Default	0	0	0	0	0	0	0	0

Bit 0 to Bit 1 / Transmit HDLC FIFO Low Watermark Select (TFLWM0 to TFLWM1)

TFLWM1	TFLWM0	Transmit FIFO Watermark
0	0	4 bytes
0	1	16 bytes
1	0	32 bytes
1	1	48 bytes

Bits 2 to 7 / Unused. Must be set = 0 for proper operation.

9.17.2 HDLC Status and Information

TLS2 provides status information for the transmit HDLC controller. When a particular event has occurred (or is occurring), the appropriate bit in one of these registers will be set to a one. Some of the bits in these registers are latched and some are real time bits that are not latched. This section contains register descriptions that list which bits are latched and which are real time. With the latched bits, when an event occurs and a bit is set to a one, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again. The real time bits report the current instantaneous conditions that are occurring and the history of these bits is not latched.

Like the other latched status registers, the user will follow a read of the status bit with a write. The byte written to the register will inform the device which of the latched bits the user wishes to clear (the real-time bits are not affected by writing to the status register). The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to clear and a zero in the bit positions he or she does not wish to clear.

The HDLC status register, TLS2 has the ability to initiate a hardware interrupt via the $\overline{INT}$ output signal. Each of the events in this register can be either masked or unmasked from the interrupt pin via the receive HDLC Interrupt Mask Register (TIM2). Interrupts will force the $\overline{INT}$ signal low when the event occurs. The $\overline{INT}$ pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

Register Name: **TRTS2**
Register Description: **Transmit Real-Time Status Register 2 (HDLC)**
Register Address: **1B1h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TEMPTY	TFULL	TLWM	TNF
Default	0	0	0	0	0	0	0	0

All bits in this register are real time.

Bit 0 / Transmit FIFO Not Full Condition (TNF). Set when the transmit 64-byte FIFO has at least 1 byte available.

Bit 1 / Transmit FIFO Below Low Watermark Condition (TLWM). Set when the transmit 64-byte FIFO empties beyond the low watermark as defined by the Transmit Low Watermark Bits (TLWM).

Bit 2 / Transmit FIFO Full (TFULL). A real-time bit that is set high when the FIFO is full.

Bit 3 / Transmit FIFO Empty (TEMPTY). A real-time bit that is set high when the FIFO is empty.

Bits 4 to 7 / Unused

Register Name: **TLS2**
Register Description: **Transmit Latched Status Register 2 (HDLC)**
Register Address: **191h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	TFDLE	TUDR	TMEND	TLWMS	TNFS
Default	0	0	0	0	0	0	0	0

All bits in this register are latched and can create interrupts.

Bit 0 / Transmit FIFO Not Full Set Condition (TNFS). Set when the transmit 64–byte FIFO has at least one empty byte available for write. Rising edge detect of TNF. Indicates change of state from full to not full.

Bit 1 / Transmit FIFO Below Low Watermark Set Condition (TLWMS). Set when the transmit 64-byte FIFO empties beyond the low watermark as defined by the Transmit Low Watermark Bits (TLWM) (rising edge detect of TLWM).

Bit 2 / Transmit Message End Event (TMEND). Set when the transmit HDLC controller has finished sending a message.

Bit 3 / Transmit FIFO Underrun Event (TUDR). Set when the transmit FIFO empties out without having seen the TMEND bit set. An abort is automatically sent.

Bit 4 / Transmit FDL Register Empty (TFDLE). Set when the TFDL register has shifted out all 8 bits. Useful if the user wants to manually use the TFDL register to send messages, instead of using the HDLC or BOC controller circuits.

Bits 5 to 7 / Unused

Register Name: **TIM2**
Register Description: **Transmit Interrupt Mask Register 2**
Register Address: **1A1h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	TFDLE	TUDR	TMEND	TLWMS	TNFS
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit FIFO Not Full Set Condition (TNFS)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Transmit FIFO Below Low Watermark Set Condition (TLWMS)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Transmit Message End Event (TMEND)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Transmit FIFO Underrun Event (TUDR)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Transmit FDL Register Empty (TFDLE)
0 = interrupt masked
1 = interrupt enabled

Bits 5 to 7 / Unused. Must be set = 0 for proper operation.

9.17.3 FIFO Information

The Transmit FIFO Buffer Available register indicates the number of bytes that can be written into the transmit FIFO. The count form this register informs the host as to how many bytes can be written into the transmit FIFO without overflowing the buffer. This is a real-time register. The count shall remain valid and stable during the read cycle.

Register Name: **TFBA**
Register Description: **Transmit HDLC FIFO Buffer Available**
Register Address: **1B3h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name		TFBA6	TFBA5	TFBA4	TFBA3	TFBA2	TFBA1	TFBA0
Default	0	0	0	0	0	0	0	0

Bits 0 to 6 / Transmit FIFO Bytes Available (TFBAO to TFBA6). TFBA0 is the LSB.

Register Name: **THF**
Register Description: **Transmit HDLC FIFO**
Register Address: **1B4h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	THD7	THD6	THD5	THD4	THD3	THD2	THD1	THD0
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit HDLC Data Bit 0 (THD0). LSB of a HDLC packet data byte.

Bit 1 / Transmit HDLC Data Bit 1 (THD1)

Bit 2 / Transmit HDLC Data Bit 2 (THD2)

Bit 3 / Transmit HDLC Data Bit 3 (THD3)

Bit 4 / Transmit HDLC Data Bit 4 (THD4)

Bit 5 / Transmit HDLC Data Bit 5 (THD5)

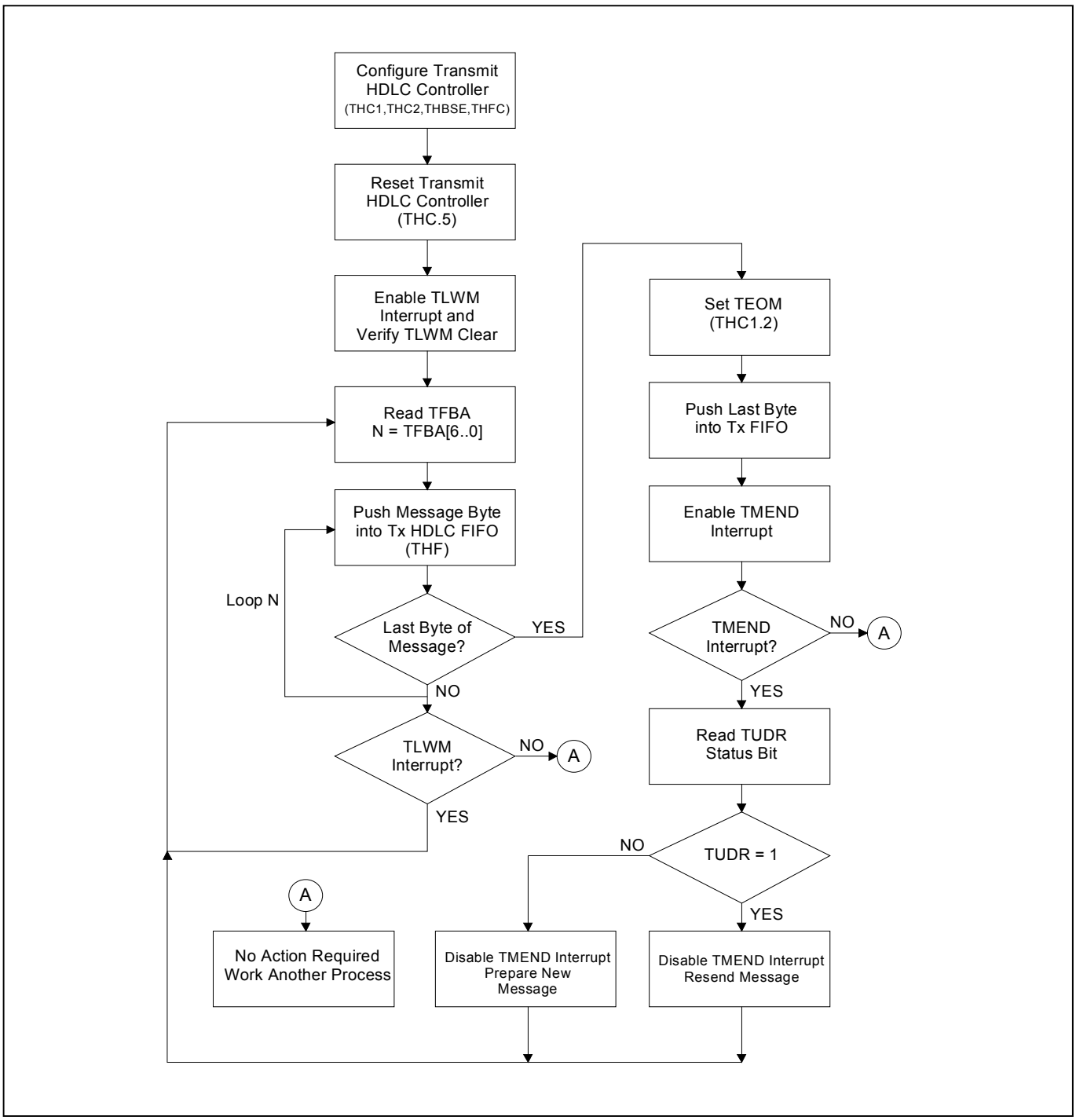
Bit 6 / Transmit HDLC Data Bit 6 (THD6)

Bit 7 / Transmit HDLC Data Bit 7 (THD7). MSB of a HDLC packet data byte.

9.18 HDLC Transmit Example

The HDLC status registers in the DS26401 allow for flexible software interface to meet the user's preferences. When transmitting HDLC messages, the host can chose to be interrupt driven, or to poll to desired status registers, or a combination of polling and interrupt processes may be used. An example routine for using the DS26401 HDLC receiver is given in Figure 9-1.

Figure 9-1. HDLC Message Transmit Example



9.19 Programmable In-Band Loop-Code Generator

The DS26401 has the ability to generate and detect a repeating bit pattern from one to eight bits or sixteen bits in length. This function is available only in T1 mode. To transmit a pattern, the user will load the pattern to be sent into the Transmit Code Definition registers (TCD1&TCD2) and select the proper length of the pattern by setting the TC0 and TC1 bits in Transmit Control Register 4 (TCR4). When generating a 1-, 2-, 4-, 8-, or 16-bit pattern both transmit code definition registers (TCD1&TCD2) must be filled with the proper code. Generation of a 3, 5, 6 and 7 bit pattern only requires TCD1 to be filled. Once this is accomplished, the pattern will be transmitted as long as the TLOOP control bit (TCR3.0) is enabled. Normally (unless the transmit formatter is programmed to not insert the F-bit position) the framer will overwrite the repeating pattern once every 193 bits to allow the F–bit position to be sent.

As an example, to transmit the standard “loop-up” code for Channel Service Units (CSUs), which is a repeating pattern of ...10000100001..., set TCD1 = 80h, TC0=0, TC1=0, and TCR3.0 = 1.

This register definition is repeated here for convenience.

Register Name: **TCR4**
Register Description: **Transmit Control Register 4**
Register Address: **186h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	TRAIM	TAISM	TC1	TC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 1 / Transmit Code Length Definition Bits (TC0 to TC1)

TC1	TC0	LENGTH SELECTED (BITS)
0	0	5
0	1	6/3
1	0	7
1	1	16/8/4/2/1

Bit 2 / Transmit AIS Mode (TAISM). Determines the pattern sent when TAIS (TCR1.1) is activated.
0 = transmit normal AIS (unframed all ones) upon activation with TCR1.1
1 = transmit AIS-CI (T1.403) upon activation with TCR1.1

Bit 3 / Transmit RAI Mode (TRAIM). Determines the pattern sent when TRAI (TCR1.0) is activated in ESF frame mode only.
0 = transmit normal RAI upon activation with TCR1.0
1 = transmit RAI-CI (T1.403) upon activation with TCR1.0

Bits 4 to 7 / Unused. Must be set = 0 for proper operation.

Register Name: **TCD1**
Register Description: **Transmit Code Definition Register 1**
Register Address: **1ACh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Code Definition Bit 0 (C0). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 1 / Transmit Code Definition Bit 1 (C1). A Don't Care if a 5- or 6-bit length is selected.

Bit 2 / Transmit Code Definition Bit 2 (C2). A Don't Care if a 5-bit length is selected.

Bit 3 / Transmit Code Definition Bit 3 (C3)

Bit 4 / Transmit Code Definition Bit 4 (C4)

Bit 5 / Transmit Code Definition Bit 5 (C5)

Bit 6 / Transmit Code Definition Bit 6 (C6)

Bit 7 / Transmit Code Definition Bit 7 (C7). First bit of the repeating pattern.

Register Name: **TCD2**
Register Description: **Transmit Code Definition Register 2**
Register Address: **1ADh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Transmit Code Definition Bit 0 to 7 (C0 to C7). A Don't Care if a 5-, 6-, or 7-bit length is selected.

9.20 Interleaved PCM Bus Operation (IBO)

In many architectures, the PCM outputs of individual framers are combined into higher speed PCM buses to simplify transport across the system backplane. The DS26401 can be configured to allow PCM data to be multiplexed into higher speed buses eliminating external hardware, saving board space and cost. The DS26401 can be configured for channel or frame interleave.

The interleaved PCM bus option (IBO) supports three bus speeds. The 4.096 MHz bus speed allows two PCM data streams to share a common bus. The 8.192 MHz bus speed allows four PCM data streams to share a common bus. The 16.384 MHz bus speed allows 8 PCM data streams to share a common bus. The receive elastic stores of each transceiver must be enabled. Via the IBO register the user can configure each framer for a specific bus position. For all IBO bus configurations each framer is assigned an exclusive position in the high speed PCM bus. The 8kHz frame sync can be generated from the system backplane or from the first device on the bus. All other devices on the bus must have their frame syncs configured as inputs. Relative to this common frame sync, the devices will await their turn to drive or sample the bus according to the settings of the DA0, DA1 and DA2 bits of the TIBOC register.

9.20.1 Channel Interleave

In channel interleave mode data is output to the PCM Data Out bus one channel at a time from each of the connected DS26401s until all channels of frame n from each framer has been placed on the bus. This mode can be used even when the DS26401s are operating asynchronous to each other. The elastic stores will manage slip conditions. The DS26401 provides an active-low signal (TIBO_OEB) during bus active times. TIBO_OEB can be used for bus multiplexer or tri-state buffer control.

9.20.2 Frame Interleave

In frame interleave mode data is output to the PCM Data Out bus one frame at a time from each of the framers. This mode is used only when all connected DS26401s are operating in a synchronous fashion (all inbound T1 or E1 lines are synchronous) and are synchronous with the system clock (system clock derived from T1 or E1 line). In this mode, slip conditions are not allowed.

Register Name: **TIBOC**
Register Description: **Transmit Interleave Bus Operation Control Register**
Register Address: **188h**

Bit #	7	6	5	4	3	2	1	0
Name	—	IBS1	IBS0	IBOSEL	IBOEN	DA2	DA1	DA0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2 / Device Assignment Bits (DA0 to DA2)

DA2	DA1	DA0	Device Position
0	0	0	1st Device on bus
0	0	1	2nd Device on bus
0	1	0	3rd Device on bus
0	1	1	4th Device on bus
1	0	0	5th Device on bus
1	0	1	6th Device on bus
1	1	0	7th Device on bus
1	1	1	8th Device on bus

Bit 3 / Interleave Bus Operation Enable (IBOEN)
0 = Interleave Bus Operation disabled.
1 = Interleave Bus Operation enabled.

Bit 4 / Interleave Bus Operation Select (IBOSEL). This bit selects channel or frame interleave mode.
0 = Channel Interleave
1 = Frame Interleave

Bits 5 to 6 / IBO Bus Size bit 1 (IBS0 to IBS1). Indicates how many devices on the bus.

IBS1	IBS0	Bus Size
0	0	2 Devices on bus
0	1	4 Devices on bus
1	0	8 Devices on bus
1	1	Reserved for future use

Bit 7 / Unused. Must be set = 0 for proper operation.

9.21 Interfacing the T1 Tx Formatter to the BERT

Data from the BERT can be inserted into the DS26401 transmit formatter data stream by using the registers described below. Either framed or unframed format can be transmitted, controlled by the TBFUS bit in the TBICR. Any signal DS0, combination of DS0s, or the entire bandwidth can be replaced with the BERT data as controlled by the TBCS registers.

Note that one BERT resource is shared between all 8 framers. Therefore, the TBEN bit should be set for only one framer at a time. If multiple framers have the TBEN bit set, the lower number framer will be assigned the resource.

Register Name: **TBICR**
Register Description: **Transmit BERT Interface Control Register**
Register Address: **18Ah + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	TBDC	TBFUS	TBEN
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit BERT Enable (TBEN)
0 = Transmit BERT is not assigned to this framer.
1 = Transmit BERT is assigned to this framer.

Bit 1 / Transmit BERT Framed/Unframed Select (TBFUS)
0 = The framer will not provide data from the F-bit position (framed)
1 = The framer will clock data from the F-bit position (unframed)

Bit 2 / Transmit BERT Direction Control (TBDC)
0 = Transmit Path: The BERT transmits toward the network via the TPOS and TNEG pins.
1 = Backplane: The BERT transmits toward the system backplane via the RSER pin.

Bits 3 to 7 / Unused. Must be set = 0 for proper operation.

Register Name: **TBCS1, TBCS2, TBCS3**
Register Description: **Transmit BERT Channel Select Registers**
Register Address: **0D4h, 0D5h, 0D6h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Setting any of the CH1 through CH24 bits in the TBCS1 through TBCS3 registers will map data from those channels to the on-board BERT. TBEN must be set to one for these registers to function. Multiple, or all channels may be selected simultaneously. These registers affect the transmit-side framer only.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**TBCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**TBCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**TBCS3**

Register Name: **TBBS**
Register Description: **Transmit BERT Bit Suppress Register**
Register Address: **18Bh**

Bit #	7	6	5	4	3	2	1	0
Name	BSE8	BSE7	BSE6	BSE5	BSE4	BSE3	BSE2	BSE1
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Channel Bit 1 Suppress (BSE1). LSB of the channel. Set to one to stop this bit from being used.

Bit 1 / Transmit Channel Bit 2 Suppress (BSE2). Set to one to stop this bit from being used.

Bit 2 / Transmit Channel Bit 3 Suppress (BSE3). Set to one to stop this bit from being used.

Bit 3 / Transmit Channel Bit 4 Suppress (BSE4). Set to one to stop this bit from being used.

Bit 4 / Transmit Channel Bit 5 Suppress (BSE5). Set to one to stop this bit from being used.

Bit 5 / Transmit Channel Bit 6 Suppress (BSE6). Set to one to stop this bit from being used.

Bit 6 / Transmit Channel Bit 7 Suppress (BSE7). Set to one to stop this bit from being used.

Bit 7 / Transmit Channel Bit 8 Suppress (BSE8). MSB of the channel. Set to one to stop this bit from being used.

9.22 T1 Transmit Synchronizer

When enabled, the DS26401 transmitter has the ability to identify the D4 or ESF frame boundary within the incoming NRZ data stream at TSER. The TFM (TCR3.2) control bit determines whether the transmit synchronizer searches for the D4 or ESF multiframe. Additional control signals for the transmit synchronizer are located in the TSYNCC register. The Transmit Latched Status 3 (TLS3) register provides a latched status bit (LOFD) to indicate that a Loss-of-Frame synchronization has occurred, and a real-time bit (LOF) which is set high when the synchronizer is searching for frame/multiframe alignment. The LOFD bit can be enabled to cause an interrupt condition on $\overline{INT}$.

Note that when the transmit synchronizer is used, the TSYNC signal should be set as an output (TSIO = 1) and the recovered frame sync pulse will be output on this signal. The recovered multiframe sync pulse will be output if enabled with TIOCR.0 (TSM = 1). The transmit synchronizer cannot be used while the transmit elastic store is enabled.

Register Name: **TSYNCC**
Register Description: **Transmit Synchronizer Control Register**
Register Address: **18Eh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	TSEN	SYNCE	RESYNC
Default	0	0	0	0	0	0	0	0

Bit 0 / Resynchronize (RESYNC)
When toggled from low to high, a resynchronization of the transmit side framer is initiated. Must be cleared and set again for a subsequent resync.

Bit 1 / Sync Enable (SYNCE)
0 = auto resync enabled
1 = auto resync disabled

Bit 2 / Transmit Synchronizer Enable (TSEN)
0 = Transmit Synchronizer Disabled
1 = Transmit Synchronizer Enabled

Bits 3 to 7 / Unused. Must be set = 0 for proper operation.

Register Name: **TLS3**
Register Description: **Transmit Latched Status Register 3 (Synchronizer)**
Register Address: **192h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	LOF	LOFD
Default	0	0	0	0	0	0	0	0

Bit 0 / Loss Of Frame Synchronization Detect (LOFD). This latched bit is set when the transmit synchronizer is searching for the sync pattern in the incoming data stream.

Bit 1 / Loss of Frame (LOF). A real-time bit that indicates that the transmit synchronizer is searching for the sync pattern in the incoming data stream.

Bits 2 to 7 / Unused

Register Name: **TIM3**
Register Description: **Transmit Interrupt Mask Register 3 (Synchronizer)**
Register Address: **1A2h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	LOFD
Default	0	0	0	0	0	0	0	0

Bit 0 / Loss Of Frame Synchronization Detect (LOFD)
0 = Interrupt Masked
1 = Interrupt Enabled

Bits 1 to 7 / Unused. Must be set = 0 for proper operation.

10. E1 RECEIVER

10.1 E1 Receiver Register Map

ADDRESS	TYPE	FUNCTION	NAME	PAGE
000	—	Unused	—	—
001	—	Unused	—	—
002	—	Unused	—	—
003	—	Unused	—	—
004	—	Unused	—	—
005	—	Unused	—	—
006	—	Unused	—	—
007	—	Unused	—	—
008	—	Unused	—	—
009	—	Unused	—	—
00A	—	Unused	—	—
00B	—	Unused	—	—
00C	—	Unused	—	—
00D	—	Unused	—	—
00E	—	Unused	—	—
00F	—	Unused	—	—
010	R/W	Rx HDLC Control	RHC	200
011	R/W	Rx HDLC Bit Suppress	RHBSE	200
012	R/W	Rx DS0 Monitor Select	RDS0SEL	181
013	R/W	Rx Signaling Control	RSIGC	184
014	—	Unused	—	—
015	—	Unused	—	—
016	—	Unused	—	—
017	—	Unused	—	—
018	—	Unused	—	—
019	—	Unused	—	—
01A	—	Unused	—	—
01B	—	Unused	—	—
01C	R/W	Rx Test Register 1	RTEST1	—
01D	R/W	Rx Test Register 2	RTEST2	—
01E	R/W	Rx Test Register 3	RTEST3	—
01F	R/W	Rx Test Register 4	RTEST4	—
020	R/W	Rx Idle Definition 1	RIDR1	76
021	R/W	Rx Idle Definition 2	RIDR2	76
022	R/W	Rx Idle Definition 3	RIDR3	76
023	R/W	Rx Idle Definition 4	RIDR4	76
024	R/W	Rx Idle Definition 5	RIDR5	76
025	R/W	Rx Idle Definition 6	RIDR6	76
026	R/W	Rx Idle Definition 7	RIDR7	76
027	R/W	Rx Idle Definition 8	RIDR8	76
028	R/W	Rx Idle Definition 9	RIDR9	76
029	R/W	Rx Idle Definition 10	RIDR10	76
02A	R/W	Rx Idle Definition 11	RIDR11	76
02B	R/W	Rx Idle Definition 12	RIDR12	76
02C	R/W	Rx Idle Definition 13	RIDR13	76
02D	R/W	Rx Idle Definition 14	RIDR14	76
02E	R/W	Rx Idle Definition 15	RIDR15	76
02F	R/W	Rx Idle Definition 16	RIDR16	76
030	R/W	Rx Idle Definition 17	RIDR17	76
031	R/W	Rx Idle Definition 18	RIDR18	76
032	R/W	Rx Idle Definition 19	RIDR19	76
033	R/W	Rx Idle Definition 20	RIDR20	76
034	R/W	Rx Idle Definition 21	RIDR21	76
035	R/W	Rx Idle Definition 22	RIDR22	76
036	R/W	Rx Idle Definition 23	RIDR23	76
037	R/W	Rx Idle Definition 24	RIDR24	76

ADDRESS	TYPE	FUNCTION	NAME	PAGE
038	R/W	Rx Idle Definition 25	RIDR25	76
039	R/W	Rx Idle Definition 26	RIDR26	76
03A	R/W	Rx Idle Definition 27	RIDR27	76
03B	R/W	Rx Idle Definition 28	RIDR28	76
03C	R/W	Rx Idle Definition 29	RIDR29	76
03D	R/W	Rx Idle Definition 30	RIDR30	76
03E	R/W	Rx Idle Definition 31	RIDR31	76
03F	R/W	Rx Idle Definition 32	RIDR32	76
040	R	Rx Signaling 1	RS1	185
041	R	Rx Signaling 2	RS2	185
042	R	Rx Signaling 3	RS3	185
043	R	Rx Signaling 4	RS4	185
044	R	Rx Signaling 5	RS5	185
045	R	Rx Signaling 6	RS6	185
046	R	Rx Signaling 7	RS7	185
047	R	Rx Signaling 8	RS8	185
048	R	Rx Signaling 9	RS9	185
049	R	Rx Signaling 10	RS10	185
04A	R	Rx Signaling 11	RS11	185
04B	R	Rx Signaling 12	RS12	185
04C	R	Rx Signaling 13	RS13	185
04D	R	Rx Signaling 14	RS14	185
04E	R	Rx Signaling 15	RS15	185
04F	R	Rx Signaling 16	RS16	185
050	R	Rx Line-Code Violation Counter 1	LCVCR1	66
051	R	Rx Line-Code Violation Counter 2	LCVCR2	66
052	R	Rx Path-Code Violation Counter 1	PCVCR1	67
053	R	Rx Path-Code Violation Counter 2	PCVCR2	67
054	R	Rx Frames Out-of-Sync Counter 1	FOSCR1	68
055	R	Rx Frames Out-of-Sync Counter 2	FOSCR2	68
056	R	Receive E-Bit Counter 1	EBCR1	180
057	R	Receive E-Bit Counter 2	EBCR2	180
058	—	Unused	—	—
059	—	Unused	—	—
05A	—	Unused	—	—
05B	—	Unused	—	—
05C	—	Unused	—	—
05D	—	Unused	—	—
05E	—	Unused	—	—
05F	—	Unused	—	—
060	R	Rx DS0 Monitor	RDS0M	181
061	—	Unused	—	—
062	R	Receive Real-Time Status 7	RRTS7	—
063	—	Unused	—	—
064	R	Receive Align Frame	RAF	194
065	R	Receive Non-Align Frame	RNAF	195
066	R	Receive Si Bits for Align Frame	RSiAF	195
067	R	Receive Si Bits for Non-Align Frame	RSiNAF	196
068	R	Receive Remote Alarm Bits	RRA	196
069	R	Receive Sa4 Bits	RSa4	197
06A	R	Receive Sa5 Bits	RSa5	197
06B	R	Receive Sa6 Bits	RSa6	198
06C	R	Receive Sa7 Bits	RSa7	198
06D	R	Receive Sa8 Bits	RSa8	199
06E	—	Unused	—	—
06F	—	Unused	—	—
070	—	Unused	—	—
071	—	Unused	—	—
072	—	Unused	—	—
073	—	Unused	—	—
074	—	Unused	—	—

ADDRESS	TYPE	FUNCTION	NAME	PAGE
075	—	Unused	—	—
076	—	Unused	—	—
077	—	Unused	—	—
078	—	Unused	—	—
079	—	Unused	—	—
07A	—	Unused	—	—
07B	—	Unused	—	—
07C	—	Unused	—	—
07D	—	Unused	—	—
07E	—	Unused	—	—
07F	—	Unused	—	—
080	R/W	Rx Master Mode	RMMR	156
081	R/W	Rx Control 1	RCR1	158
082	R/W	Rx Control 2	RCR2	159
083	R/W	Rx Control 3	RCR3	160
084	R/W	Rx I/O Configuration	RIOCR	161
085	R/W	Rx Elastic Store Control	RESCR	190
086	R/W	Rx Error Count Configuration	ERCNT	176
087	R/W	Rx HDLC FIFO Control	RHFC	201
088	R/W	Rx Interleave Bus Op Control	RIBOC	209
089	—	Unused	—	—
08A	R/W	Rx BERT Interface Control	RBICR	210
08B	R/W	Rx BERT Bit Suppress Enable	RBBS	211
08C	—	Unused	—	—
08D	—	Unused	—	—
08E	R/W	Rx Test Register 5	RTEST5	
08F	R/W	Rx Test Register 6	RTEST6	
090	R/W	Rx Latched Status 1	RLS1	54
091	R/W	Rx Latched Status 2	RLS2	56
092	R/W	Rx Latched Status 3	RLS3	57
093	R/W	Rx Latched Status 4	RLS4	59
094	R/W	Rx Latched Status 5 (HDLC)	RLS5	97
095	—	Unused	—	—
096	—	Unused	—	—
097	—	Unused	—	—
098	R/W	Rx Signaling Change-of-State Status 1	RSS1	74
099	R/W	Rx Signaling Change-of-State Status 2	RSS2	74
09A	R/W	Rx Signaling Change-of-State Status 3	RSS3	74
09B	R/W	Rx Signaling Change-of-State Status 4	RSS4	74
09C	—	Unused	—	—
09D	—	Unused	—	—
09E	—	Unused	—	—
09F	R/W	Rx Interrupt Information Reg	RIIR	157
0A0	R/W	Rx Interrupt Mask Reg 1	RIM1	167
0A1	R/W	Rx Interrupt Mask Reg 2	RIM2	169
0A2	R/W	Rx Interrupt Mask Reg 3	RIM3	171
0A3	R/W	Rx Interrupt Mask Reg 4	RIM4	174
0A4	R/W	Rx Interrupt Mask Reg 5 (HDLC)	RIM5	206
0A5	—	Unused	—	—
0A6	—	Unused	—	—
0A7	—	Unused	—	—
0A8	R/W	Rx Signaling Change-of-State Enable 1	RSCSE1	186
0A9	R/W	Rx Signaling Change-of-State Enable 2	RSCSE2	186
0AA	R/W	Rx Signaling Change-of-State Enable 3	RSCSE3	186
0AB	R/W	Rx Signaling Change-of-State Enable 4	RSCSE4	186
0AC	—	Unused	—	—
0AD	—	Unused	—	—
0AE	—	Unused	—	—
0AF	—	Unused	—	—
0B0	R	Rx Real-Time Status 1	RRTS1	165
0B1	—	Unused	—	—

ADDRESS	TYPE	FUNCTION	NAME	PAGE
0B2	R	Rx Real-Time Status 3	RRTS3	169
0B3	—	Unused	—	—
0B4	R	Rx Real-Time Status 5 (HDLC)	RRTS5	204
0B5	R	Rx HDLC Packet Bytes Available	RHPBA	202
0B6	R	Rx HDLC FIFO	RHF	203
0B7	—	Unused	—	—
0B8	—	Unused	—	—
0B9	—	Unused	—	—
0BA	—	Unused	—	—
0BB	—	Unused	—	—
0BC	—	Unused	—	—
0BD	—	Unused	—	—
0BE	—	Unused	—	—
0BF	—	Unused	—	—
0C0	R/W	Rx Blank Channel Select 1	RBCS1	191
0C1	R/W	Rx Blank Channel Select 2	RBCS2	191
0C2	R/W	Rx Blank Channel Select 3	RBCS3	191
0C3	R/W	Rx Blank Channel Select 4	RBCS4	191
0C4	R/W	Rx Channel Blocking 1	RCBR1	188
0C5	R/W	Rx Channel Blocking 2	RCBR2	188
0C6	R/W	Rx Channel Blocking 3	RCBR3	188
0C7	R/W	Rx Channel Blocking 4	RCBR4	188
0C8	R/W	Rx Signaling Insertion 1	RSI1	186
0C9	R/W	Rx Signaling Insertion 2	RSI2	186
0CA	R/W	Rx Signaling Insertion 3	RSI3	186
0CB	R/W	Rx Signaling Insertion 4	RSI4	186
0CC	R/W	Rx Gapped Clock Channel Select 1	RGCCS1	193
0CD	R/W	Rx Gapped Clock Channel Select 2	RGCCS2	193
0CE	R/W	Rx Gapped Clock Channel Select 3	RGCCS3	193
0CF	R/W	Rx Gapped Clock Channel Select 4	RGCCS4	193
0D0	R/W	Rx Channel Idle Code Enable 1	RCICE1	187
0D1	R/W	Rx Channel Idle Code Enable 2	RCICE2	187
0D2	R/W	Rx Channel Idle Code Enable 3	RCICE3	187
0D3	R/W	Rx Channel Idle Code Enable 4	RCICE4	187
0D4	R/W	Rx BERT Channel Select 1	RBCS1	191
0D5	R/W	Rx BERT Channel Select 2	RBCS2	191
0D6	R/W	Rx BERT Channel Select 3	RBCS3	191
0D7	R/W	Rx BERT Channel Select 4	RBCS4	191
0D8	—	Unused	—	—
0D9	—	Unused	—	—
0DA	—	Unused	—	—
0DB	—	Unused	—	—
0DC	—	Unused	—	—
0DD	—	Unused	—	—
0DE	—	Unused	—	—
0DF	—	Unused	—	—
0E0	—	Unused	—	—
0E1	—	Unused	—	—
0E2	—	Unused	—	—
0E3	—	Unused	—	—
0E4	—	Unused	—	—
0E5	—	Unused	—	—
0E6	—	Unused	—	—
0E7	—	Unused	—	—
0E8	—	Unused	—	—
0E9	—	Unused	—	—
0EA	—	Unused	—	—
0EB	—	Unused	—	—
0EC	—	Unused	—	—
0ED	—	Unused	—	—
0EE	—	Unused	—	—

ADDRESS	TYPE	FUNCTION	NAME	PAGE
0EF	—	Unused	—	—
0F0		Used by Global Functions		—
0F1		Used by Global Functions		—
0F2	—	Unused	—	—
0F3	—	Unused	—	—
0F4	—	Unused	—	—
0F5	—	Unused	—	—
0F6	—	Unused	—	—
0F7	—	Unused	—	—
0F8		Used by Global Functions		—
0F9		Used by Global Functions		—
0FA		Used by Global Functions		—
0FB	—	Unused	—	—
0FC	—	Unused	—	—
0FD	—	Unused	—	—
0FE	—	Unused	—	—
0FF	—	Unused	—	—

Note : The register addresses are 9-bits wide, but are shown here in hexadecimal. Addresses with the MSB clear (0xxH) are used for the DS26401 receiver; addresses with the MSB set (1xxH) are used for the DS26401 transmitter.

10.2 E1 Receive Framer Description and Operation

Eight fully independent DS1/E1 framers are included within the DS26401. The framers are designed to interface seamlessly to the line side via an external LIU. Each framer can be individually programmed to accept AMI, HDB3 (E1), B8ZS (T1), or NRZ data. In E1 mode each framer supports FAS, CRC-4, and CAS frame formats, and detects/reports common alarms such as AIS, RAI, LOS, and LOF. Performance monitor counters are maintains for each port which report bipolar/line code violations, CRC-4 errors, FAS errors, and E-bits.

Each framer has an HDLC controller which can be mapped into a single time slot, or Sa4 to Sa8 bits (E1 Mode) or the FDL (T1 Mode) and includes 64 byte FIFO buffers in both the transmit and receive paths.

Host interface is simplified with status registers optimized for either interrupt driven or polled environments. In many cases, status bits are reported both real-time and latched on change-of-state with separate bits for each state change. Most latched bits can be mapped to generate an external interrupt on the $\overline{INT}$ pin.

Interface to the system backplane is simplified with flexible, 2 frame elastic-store buffers. An interleaved backplane option is also provided that supports 4.096, 8.192, or 16.384 MHz operation.

Additional details concerning the operation of the E1 framer are included within the register descriptions within this section.

10.3 Receive Master Mode Register

The Receive Master Mode Register (RMMR) controls the initialization of the receive side framer. The FRM_EN bit may be left 'low' if the framer for that particular port is not going to be used, putting the circuit in a low-power (sleep) state.

Register Name: **RMMR**
Register Description: **Receive Master Mode Register**
Register Address: **080h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	FRM_EN	INIT_DONE	—	—	—	—	SFTRST	T1/E1
Default	0	0	0	0	0	0	0	0

Bit 0 / Receiver T1/E1 Mode Select (T1/E1). Sets operating mode for receiver only! This bit must be set to the desired state before writing INIT_DONE.
0 = T1 operation
1 = E1 operation

Bit 1 / Soft Reset (SFTRST). Level sensitive processor reset. Should be taken high then low to reset and initialize the internal processor.
0 = Normal operation
1 = Hold the internal RISC in reset. This bit only affects the receive side processor.

Bits 2 to 5 / Unused. Must be set = 0 for proper operation.

Bit 6 / Initialization Done (INIT_DONE). The host (user) must set this bit once he/she has written the configuration registers. The host is required to write or clear all RAM based registers (addresses 00H to 7FH) prior to setting this bit. Once INIT_DONE is set, the internal processor will check the FRM_EN bit. If enabled, the internal processor continues executing based on the initial configuration.

Bit 7 / Framer Enable (FRM_EN). This bit must be written with the desired value prior to setting INIT_DONE.
0 = Framer disabled – held in low power state
1 = Framer enabled – all features active

10.4 Interrupt Information Registers

The Interrupt Information Registers provide an indication of which DS26401 Status Registers are generating an interrupt. When an interrupt occurs, the host can read RIIR to quickly identify which of the 6 E1 receive status registers are causing the interrupt. The Interrupt Information Register bits will clear once the appropriate interrupt has been serviced and cleared, as long as no other interrupt condition is present in the associated status register. Status bits that have been masked via the Receive Interrupt Mask (RIMx) registers, will also be masked from the IIR registers.

Register Name: **RIIR**
Register Description: **Receive Interrupt Information Register**
Register Address: **09Fh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name			RLS6	RLS5	RLS4	RLS3	RLS2	RLS1
Default	0	0	0	0	0	0	0	0

10.5 E1 Receive Control Registers

Register Name: **RCR1**
Register Description: **Receive Control Register 1**
Register Address: **081h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	RHDB3	RSIGM	RG802	RCRC4	FRC	SYNCE	RESYNC
Default	0	0	0	0	0	0	0	0

Bit 0 / Resynchronize (RESYNC)
When toggled from low to high, a resynchronization of the receive-side framer is initiated. Must be cleared and set again for a subsequent resync.

Bit 1 / Sync Enable (SYNCE)
0 = auto resync enabled
1 = auto resync disabled

Bit 2 / Frame Resync Criteria (FRC)
0 = resync if FAS received in error 3 consecutive times
1 = resync if FAS or bit 2 of non-FAS is received in error 3 consecutive times

Bit 3 / Receive CRC4 Enable (RCRC4)
0 = CRC4 disabled
1 = CRC4 enabled

Bit 4 / Receive G.802 Enable (RG802)
0 = do not force RCHBLK high during bit 1 of time slot 26
1 = force RCHBLK high during bit 1 of time slot 26

Bit 5 / Receive Signaling Mode Select (RSIGM)
0 = CAS signaling mode
1 = CCS signaling mode

Bit 6 / Receive HDB3 Enable (RHDB3)
0 = HDB3 disabled
1 = HDB3 enabled

Bit 7 / Unused. Must be set = 0 for proper operation.

Table 10-1. E1 Sync/Resync Criteria

FRAME OR MULTIFRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frame N and N + 2, and FAS not present in frame N + 1	Three consecutive incorrect FAS received Alternate: (RCR1.2 = 1) The above criteria is met or three consecutive incorrect bit 2 of non-FAS received	G.706 4.1.1 and 4.1.2
CRC4	Two valid MF alignment words found within 8 ms	915 or more CRC4 code words out of 1000 received in error	G.706 4.2 and 4.3.2
CAS	Valid MF alignment word found. Alternate: (RSIGC.4 = 1) Valid MF alignment word found and previous time slot 16 contains code other than all zeros.	Two consecutive MF alignment words received in error or for a period of 1 multiframe, all the bits in time slot 16 are zero. Alternate: (RSIGC.4 = 1) The above criteria is met or 1 multiframe is received with all bits in time slot 16 set to 0.	G.732 5.2

Register Name: **RCR2**
Register Description: **Receive Control Register 2**
Register Address: **082h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	RLOSA
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Loss of Signal Alternate Criteria (RLOSA). Defines the criteria for an LOS condition.
0 = LOS declared upon 255 consecutive zeros (125μs)
1 = LOS declared upon 2048 consecutive zeros (1ms)

Bits 1 to 7/ Unused. Must be set = 0 for proper operation.

Register Name: **RCR3**
Register Description: **Receive Control Register 3**
Register Address: **083h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	IDF	—	RSERC	—	—	RLB	PLB	FLB
Default	0	0	0	0	0	0	0	0

Bit 0 / Framer Loopback (FLB)
0 = loopback disabled
1 = loopback enabled

This loopback is useful in testing and debugging applications. In FLB, the DS26401 will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1) (T1 mode) an unframed all one's code will be transmitted at TPOS and TNEG
   (E1 mode) normal data will be transmitted at TPOS and TNEG
2) Data at RPOS and RNEG will be ignored
3) All receive side signals will take on timing synchronous with TCLK instead of RCLK.
   Please note that it is not acceptable to have RCLK tied to TCLK during this loopback because this will cause an unstable condition.

Bit 1 / Payload Loopback (PLB)
0 = loopback disabled
1 = loopback enabled

When PLB is enabled, the following will occur:

1) Data will be transmitted from the TPOS and TNEG pins synchronous with RCLK instead of TCLK
2) All of the receive side signals will continue to operate normally
3) The TCHCLK and TCHBLK signals are forced low
4) Data at the TSER pin is ignored

Normally, this loopback is only enabled when ESF framing is being performed but can be enabled also in D4 framing applications. In a PLB situation, the DS26401 will loop the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, they are reinserted by the DS26401.

Bit 2 / Remote Loopback (RLB)
0 = loopback disabled
1 = loopback enabled

In this loopback, data input via the RPOS and RNEG pins will be transmitted back to the TPOS and TNEG pins. Data will continue to pass through the receive side framer of the DS26401 as it would normally and the data from the transmit side formatter will be ignored.

Bits 3, 4, 6 / Unused. Must be set = 0 for proper operation.

Bit 5 / RSER Control (RSERC)
0 = allow RSER to output data as received under all conditions (normal operation)
1 = force RSER to one under loss of frame alignment conditions

Bit 7 / Input Data Format (IDF)
0 = Bipolar data is expected at RPOS and RNEG (either AMI or B8ZS)
1 = NRZ data is expected at RPOS. The BPV counter will be disabled and RNEG will be ignored by the DS26401.

Register Name: **RIOCR**
Register Description: **Receive I/O Configuration Register**
Register Address: **084h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RCLKINV	RSYNCINV	H100EN	RSCLKM	—	RSIO	RSMS2	RSMS1
Default	0	0	0	0	0	0	0	0

Bit 0 / RSYNC Mode Select 1 (RSMS1). Selects frame or multiframe pulse when RSYNC pin is in output mode. In input mode (elastic store must be enabled) multiframe mode is only useful when receive signaling reinsertion is enabled.
0 = frame mode
1 = multiframe mode

Bit 1 / RSYNC Mode Select 2 (RSMS2)
T1: RSYNC pin must be programmed in the output frame mode
0 = do not pulse double wide in signaling frames
1 = do pulse double wide in signaling frames
E1: RSYNC pin must be programmed in the output multiframe mode
0 = RSYNC outputs CAS multiframe boundaries
1 = RSYNC outputs CRC4 multiframe boundaries

Bit 2 / RSYNC I/O Select (RSIO). (Note: This bit must be set to zero when elastic store is disabled.)
0 = RSYNC is an output
1 = RSYNC is an input (only valid if elastic store enabled)

Bit 3 / Unused. Must be set = 0 for proper operation.

Bit 4 / RSYSCLK Mode Select (RSCLKM)
0 = if RSYSCLK is 1.544MHz
1 = if RSYSCLK is 2.048MHz or IBO enabled

Bit 5 / H.100 SYNC Mode (H100EN). See Section 10.6.
0 = Normal operation
1 = RSYNC and TSSYNC shifted

Bit 6 / RSYNC Invert (RSYNCINV)
0 = No inversion
1 = Invert RSYNC as either input or output

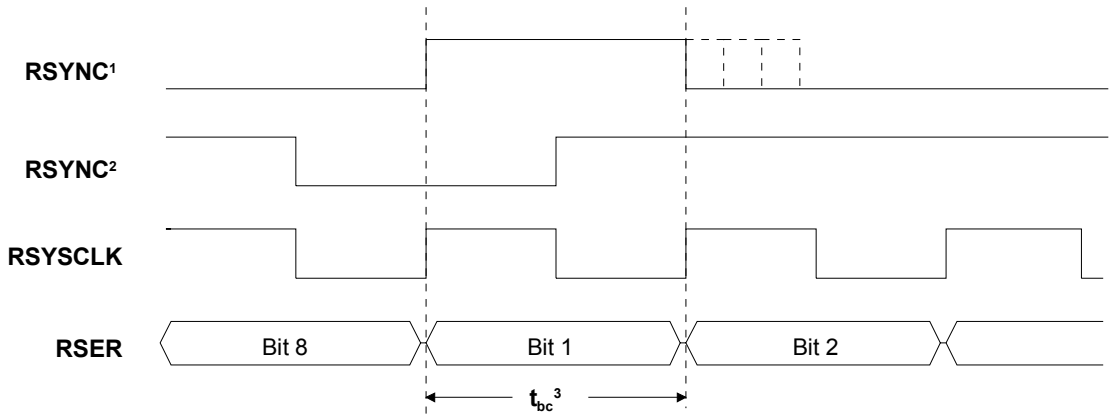
Bit 7 / RCLK Invert (RCLKINV)
0 = No inversion
1 = Invert RCLK input

10.6 H.100 (CT Bus) Compatibility

The H.100 (or CT Bus) is a synchronous, bit-serial, TDM transport bus operating at 8.192MHz. The H.100 standard also allows compatibility modes to operate at 2.048MHz, 4.096MHz, or 8.192MHz. The control bit H100EN (RIOCR.5), when combined with RSYNCINV and TSSYNCINV allows the DS26401 to accept the CT-Bus compatible frame sync signal (/CT_FRAME) at the RSYNC and TSSYNC inputs. The following rules apply to the H100EN control bit:

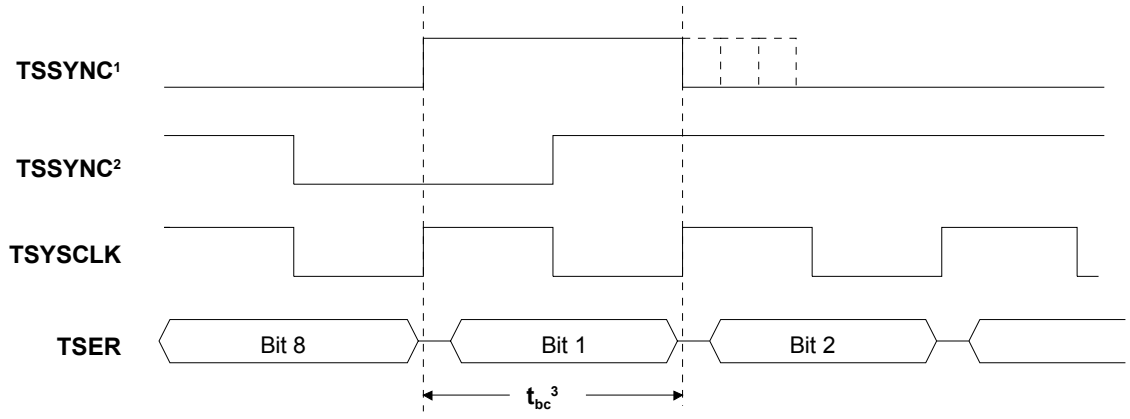
1) The H100EN bit controls the sampling point for the RSYNC (input mode) and TSSYNC only (the RSYNC output and other sync signals are not affected).
2) The H100EN bit would always be used in conjunction with the receive and transmit elastic store buffers.
3) The H100EN bit would typically be used with 8.192MHz IBO mode (Section 8.21), but could also be used with 4.096MHz IBO mode or 2.048MHz backplane operation.
4) The H100EN bit in RIOCR controls both RSYNC and TSSYNC (i.e., there is no separate control bit for the TSSYNC).
5) The H100EN bit does ***not*** invert the expected signal, RSYNCINV (RIOCR) and TSSYNCINV (TIOCR) must be set 'high' to invert the inbound sync signals.

Figure 10-1. RSYNC Input in H.100 (CT Bus) Mode



NOTE 1: RSYNC INPUT MODE IN NORMAL OPERATION.
NOTE 2: RSYNC INPUT MODE, H100EN = 1 and RSYNCINV = 1.
NOTE 3: t_{bc} (BIT-CELL TIME) = 122ns (typ). t_{bc} = 244ns or 488ns ALSO ACCEPTABLE.

Figure 10-2. TSSYNC Input in H.100 (CT Bus) Mode



NOTE 1: TSSYNC IN NORMAL OPERATION.
NOTE 2: TSSYNC WITH H100EN = 1 and TSSYNCINV = 1.
NOTE 3: t_{bc} (BIT-CELL TIME) = 122ns (typ). t_{bc} = 244ns or 488ns ALSO ACCEPTABLE.

10.7 E1 Receive Status and Information

When a particular event has occurred (or is occurring), the appropriate bit in one of these registers will be set to a one. Status bits may operate in either a latched or real-time fashion. Some latched bits may be enabled to generate a hardware interrupt via the $\overline{INT}$ signal.

Real-Time Bits
Some status bits operate in a real-time fashion. These bits are read-only and indicate the present state of an alarm or a condition. Real-time bits remain stable and valid during the host read operation. The current value of the internal status signals can be read at any time from the real time status registers without changing any the latched status register bits

Latched Bits
When an event or an alarm occurs and a latched bit is set to a one, it will remain set until cleared by the user. These bits typically respond on a change-of-state for an alarm, condition, or event; and operate in a read-then-write fashion. The user should read the value of the desired status bit, and then write a 1 to that particular bit location in order to clear the latched value (write a 0 to locations not to be cleared). Once the bit is cleared, it will not be set again until the event has occurred again.

Mask Bits
Some of the alarms and events can be either masked or unmasked from the interrupt pin via the Interrupt Mask Registers (RIMx). When unmasked, the $\overline{INT}$ signal will be forced low when the enabled event or condition occurs. The $\overline{INT}$ pin will be allowed to return high (if no other unmasked interrupts are present) when the user reads then clears (with a write) the alarm bit that caused the interrupt to occur. Note that the latched status bit and the INT pin will clear even if the alarm is still present.

Note that some conditions may have multiple status indications. For example, Receive Loss of Frame (RLOF) provides the following indications:

RRTS1.0 (RLOF)	Real-time indication that the receiver is not synchronized with incoming data stream. Read-only bit that remains high as long as the condition is present.
RLS1.0 (RLOFD)	Latched indication that the receiver has loss synchronization since the bit was last cleared. Bit will clear when written by the user, even if the condition is still present (rising edge detect of RRTS1.0).
RLS1.4 (RLOFC)	Latched indication that the receiver has reacquired synchronization since the bit was last cleared. Bit will clear when written by the user, even if the condition is still present (falling edge detect of RRTS1.0).

Table 10-2. E1 Alarm Criteria

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC.
RLOF	An RLOF condition exist on power up prior to initial synchronization, when a resync criteria has been met, or when a manual resync has been initiated via RCR1.0		
RLOS	255 or 2048 consecutive zeros received as determined by RCR2.0	In 255-bit times, at least 32 ones are received	G.775/G.962
RRAI	Bit 3 of non-align frame set to one for three consecutive occasions	Bit 3 of non-align frame set to zero for three consecutive occasions	O.162
RAIS	Fewer than three zeros in two frames (512 bits)	More than two zeros in two frames (512 bits)	O.162
RDMA	Bit 6 of time slot 16 in frame 0 has been set for two consecutive multiframes		
V52LNK	2 out of 3 Sa7 bits are zero		G.965

Register Name: **RRTS1**
Register Description: **Receive Real-Time Status Register 1**
Register Address: **0B0h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	RRAI	RAIS	RLOS	RLOF
Default	0	0	0	0	0	0	0	0

All bits in this register are real-time (not latched).

Bit 0 / Receive Loss of Frame Condition (RLOF). Set when the DS26401 is not synchronized to the received data stream.

Bit 1 / Receive Loss of Signal Condition (RLOS). Set when 255 (or 2048 if RCR2.0 = 1) consecutive zeros have been detected at RPOS and RNEG.

Bit 2 / Receive Alarm Indication Signal Condition (RAIS). Set when an unframed all one's code is received at RPOS and RNEG.

Bit 3 / Receive Remote Alarm Indication Condition (RRAI). Set when a remote alarm is received at RPOS and RNEG.

Bits 4 to 7 / Unused

Register Name: **RLS1**
Register Description: **Receive Latched Status Register 1**
Register Address: **090h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RRAIC	RAISC	RLOSC	RLOFC	RRAID	RAISD	RLOSD	RLOFD
Default	0	0	0	0	0	0	0	0

All bits in this register are latched and can create interrupts.

Bit 0 / Receive Loss of Frame Condition Detect (RLOFD). Change of state indication that the DS26401 has lost synchronized to the received data stream (rising edge detect of RLOF).

Bit 1 / Receive Loss of Signal Condition Detect (RLOSD). Change of state indication. Set when 255 (or 2048 if RCR2.0 = 1) consecutive zeros have been detected at RPOS and RNEG (rising edge detect of RLOS).

Bit 2 / Receive AIS Condition Detect (RAISD). Change of state indication. Set when an unframed all one's code is received at RPOS and RNEG (rising edge detect of RAIS).

Bit 3 / Receive Remote Alarm Condition Detect (RRAID). Change of state indication. Set when a remote alarm is received at RPOS and RNEG (rising edge detect of RRAI).

Bit 4 / Receive Loss of Frame Condition Clear (RLOFC). Change of state indication. Set when an RLOF condition has cleared (falling edge detect of RLOF).

Bit 5 / Receive Loss of Signal Condition Clear (RLOSC). Change of state indication. Set when an RLOS condition has cleared (falling edge detect of RLOS).

Bit 6 / Receive AIS Condition Clear (RAISC). Change of state indication. Set when a RAIS condition has cleared (falling edge detect of RAIS).

Bit 7 / Receive Remote Alarm Condition Clear (RRAIC). Change of state indication. Set when a RRAI condition has cleared (falling edge detect of RRAI).

Register Name: **RIM1**
Register Description: **Receive Interrupt Mask Register 1**
Register Address: **0A0h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RRAIC	RAISC	RLOSC	RLOFC	RRAID	RAISD	RLOSD	RLOFD
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Loss of Frame Detect (RLOFD)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Receive Loss of Signal Detect (RLOSD)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Receive AIS Detect (RAISD)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Receive Remote Alarm Detect (RRAID)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Receive Loss of Frame Clear (RLOFC)
0 = interrupt masked
1 = interrupt enabled

Bit 5 / Receive Loss of Signal Clear (RLOSC)
0 = interrupt masked
1 = interrupt enabled

Bit 6 / Receive AIS Clear (RAISC)
0 = interrupt masked
1 = interrupt enabled

Bit 7 / Receive Remote Alarm Clear (RRAIC)
0 = interrupt masked
1 = interrupt enabled

Register Name: **RLS2**
Register Description: **Receive Latched Status Register 2**
Register Address: **091h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	CRCRC	CASRC	FASRC	RSA1	RSA0	RCMF	RAF
Default	0	0	0	0	0	0	0	0

All bits in this register are latched. Bits 0 to 3 can cause interrupts. There is no associated real-time register.

Bit 0 / Receive Align Frame Event (RAF). Set every 250μs at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.

Bit 1 / Receive CRC4 Multiframe Event (RCMF). Set on CRC4 multiframe boundaries; will continue to be set every 2ms on an arbitrary boundary if CRC4 is disabled.

Bit 2 / Receive Signaling All Zeros Event (RSA0). Set when over a full MF, time slot 16 contains all zeros.

Bit 3 / Receive Signaling All Ones Event (RSA1). Set when the contents of time slot 16 contain less than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.

Bit 4 / FAS Resync Criteria Met Event (FASRC). Set when 3 consecutive FAS words are received in error.

Bit 5 / CAS Resync Criteria Met Event (CASRC). Set when 2 consecutive CAS MF alignment words are received in error.

Bit 6 / CRC Resync Criteria Met Event (CRCRC). Set when 915/1000 codewords are received in error.

Bit 7 / Unused

Register Name: **RIM2**
Register Description: **Receive Interrupt Mask Register 2**
Register Address: **0A1h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	RSA1	RSA0	RCMF	RAF
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Align Frame Event (RAF)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Receive CRC4 Multiframe Event (RCMF)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Receive Signaling All Zeros Event (RSA0)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Receive Signaling All Ones Event (RSA1)
0 = interrupt masked
1 = interrupt enabled

Bits 4 to 7 / Unused. Must be set = 0 for proper operation.

Register Name: **RRTS3**
Register Description: **Receive Real-Time Status Register 3**
Register Address: **0B2h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	LORC	—	V52LNK	RDMA
Default	0	0	0	0	0	0	0	0

All bits in this register are real-time (not latched).

Bit 0 / Receive Distant MF Alarm Condition (RDMA). Set when bit-6 of time slot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.

Bit 1 / V5.2 Link Detected Condition (V52LNK). Set on detection of a V5.2 link identification signal. (G.965).

Bits 2, 4 to 7 / Unused.

Bit 3 / Loss of Receive Clock Condition (LORC). Set when the RCLK pin has not transitioned for one channel time.

Register Name: **RLS3**
Register Description: **Receive Latched Status Register 3**
Register Address: **092h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	LORCC	—	V52LNKC	RDMAC	LORCD	—	V52LNKD	RDMAD
Default	0	0	0	0	0	0	0	0

All bits in this register are latched and can create interrupts.

Bit 0 / Receive Distant MF Alarm Detect (RDMAD). Change of state indication. Set when bit 6 of time slot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode. This is the rising edge detect of RDMA.

Bit 1 / V5.2 Link Detect (V52LNKD). Change of state indication. Set on detection of a V5.2 link identification signal. (G.965). This is the rising edge detect of V52LNK.

Bits 2, 6 / Unused

Bit 3 / Loss of Receive Clock Detect (LORCD). Change of state indication. Set when the RCLK pin has not transitioned for one channel time (rising edge detect of LORC).

Bit 4 / Receive Distant MF Alarm Clear (RDMAC). Change of state indication. Set when a RDMA condition has cleared (falling edge detect of RDMA).

Bit 5 / V5.2 Link Detected Clear (V52LNKC). Change of state indication. Set when a V52LNK condition has cleared (falling edge detect of V52LNK).

Bit 7 / Loss of Receive Clock Clear (LORCC). Change of state indication. Set when a LORC condition has cleared (falling edge detect of LORC).

Register Name: **RIM3**
Register Description: **Receive Interrupt Mask Register 3**
Register Address: **0A2h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	LORCC	—	V52LNKC	RDMAC	LORCD	—	V52LNKD	RDMAD
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Distant MF Alarm Detect (RDMAD)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / V5.2 Link Detect (V52LNKD)
0 = interrupt masked
1 = interrupt enabled

Bits 2, 6 / Unused. Must be set = 0 for proper operation.

Bit 3 / Loss of Receive Clock Detect (LORCD)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Receive Distant MF Alarm Clear (RDMAC)
0 = interrupt masked
1 = interrupt enabled

Bit 5 / V5.2 Link Detected Clear (V52LNKC)
0 = interrupt masked
1 = interrupt enabled

Bit 7 / Loss of Receive Clock Clear (LORCC)
0 = interrupt masked
1 = interrupt enabled

Register Name: **RRTS7**
Register Description: **Receive Real-Time Status Register 7**
Register Address: **062h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	CSC5	CSC4	CSC3	CSC2	CSC0	CRC4SA	CASSA	FASSA
Default	0	0	0	0	0	0	0	0

All bits in this register are real-time (not latched).

Bit 0 / FAS Sync Active (FASSA). Set while the synchronizer is searching for alignment at the FAS level.

Bit 1 / CAS MF Sync Active (CASSA). Set while the synchronizer is searching for the CAS MF alignment word.

Bit 2 / CRC4 MF Sync Active (CRC4SA). Set while the synchronizer is searching for the CRC4 MF alignment word.

Bits 3 to 7 / CRC4 Sync Counter Bits (CSC0 and CSC2 to CSC4). The CRC4 Sync Counter increments each time the 8ms CRC4 multiframe search times out. The counter is cleared when the framer has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (RCR1.3 = 0). This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC4 level. ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400ms, then the search should be abandoned and proper action taken. The CRC4 Sync Counter rolls over. CSC0 is the LSB of the 6-bit counter. (Note: The next to LSB is not accessible. CSC1 is omitted to allow resolution to >400ms using 5 bits.)

Register Name: **RLS4**
Register Description: **Receive Latched Status Register 4**
Register Address: **093h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RESF	RESEM	RSLIP	—	RSCOS	1SEC	TIMER	RMF
Default	0	0	0	0	0	0	0	0

All bits in this register are latched. There is no associated real-time register.

Bit 0 / Receive Multiframe Event (RMF). Set every 2.0ms on receive CAS multiframe boundaries to alert host the signaling data is available. Continues to set on an arbitrary 2.0ms boundary when CAS signaling is not enabled.

Bit 1 / Timer Event (TIMER). Follows the error counter update interval as determined by the ECUS bit in the Error Counter Configuration Register (ERCNT).

T1: Set on increments of 1 second or 42ms based on RCLK.
E1: Set on increments of 1 second or 62.5ms based on RCLK.

Bit 2 / One-Second Timer (1SEC). Set on every one-second interval based on RCLK.

Bit 3 / Receive Signaling Change Of State Event (RSCOS). Set when any channel selected by the Receive Signaling Change Of State Interrupt Enable registers (RSCSE1 through RSCSE3), changes signaling state.

Bit 4 / Unused

Bit 5 / Receive Elastic Store Slip Occurrence Event (RSLIP). Set when the receive elastic store has either repeated or deleted a frame.

Bit 6 / Receive Elastic Store Empty Event (RESEM). Set when the receive elastic store buffer empties and a frame is repeated.

Bit 7 / Receive Elastic Store Full Event (RESF). Set when the receive elastic store buffer fills and a frame is deleted.

Register Name: **RIM4**
Register Description: **Receive Interrupt Mask Register 4**
Register Address: **0A3h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RESF	RESEM	RSLIP	—	RSCOS	1SEC	TIMER	RMF
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Multiframe Event (RMF)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Timer Event (TIMER)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / One-Second Timer (1SEC)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Receive Signaling Change Of State Event (RSCOS)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Unused. Must be set = 0 for proper operation.

Bit 5 / Receive Elastic Store Slip Occurrence Event (RSLIP)
0 = interrupt masked
1 = interrupt enabled

Bit 6 / Receive Elastic Store Empty Event (RESEM)
0 = interrupt masked
1 = interrupt enabled

Bit 7 / Receive Elastic Store Full Event (RESF)
0 = interrupt masked
1 = interrupt enabled

10.8 E1 Error Count Registers

The DS26401 contains four counters that are used to accumulate line coding errors, path errors, and synchronization errors. Counter update options include one-second boundaries, 42ms (T1 mode only), 62.5ms (E1 mode only), or manually. See Error Counter Configuration Register (ERCNT). When updated automatically, the user can use the interrupt from the timer to determine when to read these registers. All four counters will saturate at their respective maximum counts and they will not rollover. The Line-Code Violation Count Register has the potential to saturate, but the bit error would have to exceed 10E-2 before this would occur. All other counters will roll over.

Several options are available for latching the performance counters:

1) Each framer's counters are latched independently based on independent one-second interval timers.
2) Each framer's counters are latched independently based on independent 62.5ms interval timers.
3) Each framer's counters are latched independently with a low to high transition on the respective MECU control bit.
4) Counters from selected framers are latched synchronously at the one-second interval supplied by framer_#1.
5) Counters from selected framers are synchronously latched manually with the Global Counter Latch Enable (GCLE) bit in GCR1.

The following table shows configuration bit settings in the ERCNT register for each of the 5 modes mentioned above:

Control Bit	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
EAMS	0	0	1	0	1
ECUS	0	1	X	0	0
MECU	0	0	0 to 1	0	0
MCUS	0	0	0	0	1
1SECS	0	0	0	1	0

Register Name: **ERCNT**
Register Description: **Error Counter Configuration Register**
Register Address: **086h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	1SECS	MCUS	MECU	ECUS	EAMS	—	—	LCVCRF
Default	0	0	0	0	0	0	0	0

Bit 0 / E1 Line Code Violation Count Register Function Select (LCVCRF)
0 = do not count excessive zeros
1 = count excessive zeros

Bits 1, 2 / Unused. Must be set = 0 for proper operation.

Bit 3 / Error Accumulation Mode Select (EAMS)
0 = ERCNT.4 determines accumulation time (timed update)
1 = ERCNT.5 determines accumulation time (manual update)

Bit 3 / Error Accumulation Mode Select (EAMS)
0 = ERCNT.4 determines accumulation time (timed update)
1 = ERCNT.5 determines accumulation time (manual update)

Bit 4 / Error Counter Update Select (ECUS)
T1 mode:
0 = Update error counters once a second
1 = Update error counters every 42ms (336 frames)
E1 mode:
0 = Update error counters once a second
1 = Update error counters every 62.5ms (500 frames)

Bit 5 / Manual Error Counter Update (MECU). When enabled by ERCNT.3, the changing of this bit from a 0 to a 1 allows the next clock cycle to load the error counter registers with the latest counts and reset the counters. The user must wait a minimum of 250μs before reading the error count registers to allow for proper update.

Bit 6 / Manual Counter Update Select (MCUS). When manual update mode is enabled with EAMS, this bit can be used to allow the GLCE bit in GCR1 to latch all counters. Useful for synchronously latching counters of multiple framers.
0 = MECU is used to manually latch counters.
1 = GLCE is used to manually latch counters.

Bit 7 / One-Second Select (1SECS). When timed update is enabled by EAMS, setting this bit for a specific framer will allow that framer's counters to latch on the one-second reference from framer #1. Note that this bit should always be clear for framer #1.
0 = Use internally generated one-second timer.
1 = Use 1 second timer from framer #1.

10.8.1 E1 Line Code Violation Count Register (LCVCR)

Either bipolar violations or code violations can be counted. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receive side, HDB3 codewords are not counted as BPVs. If ERCNT.0 is set, then the LVC counts code violations as defined in ITU O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the framer should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on an E1 line would have to be greater than 10** - 2 before the VCR would saturate. See Table 10-3.

Table 10-3. E1 Line Code Violation Counting Options

E1 CODE VIOLATION SELECT (ERCNT.0)	WHAT IS COUNTED IN THE LCVCRs
0	BPVs
1	CVs

Register Name: **LCVCR1**
Register Description: **Line Code Violation Count Register 1**
Register Address: **050h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	LCVC15	LCVC14	LCVC13	LCVC12	LCVC11	LCVC10	LCVC9	LCCV8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Line Code Violation Counter Bits 8 to 15 (LCVC8 to LCVC15). LCV15 is the MSB of the 16-bit code violation count.

Register Name: **LCVCR2**
Register Description: **Line Code Violation Count Register 2**
Register Address: **051h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	LCVC7	LCVC6	LCVC5	LCVC4	LCVC3	LCVC2	LCVC1	LCVC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Line Code Violation Counter Bits 0 to 7 (LCVC0 to LCVC7). LCV0 is the LSB of the 16-bit code violation count.

10.8.2 E1 Path Code Violation Count Register (PCVCR)

In E1 operation, the Path Code Violation Count register records CRC4 errors. Since the maximum CRC4 count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

The Path Code Violation Count Register 1 (PCVCR1) is the most significant word and PCVCR2 is the least significant word of a 16-bit counter that records path violations (PVs).

Register Name: **PCVCR1**
Register Description: **Path Code Violation Count Register 1**
Register Address: **052h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	PCVC15	PCVC14	PCVC13	PCVC12	PCVC11	PCVC10	PCVC9	PCVC8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Path Code Violation Counter Bits 8 to 15 (PCVC8 to PCVC15). PCVC15 is the MSB of the 16-bit path code violation count.

Register Name: **PCVCR2**
Register Description: **Path Code Violation Count Register 2**
Register Address: **053h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	PCVC7	PCVC6	PCVC5	PCVC4	PCVC3	PCVC2	PCVC1	PCVC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Path Code Violation Counter Bits 0 to 7 (PCVC0 to PCVC7). PCVC0 is the LSB of the 16-bit path code violation count.

10.8.3 E1 Frames Out-of-Sync Count Register (FOSCR)

In E1 mode, the FOSCR counts word errors in the Frame Alignment Signal in time slot 0. This counter is disabled when RLOF is high. FAS errors will not be counted when the framer is searching for FAS alignment and/or synchronization at either the CAS or CRC4 multiframe level. Since the maximum FAS word error count in a one-second period is 4000, this counter cannot saturate.

The Frames Out of Sync Count Register 1 (FOSCR1) is the most significant word and FOSCR2 is the least significant word of a 16-bit counter that records frames out of sync.

Register Name: **FOSCR1**
Register Description: **Frames Out Of Sync Count Register 1**
Register Address: **054h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	FOS15	FOS14	FOS13	FOS12	FOS11	FOS10	FOS9	FOS8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Frames Out of Sync Counter Bits 8 to 15 (FOS8 to FOS15). FOS15 is the MSB of the 16-bit frames out of sync count.

Register Name: **FOSCR2**
Register Description: **Frames Out Of Sync Count Register 2**
Register Address: **055h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	FOS7	FOS6	FOS5	FOS4	FOS3	FOS2	FOS1	FOS0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Frames Out of Sync Counter Bits 0 to 7 (FOS0 to FOS7). FOS0 is the LSB of the 16-bit frames out of sync count.

10.8.4 E-Bit Counter (EBCR)

This counter is only available in E1 mode. E–bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 16-bit counter that records Far End Block Errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers will increment once each time the received E-bit is set to zero. Since the maximum E-bit count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

Register Name: **EBCR1**
Register Description: **E–Bit Count Register 1**
Register Address: **056h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	EB15	EB14	EB13	EB12	EB11	EB10	EB9	EB8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / E-Bit Counter Bits 8 to 15 (EB8 to EB15). EB15 is the MSB of the 16-bit E-Bit count.

Register Name: **EBCR2**
Register Description: **E–Bit Count Register 2**
Register Address: **057h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / E-Bit Counter Bits 0 to 7 (EB0 to EB7). EB0 is the LSB of the 16-bit E-Bit count.

10.9 DS0 Monitoring Function

The DS26401 has the ability to monitor one DS0 64kbps channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the receive direction, the RCM0 to RCM4 bits in the RDS0SEL register need to be properly set and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the Receive DS0 (RDS0M) register. The RCM0 to RCM4 bits should be programmed with the decimal decode of the appropriate E1 channel. E1 channels 1 through 32 map to register values 0 through 31. For example, if DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into RDS0SEL:

RCM4 = 0
RCM3 = 1
RCM2 = 1
RCM1 = 1
RCM0 = 0

Register Name: **RDS0SEL**
Register Description: **Receive Channel Monitor Select**
Register Address: **012h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	RCM4	RCM3	RCM2	RCM1	RCM0
Default	0	0	0	0	0	0	0	0

Bits 0 to 4 / Receive Channel Monitor Bits (RCM0 to RCM4). RCM0 is the LSB of a 5-bit channel select that determines which receive DS0 channel data will appear in the RDS0M register.

Bits 5 to 7 / Unused. Must be set = 0 for proper operation.

Register Name: **RDS0M**
Register Description: **Receive DS0 Monitor Register**
Register Address: **060h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	B1	B2	B3	B4	B5	B6	B7	B8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Receive DS0 Channel Bits (B1 to B8). Receive channel data that has been selected by the Receive Channel Monitor Select Register. B8 is the LSB of the DS0 channel (last bit to be received).

10.10 E1 Receive Signaling Operation

There are two methods to access receive signaling data—processor-based (i.e., software-based) or hardware based. Processor-based refers to access through the transmit and receive signaling registers, RS1–RS16. Hardware-based refers to the RSIG pin. Both methods can be used simultaneously.

10.10.1 Processor-Based Signaling

Signaling data is sampled in the receive data stream and copied into the receive signaling registers, RS1 through RS16.. The signaling information in these registers is always updated on multiframe boundaries. This function is always enabled.

10.10.2 Change Of State

In order to avoid constantly monitoring of the receive signaling registers the DS26401 can be programmed to alert the host when any specific channel or channels undergo a change of their signaling state. RSCSE1 through RSCSE4 for E1 are used to select which channels can cause a change of state indication. The change of state is indicated in Latched Status Register 4 (RLS4.3). If signaling integration is enabled then the new signaling state must be constant for 3 multiframes before a change of state indication is indicated. The user can enable the $\overline{INT}$ pin to toggle low upon detection of a change in signaling by setting the appropriate interrupt mask bit RIM4.3. The signaling integration mode is global and cannot be enabled on a channel-by-channel basis.

The user can identity which channels have undergone a signaling change of state by reading the Receive Signaling Status (RSS1 through RSS4) registers. The information from these registers tell the user which RSx register to read for the new signaling data. All changes are indicated in the RSS1–RSS4 registers regardless of the RSCSE1–RSCSE4 registers.

10.10.3 Hardware-Based Receive Signaling

In hardware based signaling the signaling data can be obtained from the RSER pin or the RSIG pin. RSIG is a signaling PCM stream output on a channel-by-channel basis from the signaling buffer. The E1 TS16 signaling data is still present in the original data stream at RSER. The signaling buffer provides signaling data to the RSIG pin and also allows signaling data to be re-inserted into the original data stream in a different alignment that is determined by a multiframe signal from the RSYNC pin. In this mode, the receive elastic store may be enabled or disabled. If the receive elastic store is enabled, then the backplane clock (RSYSCLK) can be either 1.544 MHz or 2.048MHz. If IBO mode is enabled then RSYSCLK may also be 4.096MHz, 8.192MHz, or 16.384MHz. The ABCD signaling bits are output on RSIG in the lower nibble of each channel. The RSIG data is updated once per CAS multiframe (2ms) unless a freeze is in effect. See the timing diagrams in Section 13.4 for some examples.

10.10.4 Signaling Debounce

When signaling integration is enabled the signaling data at RSIG is automatically debounced. Signaling must be constant for three multiframes before being up-dated at RSIG. Signaling debounce is enabled on a global basis.

10.10.5 Receive Signaling Reinsertion at RSER

In this mode, the user will provide a multiframe sync at the RSYNC pin and the signaling data will be reinserted based on this alignment. In T1 mode, this results in two copies of the signaling data in the RSER data stream. The original signaling data based on the Fs/ESF frame positions and the realigned data based on the user supplied multiframe sync applied at RSYNC. In voice channels this extra copy of signaling data is of little consequence. Re-insertion can be avoided in data channels since this feature is activated on a per-channel basis. For reinsertion, the elastic store must be enabled, however, the backplane clock can be either 1.544MHz or 2.048MHz.

Signaling reinsertion mode is enabled, on a per-channel basis by setting the Receive Signaling Re-insertion Channel Select bit high in the RSI register. The channels that are to have signaling reinserted are selected by writing to the RSI1-RSI4 registers. In E1 mode, the user will generally select all channels or none for reinsertion.

10.10.6 Receive Signaling Freeze

The signaling data in the four multiframe signaling buffer will be frozen in a known good state upon either a loss of synchronization (OOF event), carrier loss, or change of frame alignment. To allow this freeze action to occur, the RSFE control bit (RSIGC.1) should be set high. The user can force a freeze by setting the RSFF control bit (RSIGC.2) high. The RSIGF output pin provides a hardware indication that a freeze is in effect. The four multiframe buffer provides a three multiframe delay in the signaling bits provided at the RSIG pin (and at the RSER pin if Receive Signaling Reinsertion is enabled). When freezing is enabled (RSFE = 1), the signaling data will be held in the last known good state until the corrupting error condition subsides. When the error condition subsides, the signaling data will be held in the old state for at least an additional 6ms before being allowed to be updated with new signaling data.

Register Name: **RSIGC**
Register Description: **Receive Signaling Control Register**
Register Address: **013h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	CASMS	—	RSFF	RSFE	RSIE
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Signaling Integration Enable (RSIE)
0 = signaling changes of state reported on any change in selected channels
1 = signaling must be stable for 3 multiframes in order for a change of state to be reported

Bit 1 / Receive Signaling Freeze Enable (RSFE)
0 = no freezing of receive signaling data will occur
1 = allow freezing of receive signaling data at RSIG (and RSER if Receive Signaling Re-insertion is enabled).

Bit2 / Receive Signaling Force Freeze (RSFF). Freezes receive-side signaling at RSIG (and RSER if Receive Signaling Reinsertion is enabled); will override Receive Freeze Enable (RFE).
0 = do not force a freeze event
1 = force a freeze event

Bits 3, 5 to 7 / Unused. Must be set = 0 for proper operation.

Bit 4 / CAS Mode Select (CASMS)
0 = The DS26401 will initiate a resync when two consecutive multiframe alignment signals have been received with an error.
1 = The DS26401 will initiate a resync when two consecutive multiframe alignment signals have been received with an error, or 1 multiframe has been received with all the bits in time slot 16 in state 0. Alignment criteria is met when at least one bit in state 1 is present in the time slot 16 preceding the multiframe alignment signal first detected (G.732 alternate criteria).

Register Name: **RS1 to RS16**
Register Description: **Receive Signaling Registers**
Register Address: **040h to 04Fh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

The Receive Signaling Registers are frozen and not updated during a loss of sync condition.They contain the most recent signaling information before the LOF occurred.

(MSB)							**(LSB)**	
0	0	0	0	X	Y	X	X	**RS1**
CH1-A	CH1-B	CH1-C	CH1-D	CH16-A	CH16-B	CH16-C	CH16-D	**RS2**
CH2-A	CH2-B	CH2-C	CH2-D	CH17-A	CH17-B	CH17-C	CH17-D	**RS3**
CH3-A	CH3-B	CH3-C	CH3-D	CH18-A	CH18-B	CH18-C	CH18-D	**RS4**
CH4-A	CH4-B	CH4-C	CH4-D	CH19-A	CH19-B	CH19-C	CH19-D	**RS5**
CH5-A	CH5-B	CH5-C	CH5-D	CH20-A	CH20-B	CH20-C	CH20-D	**RS6**
CH6-A	CH6-B	CH6-C	CH6-D	CH21-A	CH21-B	CH21-C	CH21-D	**RS7**
CH7-A	CH7-B	CH7-C	CH7-D	CH22-A	CH22-B	CH22-C	CH22-D	**RS8**
CH8-A	CH8-B	CH8-C	CH8-D	CH23-A	CH23-B	CH23-C	CH23-D	**RS9**
CH9-A	CH9-B	CH9-C	CH9-D	CH24-A	CH24-B	CH24-C	CH24-D	**RS10**
CH10-A	CH10-B	CH10-C	CH10-D	CH25-A	CH25-B	CH25-C	CH25-D	**RS11**
CH11-A	CH11-B	CH11-C	CH11-D	CH26-A	CH26-B	CH26-C	CH26-D	**RS12**
CH12-A	CH12-B	CH12-C	CH12-D	CH27-A	CH27-B	CH27-C	CH27-D	**RS13**
CH13-A	CH13-B	CH13-C	CH13-D	CH28-A	CH28-B	CH28-C	CH28-D	**RS14**
CH14-A	CH14-B	CH14-C	CH14-D	CH29-A	CH29-B	CH29-C	CH29-D	**RS15**
CH15-A	CH15-B	CH15-C	CH15-D	CH30-A	CH30-B	CH30-C	CH30-D	**RS16**

Register Name: **RSS1, RSS2, RSS3, RSS4**
Register Description: **Receive Signaling Status Registers**
Register Address: **098h, 099h, 09Ah, 09ABh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

When a channel's signaling data changes state, the respective bit in registers RSS1-RSS4 will be set and latched. The RSCOS bit (RLSR4.3) will be set if the channel was also enabled by setting the appropriate bit in RSCSE1-4. The $\overline{INT}$ signal will go low if enabled by the interrupt mask bit RIM4.3. The bit will remain set until read. Note that in CAS mode, the LSB of RSS1 would typically represent the CAS alignment bits, and the LSB of RSS3 represents reserved bits and the distant multiframe alarm.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1*	**RSS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RSS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17*	**RSS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**RSS4**

Status bits in this register are latched.

Register Name: **RSCSE1, RSCSE2, RSCSE3, RSCSE4**
Register Description: **Receive Signaling Change of State Enable**
Register Address: **0A8h, 0A9h, 0AAH, 0ABh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Setting any of the CH1 through CH32 bits in the RSCSE1 through RSCSE4 registers cause RSCOS (RLSR4.3) to be set when that channel's signaling data changes state.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1*	**RSCSE1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RSCSE2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17*	**RSCSE3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**RSCSE4**

Register Name: **RSI1, RSI2, RSI3, RSI4**
Register Description: **Receive Signaling Reinsertion Enable Registers**
Register Address: **0C8h, 0C9h, 0CAh, 0CBh [+ (200h * n) :where n= 0to7, for Ports 1to8]**

Setting any of the CH1 through CH32 bits in the RSI1 through RSI4 registers cause signaling data to be reinserted for the associated channel.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RSI1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RSI2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RSI3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**RSI4**

10.11 E1 Receive Per-Channel Idle Code Insertion

Channel data can be replaced by an idle code on a per-channel basis in the transmit and receive directions. Thirty-two Receive Idle Definition Registers (RIDR1-RIDR32) are provided to set the 8-bit idle code for each channel. The Receive Channel Idle Code Enable registers (RCICE1-4) are used to enable idle code replacement on a per channel basis.

Register Name: **RIDR1 to RIDR32**
Register Description: **Receive Idle Code Definition Registers 1 to 32**
Register Address: **020h to 03Fh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Per-Channel Idle Code Bits (C0 to C7). C0 is the LSB of the Code (this bit is transmitted last). Address 20H is for channel 1, address 3FH is for channel 32.

The Receive Channel Idle Code Enable Registers (RCICE1/2/3/4) are used to determine which of the 32 E1 channels from the E1 line to the backplane should be overwritten with the code placed in the Receive Idle Code Definition Register.

Register Name: **RCICE1, RCICE2, RCICE3, RCICE4**
Register Description: **Receive Channel Idle Code Enable Registers**
Register Address: **0D0h, 0D1h, 0D2h, 0D3h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RCICE1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RCICE2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RCICE3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**RCICE4**

Bits 0 to 7 / Receive Channels 1 to 32 Code Insertion Control Bits (CH1 to CH32)
0 = do not insert data from the Idle Code Array into the receive data stream
1 = insert data from the Idle Code Array into the receive data stream

10.12 Receive Channel Blocking Operation

The Receive Channel blocking Registers (RCBR1 / RCBR2 / RCBR3 / RCBR4) and the Transmit Channel Blocking Registers (TCBR1 / TCBR2 / TCBR3 / TCBR4) control the RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHBLK pins are user programmable outputs that can be forced high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN–PRI applications. When the appropriate bits are set to a one, the RCHBLK and TCHBLK pin will be held high during the entire corresponding channel time.

Register Name: **RCBR1, RCBR2, RCBR3, RCBR4**
Register Description: **Receive Channel Blocking Registers**
Register Address: **0C4h, 0C5h, 0C6h, 0C7h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RCBR1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RCBR2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RCBR3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**RCBR4**

Bits 0 to 7 / Receive Channels 1 to 32 Channel Blocking Control Bits (CH1 to CH32)
0 = force the RCHBLK pin to remain low during this channel time
1 = force the RCHBLK pin high during this channel time

10.13 Receive Elastic Stores Operation

The DS26401 contains dual two-frame elastic stores, one for the receive direction, and one for the transmit direction. Both elastic stores are fully independent. The transmit and receive side elastic stores can be enabled/disabled independent of each other. Also, each elastic store can interface to either a 1.544MHz or 2.048/4.096/8.192/16.384MHz backplane without regard to the backplane rate of the other elastic store.

The elastic stores have two main purposes. First, they can be used for rate conversion. When the DS26401 is in the T1 mode, the elastic stores can rate convert the T1 data stream to a 2.048MHz backplane. In E1 mode, the elastic store can rate convert the E1 data stream to a 1.544MHz backplane. Secondly, they can be used to absorb the differences in frequency and phase between the T1 or E1 data stream and an asynchronous (i.e., not locked) backplane clock (which can be 1.544MHz or 2.048MHz). In this mode, the elastic stores will manage the rate difference and perform controlled slips, deleting or repeating frames of data in order to manage the difference between the network and the backplane.

If the elastic store is enabled, then either CAS or CRC4 multiframe boundaries will be indicated via the RMSYNC output as controlled by the RSMS2 control bit (RIOCR.1). If the user selects to apply a 1.544 MHz clock to the RSYSCLK pin, then the RBCS registers will determine which channels of the received E1 data stream will be deleted. In this mode an F-bit location is inserted into the RSER data and set to one. Also, in 1.544 MHz applications, the RCHBLK output will not be active in Channels 25 through 32 (or in other words, RCBR4 is not active). If the two-frame elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data will be repeated at RSER and the RLS4.5 and RLS4.6 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the RLS4.5 and RLS4.7 bits will be set to a one.

The elastic stores can also be used to multiplex T1 or E1 data streams into higher backplane rates. This is the Interleave Bus Option (IBO) which is discussed in Section 10.17.

Register Name: **RESCR**
Register Description: **Receive Elastic Store Control Register**
Register Address: **085h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RDATFMT	RGCLKEN	—	RSZS	RESALGN	RESR	RESMDM	RESE
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Elastic Store Enable (RESE)
0 = elastic store is bypassed
1 = elastic store is enabled

Bit 1 / Receive Elastic Store Minimum Delay Mode (RESMDM)
0 = elastic stores operate at full two frame depth
1 = elastic stores operate at 32-bit depth

Bit 2 / Receive Elastic Store Reset (RESR). Setting this bit from a zero to a one will force the read pointer into the same frame that the write pointer is exiting, minimizing the delay through the elastic store. If this command should place the pointers within the slip zone (see bit 4), then an immediate slip will occur and the pointers will move back to opposite frames. Should be toggled after RSYSCLK has been applied and is stable. Do not leave this bit set HIGH.

Bit 3 / Receive Elastic Store Align (RESALGN). Setting this bit from a zero to a one will force the receive elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command will be executed and the data will be disrupted. Should be toggled after RSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align.

Bit 4 / Receive Slip Zone Select (RSZS). This bit determines the minimum distance allowed between the elastic store read and write pointers before forcing a controlled slip. This bit is only applies during T1 to E1 or E1 to T1 conversion applications.
0 = force a slip at 9 bytes or less of separation (used for clustered blank channels)
1 = force a slip at 2 bytes or less of separation (used for distributed blank channels)

Bit 5 / Unused. Must be set = 0 for proper operation.

Bit 6 / Receive Gapped Clock Enable (RGPCKEN)
0 = RCHCLK functions normally
1 = Enable gapped bit clock output on RCHCLK

Bit 7 / Receive Channel Data Format (RDATFMT)
0 = 64kbps (data contained in all 8 bits)
1 = 56kbps (data contained in 7 out of the 8 bits)

RGPCKEN and RDATFMT are not associated with the elastic store and will be explained in the fractional support section.

10.13.1 Mapping E1 Channels Onto a 1.544MHz Backplane

The user can use the RSCLKM bit in RIOCR.4 to enable the receive elastic store to operate with a 1.544MHz backplane (24 channels / frame + F-bit). In this mode, the user can chose which of the E1 time slots will be ignored (not transmitted onto RSER) by programming the Receive Blank Channel Select registers (RBCS1-4). A logic 1 in the associated bit location will cause the DS26401 elastic store to ignore the incoming E1 data for that channel. Typically the user will want to program eight channels to be ignored. The default (power-up) configuration will ignore channels 25 to 32, so that the first 24 E1 channels are mapped into the 24 channels of the 1.544MHz backplane. In this mode the F-bit location at RSER is always set to 1.

For example, if the user wants to ignore E1 time slots 0 (channel 1) and ts 16 (channel 17), the RBCS registers would be programmed as follows:

RBCS1 = 01h
RBCS2 = 00h
RBCS3 = 01h
RBCS4 = FCh

Register Name: **RBCS1, RBCS2, RBCS3, RBCS4**
Register Description: **Receive Blank Channel Select Registers**
Register Address: **0C0h, 0C1h, 0C2h, 0C3h**

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RBCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RBCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RBCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**RBCS4**

Bits 0 to 7 / Receive Blank Channel Select for Channels 1 to 32 (RBCS1 to 32)
0 = do not ignore this channel (send to RSER)
1 = ignore this E1 channel (do not send to RSER)

Note that when two or more sequential channels are chosen to be ignored, the receive slip zone select bit should be set to zero. If the ignore channels are distributed (such as 1, 5, 9, 13, 17, 21, 25, 29), then the RSZS bit can be set to one, which may provide a lower occurrence of slips in certain applications.

10.13.2 Additional E1 Receive Elastic Store Information

If the receive side elastic store is enabled, then the user must provide either a 1.544MHz or 2.048MHz clock at the RSYSCLK pin. For higher rate system clock applications, see the Interleave Bus Option section. The user has the option of either providing a frame/multiframe sync at the RSYNC pin or having the RSYNC pin provide a pulse on frame/multiframe boundaries. If Signaling Reinsertion is enabled, signaling data in TS16 is re-aligned to the multiframe sync input on RSYNC. Otherwise, a multiframe sync input on RSYNC is treated as a simple frame boundary by the elastic store. The framer will always indicate frame boundaries on the network side of the elastic store via the RFSYNC output whether the elastic store is enabled or not. Multiframe boundaries will always be indicated via the RMSYNC output. If the elastic store is enabled, then RMSYNC will output the multiframe boundary on the backplane side of the elastic store. When the device is receiving E1 and the backplane is enabled for 1.544MHz operation, the RMSYNC signal will output the E1 multiframe boundaries as delayed through the elastic store.

10.13.2.1 Elastic Stores Initialization

There are two elastic store initializations that may be used to improve performance in certain applications, Elastic Store Reset and Elastic Store Align. Both of these involve the manipulation of the elastic store's read and write pointers and are useful primarily in synchronous applications (RSYSCLK/TSYSCLK are locked to RCLK/TCLK, respectively). The elastic store reset is used to minimize the delay through the elastic store. The elastic store align bit is used to 'center' the read/write pointers to the extent possible.

Elastic Store Delay After Initialization

INITIALIZATION	REGISTER BIT	DELAY
Receive Elastic Store Reset	RESCR.2	N bytes < Delay < 1 Frame + N bytes
Transmit Elastic Store Reset	TESCR.2	N bytes < Delay < 1 Frame + N bytes
Receive Elastic Store Align	RESCR.3	1/2 Frame < Delay < 1 1/2 Frames
Transmit Elastic Store Align	TESCR.3	1/2 Frame < Delay < 1 1/2 Frames

N = 9 for RSZS = 0

N = 2 for RSZS = 1

10.13.2.2 Minimum Delay Mode

Elastic store minimum delay mode may be used when the elastic store's system clock is locked to its network clock (i.e., RCLK locked to RSYSCLK for the receive side and TCLK locked to TSYSCLK for the transmit side). RESCR.1 enable the receive elastic store minimum delay mode. When enabled the elastic stores will be forced to a maximum depth of 32 bits instead of the normal two-frame depth. This feature is useful primarily in T1 applications that interface to a 2.048MHz bus. Certain restrictions apply when minimum delay mode is used. In addition to the restriction mentioned above, RSYNC must be configured as an output when the receive elastic store is in minimum delay mode and TSYNC must be configured as an output when transmit minimum delay mode is enabled. In a typical application RSYSCLK and TSYSCLK are locked to RCLK, and RSYNC (frame output mode) is connected to TSSYNC (frame input mode). All of the slip contention logic in the framer is disabled (since slips cannot occur). On power-up after the RSYSCLK and TSYSCLK signals have locked to their respective network clock signals, the elastic store reset bit (RESCR.2) should be toggled from a zero to a one to ensure proper operation.

10.14 Fractional E1 Support (Gapped Clock Mode)

The DS26401 can be programmed to output gapped clocks for selected channels in the receive and transmit paths to simplify connections into a USART or LAPD controller in Fractional T1/E1 or ISDN–PRI applications. When the gapped clock feature is enabled, a gated clock is output on the RCHCLK signal. The channel selection is controlled via the receive-gapped-clock channel-select registers (RGCCS1–RGCCS4). The receive path is enabled for gapped clock mode with the RGCLKEN bit (RESCR.6). Both 56kbps and 64kbps channel formats are supported as determined by RESCR.7. When 56kbps mode is selected, the clock corresponding to the Data/Control bit in the channel is omitted (only the seven most significant bits of the channel have clocks).

Register Name: **RGCCS1, RGCCS2, RGCCS3, RGCCS4**
Register Description: **Receive Gapped Clock Channel Select Registers**
Register Address: **0CCh, 0CDh, 0CEh, 0CFh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RGCCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RGCCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RGCCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**RGCCS4**

Bits 0 to 7 / Receive Channels 1 to 32 Gapped Clock Channel Select Bits (CH1 to CH32)

0 = no clock is present on RCHCLK during this channel time
1 = force a clock on RCHCLK during this channel time. The clock will be synchronous with RCLK if the elastic store is disabled, and synchronous with RSYSCLK if the elastic store is enabled.

10.15 Additional Sa-Bit and Si-Bit Receive Operation (E1 Mode)

When operated in the E1 mode the DS21411 receiver provides extended access to both the Sa and the Si bits. The RAF and RNAF registers will always report the data as it received in the Sa and Si bit locations. The RAF and RNAF registers are updated on align frame boundaries. The setting of the Receive Align Frame bit in Latched Status Register 2 (RLS2.0) will indicate that the contents of the RAF and RNAF have been updated. The host can use the RLS2.0 bit to know when to read the RAF and RNAF registers. The host has 250μs to retrieve the data before it is lost.

Also there are eight registers (RsiAF, RSiNAF, RRA, Rsa4 to Rsa8) that report the Si and Sa bits as they are received. These registers are updated with the setting of the Receive CRC4 Multiframe bit in Latched Status Register 2 (RLS2.1). The host can use the RLS2.1 bit to know when to read these registers. The user has 2ms to retrieve the data before it is lost. Please see the register descriptions below for additional information.

Register Name: **RAF**
Register Description: **Receive Align Frame Register**
Register Address: **064h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	Si	0	0	1	1	0	1	1
Default	0	0	0	0	0	0	0	0

Bit 0 / Frame Alignment Signal Bit (1)

Bit 1 / Frame Alignment Signal Bit (1)

Bit 2 / Frame Alignment Signal Bit (0)

Bit 3 / Frame Alignment Signal Bit (1)

Bit 4 / Frame Alignment Signal Bit (1)

Bit 5 / Frame Alignment Signal Bit (0)

Bit 6 / Frame Alignment Signal Bit (0)

Bit 7 / International Bit (Si)

Register Name: **RNAF**
Register Description: **Receive Non-Align Frame Register**
Register Address: **065h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
Default	0	0	0	0	0	0	0	0

Bit 0 / Additional Bit 8 (Sa8)

Bit 1 / Additional Bit 7 (Sa7)

Bit 2 / Additional Bit 6 (Sa6)

Bit 3 / Additional Bit 5 (Sa5)

Bit 4 / Additional Bit 4 (Sa4)

Bit 5 / Remote Alarm (A)

Bit 6 / Frame Non-Alignment Signal Bit (1)

Bit 7 / International Bit (Si)

Register Name: **RsiAF**
Register Description: **Received Si Bits of the Align Frame**
Register Address: **066h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	SiF14	SiF12	SiF10	SiF8	SiF6	SiF4	SiF2	SiF0
Default	0	0	0	0	0	0	0	0

Bit 0 / Si Bit of Frame 0 (SiF0)

Bit 1 / Si Bit of Frame 2 (SiF2)

Bit 2 / Si Bit of Frame 4 (SiF4)

Bit 3 / Si Bit of Frame 6 (SiF6)

Bit 4 / Si Bit of Frame 8 (SiF8)

Bit 5 / Si Bit of Frame 10 (SiF10)

Bit 6 / Si Bit of Frame 12 (SiF12)

Bit 7 / Si Bit of Frame 14 (SiF14)

Register Name: **RSiNAF**
Register Description: **Received Si Bits of the Non-Align Frame**
Register Address: **067h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	SiF15	SiF13	SiF11	SiF9	SiF7	SiF5	SiF3	SiF1
Default	0	0	0	0	0	0	0	0

Bit 0 / Si Bit of Frame 1 (SiF1)

Bit 1 / Si Bit of Frame 3 (SiF3)

Bit 2 / Si Bit of Frame 5 (SiF5)

Bit 3 / Si Bit of Frame 7 (SiF7)

Bit 4 / Si Bit of Frame 9 (SiF9)

Bit 5 / Si Bit of Frame 11 (SiF11)

Bit 6 / Si Bit of Frame 13 (SiF13)

Bit 7 / Si Bit of Frame 15 (SiF15)

Register Name: **RRA**
Register Description: **Received Remote Alarm**
Register Address: **068h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RRAF15	RRAF13	RRAF11	RRAF9	RRAF7	RRAF5	RRAF3	RRAF1
Default	0	0	0	0	0	0	0	0

Bit 0 / Remote Alarm Bit of Frame 1 (RRAF1)

Bit 1 / Remote Alarm Bit of Frame 3 (RRAF3)

Bit 2 / Remote Alarm Bit of Frame 5 (RRAF5)

Bit 3 / Remote Alarm Bit of Frame 7 (RRAF7)

Bit 4 / Remote Alarm Bit of Frame 9 (RRAF9)

Bit 5 / Remote Alarm Bit of Frame 11 (RRAF11)

Bit 6 / Remote Alarm Bit of Frame 13 (RRAF13)

Bit 7 / Remote Alarm Bit of Frame 15 (RRAF15)

Register Name: **RSa4**
Register Description: **Received Sa4 Bits**
Register Address: **069h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RSa4F15	RSa4F13	RSa4F11	RSa4F9	RSa4F7	RSa4F5	RSa4F3	RSa4F1
Default	0	0	0	0	0	0	0	0

Bit 0 / Sa4 Bit of Frame 1 (RSa4F1)

Bit 1 / Sa4 Bit of Frame 3 (RSa4F3)

Bit 2 / Sa4 Bit of Frame 5 (RSa4F5)

Bit 3 / Sa4 Bit of Frame 7 (RSa4F7)

Bit 4 / Sa4 Bit of Frame 9 (RSa4F9)

Bit 5 / Sa4 Bit of Frame 11 (RSa4F11)

Bit 6 / Sa4 Bit of Frame 13 (RSa4F13)

Bit 7 / Sa4 Bit of Frame 15 (RSa4F15)

Register Name: **RSa5**
Register Description: **Received Sa5 Bits**
Register Address: **06Ah + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RSa5F15	RSa5F13	RSa5F11	RSa5F9	RSa5F7	RSa5F5	RSa5F3	RSa5F1
Default	0	0	0	0	0	0	0	0

Bit 0 / Sa5 Bit of Frame 1 (RSa5F1)

Bit 1 / Sa5 Bit of Frame 3 (RSa5F3)

Bit 2 / Sa5 Bit of Frame 5 (RSa5F5)

Bit 3 / Sa5 Bit of Frame 7 (RSa5F7)

Bit 4 / Sa5 Bit of Frame 9 (RSa5F9)

Bit 5 / Sa5 Bit of Frame 11 (RSa5F11)

Bit 6 / Sa5 Bit of Frame 13 (RSa5F13)

Bit 7 / Sa5 Bit of Frame 15 (RSa5F15)

Register Name: **RSa6**
Register Description: **Received Sa6 Bits**
Register Address: **06Bh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RSa6F15	RSa6F13	RSa6F11	RSa6F9	RSa6F7	RSa6F5	RSa6F3	RSa6F1
Default	0	0	0	0	0	0	0	0

Bit 0 / Sa6 Bit of Frame 1 (RSa6F1)

Bit 1 / Sa6 Bit of Frame 3 (RSa6F3)

Bit 2 / Sa6 Bit of Frame 5 (RSa6F5)

Bit 3 / Sa6 Bit of Frame 7 (RSa6F7)

Bit 4 / Sa6 Bit of Frame 9 (RSa6F9)

Bit 5 / Sa6 Bit of Frame 11 (RSa6F11)

Bit 6 / Sa6 Bit of Frame 13 (RSa6F13)

Bit 7 / Sa6 Bit of Frame 15 (RSa6F15)

Register Name: **RSa7**
Register Description: **Received Sa7 Bits**
Register Address: **06Ch + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RSa7F15	RSa7F13	RSa7F11	RSa7F9	RSa7F7	RSa7F5	RSa7F3	RSa7F1
Default	0	0	0	0	0	0	0	0

Bit 0 / Sa7 Bit of Frame 1 (RSa7F1)

Bit 1 / Sa7 Bit of Frame 3 (RSa7F3)

Bit 2 / Sa7 Bit of Frame 5 (RSa7F5)

Bit 3 / Sa7 Bit of Frame 7 (RSa7F7)

Bit 4 / Sa7 Bit of Frame 9 (RSa7F9)

Bit 5 / Sa7 Bit of Frame 11 (RSa7F11)

Bit 6 / Sa7 Bit of Frame 13 (RSa7F13)

Bit 7 / Sa7 Bit of Frame 15 (RSa4F15)

Register Name: **RSa8**
Register Description: **Received Sa8 Bits**
Register Address: **06Dh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RSa8F15	RSa8F13	RSa8F11	RSa8F9	RSa8F7	RSa8F5	RSa8F3	RSa8F1
Default	0	0	0	0	0	0	0	0

Bit 0 / Sa8 Bit of Frame 1 (RSa8F1)

Bit 1 / Sa8 Bit of Frame 3 (RSa8F3)

Bit 2 / Sa8 Bit of Frame 5 (RSa8F5)

Bit 3 / Sa8 Bit of Frame 7 (RSa8F7)

Bit 4 / Sa8 Bit of Frame 9 (RSa8F9)

Bit 5 / Sa8 Bit of Frame 11 (RSa8F11)

Bit 6 / Sa8 Bit of Frame 13 (RSa8F13)

Bit 7 / Sa8 Bit of Frame 15 (RSa8F15)

10.16 Receive HDLC Controller

Each framer port has an HDLC controller with 64-byte FIFOs. The HDLC controllers automatically generate and detect flags, generate and check the CRC checksum, generate and detect abort sequences, stuff and destuff zeros, and byte align to the data stream.

Register Name: **RHC**
Register Description: **Receive HDLC Control Register**
Register Address: **010h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RCRCD	RHR	RHMS	RHCS4	RHCS3	RHCS2	RHCS1	RHCS0
Default	0	0	0	0	0	0	0	0

Bit 0 to Bit 4 / Receive HDLC Channel Select (RHCSx). These bits determine which DS0 is mapped to the HDLC controller when enabled with RHMS = 0. RHCS0 to RHCS4 = all 0s selects channel 1, RHCS0 to RHCS4 = all 1s selects channel 32 (E1).

Bit 5 / Receive HDLC Mapping Select (RHMS)
0 = Receive HDLC assigned to channels
1 = Receive HDLC assigned to FDL (T1 mode), Sa Bits (E1 mode)

Bit 6 / Receive HDLC Reset (RHR). Will reset the receive HDLC controller and flush the receive FIFO. Must be cleared and set again for a subsequent reset.
0 = Normal operation
1 = Reset receive HDLC controller and flush the receive FIFO

Bit 7 / Receive CRC16 Display (RCRCD)
0 = Do not write received CRC16 code to FIFO
1= Write received CRC16 code to FIFO after last octet of packet

Register Name: **RHBSE**
Register Description: **Receive HDLC Bit Suppress Register**
Register Address: **011h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	BSE8	BSE7	BSE6	BSE5	BSE4	BSE3	BSE2	BSE1
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Channel Bit 1 Suppress/Sa8 Bit Suppress (BSE1). LSB of the channel. Set to one to stop this bit from being used.

Bit 1 / Receive Channel Bit 2 Suppress/Sa7 Bit Suppress (BSE2). Set to one to stop this bit from being used

Bit 2 / Receive Channel Bit 3 Suppress/Sa6 Bit Suppress (BSE3). Set to one to stop this bit from being used

Bit 3 / Receive Channel Bit 4 Suppress/Sa5 Bit Suppress (BSE4). Set to one to stop this bit from being used

Bit 4 / Receive Channel Bit 5 Suppress/Sa4 Bit Suppress (BSE5). Set to one to stop this bit from being used

Bit 5 / Receive Channel Bit 6 Suppress (BSE6). Set to one to stop this bit from being used.

Bit 6 / Receive Channel Bit 7 Suppress (BSE7). Set to one to stop this bit from being used.

Bit 7 / Receive Channel Bit 8 Suppress (BSE8). MSB of the channel. Set to one to stop this bit from being used.

10.16.1 HDLC FIFO Control

Control of the receive FIFO is accomplished via the Receive HDLC FIFO Control (RHFC). The FIFO Control register sets the watermarks for the receive FIFO.

When the receive FIFO fills above the high watermark, the RHWM bit (RRTS5.1) will be set. RHWM is a real-time bit and will remain set as long as the receive FIFO's write pointer is above the watermark. If enabled, this condition can also cause an interrupt via the $\overline{INT}$ pin.

Register Name: **RHFC**
Register Description: **Receive HDLC FIFO Control Register**
Register Address: **087h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	RFHWM1	RFHWM0
Default	0	0	0	0	0	0	0	0

Bits 0 to 1 / Receive FIFO High Watermark Select (RFHWM0 to RFHWM1)

RFHWM1	RFHWM0	Receive FIFO Watermark (bytes)
0	0	4
0	1	16
1	0	32
1	1	48

Bits 2 to 7/ Unused. Must be set = 0 for proper operation.

10.16.2 Receive Packet Bytes Available

The lower 6 bits of the Receive Packet Bytes Available register indicates the number of bytes (0 through 64) that can be read from the receive FIFO. The value indicated by this register informs the host as to how many bytes can be read from the receive FIFO without going past the end of a message. This value will refer to one of four possibilities, the first part of a packet, the continuation of a packet, the last part of a packet, or a complete packet. After reading the number of bytes indicated by this register the host then checks the HDLC Status register for detailed message status.

If the value in the RHPBA register refers to the beginning portion of a message or continuation of a message then the MSB of the RHPBA register will return a value of 1. This indicates that the host may safely read the number of bytes returned by the lower 6 bits of the RHPBA register but there is no need to check the information register since the packet has not yet terminated (successfully or otherwise).

Register Name: **RHPBA**
Register Description: **Receive HDLC Packet Bytes Available Register**
Register Address: **0B5h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	MS	RPBA6	RPBA5	RPBA4	RPBA3	RPBA2	RPBA1	RPBA0
Default	0	0	0	0	0	0	0	0

Bits 0 to 6 / Receive FIFO Packet Bytes Available Count (RPBA0 to RPBA6). RPBA0 is the LSB.

Bit 7 / Message Status (MS)

0 = Bytes indicated by RPBA0 through RPBA6 are the end of a message. Host must check the HDLC Status register for details.
1 = Bytes indicated by RPBA0 through RPBA6 are the beginning or continuation of a message. The host does not need to check the HDLC Status.

Register Name: **RHF**
Register Description: **Receive HDLC FIFO Register**
Register Address: **0B6h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	RHD7	RHD6	RHD5	RHD4	RHD3	RHD2	RHD1	RHD0
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive HDLC Data Bit 0 (RHD0). LSB of a HDLC packet data byte.

Bit 1 / Receive HDLC Data Bit 1 (RHD1)

Bit 2 / Receive HDLC Data Bit 2 (RHD2)

Bit 3 / Receive HDLC Data Bit 3 (RHD3)

Bit 4 / Receive HDLC Data Bit 4 (RHD4)

Bit 5 / Receive HDLC Data Bit 5 (RHD5)

Bit 6 / Receive HDLC Data Bit 6 (RHD6)

Bit 7 / Receive HDLC Data Bit 7 (RHD7). MSB of a HDLC packet data byte.

10.16.3 HDLC Status and Information

RRTS5 and RLS5 provide status information for the receive HDLC controller. When a particular event has occurred (or is occurring), the appropriate bit in one of these registers will be set to a one. With the latched bits, when an event occurs and a bit is set to a one, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again. The real-time bits report the current instantaneous conditions that are occurring and the history of these bits is not latched.

Like the other latched status registers, the user will follow a read of the status bit with a write. The byte written to the register will inform the device which of the latched bits the user wishes to clear (the real time bits are not affected by writing to the status register). The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to clear and a zero in the bit positions he or she does not wish to clear.

The HDLC status register RLS5 has the ability to initiate a hardware interrupt via the $\overline{INT}$ output signal. Each of the events in this register can be either masked or unmasked from the interrupt pin via the receive HDLC Interrupt Mask Register (RIM5). Interrupts will force the $\overline{INT}$ signal low when the event occurs. The $\overline{INT}$ pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

Register Name: **RRTS5**
Register Description: **Receive Real-Time Status 5 (HDLC)**
Register Address: **0B4h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	PS2	PS1	PS0	—-	—	RHWM	RNE
Default	0	0	0	0	0	0	0	0

All bits in this register are real-time.

Bit 0 / Receive FIFO Not Empty Condition (RNE). Set when the receive 64-byte FIFO has at least one byte available for a read. This is a real-time bit.

Bit 1 / Receive FIFO Above High Watermark Condition (RHWM). Set when the receive 64-byte FIFO fills beyond the high watermark as defined by the Receive HDLC FIFO Control Register (RHFC). This is a real-time bit.

Bits 2, 3, 7 / Unused

Bits 4 to 6 / Receive Packet Status (PS0 to PS2). These are real-time bits indicating the status as of the last read of the receive FIFO.

PS2	PS1	PS0	PACKET STATUS
0	0	0	**In Progress:** End of message has not yet been reached.
0	0	1	**Packet OK:** Packet ended with correct CRC codeword.
0	1	0	**CRC Error:** A closing flag was detected, preceded by a corrupt CRC codeword.
0	1	1	**Abort:** Packet ended because an abort signal was detected (7 or more ones in a row).
1	0	0	**Overrun:** HDLC controller terminated reception of packet because receive FIFO is full.

Register Name: **RLS5**
Register Description: **Receive Latched Status Register 5 (HDLC)**
Register Address: **094h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	ROVR	RHOBT	RPE	RPS	RHWMS	RNES
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive FIFO Not Empty Set Event (RNES). Set when the receive FIFO has transitioned from ‘empty’ to ‘not-empty’ (at least one byte has been put into the FIFO). Rising edge detect of RNE.

Bit 1 / Receive FIFO Above High Watermark Set Event (RHWMS). Set when the receive 64-byte FIFO crosses the high watermark as defined by the Receive HDLC FIFO Control Register (RHFC). Rising edge detect of RHWM.

Bit 2 / Receive Packet Start Event (RPS). Set when the HDLC controller detects an opening byte. This is a latched bit and will be cleared when read.

Bit 3 / Receive Packet End Event (RPE). Set when the HDLC controller detects either the finish of a valid message (i.e., CRC check complete) or when the controller has experienced a message fault such as a CRC checking error, or an overrun condition, or an abort has been seen. This is a latched bit and will be cleared when read.

Bit 4 / Receive HDLC Opening Byte Event (RHOBT). Set when the next byte available in the receive FIFO is the first byte of a message.

Bit 5 / Receive FIFO Overrun (ROVR). Set when the receive HDLC controller has terminated packet reception because the FIFO buffer is full.

Bits 6, 7 / Unused

Register Name: **RIM5**
Register Description: **Receive Interrupt Mask 5 (HDLC)**
Register Address: **0A4h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	ROVR	RHOBT	RPE	RPS	RHWMS	RNES
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive FIFO Not Empty Set Event (RNES).
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Receive FIFO Above High Watermark Set Event (RHWMS)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Receive Packet Start Event (RPS)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Receive Packet End Event (RPE)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Receive HDLC Opening Byte Event (RHOBT)
0 = interrupt masked
1 = interrupt enabled

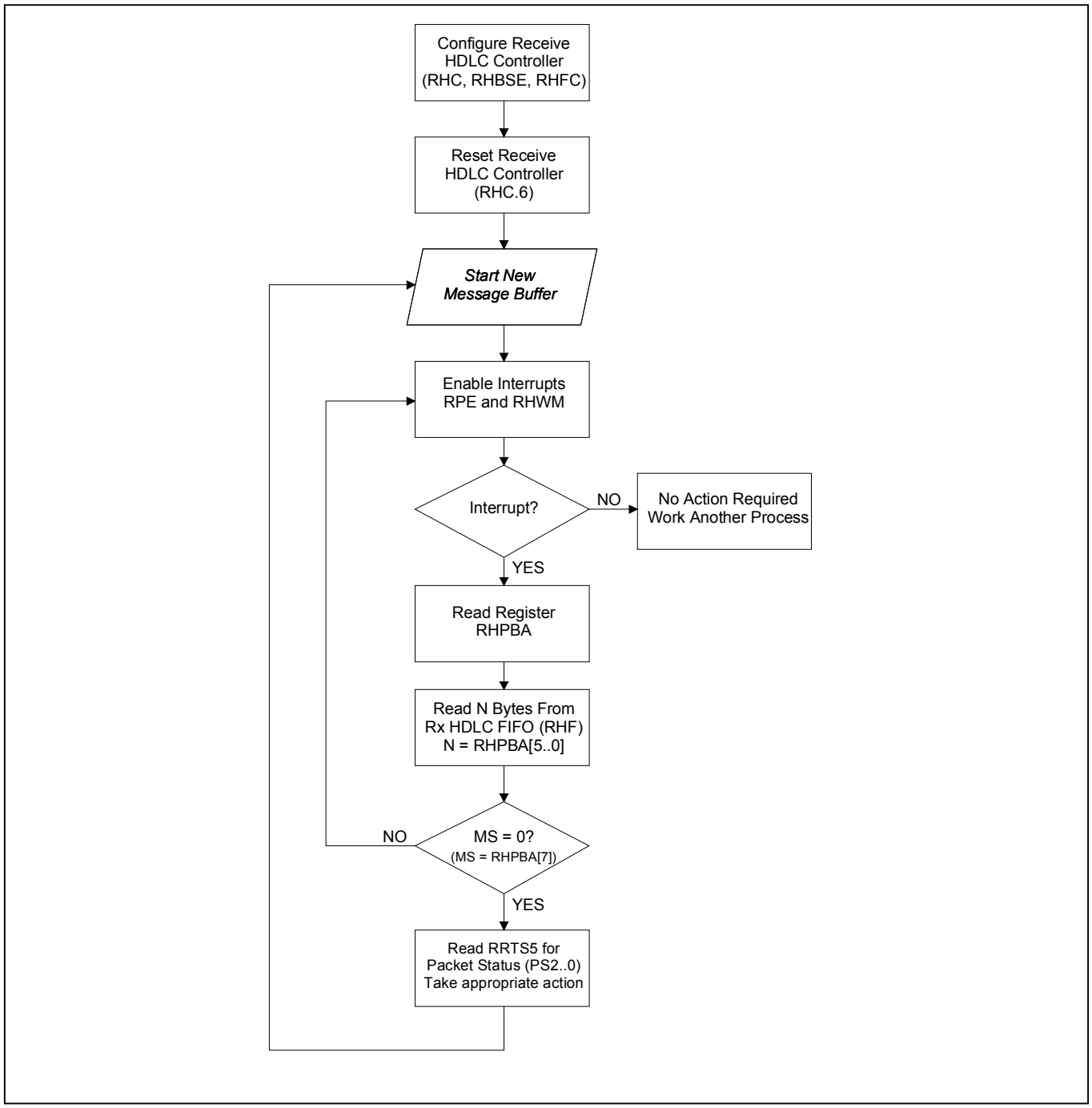
Bit 5 / Receive FIFO Overrun (ROVR)
0 = interrupt masked
1 = interrupt enabled

Bits 6, 7 / Unused. Must be set = 0 for proper operation.

HDLC Receive Example

The HDLC status registers in the DS26401 allow for flexible software interface to meet the user's preferences. When receiving HDLC messages, the host can chose to be interrupt driven, or to poll to desired status registers, or a combination of polling and interrupt processes may be used. An example routine for using the DS26401 HDLC receiver is given in Figure 10-3.

Figure 10-3. Receive HDLC Example



10.17 Interleaved PCM Bus Operation (IBO)

In many architectures, the PCM outputs of individual framers are combined into higher speed PCM buses to simplify transport across the system backplane. The DS26401 can be configured to allow PCM data to be multiplexed into higher speed buses eliminating external hardware, saving board space and cost. The DS26401 can be configured for channel or frame interleave.

The interleaved PCM bus option (IBO) supports three bus speeds. The 4.096MHz bus speed allows two PCM data streams to share a common bus. The 8.192MHz bus speed allows four PCM data streams to share a common bus. The 16.384MHz bus speed allows 8 PCM data streams to share a common bus. The receive elastic stores of each transceiver must be enabled. Via the IBO register the user can configure each framer for a specific bus position. For all IBO bus configurations each framer is assigned an exclusive position in the high speed PCM bus. The 8kHz frame sync can be generated from the system backplane or from the first device on the bus. All other devices on the bus must have their frame syncs configured as inputs. Relative to this common frame sync, the devices will await their turn to drive or sample the bus according to the settings of the DA0, DA1 and DA2 bits of the RIBOC register.

10.17.1 Channel Interleave

In channel interleave mode data is output to the PCM Data Out bus one channel at a time from each of the connected DS26401s until all channels of frame n from each framer has been placed on the bus. This mode can be used even when the DS26401s are operating asynchronous to each other. The elastic stores will manage slip conditions. The DS26401 provides an active high signal (RIBO_OE) during bus active times. RIBO_OE can be used for bus multiplexer or tri-state buffer control.

10.17.2 Frame Interleave

In frame interleave mode data is output to the PCM Data Out bus one frame at a time from each of the framers. This mode is used only when all connected DS26401s are operating in a synchronous fashion (all inbound T1 or E1 lines are synchronous) and are synchronous with the system clock (system clock derived from T1 or E1 line). In this mode, slip conditions are not allowed.

Register Name: **RIBOC**
Register Description: **Receive Interleave Bus Operation Control Register**
Register Address: **084h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	IBS1	IBS0	IBOSEL	IBOEN	DA2	DA1	DA0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2 / Device Assignment Bits (DA0 to DA2)

DA2	DA1	DA0	Device Position
0	0	0	1st Device on bus
0	0	1	2nd Device on bus
0	1	0	3rd Device on bus
0	1	1	4th Device on bus
1	0	0	5th Device on bus
1	0	1	6th Device on bus
1	1	0	7th Device on bus
1	1	1	8th Device on bus

Bit 3 / Interleave Bus Operation Enable (IBOEN)
0 = Interleave Bus Operation disabled.
1 = Interleave Bus Operation enabled.

Bit 4 / Interleave Bus Operation Select (IBOSEL). This bit selects channel or frame interleave mode.
0 = Channel Interleave
1 = Frame Interleave

Bits 5, 6 / IBO Bus Size bit 1 (IBS0 to IBS1). Indicates how many devices on the bus.

IBS1	IBS0	Bus Size
0	0	2 Devices on bus (4.096MHz)
0	1	4 Devices on bus (8.192MHz)
1	0	8 Devices on bus (16.384MHz)
1	1	Reserved for future use

Bit 7 / Unused. Must be set = 0 for proper operation.

10.18 Interfacing the E1 Rx Framer to the BERT

Data from the DS26401 receive framer can be ported to the on-chip BERT by using the registers described below. Any single DS0 or combination of DS0s can be extracted from the data stream up to the entire T1 payload as controlled by the RBCS registers.

Note that one BERT resource is shared between all 8 framers. Therefore, the RBEN bit should be set for only one framer at a time. If multiple framers have the RBEN bit set, the lower number framer will be assigned the resource. Details concerning the on-chip BERT can be found in Section 12.

Register Name: **RBICR**
Register Description: **Receive BERT Interface Control Register**
Register Address: **08Ah + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	RBDC	—	RBEN
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive BERT Enable (RBEN)
0 = Receive BERT is not assigned to this framer
1 = Receive BERT is assigned to this framer

Bit 1 / Unused. Must be set = 0 for proper operation.

Bit 2 / Receive BERT Direction Control (RBDC)
0 = Receive Path: The BERT receives data from the network side via RPOS and RNEG.
1 = Backplane: The BERT receives data from the system backplane via the TSER pin.

Bits 2 to 7 / Unused. Must be set = 0 for proper operation.

Register Name: **RBCS1, RBCS2, RBCS3, RBCS4**
Register Description: **Receive BERT Channel Select Registers**
Register Address: **0D4h, 0D5h, 0D6h, 0D7h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Setting any of the CH1 through CH32 bits in the RBCS1 through RBCS4 registers will map data from those channels to the on-board BERT. RBEN must be set to one for these registers to have effect. Multiple, or all channels may be selected simultaneously. These registers work with the receive-side framer only.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**RBCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**RBCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**RBCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**RBCS4**

Register Name: **RBBS**
Register Description: **Receive BERT Bit Suppress Register**
Register Address: **08Bh**

Bit #	7	6	5	4	3	2	1	0
Name	BSE8	BSE7	BSE6	BSE5	BSE4	BSE3	BSE2	BSE1
Default	0	0	0	0	0	0	0	0

Bit 0 / Receive Channel Bit 1 Suppress (BSE1). LSB of the channel. Set to one to stop this bit from being used.

Bit 1 / Receive Channel Bit 2 Suppress (BSE2). Set to one to stop this bit from being used.

Bit 2 / Receive Channel Bit 3 Suppress (BSE3). Set to one to stop this bit from being used.

Bit 3 / Receive Channel Bit 4 Suppress (BSE4). Set to one to stop this bit from being used.

Bit 4 / Receive Channel Bit 5 Suppress (BSE5). Set to one to stop this bit from being used.

Bit 5 / Receive Channel Bit 6 Suppress (BSE6). Set to one to stop this bit from being used.

Bit 6 / Receive Channel Bit 7 Suppress (BSE7). Set to one to stop this bit from being used.

Bit 7 / Receive Channel Bit 8 Suppress (BSE8). MSB of the channel. Set to one to stop this bit from being used.

11. E1 TRANSMIT

11.1 E1 Transmit Register Map

ADDRESS	TYPE	FUNCTION	NAME	PAGE
100	—	Unused	—	—
101	—	Unused	—	—
102	—	Unused	—	—
103	—	Unused	—	—
104	—	Unused	—	—
105	—	Unused	—	—
106	—	Unused	—	—
107	—	Unused	—	—
108	—	Unused	—	—
109	—	Unused	—	—
10A	—	Unused	—	—
10B	—	Unused	—	—
10C	—	Unused	—	—
10D	—	Unused	—	—
10E	—	Unused	—	—
10F	—	Unused	—	—
110	R/W	Tx HDLC Control 1	THC1	248
111	R/W	Tx HDLC Bit Suppress	THBSE	249
112	—	Unused	—	—
113	R/W	Tx HDLC Control 2	THC2	249
114	R/W	Tx Sa Bit Control Register	TSACR	246
115	—	Unused	—	—
116	—	Unused	—	—
117	—	Unused	—	—
118	R/W	Tx Software Signaling Insertion Enable 1	SSIE1	121
119	R/W	Tx Software Signaling Insertion Enable 2	SSIE2	121
11A	R/W	Tx Software Signaling Insertion Enable 3	SSIE3	121
11B	R/W	Tx Software Signaling Insertion Enable 4	SSIE4	121
11C	R/W	Tx Test Register 1	TTEST1	—
11D	R/W	Tx Test Register 2	TTEST2	—
11E	R/W	Tx Test Register 3	TTEST3	—
11F	R/W	Tx Test Register 4	TTEST4	—
120	R/W	Tx Idle Definition 1	TIDR1	233
121	R/W	Tx Idle Definition 2	TIDR2	233
122	R/W	Tx Idle Definition 3	TIDR3	233
123	R/W	Tx Idle Definition 4	TIDR4	233
124	R/W	Tx Idle Definition 5	TIDR5	233
125	R/W	Tx Idle Definition 6	TIDR6	233
126	R/W	Tx Idle Definition 7	TIDR7	233
127	R/W	Tx Idle Definition 8	TIDR8	233
128	R/W	Tx Idle Definition 9	TIDR9	233
129	R/W	Tx Idle Definition 10	TIDR10	233
12A	R/W	Tx Idle Definition 11	TIDR11	233
12B	R/W	Tx Idle Definition 12	TIDR12	233
12C	R/W	Tx Idle Definition 13	TIDR13	233
12D	R/W	Tx Idle Definition 14	TIDR14	233
12E	R/W	Tx Idle Definition 15	TIDR15	233
12F	R/W	Tx Idle Definition 16	TIDR16	233
130	R/W	Tx Idle Definition 17	TIDR17	233
131	R/W	Tx Idle Definition 18	TIDR18	233
132	R/W	Tx Idle Definition 19	TIDR19	233
133	R/W	Tx Idle Definition 20	TIDR20	233
134	R/W	Tx Idle Definition 21	TIDR21	233
135	R/W	Tx Idle Definition 22	TIDR22	233
136	R/W	Tx Idle Definition 23	TIDR23	233
137	R/W	Tx Idle Definition 24	TIDR24	233

ADDRESS	TYPE	FUNCTION	NAME	PAGE
138	R/W	Tx Idle Definition 25	TIDR25	233
139	R/W	Tx Idle Definition 26	TIDR26	233
13A	R/W	Tx Idle Definition 27	TIDR27	233
13B	R/W	Tx Idle Definition 28	TIDR28	233
13C	R/W	Tx Idle Definition 29	TIDR29	233
13D	R/W	Tx Idle Definition 30	TIDR30	233
13E	R/W	Tx Idle Definition 31	TIDR31	233
13F	R/W	Tx Idle Definition 32	TIDR32	233
140	R/W	Tx Signaling 1	TS1	231
141	R/W	Tx Signaling 2	TS2	231
142	R/W	Tx Signaling 3	TS3	231
143	R/W	Tx Signaling 4	TS4	231
144	R/W	Tx Signaling 5	TS5	231
145	R/W	Tx Signaling 6	TS6	231
146	R/W	Tx Signaling 7	TS7	231
147	R/W	Tx Signaling 8	TS8	231
148	R/W	Tx Signaling 9	TS9	231
149	R/W	Tx Signaling 10	TS10	231
14A	R/W	Tx Signaling 11	TS11	231
14B	R/W	Tx Signaling 12	TS12	231
14C	R/W	Tx Signaling 13	TS13	231
14D	R/W	Tx Signaling 14	TS14	231
14E	R/W	Tx Signaling 15	TS15	231
14F	R/W	Tx Signaling 16	TS16	231
150	R/W	Tx Channel Idle Code Enable 1	TCICE1	233
151	R/W	Tx Channel Idle Code Enable 2	TCICE2	233
152	R/W	Tx Channel Idle Code Enable 3	TCICE3	233
153	R/W	Tx Channel Idle Code Enable 4	TCICE4	233
154	—	Unused	—	—
155	—	Unused	—	—
156	—	Unused	—	—
157	—	Unused	—	—
158	—	Unused	—	—
159	—	Unused	—	—
15A	—	Unused	—	—
15B	—	Unused	—	—
15C	—	Unused	—	—
15D	—	Unused	—	—
15E	—	Unused	—	—
15F	—	Unused	—	—
160	—	Unused	—	—
161	—	Unused	—	—
162	—	Unused	—	—
163	—	Unused	—	—
164	R/W	Tx Align Frame	TAF	241
165	R/W	Tx Non-Align Frame	TNAF	241
166	R/W	Tx Si bits for Align Frame	TSiAF	242
167	R/W	Tx Si bits for Non-Align Frame	TSiNAF	242
168	R/W	Tx Remote Alarm	TRA	243
169	R/W	Tx Sa4 Bits	TSa4	243
16A	R/W	Tx Sa5 Bits	TSa5	244
16B	R/W	Tx Sa6 Bits	TSa6	244
16C	R/W	Tx Sa7 Bits	TSa7	245
16D	R/W	Tx Sa8 Bits	TSa8	245
16E	—	Unused	—	—
16F	—	Unused	—	—
170	—	Unused	—	—
171	—	Unused	—	—
172	—	Unused	—	—
173	—	Unused	—	—
174	—	Unused	—	—

ADDRESS	TYPE	FUNCTION	NAME	PAGE
175	—	Unused	—	—
176	—	Unused	—	—
177	—	Unused	—	—
178	—	Unused	—	—
179	—	Unused	—	—
17A	—	Unused	—	—
17B	—	Unused	—	—
17C	—	Unused	—	—
17D	—	Unused	—	—
17E	—	Unused	—	—
17F	—	Unused	—	—
180	R/W	Tx Master Mode	TMMR	217
181	R/W	Tx Control 1	TCR1	219
182	R/W	Tx Control 2	TCR2	220
183	R/W	Tx Control 3	TCR3	222
184	R/W	Tx I/O Configuration	TIOCR	114
185	R/W	Tx Elastic Store Control	TESCR	237
186	—	Unused	—	—
187	R/W	Tx HDLC FIFO Control	THFC	250
188	R/W	Tx Interleave Bus Op Control	TIBOC	257
189	R/W	Tx DS0 Monitor Select	TDS0SEL	229
18A	R/W	Tx BERT Interface Control	TBICR	258
18B	R/W	Tx BERT Bit Suppress En	TBBS	259
18C	—	Unused	—	—
18D	—	Unused	—	—
18E	R/W	Tx Synchronizer Control	TSYNCC	260
18F	R/W	Tx Test Register 5	TTEST5	—
190	R/W	Tx Latched Status 1	TLS1	226
191	R/W	Tx Latched Status 2 (HDLC)	TLS2	252
192	R/W	Tx Latched Status 3 (SYNC)	TLS3	261
193	—	Unused	—	—
194	—	Unused	—	—
195	—	Unused	—	—
196	—	Unused	—	—
197	—	Unused	—	—
198	—	Unused	—	—
199	—	Unused	—	—
19A	—	Unused	—	—
19B	—	Unused	—	—
19C	—	Unused	—	—
19D	—	Unused	—	—
19E	—	Unused	—	—
19F	R/W	Tx Interrupt Information Register	TIIR	218
1A0	R/W	Tx Interrupt Mask Register 1	TIM1	227
1A1	R/W	Tx Interrupt Mask Register 2 (HDLC)	TIM2	253
1A2	R/W	Tx Interrupt Mask Register 3 (SYNC)	TIM3	261
1A3	—	Unused	—	—
1A4	—	Unused	—	—
1A5	—	Unused	—	—
1A6	—	Unused	—	—
1A7	—	Unused	—	—
1A8	—	Unused	—	—
1A9	—	Unused	—	—
1AA	—	Unused	—	—
1AB	—	Unused	—	—
1AC	—	Unused	—	—
1AD	—	Unused	—	—
1AE	—	Unused	—	—
1AF	—	Unused	—	—
1B0	—	Unused	—	—
1B1	R	Tx Real-Time Status Register 2 (HDLC)	TRTS2	251

ADDRESS	TYPE	FUNCTION	NAME	PAGE
1B2	—	Unused	—	—
1B3	R	Tx HDLC FIFO Buffer Available	TFBA	254
1B4	W	Tx HDLC FIFO	THF	254
1B5	—	Unused	—	—
1B6	—	Unused	—	—
1B7	—	Unused	—	—
1B8	—	Unused	—	—
1B9	—	Unused	—	—
1BA	—	Unused	—	—
1BB	R	Tx DS0 Monitor	TDS0M	229
1BC	—	Unused	—	—
1BD	—	Unused	—	—
1BE	—	Unused	—	—
1BF	—	Unused	—	—
1C0	R/W	Tx Blank Channel Select 1	TBCS1	259
1C1	R/W	Tx Blank Channel Select 2	TBCS2	259
1C2	R/W	Tx Blank Channel Select 3	TBCS3	259
1C3	R/W	Tx Blank Channel Select 4	TBCS4	259
1C4	R/W	Tx Channel Blocking 1	TCBR1	234
1C5	R/W	Tx Channel Blocking 2	TCBR2	234
1C6	R/W	Tx Channel Blocking 3	TCBR3	234
1C7	R/W	Tx Channel Blocking 4	TCBR4	234
1C8	R/W	Tx Hardware Signaling Channel Select 1	THSCS1	232
1C9	R/W	Tx Hardware Signaling Channel Select 2	THSCS2	232
1CA	R/W	Tx Hardware Signaling Channel Select 3	THSCS3	232
1CB	R/W	Tx Hardware Signaling Channel Select 4	THSCS4	232
1CC	R/W	Tx Gapped Clock Channel Select 1	TGCCS1	239
1CD	R/W	Tx Gapped Clock Channel Select 2	TGCCS2	239
1CE	R/W	Tx Gapped Clock Channel Select 3	TGCCS3	239
1CF	R/W	Tx Gapped Clock Channel Select 4	TGCCS4	239
1D0	R/W	Per-Channel Loopback Enable 1	PCL1	118
1D1	R/W	Per-Channel Loopback Enable 2	PCL2	118
1D2	R/W	Per-Channel Loopback Enable 3	PCL3	118
1D3	R/W	Per-Channel Loopback Enable 4	PCL4	—
1D4	R/W	Tx BERT Channel Select 1	TBCS1	259
1D5	R/W	Tx BERT Channel Select 2	TBCS2	259
1D6	R/W	Tx BERT Channel Select 3	TBCS3	259
1D7	R/W	Tx BERT Channel Select 4	TBCS4	259
1D8	—	Unused	—	—
1D9	—	Unused	—	—
1DA	—	Unused	—	—
1DB	—	Unused	—	—
1DC	—	Unused	—	—
1DD	—	Unused	—	—
1DE	—	Unused	—	—
1DF	—	Unused	—	—
1E0–1FF	—	Unused	—	—

Note: The register addresses are 9 bits wide, but are shown here in hexadecimal. Addresses with the MSB clear (0xxH) are used for the DS26401 receiver; addresses with the MSB set (1xxH) are used for the DS26401 transmitter.

11.2 E1 Transmit Formatter Description and Operation

Eight fully independent DS1/E1 transmit formatters are included within the DS26401. The formatters are designed to interface seamlessly to the line side via an external LIU. Each port can be individually programmed to transmit AMI, HDB3 (E1), or NRZ data. In E1 mode, each formatter supports FAS, CRC-4, and CAS frame formats, transmits common alarms such as AIS and RAI.

Each transmitter has an HDLC controllers which can be mapped into a single time slot, or Sa4 to Sa8 bits (E1 mode) or the FDL (T1 mode) and has 64-byte FIFO buffers in both the transmit and receive paths.

Host interface is simplified with status registers optimized for either interrupt driven or polled environments. In many cases, status bits are reported both real-time and latched on change-of-state with separate bits for each state change. Most latched bits can be mapped to generate an external interrupt on the $\overline{INT}$ pin.

Additional details concerning the operation of the E1 formatter are included within the register descriptions within this section.

11.3 Transmit Master Mode Register

The Transmit Master Mode Register (TMMR) controls the initialization of the transmit side formatter. The FRM_EN bit may be left 'low' if the formatter for that particular port is not going to be used, putting the circuit in a low-power (sleep) state.

Register Name: **TMMR**
Register Description: **Transmit Master Mode Register**
Register Address: **180h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	FRM_EN	INIT_DONE	—	—	—	—	SFTRST	T1/E1
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmitter T1/E1 Mode Select (T1/E1). Sets operating mode for transmitter only! This bit must be written with the desired value prior to setting INIT_DONE.
0 = T1 operation
1 = E1 operation

Bit 1 / Soft Reset (SFTRST). Level sensitive processor reset. Should be taken high then low to reset and initialize the internal processor.
0 = Normal Operation
1 = Hold the internal RISC in reset. This bit only affects the transmit side processor.

Bits 2 to 5 / Unused. Must be set = 0 for proper operation.

Bit 6 / Initialization Done (INIT_DONE). The host (user) must set this bit once he/she has written the configuration registers. The host is required to write or clear all RAM based registers (addresses 100H to 17FH) prior to setting this bit. Once INIT_DONE is set, the internal processor will check the FRM_EN bit. If enabled, the internal processor continues executing based on the initial configuration.

Bit 7 / Framer Enable (FRM_EN). This bit must be written with the desired value prior to setting INIT_DONE.
0 = Framer disabled – held in low power state
1 = Framer enabled – all features active

11.4 Interrupt Information Registers

The Interrupt Information Registers provide an indication of which DS26401 Status Registers are generating an interrupt. When an interrupt occurs, the host can read TIIR to quickly identify which of the transmit status registers are causing the interrupt(s). These are real-time registers in that the bits will clear once the appropriate interrupt has been serviced and cleared.

Register Name: **TIIR**
Register Description: **Transmit Interrupt Information Register**
Register Address: **19Fh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	TLS3	TLS2	TLS1
Default	0	0	0	0	0	0	0	0

11.5 E1 Transmit Control Registers

Register Name: **TCR1**
Register Description: **Transmit Control Register 1**
Register Address: **181h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TFPT	T16S	TG802	TSiS	TSA1	THDB3	TAIS	TCRC4
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit CRC4 Enable (TCRC4)
0 = CRC4 disabled
1 = CRC4 enabled

Bit 1 / Transmit AIS (TAIS)
0 = transmit data normally
1 = transmit an unframed all-ones code at TPOS and TNEG

Bit 2 / Transmit HDB3 Enable (THDB3)
0 = HDB3 disabled
1 = HDB3 enabled

Bit 3 / Transmit Signaling All Ones (TSA1)
0 = normal operation
1 = force time slot 16 in every frame to all ones

Bit 4 / Transmit International Bit Select (TSiS)
0 = sample Si bits at TSER pin
1 = source Si bits from TAF and TNAF registers (in this mode, TCR1.7 must be set to 0)

Bit 5 / Transmit G.802 Enable (TG802)
0 = do not force TCHBLK high during bit 1 of time slot 26
1 = force TCHBLK high during bit 1 of time slot 26

Bit 6 / Transmit Time Slot 16 Data Select (T16S)
0 = time slot 16 determined by the SSIEx and THSCS registers
1 = source time slot 16 from TS1 to TS16 registers

Bit 7 / Transmit Time Slot 0 Pass Through (TFPT)
0 = FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers
1 = FAS bits/Sa bits/Remote Alarm sourced from TSER

Register Name: **TCR2**
Register Description: **Transmit Control Register 2**
Register Address: **182h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	AEBE	AAIS	ARA	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bits 0 to 4 / Unused. Must be set = 0 for proper operation.

Bit 5 / Automatic Remote Alarm Generation (ARA)
0 = disabled
1 = enabled

Bit 6 / Automatic AIS Generation (AAIS)
0 = disabled
1 = enabled

Bit 7 / Automatic E-Bit Enable (AEBE)
0 = E-bits not automatically set in the transmit direction
1 = E-bits automatically set in the transmit direction

11.6 Automatic Alarm Generation

The device can be programmed to automatically transmit AIS or Remote Alarm. When automatic AIS generation is enabled (TCR2.6 = 1), the device monitors the receive side framer to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all one's) reception, or loss of receive carrier (or signal). If any one (or more) of the above conditions is present, then the framer forces an AIS.

When automatic RAI generation is enabled (TCR2.5 = 1), the framer monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all ones) reception, or loss of receive carrier (or signal) or if CRC4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC4 is enabled). If any one (or more) of the above conditions is present, then the framer will transmit a RAI alarm. RAI generation conforms to ETS 300 011 specifications and a constant Remote Alarm will be transmitted if the DS26401 cannot find CRC4 multiframe synchronization within 400ms as per G.706.

Note: It is an illegal state to have both automatic AIS generation and automatic Remote Alarm generation enabled at the same time.

Register Name: **TCR3**
Register Description: **Transmit Control Register 3**
Register Address: **183h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	ODF	ODM	TCSS1	TCSS0	MFRS	—	IBPV	CRC4R
Default	0	0	0	0	0	0	0	0

Bit 0 / CRC-4 Recalculate (CRC4R)
0 = transmit CRC-4 generation and insertion operates in normal mode
1 = transmit CRC-4 generation operates according to G.706 Intermediate Path Recalculation method.

Bit 1 / Insert BPV (IBPV). A 0-to-1 transition on this bit will cause a single BiPolar Violation (BPV) to be inserted into the transmit data stream. Once this bit has been toggled from a 0 to a 1, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted.

Bit 2 / Unused. Must be set = 0 for proper operation.

Bit 3 / Multiframe Reference Select (MFRS). This bit selects the source for the transmit formatter multiframe boundary.
0 = Normal Operation. Transmit multiframe boundary is determined by 'line-side' counters referenced to TSYNC when TSYNC is an input. Free running when TSYNC is an output.
1 = Pass-Forward Operation. Tx multiframe boundary determined by 'system-side' counters referenced to TSSYNC input, which is then 'passed forward' to the line side clock domain. This mode can only be used when the transmit elastic store is enabled with a synchronous backplane (i.e., no frame slips allowed). This mode must be used to allow Tx hardware signaling insertion while the Tx elastic store is enabled.

Bit 4 / Transmit Clock Source Select bit 0 (TCSS0)

Bit 5 / Transmit Clock Source Select bit 1 (TCSS1)

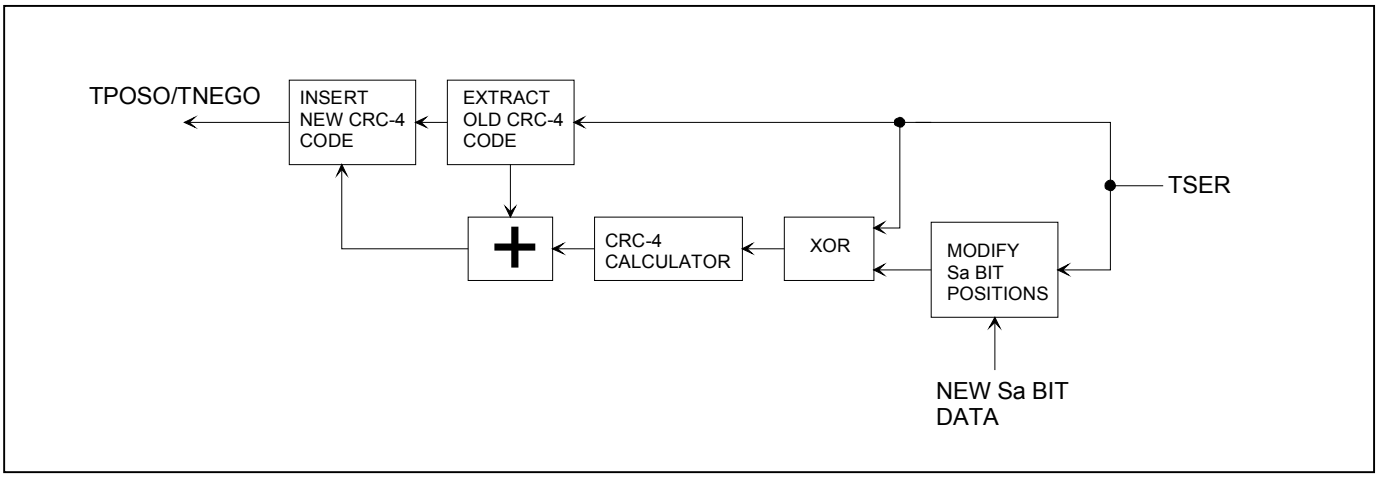
TCSS1	TCSS0	Transmit Clock Source
0	0	The TCLK pin is always the source of Transmit Clock.
0	1	Switch to the clock present at RCLK when the signal at the TCLK pin fails to transition after 1 channel time.
1	0	For Future Use
1	1	Use the signal present at RCLK as the Transmit Clock. The TCLK pin is ignored.

Bit 6 / Output Data Mode (ODM)
0 = pulses at TPOS and TNEG are one full TCLK period wide
1 = pulses at TPOS and TNEG are 1/2 TCLK period wide

Bit 7 / Output Data Format (ODF)
0 = bipolar data at TPOS and TNEG
1 = NRZ data at TPOS; TNEG = 0

11.7 G.706 Intermediate CRC-4 Updating (E1 Mode Only)

The DS26401 can implement the G.706 CRC-4 recalculation at intermediate path points. When this mode is enabled, the data stream presented at TSER will already have the FAS/NFAS, CRC multiframe alignment word and CRC-4 checksum in time slot 0. The user can modify the Sa bit positions and this change in data content will be used to modify the CRC-4 checksum. This modification however will not corrupt any error information the original CRC-4 checksum may contain. In this mode of operation, TSYNC must be configured to multiframe mode. The data at TSER must be aligned to the TSYNC signal. If TSYNC is an input then the user must assert TSYNC aligned at the beginning of the multiframe relative to TSER. If TSYNC is an output, the user must multiframe align the data presented to TSER. This mode is enabled with the TCR3.0 control bit (CRC4R).



Register Name: **TIOCR**
Register Description: **Transmit I/O Configuration Register**
Register Address: **184h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TCLKINV	TSYNCINV	TSSYNCINV	TSCLKM	TSSM	TSIO	—	TSM
Default	0	0	0	0	0	0	0	0

Bit 0 / TSYNC Mode Select (TSM). Selects frame or multiframe mode for the TSYNC pin.
0 = frame mode
1 = multiframe mode

Bit 1 / Unused. Must be set = 0 for proper operation.

Bit 2 / TSYNC I/O Select (TSIO)
0 = TSYNC is an input
1 = TSYNC is an output

Bit 3 / TSSYNC Mode Select (TSSM). Selects frame or multiframe mode for the TSSYNC pin.
0 = frame mode
1 = multiframe mode

Bit 4 / TSYSCLK Mode Select (TSCLKM)
0 = if TSYSCLK is 1.544MHz
1 = if TSYSCLK is 2.048/4.096/8.192/16.384MHz or IBO enabled (see Section 9.20 for details on IBO function)

Bit 5 / TSSYNC Invert (TSSYNCINV)
0 = No inversion
1 = Invert

Bit 6 / TSYNC Invert (TSYNCINV)
1 = Invert

Bit 7 / TCLK Invert (TCLKINV)
0 = No inversion
1 = Invert

11.8 E1 Transmit Status and Information

When a particular event has occurred (or is occurring), the appropriate bit in one of these registers will be set to a one. Status bits may operate in either a latched or real-time fashion. Some latched bits may be enabled to generate a hardware interrupt via the $\overline{INT}$ signal.

Real-Time Bits
Some status bits operate in a real-time fashion. These bits are read-only and indicate the present state of an alarm or a condition. Real-time bits will remain stable, and valid during the host read operation. The current value of the internal status signals can be read at any time from the real-time status registers without changing any the latched status register bits

Latched Bits
When an event or an alarm occurs and a latched bit is set to a one, it will remain set until cleared by the user. These bits typically respond on a change-of-state for an alarm, condition, or event; and operate in a read-then-write fashion. The user should read the value of the desired status bit, and then write a 1 to that particular bit location in order to clear the latched value (write a '0' to locations not to be cleared). Once the bit is cleared, it will not be set again until the event has occurred again.

Mask Bits
Some of the alarms and events can be either masked or unmasked from the interrupt pin via the Interrupt Mask Registers (TIMx). When unmasked, the $\overline{INT}$ signal will be forced low when the enabled event or condition occurs. The $\overline{INT}$ pin will be allowed to return high (if no other unmasked interrupts are present) when the user reads then clears (with a write) the alarm bit that caused the interrupt to occur. Note that the latched status bit and the $\overline{INT}$ pin will clear even if the alarm is still present.

Register Name: **TLS1**
Register Description: **Transmit Latched Status Register 1**
Register Address: **190h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TESF	TESEM	TSLIP	—	TAF	TMF	LOTCC	LOTC
Default	0	0	0	0	0	0	0	0

All bits in this register are latched and can cause interrupts.

Bit 0 / Loss of Transmit Clock Condition (LOTC). Set when the TCLK pin has not transitioned for approximately 3 clock periods. Will force the LOTC pin high if enabled. The host can clear this bit even if the condition is still present. The LOTC pin will remain high while the condition exists, even if the host has cleared the status bit. If enabled by TIM1.0, the $\overline{INT}$ pin transitions low when this bit is set, and transitions high when this bit is cleared (if no other unmasked interrupt conditions exist).

Bit 1 / Loss of Transmit Clock Condition Clear (LOTCC). Set when the LOTC condition has cleared (a clock has been sensed at the TCLK pin).

Bit 2 / Transmit Multiframe Event (TMF). Set every 2ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.

Bit 3 / Transmit Align Frame Event (TAF). Set every 250μs at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.

Bit 4 / Unused

Bit 5 / Transmit Elastic Store Slip Occurrence Event (TSLIP). Set when the transmit elastic store has either repeated or deleted a frame.

Bit 6 / Transmit Elastic Store Empty Event (TESEM). Set when the transmit elastic store buffer empties and a frame is repeated.

Bit 7 / Transmit Elastic Store Full Event (TESF). Set when the transmit elastic store buffer fills and a frame is deleted.

Register Name: **TIM1**
Register Description: **Transmit Interrupt Mask Register 1**
Register Address: **1A0h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TESF	TESEM	TSLIP	—	TAF	TMF	LOTCC	LOTC
Default	0	0	0	0	0	0	0	0

Bit 0 / Loss of Transmit Clock Condition (LOTC)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Loss of Transmit Clock Clear Condition (LOTCC)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Transmit Multiframe Event (TMF)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Bit 3 / Transmit Align Frame Event (TAF)
0 = interrupt masked
1 = interrupt enabled

Bit 4 / Unused. Must be set = 0 for proper operation.

Bit 5 / Transmit Elastic Store Slip Occurrence Event (TSLIP)
0 = interrupt masked
1 = interrupt enabled

Bit 6 / Transmit Elastic Store Empty Event (TESEM)
0 = interrupt masked
1 = interrupt enabled

Bit 7 / Transmit Elastic Store Full Event (TESF)
0 = interrupt masked
1 = interrupt enabled

11.9 Per-Channel Loopback

The Per-Channel Loopback Registers (PCLRs) determine which channels (if any) from the backplane should be replaced with the data from the receive side or in other words, off of the T1 or E1 line. If this loopback is enabled, then transmit and receive clocks and frame syncs must be synchronized. One method to accomplish this would be to tie RCLK to TCLK and RFSYNC to TSYNC. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

Each of the bit position in the Per-Channel Loopback Registers (PCLR1/PCLR2/PCLR3/PCLR4) represent a time slot in the outgoing frame. When these bits are set to a one, data from the corresponding receive channel will replace the data on TSER for that channel.

Register Name: **PCL1, PCL2, PCL3, PCL4**
Register Description: **Per-Channel Loopback Enable Registers**
Register Address: **1D0h, 1D1h, 1D2h, 1D3h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**PCL1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**PCL2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**PCL3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**PCL4**

Bits 0 to 7 / Per-Channel Loopback Enable for Channels 1 to 32 (CH1 to CH32)

0 = Loopback disabled
1 = Enable Loopback. Source data from the corresponding receive channel

11.10 E1 Transmit DS0 Monitoring Function

The DS26401 has the ability to monitor one DS0 64kbps channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction the user will determine which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the TDS0SEL register. In the receive direction, the RCM0 to RCM4 bits in the RDS0SEL register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits will appear in the Transmit DS0 Monitor (TDS0M) register and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the Receive DS0 (RDS0M) register. The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate T1or E1 channel. T1 channels 1 through 24 map to register values 0 through 23. E1 channels 1 through 32 map to register values 0 through 31. For example, if DS0 channel 6 in the transmit direction and DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into TDS0SEL and RDS0SEL:

TCM4 = 0	RCM4 = 0
TCM3 = 0	RCM3 = 1
TCM2 = 1	RCM2 = 1
TCM1 = 0	RCM1 = 1
TCM0 = 1	RCM0 = 0

Register Name: **TDS0SEL**
Register Description: **Transmit DS0 Channel Monitor Select**
Register Address: **189h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	TCM4	TCM3	TCM2	TCM1	TCM0
Default	0	0	0	0	0	0	0	0

Bits 0 to 4 / Transmit Channel Monitor Bits (TCM0 to TCM4). TCM0 is the LSB of a 5 bit channel select that determines which transmit channel data will appear in the TDS0M register.

Bits 5 to 7 / Unused. Must be set = 0 for proper operation.

Register Name: **TDS0M**
Register Description: **Transmit DS0 Monitor Register**
Register Address: **1BBh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	B1	B2	B3	B4	B5	B6	B7	B8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Transmit DS0 Channel Bits (B1 to B8). Transmit channel data that has been selected by the Transmit Channel Monitor Select Register. B8 is the LSB of the DS0 channel (last bit to be transmitted).

11.11 E1 Transmit Signaling Operation

There are two methods to provide transmit signaling data—processor-based (i.e., software-based) or hardware-based. Processor-based refers to access through the transmit signaling registers, TS1-TS16, while hardware-based refers to using the TSIG pins. Both methods can be used simultaneously.

11.11.1 Processor-Based Mode

In processor-based mode, signaling data is loaded into the Transmit Signaling registers (TS1–TS16) via the host interface. On multiframe boundaries, the contents of these registers are loaded into a shift register for placement in the appropriate bit position in the outgoing data stream. The user can utilize the Transmit Multiframe Interrupt in Latched Status Register 1 (TLS1.2) to know when to update the signaling bits. The user need not update any transmit signaling register for which there is no change of state for that register.

Each Transmit Signaling Register contains the TS16 CAS signaling (E1) for one time slot that will be inserted into the outgoing stream if enabled to do so via TCR1.6. Signaling data can be sourced from the TS registers on a per-channel basis by utilizing the Software Signaling Insertion Enable registers, SSIE1 through SSIE4.

In E1 mode, TS16 carries the signaling information. This information can be in either CCS (Common Channel Signaling) or CAS (Channel Associated Signaling) format. The 32 time slots are referenced by two different channel number schemes in E1. In “Channel” numbering, TS0 through TS31 are labeled channels 1 through 32. In “Phone Channel” numbering TS1 through TS15 are labeled channel 1 through channel 15 and TS17 through TS31 are labeled channel 15 through channel 30.

Time Slot Numbering Schemes

TS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Channel	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Phone Channel		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

11.11.2 Hardware-Based Mode

In Hardware-Based mode, signaling data is input via the TSIG pin. This signaling PCM stream is buffered and inserted to the data stream being input at the TSER pin.

Signaling data may be input via the Transmit Hardware Signaling Channel Select (THSCS) function, the framer can be set up to take the signaling data presented at the TSIG pin and insert the signaling data into the PCM data stream that is being input at the TSER pin. The user has the ability to control which channels are to have signaling data from the TSIG pin inserted into them on a per-channel basis. The signaling insertion capabilities of the framer are available whether the transmit side elastic store is enabled or disabled. If the elastic store is enabled, the backplane clock (TSYSCLK) can be 2.048MHz. If IBO mode is enabled then TSYSCLK may also be 4.096MHz, 8.192MHz, or 16.384MHz.

Register Name: **TS1 TO TS16**
Register Description: **Transmit Signaling Registers (E1 MODE)**
Register Address: **140h to 14Fh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

CAS Format

(MSB)							(LSB)	
0	0	0	0	X	Y	X	X	**TS1**
CH1-A	CH1-B	CH1-C	CH1-D	CH16-A	CH16-B	CH16-C	CH16-D	**TS2**
CH2-A	CH2-B	CH2-C	CH2-D	CH17-A	CH17-B	CH17-C	CH17-D	**TS3**
CH3-A	CH3-B	CH3-C	CH3-D	CH18-A	CH18-B	CH18-C	CH18-D	**TS4**
CH4-A	CH4-B	CH4-C	CH4-D	CH19-A	CH19-B	CH19-C	CH19-D	**TS5**
CH5-A	CH5-B	CH5-C	CH5-D	CH20-A	CH20-B	CH20-C	CH20-D	**TS6**
CH6-A	CH6-B	CH6-C	CH6-D	CH21-A	CH21-B	CH21-C	CH21-D	**TS7**
CH7-A	CH7-B	CH7-C	CH7-D	CH22-A	CH22-B	CH22-C	CH22-D	**TS8**
CH8-A	CH8-B	CH8-C	CH8-D	CH23-A	CH23-B	CH23-C	CH23-D	**TS9**
CH9-A	CH9-B	CH9-C	CH9-D	CH24-A	CH24-B	CH24-C	CH24-D	**TS10**
CH10-A	CH10-B	CH10-C	CH10-D	CH25-A	CH25-B	CH25-C	CH25-D	**TS11**
CH11-A	CH11-B	CH11-C	CH11-D	CH26-A	CH26-B	CH26-C	CH26-D	**TS12**
CH12-A	CH12-B	CH12-C	CH12-D	CH27-A	CH27-B	CH27-C	CH27-D	**TS13**
CH13-A	CH13-B	CH13-C	CH13-D	CH28-A	CH28-B	CH28-C	CH28-D	**TS14**
CH14-A	CH14-B	CH14-C	CH14-D	CH29-A	CH29-B	CH29-C	CH29-D	**TS15**
CH15-A	CH15-B	CH15-C	CH15-D	CH30-A	CH30-B	CH30-C	CH30-D	**TS16**

CCS Format

(MSB)							(LSB)	
1	2	3	4	5	6	7	8	**TS1**
9	10	11	12	13	14	15	16	**TS2**
17	18	19	20	21	22	23	24	**TS3**
25	26	27	28	29	30	31	32	**TS4**
33	34	35	36	37	38	39	40	**TS5**
41	42	43	44	45	46	47	48	**TS6**
49	50	51	52	53	54	55	56	**TS7**
57	58	59	60	61	62	63	64	**TS8**
65	66	67	68	69	70	71	72	**TS9**
73	74	75	76	77	78	79	80	**TS10**
81	82	83	84	85	86	87	88	**TS11**
89	90	91	92	93	94	95	96	**TS12**
97	98	99	100	101	102	103	104	**TS13**
105	106	107	108	109	110	111	112	**TS14**
113	114	115	116	117	118	119	120	**TS15**
121	122	123	124	125	126	127	128	**TS16**

Register Name: **SSIE1, SSIE2, SSIE3, SSIE4**
Register Description: **Software Signaling Insertion Enable Registers**
Register Address: **118h, 119h, 11Ah, 113h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**SSIE1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**SSIE2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**SSIE3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**SSIE4**

Bits 0 to 7 / Software Signaling Insertion Enable for Channels 1 to 32 (SSIEx). These bits determine which channels are to have signaling inserted form the Transmit Signaling registers.

0 = do not source signaling data from the TS registers for this channel
1 = source signaling data from the TS registers for this channel

Register Name: **THSCS1, THSCS2, THSCS3, THSCS4**
Register Description: **Transmit Hardware Signaling Channel Select Registers**
Register Address: **1C8h, 1C9h, 1CAh, 1CBh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**THSCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**THSCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**THSCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**THSCS4**

Bits 0 to 7 / Transmit Hardware Signaling Channel Select for Channels 1 to 32 (THSCSx). These bits determine which channels have signaling data inserted from the TSIG pin into the TSER PCM data.

0 = do not source signaling data from the TSIG pin for this channel
1 = source signaling data from the TSIG pin for this channel

11.12 E1 Transmit Per-Channel Idle Code Insertion

Channel data can be replaced by an idle code on a per-channel basis in the transmit and receive directions. Thirty-two Transmit Idle Definition Registers (TIDR1-TIDR32) are provided to set the 8-bit idle code for each channel. The Transmit Channel Idle Code Enable registers (TCICE1-4) are used to enable idle code replacement on a per channel basis.

Register Name: **TIDR1 to TIDR32**
Register Description: **Transmit Idle Code Definition Registers 1 to 32**
Register Address: **120h to 13Fh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Bit #	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7 / Per-Channel Idle Code Bits (C0 to C7). C0 is the LSB of the Code (this bit is transmitted last). Address 120H is for channel 1; address 13FH is for channel 32.

Register Name: **TCICE1, TCICE2, TCICE3, TCICE4**
Register Description: **Transmit Channel Idle Code Enable Registers**
Register Address: **150h, 151h, 152h, 153Hh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

The Transmit Channel Idle Code Enable Registers (TCICE1/2/3/4) are used to determine which of the 32 E1 channels should be overwritten with the code placed in the Transmit Idle Code Definition Register.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**TCICE1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**TCICE2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**TCICE3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**TCICE4**

Bits 0 to 7 / Transmit Channels 1 to 32 Code Insertion Control Bits (CH1 to CH32)
0 = do not insert data from the Idle Code Array into the transmit data stream
1 = insert data from the Idle Code Array into the transmit data stream

11.13 E1 Transmit Channel Blocking Registers

The Receive Channel blocking Registers (RCBR1 / RCBR2 / RCBR3 / RCBR4) and the Transmit Channel Blocking Registers (TCBR1 / TCBR2 / TCBR3 / TCBR4) control RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHBLK pins are user-programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN–PRI applications. When the appropriate bits are set to a one, the RCHBLK and TCHBLK pin will be held high during the entire corresponding channel time.

Register Name: **TCBR1, TCBR2, TCBR3, TCBR4**
Register Description: **Transmit Channel Blocking Registers**
Register Address: **1C4h, 1C5h, 1C6h, 1C7h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**TCBR1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**TCBR2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**TCBR3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**TCBR4**

Bits 0 to 7 / Transmit Channels 1 to 32 Channel Blocking Control Bits (CH1 to CH32)

0 = force the TCHBLK pin to remain low during this channel time
1 = force the TCHBLK pin high during this channel time

11.14 E1 Transmit Elastic Stores Operation

The DS26401 contains dual two-frame elastic stores, one for the receive direction, and one for the transmit direction. Both elastic stores are fully independent. The transmit and receive side elastic stores can be enabled/disabled independent of each other. Also, each elastic store can interface to either a 1.544MHz or 2.048/4.096/8.192/16.384MHz backplane without regard to the backplane rate of the other elastic store.

The elastic stores have two main purposes. First, they can be used for rate conversion. When the DS26401 is in the T1 mode, the elastic stores can rate convert the T1 data stream to a 2.048MHz backplane. In E1 mode, the elastic store can rate convert the E1 data stream to a 1.544MHz backplane. Secondly, they can be used to absorb the differences in frequency and phase between the T1 or E1 data stream and an asynchronous (i.e., not locked) backplane clock (which can be 1.544MHz or 2.048MHz). In this mode, the elastic stores will manage the rate difference and perform controlled slips, deleting or repeating frames of data in order to manage the difference between the network and the backplane. Note that TCBR4 will not be active when the transmitter is enabled with a 1.544MHz backplane.

The elastic stores can also be used to multiplex T1 or E1 data streams into higher backplane rates. This is the Interleave Bus Option (IBO) which is discussed in Section 11.19.

Note that the receive elastic store status bits are contained in TLS1 with the associated interrupt bits located in TIM1. These bits indicate a receive slip event, or when the e-store FIFO is in a ‘full’ or ‘empty’ condition. See the register definition for TLS1 for additional information.

The operation of the transmit elastic store is very similar to the receive side. If the transmit side elastic store is enabled a 1.544MHz or 2.048MHz clock can be applied to the TSYSCLK input. The user must supply a frame sync pulse or a multiframe sync pulse to the TSSYNC input. For higher rate system clock applications, see the Interleave Bus Option section. Controlled slips in the transmit elastic store are reported in the TLS1.5 bit and the direction of the slip is reported in the TLS1.6 and TLS1.7 bits.

11.14.1 Elastic Stores Initialization

There are two elastic store initializations that may be used to improve performance in certain applications, Elastic Store Reset and Elastic Store Align. Both of these involve the manipulation of the elastic store's read and write pointers and are useful primarily in synchronous applications (RSYSCLK/TSYSCLK are locked to RCLK/TCLK, respectively). The elastic store reset is used to minimize the delay through the elastic store. The elastic store align bit is used to 'center' the read/write pointers to the extent possible.

Elastic Store Delay After Initialization

INITIALIZATION	REGISTER BIT	DELAY
Receive Elastic Store Reset	RESCR.2	N bytes < Delay < 1 Frame + N bytes
Transmit Elastic Store Reset	TESCR.2	N bytes < Delay < 1 Frame + N bytes
Receive Elastic Store Align	RESCR.3	1/2 Frame < Delay < 1 1/2 Frames
Transmit Elastic Store Align	TESCR.3	1/2 Frame < Delay < 1 1/2 Frames

N = 9 for TSZS = 0

N = 2 for TSZS = 1

11.14.2 Minimum Delay Mode

Elastic store minimum delay mode may be used when the elastic store's system clock is locked to its network clock (i.e., RCLK locked to RSYSCLK for the receive side and TCLK locked to TSYSCLK for the transmit side). TESCR.1 and RESCR.1 enable the transmit and receive elastic store minimum delay modes. When enabled the elastic stores will be forced to a maximum depth of 32 bits instead of the normal two-frame depth. This feature is useful primarily in applications that interface to a 2.048MHz bus. Certain restrictions apply when minimum delay mode is used. In addition to the restriction mentioned above, RSYNC must be configured as an output when the receive elastic store is in minimum delay mode and TSYNC must be configured as an output when transmit minimum delay mode is enabled. The RSYNC and TSYNC outputs are registered on the rising edge of RSYSCLK and TSYSCLK respectfully. In a typical application RSYSCLK and TSYSCLK are locked to RCLK, and RSYNC (frame output mode) is connected to TSSYNC (frame input mode). All of the slip contention logic in the framer is disabled (since slips cannot occur). On power–up after the RSYSCLK and TSYSCLK signals have locked to their respective network clock signals, the elastic store reset bits (TESCR.2 and RESCR.2) should be toggled from a zero to a one to ensure proper operation.

Register Name: **TESCR**
Register Description: **Transmit Elastic Store Control Register**
Register Address: **185h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TDATFMT	TGCLKEN	—	TSZS	TESALGN	TESR	TESMDM	TESE
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Elastic Store Enable (TESE)
0 = elastic store is bypassed
1 = elastic store is enabled

Bit 1 / Transmit Elastic Store Minimum Delay Mode (TESMDM)
0 = elastic stores operate at full two frame depth
1 = elastic stores operate at 32-bit depth

Bit 2 / Receive Elastic Store Reset (RESR). Setting this bit from a zero to a one will force the read pointer into the same frame that the write pointer is exiting, minimizing the delay through the elastic store. If this command should place the pointers within the slip zone (see bit 4), then an immediate slip will occur and the pointers will move back to opposite frames. Should be toggled after TSYSCLK has been applied and is stable. Do not leave this bit set HIGH.

Bit 3 / Transmit Elastic Store Align (TESALGN). Setting this bit from a zero to a one will force the transmit elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command will be executed and the data will be disrupted. Should be toggled after TSYSCLK has been applied and is stable. Must be cleared and set again for a subsequent align.

Bit 4 / Transmit Slip Zone Select (TSZS). This bit determines the minimum distance allowed between the elastic store read and write pointers before forcing a controlled slip. This bit is only applies during T1 to E1 or E1 to T1 conversion applications.
0 = force a slip at 9 bytes or less of separation (used for clustered blank channels)
1 = force a slip at 2 bytes or less of separation (used for distributed blank channels)

Bit 5 / Unused. Must be set = 0 for proper operation.

Bit 6 / Transmit Gapped Clock Enable (TGPCKEN).
0 = TCHCLK functions normally
1 = Enable gapped bit clock output on TCHCLK

Bit 7 / Transmit Channel Data Format (TDATFMT).
0 = 64kbps (data contained in all 8 bits)
1 = 56kbps (data contained in 7 out of the 8 bits)

Note: Bits 6 & 7 for fractional backplane support.

11.14.3 Mapping E1 Channels from a 1.544MHz Backplane

The user can use the TSCLKM bit in TIOCR.4 to enable the transmit elastic store to operate with a 1.544MHz backplane (24 channels / frame + F bit). In this mode, the user can chose which of the E1 time slots will have all ones data inserted by programming the Transmit Blank Channel Select registers (TBCS1-4). A logic 1 in the associated bit location will cause the DS26401 elastic store to force all ones at the outgoing E1 data for that channel. Typically, the user will want to program 8 channels to be 'blanked'. The default (power-up) configuration will blank channels 25 to 32, so that the first 24 E1 channels are mapped from the 24 channels of the 1.544MHz backplane.

Register Name: **TBCS1, TBCS2, TBCS3, TBCS4**
Register Description: **Transmit Blank Channel Select Registers**
Register Address: **1C0h, 1C1h, 1C2h, 1C3h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**TBCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**TBCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**TBCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**TBCS4**

Bits 0 to 7 / Transmit Blank Channel Select for Channels 1 to 32 (TBCS1 to 32)
0 = do not insert all ones for this channel
1 = insert all ones for this E1 channel

11.15 Fractional E1 Support (Gapped Clock Mode)

The DS26401 can be programmed to output gapped clocks for selected channels in the receive and transmit paths to simplify connections into a USART or LAPD controller in Fractional T1/E1 or ISDN–PRI applications. When the gapped clock feature is enabled, a gated clock is output on the TCHCLK signal. The channel selection is controlled via the transmit-gapped-clock channel-select registers (TGCCS1-TGCCS4). The transmit path is enabled for gapped clock mode with the TGCLKEN bit (TESCR.6). Both 56kbps and 64kbps channel formats are supported as determined by TESCR.7. When 56kbps mode is selected, the clock corresponding to the Data/Control bit in the channel is omitted (only the seven most significant bits of the channel have clocks).

Register Name: **TGCCS1, TGCCS2, TGCCS3, TGCCS4**
Register Description: **Transmit Gapped Clock Channel Select Registers**
Register Address: **1CCh, 1CDh, 1CEh, 1CFh [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**TGCCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**TGCCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**TGCCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**TGCCS4**

Bits 0 to 7 / Transmit Channels 1 to 32 Gapped Clock Channel Select Bits (CH1 to CH32)

0 = no clock is present on TCHCLK during this channel time
1 = force a clock on TCHCLK during this channel time. The clock will be synchronous with TCLK if the elastic store is disabled, and synchronous with TSYSCLK if the elastic store is enabled.

11.16 Additional (Sa) and International (Si) Bit Operation (E1 Mode)

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Transmit Status Register 1 (TLS1.3). The host can use the TLS1.3 bit to know when to update the TAF and TNAF registers. It has 250μs to update the data or else the old data will be retransmitted**. If the TAF an TNAF registers are only being used to source the align frame and non-align frame sync patterns then the host need only write once to these registers**. Data in the Si bit position will be overwritten if either the framer is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) have automatic E-bit insertion enabled.

There is also a set of eight registers (TSiAF, TSiNAF, TRA, TSa4 to TSa8) that via the Transmit Sa-Bit Control Register (TSaCR), can be programmed to insert both Si and Sa data. Data is sampled from these registers with the setting of the Transmit Multiframe bit in Status Register 1 (TLS1.3). The host can use the TLS1.3 bit to know when to update these registers. It has 2ms to update the data or else the old data will be retransmitted.

Register Name: **TAF**
Register Description: **Transmit Align Frame Register**
Register Address: **164h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	Si	0	0	1	1	0	1	1
Default	0	0	0	1	1	0	1	1

Bit 0 / Frame Alignment Signal Bit (1)

Bit 1 / Frame Alignment Signal Bit (1)

Bit 2 / Frame Alignment Signal Bit (0)

Bit 3 / Frame Alignment Signal Bit (1)

Bit 4 / Frame Alignment Signal Bit (1)

Bit 5 / Frame Alignment Signal Bit (0)

Bit 6 / Frame Alignment Signal Bit (0)

Bit 7 International Bit (Si)

Register Name: **TNAF**
Register Description: **Transmit Non-Align Frame Register**
Register Address: **165h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
Default	0	1	0	0	0	0	0	0

Bit 0 / Additional Bit 8 (Sa8)

Bit 1 / Additional Bit 7 (Sa7)

Bit 2 / Additional Bit 6 (Sa6)

Bit 3 / Additional Bit 5 (Sa5)

Bit 4 / Additional Bit 4 (Sa4)

Bit 5 / Remote Alarm [used to transmit the alarm (A)]

Bit 6 / Frame Non-Alignment Signal Bit (1)

Bit 7 / International Bit (Si)

Register Name: **TSiAF**
Register Description: **Transmit Si Bits of the Align Frame**
Register Address: **166h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TSiF14	TSiF12	TSiF10	TSiF8	TSiF6	TSiF4	TSiF2	TSiF0
Default	0	0	0	0	0	0	0	0

Bit 0 / Si Bit of Frame 0 (TSiF0)

Bit 1 / Si Bit of Frame 2 (TSiF2)

Bit 2 / Si Bit of Frame 4 (TSiF4)

Bit 3 / Si Bit of Frame 6 (TSiF6)

Bit 4 / Si Bit of Frame 8 (TSiF8)

Bit 5 / Si Bit of Frame 10 (TSiF10)

Bit 6 / Si Bit of Frame 12 (TSiF12)

Bit 7 / Si Bit of Frame 14 (TSiF14)

Register Name: **TSiNAF**
Register Description: **Transmit Si Bits of the Non-Align Frame**
Register Address: **167h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TSiF15	TSiF13	TSiF11	TSiF9	TSiF7	TSiF5	TSiF3	TSiF1
Default	0	0	0	0	0	0	0	0

Bit 0 / Si Bit of Frame 1 (TSiF1)

Bit 1 / Si Bit of Frame 3 (TSiF3)

Bit 2 / Si Bit of Frame 5 (TSiF5)

Bit 3 / Si Bit of Frame 7 (TSiF7)

Bit 4 / Si Bit of Frame 9 (TSiF9)

Bit 5 / Si Bit of Frame 11 (TSiF11)

Bit 6 / Si Bit of Frame 13 (TSiF13)

Bit 7 / Si Bit of Frame 15 (TSiF15)

Register Name: **TRA**
Register Description: **Transmit Remote Alarm**
Register Address: **168h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TRAF15	TRAF13	TRAF11	TRAF9	TRAF7	TRAF5	TRAF3	TRAF1
Default	0	0	0	0	0	0	0	0

Bit 0 / Remote Alarm Bit of Frame 1 (TRAF1)

Bit 1 / Remote Alarm Bit of Frame 3 (TRAF3)

Bit 2 / Remote Alarm Bit of Frame 5 (TRAF5)

Bit 3 / Remote Alarm Bit of Frame 7 (TRAF7)

Bit 4 / Remote Alarm Bit of Frame 9 (TRAF9)

Bit 5 / Remote Alarm Bit of Frame 11 (TRAF11)

Bit 6 / Remote Alarm Bit of Frame 13 (TRAF13)

Bit 7 / Remote Alarm Bit of Frame 15 (TRAF15)

Register Name: **TSa4**
Register Description: **Transmit Sa4 Bits**
Register Address: **169h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TSa4F15	TSa4F13	TSa4F11	TSa4F9	TSa4F7	TSa4F5	TSa4F3	TSa4F1
Default	0	0	0	0	0	0	0	0

Bit 0 / Sa4 Bit of Frame 1 (TSa4F1)

Bit 1 / Sa4 Bit of Frame 3 (TSa4F3)

Bit 2 / Sa4 Bit of Frame 5 (TSa4F5)

Bit 3 / Sa4 Bit of Frame 7 (TSa4F7)

Bit 4 / Sa4 Bit of Frame 9 (TSa4F9)

Bit 5 / Sa4 Bit of Frame 11 (TSa4F11)

Bit 6 / Sa4 Bit of Frame 13 (TSa4F13)

Bit 7 / Sa4 Bit of Frame 15 (TSa4F15)

Register Name: **TSa5**
Register Description: **Transmitted Sa5 Bits**
Register Address: **16Ah + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TSa5F15	TSa5F13	TSa5F11	TSa5F9	TSa5F7	TSa5F5	TSa5F3	TSa5F1
Default	0	0	0	0	0	0	0	0

Bit 0 / Sa5 Bit of Frame 1 (TSa5F1)

Bit 1 / Sa5 Bit of Frame 3 (TSa5F3)

Bit 2 / Sa5 Bit of Frame 5 (TSa5F5)

Bit 3 / Sa5 Bit of Frame 7 (TSa5F7)

Bit 4 / Sa5 Bit of Frame 9 (TSa5F9)

Bit 5 / Sa5 Bit of Frame 11 (TSa5F11)

Bit 6 / Sa5 Bit of Frame 13 (TSa5F13)

Bit 7 / Sa5 Bit of Frame 15 (TSa5F15)

Register Name: **TSa6**
Register Description: **Transmit Sa6 Bits**
Register Address: **16Bh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TSa6F15	TSa6F13	TSa6F11	TSa6F9	TSa6F7	TSa6F5	TSa6F3	TSa6F1
Default	0	0	0	0	0	0	0	0

Bit 0 / Sa6 Bit of Frame 1 (TSa6F1)

Bit 1 / Sa6 Bit of Frame 3 (TSa6F3)

Bit 2 / Sa6 Bit of Frame 5 (TSa6F5)

Bit 3 / Sa6 Bit of Frame 7 (TSa6F7)

Bit 4 / Sa6 Bit of Frame 9 (TSa6F9)

Bit 5 / Sa6 Bit of Frame 11 (TSa6F11)

Bit 6 / Sa6 Bit of Frame 13 (TSa6F13)

Bit 7 / Sa6 Bit of Frame 15 (TSa6F15)

Register Name: **TSa7**
Register Description: **Transmit Sa7 Bits**
Register Address: **16Ch + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TSa7F15	TSa7F13	TSa7F11	TSa7F9	TSa7F7	TSa7F5	TSa7F3	TSa7F1
Default	0	0	0	0	0	0	0	0

Bit 0 / Sa7 Bit of Frame 1 (TSa7F1)

Bit 1 / Sa7 Bit of Frame 3 (TSa7F3)

Bit 2 / Sa7 Bit of Frame 5 (TSa7F5)

Bit 3 / Sa7 Bit of Frame 7 (TSa7F7)

Bit 4 / Sa7 Bit of Frame 9 (TSa7F9)

Bit 5 / Sa7 Bit of Frame 11 (TSa7F11)

Bit 6 / Sa7 Bit of Frame 13 (TSa7F13)

Bit 7 / Sa7 Bit of Frame 15 (TSa4F15)

Register Name: **TSa8**
Register Description: **Transmit Sa8 Bits**
Register Address: **16Dh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TSa8F15	TSa8F13	TSa8F11	TSa8F9	TSa8F7	TSa8F5	TSa8F3	TSa8F1
Default	0	0	0	0	0	0	0	0

Bit 0 / Sa8 Bit of Frame 1 (TSa8F1)

Bit 1 / Sa8 Bit of Frame 3 (TSa8F3)

Bit 2 / Sa8 Bit of Frame 5 (TSa8F5)

Bit 3 / Sa8 Bit of Frame 7 (TSa8F7)

Bit 4 / Sa8 Bit of Frame 9 (TSa8F9)

Bit 5 / Sa8 Bit of Frame 11 (TSa8F11)

Bit 6 / Sa8 Bit of Frame 13 (TSa8F13)

Bit 7 / Sa8 Bit of Frame 15 (TSa8F15)

Register Name: **TSACR**
Register Description: **Transmit Sa Bit Control Register**
Register Address: **114h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	SiAF	SiNAF	RA	Sa4	Sa5	Sa6	Sa7	Sa8
Default	0	0	0	0	0	0	0	0

Bit 0 / Additional Bit 8 Insertion Control Bit (Sa8)
0 = do not insert data from the TSa8 register into the transmit data stream
1 = insert data from the TSa8 register into the transmit data stream

Bit 1 / Additional Bit 7 Insertion Control Bit (Sa7)
0 = do not insert data from the TSa7 register into the transmit data stream
1 = insert data from the TSa7 register into the transmit data stream

Bit 2 / Additional Bit 6 Insertion Control Bit (Sa6)
0 = do not insert data from the TSa6 register into the transmit data stream
1 = insert data from the TSa6 register into the transmit data stream

Bit 3 / Additional Bit 5 Insertion Control Bit (Sa5)
0 = do not insert data from the TSa5 register into the transmit data stream
1 = insert data from the TSa5 register into the transmit data stream

Bit 4 / Additional Bit 4 Insertion Control Bit (Sa4)
0 = do not insert data from the TSa4 register into the transmit data stream
1 = insert data from the TSa4 register into the transmit data stream

Bit 5 / Remote Alarm Insertion Control Bit (RA)
0 = do not insert data from the TRA register into the transmit data stream
1 = insert data from the TRA register into the transmit data stream

Bit 6 / International Bit in Non-Align Frame Insertion Control Bit (SiNAF)
0 = do not insert data from the TSiNAF register into the transmit data stream
1 = insert data from the TSiNAF register into the transmit data stream

Bit 7 / International Bit in Align Frame Insertion Control Bit (SiAF)
0 = do not insert data from the TSiAF register into the transmit data stream
1 = insert data from the TSiAF register into the transmit data stream

11.17 Transmit HDLC Controller

Each framer port has an HDLC controller with 64-byte FIFOs.

The HDLC controller can be mapped into a single time slot, or Sa4 to Sa8 bits (E1 Mode) or the FDL (T1 mode). This block has 64 byte FIFO buffers in both the transmit and receive paths. The user can select any specific bits within the time slot(s) to assign to the HDLC controller, as well as specific Sa bits (E1 mode). The HDLC controllers automatically generate and detect flags, generate and check the CRC checksum, generate and detect abort sequences, stuff and destuff zeros, and byte align to the data stream.

Register Name: **THC1**
Register Description: **Transmit HDLC Control Register 1**
Register Address: **110h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	NOFS	TEOML	THR	THMS	TFS	TEOM	TZSD	TCRCD
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit CRC Defeat (TCRCD). A 2-byte CRC code is automatically appended to the outbound message. This bit can be used to disable the CRC function.
0 = enable CRC generation (normal operation)
1 = disable CRC generation

Bit 1 / Transmit Zero Stuffer Defeat (TZSD). The Zero Stuffer function automatically inserts a zero in the message field (between the flags) after 5 consecutive ones to prevent the emulation of a flag or abort sequence by the data pattern. The receiver automatically removes (destuffs) any zero after 5 ones in the message field.
0 = enable the zero stuffer (normal operation)
1 = disable the zero stuffer

Bit 2 / Transmit End of Message (TEOM). Should be set to a one just before the last data byte of an HDLC packet is written into the transmit FIFO at THF. If not disabled via TCRCD, the transmitter will automatically append a 2-byte CRC code to the end of the message.

Bit 3 / Transmit Flag/Idle Select (TFS). This bit selects the inter-message fill character after the closing and before the opening flags (7Eh).
0 = 7Eh
1 = FFh

Bit 4 / Transmit HDLC Mapping Select (THMS)
0 = Transmit HDLC assigned to channels
1 = Transmit HDLC assigned to FDL(T1 mode), Sa Bits(E1 mode)

Bit 5 / Transmit HDLC Reset (THR). Will reset the transmit HDLC controller and flush the transmit FIFO. An abort followed by 7Eh or FFh flags/idle will be transmitted until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent reset.
0 = Normal operation
1 = Reset transmit HDLC controller and flush the transmit FIFO

Bit 6 / Transmit End of Message and Loop (TEOML). To loop on a message, should be set to a one just before the last data byte of an HDLC packet is written into the transmit FIFO. The message will repeat until the user clears this bit or a new message is written to the transmit FIFO. If the host clears the bit, the looping message will complete then flags will be transmitted until new message is written to the FIFO. If the host terminates the loop by writing a new message to the FIFO the loop will terminate, one or two flags will be transmitted and the new message will start. If not disabled via TCRCD, the transmitter will automatically append a 2-byte CRC code to the end of all messages.

Bit 7 / Number Of Flags Select (NOFS)
0 = send one flag between consecutive messages
1 = send two flags between consecutive messages

Register Name: **THC2**
Register Description: **Transmit HDLC Control Register 2**
Register Address: **113h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TABT	—	THCEN	THCS4	THCS3	THCS2	THCS1	THCS0
Default	0	0	0	0	0	0	0	0

Bits 0 to 4 / Transmit HDLC Channel Select (THCS0 to 4). Determines which DSO channel will have the carry the HDLC message if enabled.

Bit 5 / Transmit HDLC Controller Enable (THCEN)
0 = Transmit HDLC Controller is not enabled
1 = Transmit HDLC Controller is enabled

Bit 6 / Unused

Bit 7 / Transmit Abort (TABT). A 0-to-1 transition will cause the FIFO contents to be dumped and one FEh abort to be sent followed by 7Eh or FFh flags/idle until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent abort to be sent.

Register Name: **THBSE**
Register Description: **Transmit HDLC Bit Suppress**
Register Address: **111h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	TBSE8	TBSE7	TBSE6	TBSE5	TBSE4	TBSE3	TBSE2	TBSE1
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Bit 1 Suppress/Sa8 Bit Suppress (TBSE1). LSB of the channel. Set to one to stop this bit from being used.

Bit 1 / Transmit Bit 2 Suppress/Sa7 Bit Suppress (TBSE2). Set to one to stop this bit from being used

Bit 2 / Transmit Bit 3 Suppress/Sa6 Bit Suppress (TBSE3). Set to one to stop this bit from being used

Bit 3 / Transmit Bit 4 Suppress/Sa5 Bit Suppress (TBSE4). Set to one to stop this bit from being used

Bit 4 / Transmit Bit 5 Suppress/Sa4 Bit Suppress (TBSE5). Set to one to stop this bit from being used

Bit 5 / Transmit Bit 6 Suppress (TBSE6). Set to one to stop this bit from being used.

Bit 6 / Transmit Bit 7 Suppress (TBSE7). Set to one to stop this bit from being used.

Bit 7 / Transmit Bit 8 Suppress (TBSE8). MSB of the channel. Set to one to stop this bit from being used.

11.17.1 Transmit HDLC FIFO Control

Control of the transmit FIFO is accomplished via the Transmit HDLC FIFO Control (THFC). The FIFO Control register sets the watermarks for the receive FIFO.

When the transmit FIFO empties below the low watermark, the TLWM bit in the appropriate HDLC status register will be set. TLWM is a real-time bit and will remain set as long as the transmit FIFO's write pointer is below the watermark. If enabled, this condition can also cause an interrupt via the $\overline{INT}$ pin.

Register Name: **THFC**
Register Description: **Transmit HDLC FIFO Control Register**
Register Address: **187h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	TFLWM1	TFLWM0
Default	0	0	0	0	0	0	0	0

Bits 0, 1 / Transmit HDLC FIFO Low-Watermark Select (TFLWM0 to TFLWM1)

TFLWM1	TFLWM0	Transmit FIFO Watermark
0	0	4 bytes
0	1	16 bytes
1	0	32 bytes
1	1	48 bytes

Bits 2–7 / Unused. Must be set = 0 for proper operation.

11.17.2 HDLC Status and Information

TLS2 provides status information for the transmit HDLC controller. When a particular event has occurred (or is occurring), the appropriate bit in one of these registers will be set to a one. Some of the bits in these registers are latched and some are real-time bits that are not latched. This section contains register descriptions that list which bits are latched and which are real time. With the latched bits, when an event occurs and a bit is set to a one, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again. The real-time bits report the current instantaneous conditions that are occurring and the history of these bits is not latched.

Like the other latched status registers, the user will follow a read of the status bit with a write. The byte written to the register will inform the device which of the latched bits the user wishes to clear (the real time bits are not affected by writing to the status register). The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to clear and a zero in the bit positions he or she does not wish to clear.

The HDLC status register, TLS2 has the ability to initiate a hardware interrupt via the $\overline{INT}$ output signal. Each of the events in this register can be either masked or unmasked from the interrupt pin via the receive HDLC Interrupt Mask Register (TIM2). Interrupts will force the $\overline{INT}$ signal low when the event occurs. The $\overline{INT}$ pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

Register Name: **TRTS2**
Register Description: **Transmit Real-Time Status Register 2 (HDLC)**
Register Address: **1B1h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TEMPTY	TFULL	TLWM	TNF
Default	0	0	0	0	0	0	0	0

All bits in this register are real time.

Bit 0 / Transmit FIFO Not Full Condition (TNF). Set when the transmit 64-byte FIFO has at least one byte available.

Bit 1 / Transmit FIFO Below Low-Watermark Condition (TLWM). Set when the transmit 64-byte FIFO empties below the low watermark as defined by the Transmit Low-Watermark bits (TLWM).

Bit 2 / Transmit FIFO Full (TFULL). A real-time bit that is set high when the FIFO is full.

Bit 3 / Transmit FIFO Empty (TEMPTY). A real-time bit that is set high when the FIFO is empty.

Bits 4–7 / Unused

Register Name: **TLS2**
Register Description: **Transmit Latched Status Register 2 (HDLC)**
Register Address: **191h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TUDR	TMEND	TLWMS	TNFS
Default	0	0	0	0	0	0	0	0

All bits in this register are latched and can create interrupts.

Bit 0 / Transmit FIFO Not Full Set Condition (TNFS). Set when the transmit 64-byte FIFO has at least one empty byte available for write. Rising edge detect of TNF. Indicates change of state from full to not full.

Bit 1 / Transmit FIFO Below Low-Watermark Set Condition (TLWMS). Set when the transmit 64-byte FIFO empties beyond the low watermark as defined by the Transmit Low-Watermark bits (TLWM) (rising edge detect of TLWM).

Bit 2 / Transmit Message End Event (TMEND). Set when the transmit HDLC controller has finished sending a message.

Bit 3 / Transmit FIFO Underrun Event (TUDR). Set when the transmit FIFO empties out without having seen the TMEND bit set. An abort is automatically sent.

Bits 4 to 7 / Unused

Register Name: **TIM2**
Register Description: **Transmit Interrupt Mask Register 2**
Register Address: **1A1h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TUDR	TMEND	TLWMS	TNFS
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit FIFO Not Full Set Condition (TNFS)
0 = interrupt masked
1 = interrupt enabled

Bit 1 / Transmit FIFO Below Low Watermark Set Condition (TLWMS)
0 = interrupt masked
1 = interrupt enabled

Bit 2 / Transmit Message End Event (TMEND)
0 = interrupt masked
1 = interrupt enabled

Bit 3 / Transmit FIFO Underrun Event (TUDR)
0 = interrupt masked
1 = interrupt enabled

Bits 4 to 7 / Unused. Must be set = 0 for proper operation.

11.17.3 FIFO Information

The Transmit FIFO Buffer Available register indicates the number of bytes that can be written into the transmit FIFO. The count form this register informs the host as to how many bytes can be written into the transmit FIFO without overflowing the buffer. This is a real-time register. The count shall remain valid and stable during the read cycle.

Register Name: **TFBA**
Register Description: **Transmit HDLC FIFO Buffer Available**
Register Address: **1B3h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	TFBA6	TFBA5	TFBA4	TFBA3	TFBA2	TFBA1	TFBA0
Default	0	0	0	0	0	0	0	0

Bits 0–6 / Transmit FIFO Bytes Available (TFBAO to TFBA6). TFBA0 is the LSB.

Register Name: **THF**
Register Description: Transmit HDLC FIFO
Register Address: **1B4h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	THD7	THD6	THD5	THD4	THD3	THD2	THD1	THD0
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit HDLC Data Bit 0 (THD0). LSB of a HDLC packet data byte.

Bit 1 / Transmit HDLC Data Bit 1 (THD1)

Bit 2 / Transmit HDLC Data Bit 2 (THD2)

Bit 3 / Transmit HDLC Data Bit 3 (THD3)

Bit 4 / Transmit HDLC Data Bit 4 (THD4)

Bit 5 / Transmit HDLC Data Bit 5 (THD5)

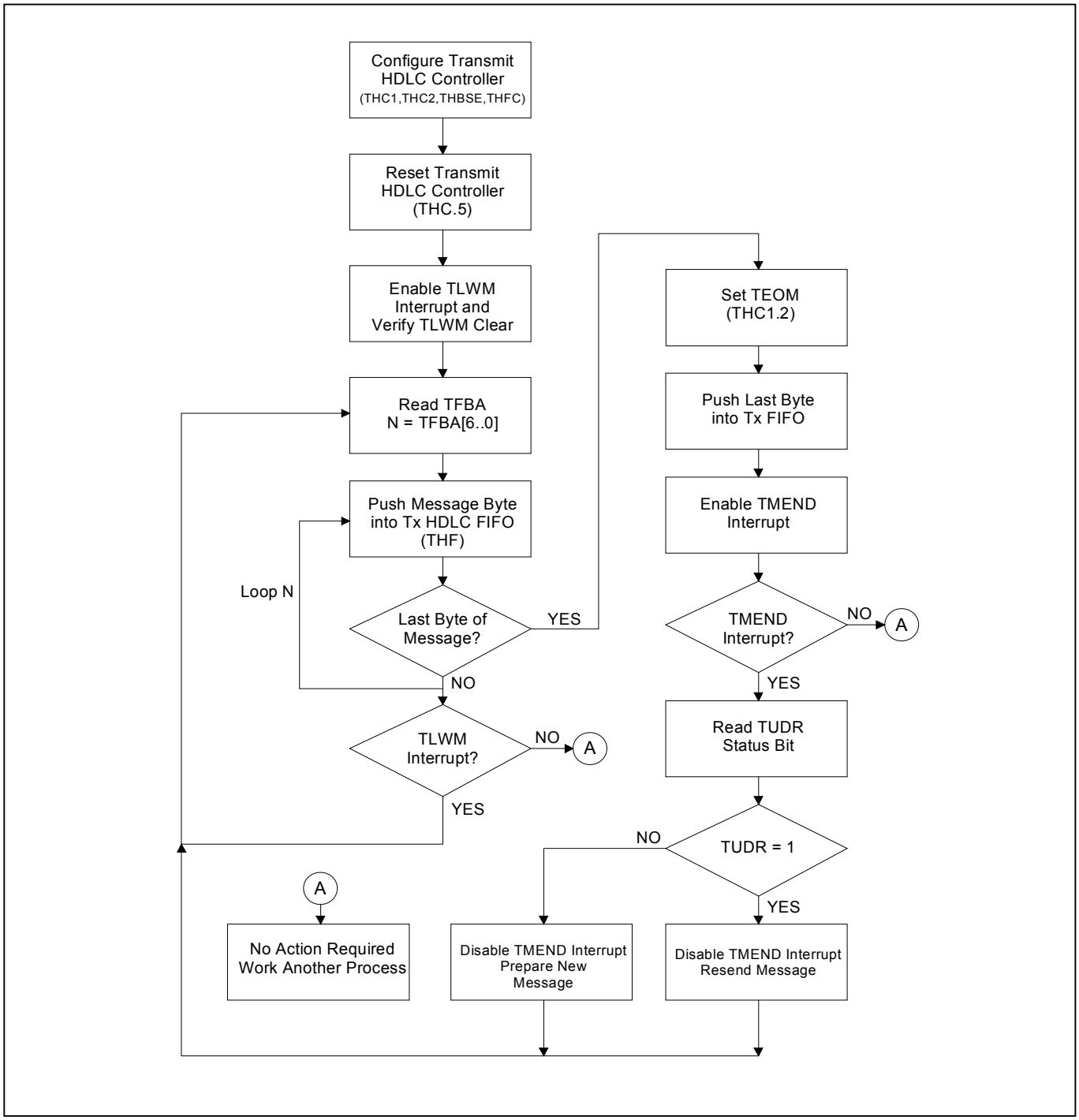
Bit 6 / Transmit HDLC Data Bit 6 (THD6)

Bit 7 / Transmit HDLC Data Bit 7 (THD7). MSB of a HDLC packet data byte.

11.18 HDLC Transmit Example

The HDLC status registers in the DS26401 allow for flexible software interface to meet the user's preferences. When transmitting HDLC messages, the host can choose to be interrupt driven, or to poll to desired status registers, or a combination of polling and interrupt processes may be used. An example routine for using the DS26401 HDLC receiver is given in Figure 11-1.

Figure 11-1. HDLC Message Transmit Example



11.19 Interleaved PCM Bus Operation (IBO)

In many architectures, the PCM outputs of individual framers are combined into higher speed PCM buses to simplify transport across the system backplane. The DS26401 can be configured to allow PCM data to be multiplexed into higher speed buses eliminating external hardware, saving board space and cost. The DS26401 can be configured for channel or frame interleave.

The interleaved PCM bus option (IBO) supports three bus speeds. The 4.096 MHz bus speed allows two PCM data streams to share a common bus. The 8.192 MHz bus speed allows four PCM data streams to share a common bus. The 16.384 MHz bus speed allows 8 PCM data streams to share a common bus. The receive elastic stores of each transceiver must be enabled. Via the IBO register the user can configure each framer for a specific bus position. For all IBO bus configurations each framer is assigned an exclusive position in the high speed PCM bus. The 8kHz frame sync can be generated from the system backplane or from the first device on the bus. All other devices on the bus must have their frame syncs configured as inputs. Relative to this common frame sync, the devices will await their turn to drive or sample the bus according to the settings of the DA0, DA1 and DA2 bits of the TIBOC register.

11.19.1 Channel Interleave

In channel interleave mode data is output to the PCM Data Out bus one channel at a time from each of the connected DS26401s until all channels of frame n from each framer has been placed on the bus. This mode can be used even when the DS26401s are operating asynchronous to each other. The elastic stores will manage slip conditions. The DS26401 provides an active low signal (TIBO_OEB) during bus active times. TIBO_OEB can be used for bus multiplexer or tri-state buffer control.

11.19.2 Frame Interleave

In frame interleave mode data is output to the PCM Data Out bus one frame at a time from each of the framers. This mode is used only when all connected DS26401s are operating in a synchronous fashion (all inbound T1 or E1 lines are synchronous) and are synchronous with the system clock (system clock derived from T1 or E1 line). In this mode, slip conditions are not allowed.

Register Name: **TIBOC**
Register Description: **Transmit Interleave Bus Operation Control Register**
Register Address: **188h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	IBS1	IBS0	IBOSEL	IBOEN	DA2	DA1	DA0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2 / Device Assignment Bits (DA0 to DA2)

DA2	DA1	DA0	Device Position
0	0	0	1st Device on bus
0	0	1	2nd Device on bus
0	1	0	3rd Device on bus
0	1	1	4th Device on bus
1	0	0	5th Device on bus
1	0	1	6th Device on bus
1	1	0	7th Device on bus
1	1	1	8th Device on bus

Bit 3 / Interleave Bus Operation Enable (IBOEN)
0 = Interleave Bus Operation disabled.
1 = Interleave Bus Operation enabled.

Bit 4 / Interleave Bus Operation Select (IBOSEL). This bit selects channel or frame interleave mode.
0 = Channel Interleave
1 = Frame Interleave

Bits 5 to 6 / IBO Bus Size Bit 1 (IBS0 to IBS1). Indicates how many devices on the bus.

IBS1	IBS0	Bus Size
0	0	2 Devices on bus
0	1	4 Devices on bus
1	0	8 Devices on bus
1	1	Reserved for future use

Bit 7 / Unused. Must be set = 0 for proper operation.

11.20 Interfacing the E1 Transmitter to the BERT

Data from the on-chip BERT can be ported to the transmit formatter by using the registers described below. Any single DS0 or combination of DS0s can be inserted into the data stream up to the entire T1 payload as controlled by the RBCS registers.

Note that one BERT resource is shared among all 8 framers. Therefore the TBEN bit should be set for only one framer at a time. If multiple framers have the TBEN bit set, the lower number framer is assigned the resource. Details concerning the on-chip BERT can be found in Section 12.

Register Name: **TBICR**
Register Description: **Transmit BERT Interface Control Register**
Register Address: **18Ah + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	TBDC	—	TBEN
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit BERT Enable (TBEN)
0 = Transmit BERT is not assigned to this framer
1 = Transmit BERT is assigned to this framer

Bits 1, 3 to 7 / Unused. Must be set = 0 for proper operation.

Bit 2 / Transmit BERT Direction Control (TBDC)
0 = Transmit Path: The BERT transmits toward the network via the TPOS and TNEG pins.
1 = Backplane: The BERT transmits toward the system backplane via the RSER pin.

Register Name: **TBCS1, TBCS2, TBCS3, TBCS4**
Register Description: **Transmit BERT Channel Select Registers**
Register Address: **1D4h, 1D5h, 1D6h, 1D7h [+ (200h x n) : where n = 0 to 7, for Ports 1 to 8]**

Setting any of the CH1 through CH32 bits in the TBCS1 through TBCS4 registers will map data into those channels from the on-board BERT. TBEN must be set to one for these registers to have effect. Multiple, or all channels may be selected simultaneously. These registers work with the transmit-side framer only.

(MSB)							**(LSB)**	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	**TBCS1**
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	**TBCS2**
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	**TBCS3**
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	**TBCS4**

Register Name: **TBBS**
Register Description: **Transmit BERT Bit Suppress Register**
Register Address: **18Bh**

Bit #	7	6	5	4	3	2	1	0
Name	BSE8	BSE7	BSE6	BSE5	BSE4	BSE3	BSE2	BSE1
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Channel Bit 1 Suppress (BSE1). LSB of the channel. Set to one to stop this bit from being used.

Bit 1 / Transmit Channel Bit 2 Suppress (BSE2). Set to one to stop this bit from being used.

Bit 2 / Transmit Channel Bit 3 Suppress (BSE3). Set to one to stop this bit from being used.

Bit 3 / Transmit Channel Bit 4 Suppress (BSE4). Set to one to stop this bit from being used.

Bit 4 / Transmit Channel Bit 5 Suppress (BSE5). Set to one to stop this bit from being used.

Bit 5 / Transmit Channel Bit 6 Suppress (BSE6). Set to one to stop this bit from being used.

Bit 6 / Transmit Channel Bit 7 Suppress (BSE7). Set to one to stop this bit from being used.

Bit 7 / Transmit Channel Bit 8 Suppress (BSE8). MSB of the channel. Set to one to stop this bit from being used.

11.21 E1 Transmit Synchronizer

The DS26401 transmitter has the ability to identify the E1 frame boundary, as well as the CRC multiframe boundaries within the incoming NRZ data stream at TSER. Control signals for the transmit synchronizer are located in the TSYNCC register. The Transmit Synchronizer Status (TSYNCS) register provides a latched status bit (LOFD) to indicate that a loss-of-frame synchronization has occurred, and a real-time bit (LOF) which is set high when the synchronizer is searching for frame/multiframe alignment. The LOFD bit can be enabled to cause an interrupt condition on $\overline{INT}$.

Note that when the transmit synchronizer is used, the TSYNC signal should be set as an output (TSIO = 1) and the recovered frame sync pulse will be output on this signal. The recovered CRC4 multiframe sync pulse will be output if enabled with TIOCR.0 (TSM = 1). The transmit synchronizer cannot be used while the transmit elastic store is enabled.

Register Name: **TSYNCC**
Register Description: **Transmit Synchronizer Control Register**
Register Address: **18Eh + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	CRC4	TSEN	SYNCE	RESYNC
Default	0	0	0	0	0	0	0	0

Bit 0 / Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the transmit-side framer is initiated. Must be cleared and set again for a subsequent resync.

Bit 1 / Sync Enable (SYNCE)
0 = auto resync enabled
1 = auto resync disabled

Bit 2 / Transmit Synchronizer Enable (TSEN)
0 = transmit synchronizer disabled
1 = transmit synchronizer enabled

Bit 3 / CRC4 Enable (RCRC4)
0 = CRC4 disabled
1 = CRC4 enabled

Bits 4 to 7 / Unused. Must be set = 0 for proper operation.

Register Name: **TLS3**
Register Description: **Transmit Latched Status Register 3 (Synchronizer)**
Register Address: **192h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	LOF	LOFD
Default	0	0	0	0	0	0	0	0

Bit 0 / Loss-of-Frame Synchronization Detect (LOFD). This latched bit is set when the transmit synchronizer is searching for the sync pattern in the incoming data stream.

Bit 1 / Loss of Frame (LOF). A real-time bit that indicates that the transmit synchronizer is searching for the sync pattern in the incoming data stream.

Bits 2 to 7 / Unused

Register Name: **TIM3**
Register Description: **Transmit Interrupt Mask Register 3 (Synchronizer)**
Register Address: **1A2h + (200h x n) : where n = 0 to 7, for Ports 1 to 8**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	LOFD
Default	0	0	0	0	0	0	0	0

Bit 0 / Loss-of-Frame Synchronization Detect (LOFD)
0 = Interrupt masked
1 = Interrupt enabled

Bits 1 to 7 / Unused. Must be set = 0 for proper operation.

12. BERT

12.1 BERT Registers

ADDRESS	NAME	TYPE	FUNCTION	PAGE
2F0	BCR1	R/W	BERT Control Register 1	267
2F1	BCR2	R/W	BERT Control Register 2	268
2F2	BCR3	R/W	BERT Control Register 3	269
2F3	BCR4	R/W	BERT Control Register 4	270
2F4	BSR	R	BERT Status Register	271
2F5	BTSR1	R/W	BERT Tap/Seed Register 1	272
2F6	BTSR2	R/W	BERT Tap/Seed Register 2	272
2F7	BTSR3	R/W	BERT Tap/Seed Register 3	272
2F8	BTSR4	R/W	BERT Tap/Seed Register 4	272
2F9	BTR	R/W	BERT TEST Register	264
2FA	BCNT1	R	BERT Count Register 1	274
2FB	BCNT2	R	BERT Count Register 2	274
2FC	BCNT3	R	BERT Count Register 3	274
2FD	BCNT4	R	BERT Count Register 4	274
2FE	BCNT5	R	BERT Count Register 5	274
2FF	BCNT6	R	BERT Count Register 6	274

12.2 BERT Description and Operation

The DS26401 contains a full-feature BERT (bit error-rate tester) that can be enabled for use with any T1/E1 port of the device. The on-chip BERT can generate and detect both pseudorandom and repeating bit patterns.

The BERT block can generate and detect the following patterns:

- Maximal-length pseudorandom patterns up to 2^{32} - 1
- Repetitive patterns in any length up to 512 octets
- QRSS pattern per T1.403

The BERT function is assigned on a per-channel basis for both the transmitter and receiver. This is accomplished by using the BERT expansion port control and channel select registers within the DS26401. Using this function, the BERT pattern can be transmitted and/or received in single or across multiple DS0s, contiguous or broken. Transmit and receive bandwidth assignments are independent of each other. The BERT resource is shared between the eight framers of the DS26401, and the BERT transmitter and receiver can be independently assigned to different ports of the octal framer if desired.

BSR contains the status information on the BERT function. The host can be alerted when there is a change of state of the BERT via this register. A major change of state is defined as either a change in the receive synchronization (i.e., the BERT has gone into or out of receive synchronization), a bit error has been detected, or an overflow has occurred in either the Bit Counter or the Error Counter. The host must read the BERT Status Register (BSR) to determine the change of state.

12.3 Pattern Generation

12.3.1 Polynomial Generation

The internal BERT has a 32-bit TAP register (BTR) used to tap up to 32 bits in the feedback path of the polynomial generator. The BERT also contains a 32-bit Seed register used to preset the polynomial generator with an initial value. The Seed values are latched on the rising edge of the TL control bit in BCR1.

The internal BERT can generate polynomial patterns of any length up to and including 2^{32} - 1. All the industry standard polynomials can be programmed using the control registers (some examples are given in Table 16-1). The polynomial is generated using a shift register of programmable length and programmable feed back tap positions. The user has access to all combination of pattern length and pattern tap locations to generate industry standard polynomials or other combinations as well. In addition, the QRSS pattern described in T1.403 is supported by setting the QRSS bit in BCR1. The T1.403 QRSS pattern is the polynomial 2^{20} - 1 with the additional requirement that "an output bit is forced to ONE whenever the next 14 bits are ZERO."

12.3.2 Repetitive Pattern Generation

In addition to polynomial patterns, the BERT can generate repetitive patterns of considerable length. The host has access to 512 bytes of memory for storing pattern. The End Repetitive Address registers (04h, and 05h) are used to program the length of the pattern itself. Memory is addressed indirectly and is used to store the pattern. Data can be sent MSB or LSB first as it appears in the memory.

Repetitive patterns can include simple patterns such as 3 in 24, but the additional memory can be used to store patterns such as DDS-n patterns or T1-n patterns. Repetitive patterns are stored in increments of 8 bits. In order to generate a repetitive pattern that is 12 bits long (3 nibbles), the pattern is written twice such that the pattern is 24 bits long (3 bytes), and repeats twice in memory. The same is true when the device is used in serial mode, a 5-bit pattern is written to memory 5 times. For example:

To generate a 00001 pattern at the serial output:
Write these bytes to memory:

RAM ADDRESS	BINARY CODE	HEX CODE
00h	00010000	10h
01h	01000010	42h
02h	00001000	08h
03h	00100001	21h
04h	10000100	84h

12.4 Pattern Synchronization

12.4.1 Synchronization

The receiver synchronizes to the same pattern that is being transmitted. The pattern must be error-free when the synchronizer is on line.

12.4.1.1 Polynomial Synchronization

Synchronization to polynomial patterns takes 50 + n clock cycles, where *n* is the exponent in the polynomial that describes the pattern. Once synchronized, any bit that does not match the polynomial is counted as a bit error.

12.4.1.2 Repetitive Pattern Synchronization

Synchronization to repetitive patterns can take several complete repetitions of the entire pattern. The actual sync time depends on the nature of the pattern and the location of the synchronization pointer. Errors that occur during synchronization could affect the sync time; at least one complete error-free repetition must be received before synchronization is declared. Once synchronized, any bit that does not match the pattern that is programmed in the on-board RAM is counted as a bit error.

12.5 BER Calculation

12.5.1 Counters

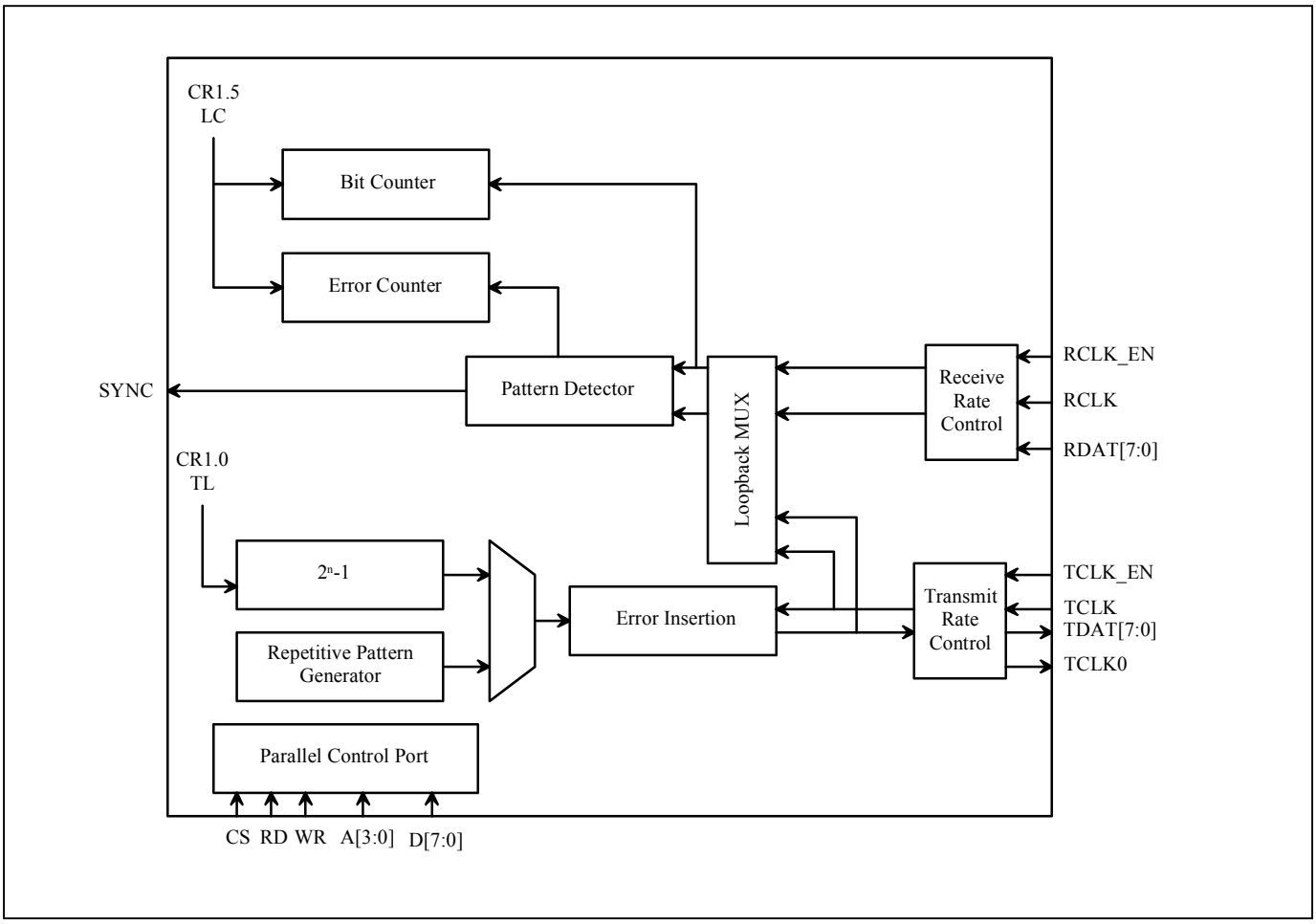
The bit counter is active at all times. Once synchronized, the error counters come on line. The receiver has large 48-bit count registers. These counters accumulate for 50,640 hours at the T1 line rate, 1.544MHz, and 38,170 hours at the E1 line rate, 2.048MHz.

To accumulate BER data, the user toggles the LC bit at T = 0. This clears the accumulators and loads the contents into the count registers. At T = 0, these results should be ignored. At this point, the device is counting bits and bit errors. At the end of the specified time interval, the user toggles the LC bit again and reads the count registers. These are the valid results used to calculate a bit-error rate.

12.6 Error Generation

The BERT can insert bit errors at a particular rate by setting the error insertion bits in Control Register 2. Injecting errors allows users to stress communication links and to check the functionality of error monitoring equipment along the path. In addition, the device can insert errors on command by setting the SBE bit in Control Register 2. The bit that occurs after the rising edge of the SBE insert bit is inverted. In the case of the QRSS pattern, this could result in a string of zeros longer than 14 bits; the DS26104 delays the erred bit by one clock cycle.

Figure 12-1. Shared BERT Block Diagram



12.7 BERT Control Registers

Register Name: **BCR1**
Register Description: **BERT Control Register 1**
Register Address: **2F0h**

Bit #	7	6	5	4	3	2	1	0
Name	BSYNCE	BRESYNC	LC	LPBK	QRSS	PS	LSB	TL
Default	0	0	0	0	0	0	0	0

Bit 0 / Transmit Load (TL). A rising edge causes the transmit shift register to be loaded with the seed value.

Bit 1 / LSB/MSB (LSB)
0 = Repetitive Pattern data is transmitted/received MSB first.
1 = Repetitive Pattern data is transmitted/received LSB first.

Bit 2 / Pattern Select (PS)
0 = Pseudorandom pattern.
1 = Repetitive pattern.

Bit 3 / Zero Suppression Select (QRSS). Forces a 1 into the pattern whenever the next 14 bit positions are all 0s. Should only be set when using the QRSS pattern.
0 = Disable 14 zero suppression.
1 = Enable 14 zero suppression per T1.403.

Bit 4 / Transmit/Receive Loopback Select (LPBK)
0 = Loop back disabled.
1 = Loop back enabled.

Bit 5 / Latch Count Registers (LC). A rising edge copies the bit count and bit error count accumulators to the appropriate registers. The accumulators are then cleared.

Bit 6 / Initiate Manual Resync Process (BRESYNC). A rising edge causes the device to go out of sync and begin resynchronization process.

Bit 7 / BERT SYNC Enable (BSYNCE)
0 = Auto resync enabled.
1 = Auto resync disabled.

Register Name: **BCR2**
Register Description: **BERT Control Register 2**
Register Address: **2F1h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TINV	RINV	SBE	EIR2	EIR1	EIR0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2 / Error Insert Bits 0 to 2 (EIB0 to EIB2). Will automatically insert bit errors at the prescribed rate into the generated data pattern. Can be used for verifying error detection features.

EIB2	EIB1	EIB0	Error Rate Inserted
0	0	0	No errors automatically inserted
0	0	1	10E-1
0	1	0	10E-2
0	1	1	10E-3
1	0	0	10E-4
1	0	1	10E-5
1	1	0	10E-6
1	1	1	10E-7

Bit 3 / Single Bit Error Insert (SBE). A low-to-high transition creates a single bit error. Must be cleared and set again for a subsequent bit error to be inserted.

Bit 4 / Receive Invert Data Enable (RINV)
0 = do not invert the incoming data stream
1 = invert the incoming data stream

Bit 5 / Transmit Invert Data Enable (TINV)
0 = do not invert the outgoing data stream
1 = invert the outgoing data stream

Bits 6, 7 / Unused. Must be set = 0 for proper operation.

Register Name: **BCR3**
Register Description: **BERT Control Register 3**
Register Address: **2F2h**

Bit #	7	6	5	4	3	2	1	0
Name	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0
Default	0	0	0	0	0	0	0	0

Bit 0 / Pattern Length Bit 0 (PL0). Bit 0 of [8:0] end address of repetitive pattern data.

Bit 1 / Pattern Length Bit 1 (PL1). Bit 1 of [8:0] end address of repetitive pattern data.

Bit 2 / Pattern Length Bit 2 (PL2). Bit 2 of [8:0] end address of repetitive pattern data.

Bit 3 / Pattern Length Bit 3 (PL3). Bit 3 of [8:0] end address of repetitive pattern data.

Bit 4 / Pattern Length Bit 4 (PL4). Bit 4 of [8:0] end address of repetitive pattern data.

Bit 5 / Pattern Length Bit 5 (PL5). Bit 5 of [8:0] end address of repetitive pattern data.

Bit 6 / Pattern Length Bit 6 (PL6). Bit 6 of [8:0] end address of repetitive pattern data.

Bit 7 / Pattern Length Bit 7 (PL7). Bit 7 of [8:0] end address of repetitive pattern data.

Register Name: **BCR4**
Register Description: **BERT Control Register 4**
Register Address: **2F3h**

Bit #	7	6	5	4	3	2	1	0
Name	TEST	TEST	CLKINV	R/W	RAM	COUNT	SEED	PL8
Default	0	0	0	0	0	0	0	0

Bit 0 / Pattern Length Bit 8 (PL8). Bit 8 (MSB) of [8:0] end address of repetitive pattern data.

Bit 1 / Select Bit for Tap/Seed Registers (SEED)
0 = Registers 0F5h – 0F8h refer to Tap Select registers.
1 = Registers 0F5h – 0F8h refer to Pre-load Seed registers.

Bit 2 / Select Bit for Registers Counter Registers (COUNT)
0 = Registers 0FAh – 0FFh refer to Bit Count Registers.
1 = Registers 0FAh – 0FFh refer to Error Count Registers.

Bit 3 / RAM Select (RAM). This bit should be set when repetitive pattern data is being loaded into the RAM.
0 = BERT state machine has control of the RAM.
1 = Parallel port has read and write access to the RAM.

Bit 4 / Read/Write Select (R/W). This bit is used with the RAM bit to read or write the RAM.
0 = Write to the RAM.
1 = Read from the RAM.

Bit 5 / TCLKO Invert (CLKINV)
0 = TCLKO polarity is normal.
1 = TCLKO polarity is inverted.

Bits 6, 7 / Factory use; must be set to zero.

12.8 BERT Status Register

The Status register contains information on the current real-time status of the BERT. When a particular event has occurred, the appropriate bit in the register is set to 1. All the bits in this register (except for BSYNC) operate in a latched fashion. This means that if an event occurs and a bit is set to a 1, it remains set until the user reads the register. For the BED, BCOF, and BECOF bits, they are cleared when read and are not set again until the event has occurred again. For RLOS, RA0, and RA1 bits, they are cleared when read if the condition no longer persists.

Register Name: **BSR**
Register Description: **BERT Status Register**
Register Address: **2F4h**

Bit #	7	6	5	4	3	2	1	0
Name	—	BRA1	BRA0	BED	BECOF	BCOF	BRLOS	BSYNC
Default	0	0	0	0	0	0	0	0

Bit 0 / BERT in Synchronization Condition (BSYNC). A real-time bit that reports the BERT's synchronization status.

Bit 1 / BERT Receive Loss of Sync (BRLOS). Set when the receiver is searching for synchronization. Once sync is achieved, this bit remains set until read. This bit is latched.

Bit 2 / Bit Counter Overflow (BCOF). Set when the bit counter overflows. Cleared when read.

Bit 3 / Bit Error Count Overflow (BECOF). Set when the bit error counter overflows. Cleared when read.

Bit 4 / Bit Error Detection (BED). Set when bit error count is non-zero. Cleared when read.

Bit 5 / BERT Receive All Zeros (BRA0). Set when 40 consecutive zeros are received in pseudorandom mode. Allowed to be cleared when a one is received.

Bit 6 / BERT Receive All Ones (BRA1). Set when 40 consecutive ones are received in pseudorandom mode. Allowed to be cleared when a zero is received.

Bit 7 / Unused. Must be set = 0 for proper operation.

12.9 Pseudorandom Pattern Registers

Bit 1 of Control Register 4 determines if the addresses point to the Tap Select or Seed registers.

The Tap Select register is used to select the length and tap positions for pseudorandom generation/reception. Each bit that is set to 1 denotes a tap at that location for the feedback path. The highest bit location set to 1 is the length of the shift register.

For example, to transmit/receive 2^{15} - 1 (O.151) BIT14 and BIT13 would be set to 1. All other bits would be 0. Table 12-1 gives Tap Select and Seed Values for many pseudorandom patterns.

The Seed Value is loaded into the transmit shift register on the rising edge of TL (CR1.0).

Register Name: **BTSR1, BTSR2, BTSR3, BTSR4**
Register Description: **BERT Tap/Seed Registers**
Register Address: **2F5h, 2F6h, 2F7h, 2F8h**

(MSB)							**(LSB)**	
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	**BTSR1**
BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	**BTSR2**
BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16	**BTSR3**
BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	**BTSR4**

Bits 0 to 7 / BERT Tap / Seed Register Bits 0 to 31
0 = do not select a tap at this bit location / seed value = 0 for this bit position
1 = do select a tap at this bit location / seed value = 1 for this bit position

Table 12-1. Pseudo-Random Pattern Generation

PATTERN TYPE	TAP1	TAP2	TAP3	TAP4	SEED1/2/3/4	TINV	RINV
2^3-1	05	00	00	00	FF	0	0
2^4-1	09	00	00	00	FF	0	0
2^5-1	12	00	00	00	FF	0	0
2^6-1	30	00	00	00	FF	0	0
2^7-1 Fractional T1 LB Activate	48	00	00	00	FF	0	0
2^7-1 Fractional T1 LB Deactivate	48	00	00	00	FF	1	1
2^7-1	41	00	00	00	FF	0	0
2^8-1 Maximal Length	B8	00	00	00	FF	0	0
2^9-1 O.153 (511 Type)	10	01	00	00	FF	0	0
2^{10}-1	40	02	00	00	FF	0	0
2^{11}-1 O.152 and O.153 (2047 Type)	00	05	00	00	FF	0	0
2^{12}-1 Maximal Length	29	08	00	00	FF	0	0
2^{13}-1 Maximal Length	0D	10	00	00	FF	0	0
2^{14}-1 Maximal Length	15	20	00	00	FF	0	0
2^{15}-1 O.151	00	60	00	00	FF	1	1
2^{16}-1 Maximal Length	08	D0	00	00	FF	0	0
2^{17}-1	04	00	01	00	FF	0	0
2^{18}-1	40	00	02	00	FF	0	0
2^{19}-1 Maximal Length	23	00	04	00	FF	0	0
2^{20}-1 O.153	04	00	08	00	FF	0	0
2^{20}-1 T1.403 QRSS (CR1.3 = 1)	00	00	09	00	FF	0	0
2^{21}-1	02	00	10	00	FF	0	0
2^{22}-1	01	00	20	00	FF	0	0
2^{23}-1 O.151	00	00	42	00	FF	1	1
2^{24}-1 Maximal Length	00	00	E1	00	FF	0	0
2^{25}-1	04	00	00	01	FF	0	0
2^{26}-1 Maximal Length	23	00	00	02	FF	0	0
2^{27}-1 Maximal Length	13	00	00	04	FF	0	0
2^{28}-1	04	00	00	08	FF	0	0
2^{29}-1	02	00	00	10	FF	0	0
2^{30}-1 Maximal Length	29	00	00	20	FF	0	0
2^{31}-1	04	00	00	40	FF	0	0
2^{32}-1 Maximal Length	03	00	20	80	FF	0	0

12.10 Count Registers

*Bit 2 of Control Register 4 determines if the addresses point to the Bit Count or Error Count registers.

The Bit Count registers comprise a 48-bit count of bits (actually RCLK cycles) received. C47 is the MSB of the 48-bit count. The bit counter increments for each cycle of RCLK when RCLK_EN is high. The bit counter is enabled regardless of synchronization. The Status Register bit BCOF is set when this 48-bit register overflows. The counter rolls over upon an overflow condition. The DS2174 latches the bit count into the Bit Count registers and clears the internal bit count when the LC bit in Control Register 1 is toggled from low to high.

The Error Count registers maintain a 48-bit count of bits received in error. The bit error counter is disabled during loss of SYNC. C47 is the MSB of the 48-bit count. The Status register bit BECOF is set when this 48-bit register overflows. The counter rolls over upon an overflow condition. The DS2174 latches the bit count into the Bit-Error Count registers and clears the internal bit-error count when the LC bit in Control Register 1 is toggled from low to high.

An external processor uses the bit count and bit-error count to compute the BER performance on a loop or channel basis.

Register Name: **BCNT1, BCNT2, BCNT3, BCNT4, BCNT5, BCNT6**
Register Description: **BERT Count Registers**
Register Address: **2FAh, 2FBh, 2FCh, 2FDh, 2FEh, 2FFh**

(MSB)							**(LSB)**	
C7	C6	C5	C4	C3	C2	C1	C0	**BCNT1**
C15	C14	C13	C12	C11	C10	C9	C8	**BCNT2**
C23	C22	C21	C20	C19	C18	C17	C16	**BCNT3**
C31	C30	C29	C28	C27	C26	C25	C24	**BCNT4**
C39	C38	C37	C36	C35	C34	C33	C32	**BCNT5**
C47	C46	C45	C44	C43	C42	C41	C40	**BCNT6**

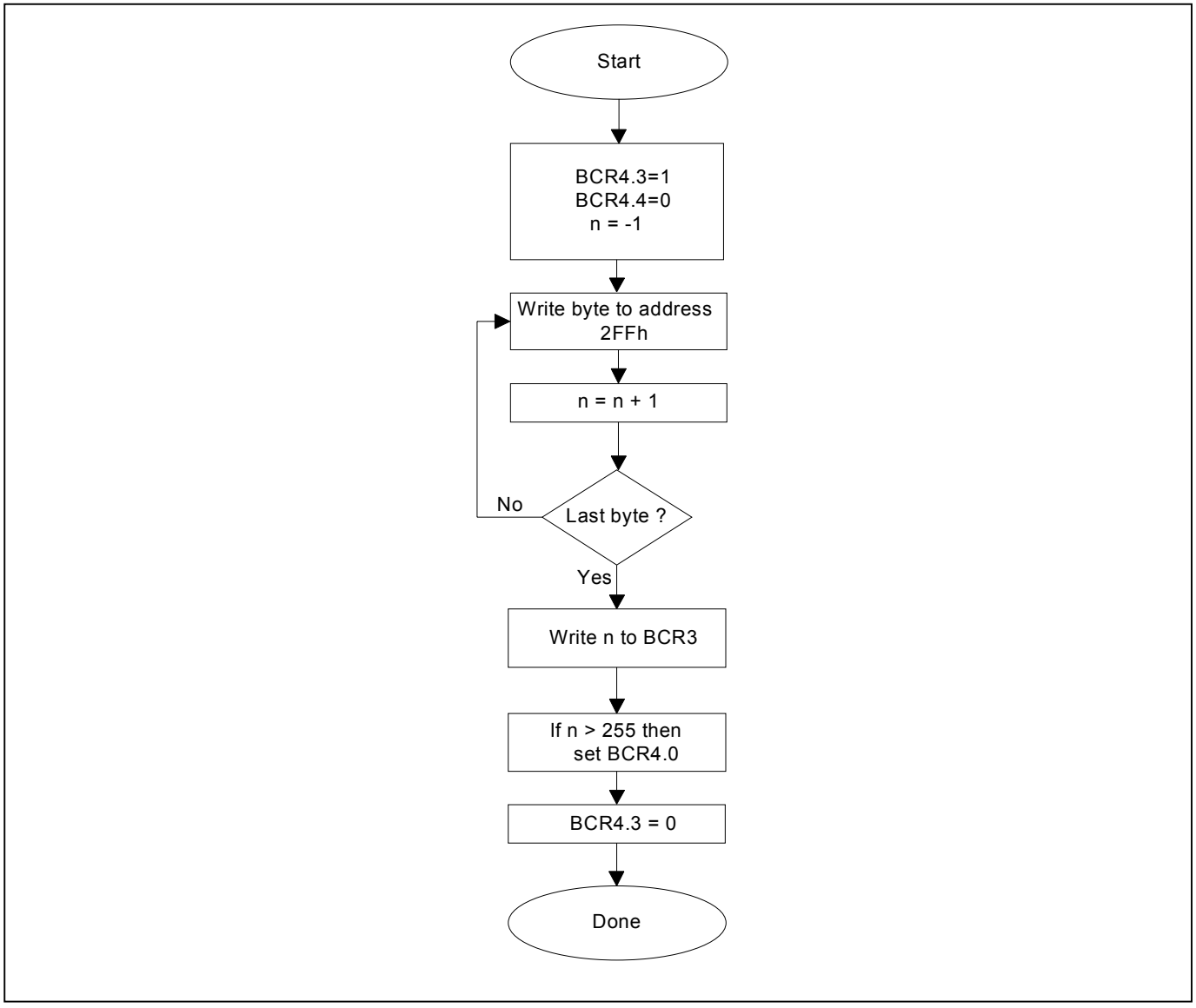
Bits 0 to 7 / BERT Count Register Bits 0 to 47
0 = do not select a tap at this bit location / seed value = 0 for this bit position
1 = do select a tap at this bit location / seed value = 1 for this bit position

12.11 RAM Access

512 bytes of memory are available for repetitive patterns. This memory is addressed indirectly. Data bytes are loaded one at a time into the Indirect Address register at address 2FFh. The RAM mode control bit, BCR4.3, determines the access to the RAM. If BCR4.3 = 0, the RAM is under control of the BERT state machine. If BCR4.3 = 1, then the RAM is under the control of the parallel port. BCR4.3 = 1 is the topic of this discussion.

The accompanying flowchart describes the algorithm used to write repetitive patterns to the RAM. The programmer initializes a counter (n) to -1 in software, then sets BCR4.3 and clears BCR4.4. The rising edge of BCR4.3 resets the RAM address pointer to address 00h. Address 0FFh becomes the indirect access port to the RAM. A write cycle on the parallel port to address 2FFh writes to the address in RAM pointed to by the address pointer. The end of the write cycle, rising edge of WR, will increment the address pointer. The programmer then increments the counter (n) by 1 and loops until the pattern load is complete. Clear BCR4.3 to return control of the RAM to the BERT state machine. Finally, write the value in the counter (n) back to address 2F4h and 2F5h to mark the last address of the pattern in memory.

The RAM contents can be verified by executing the same algorithm, replacing the parallel port write with a read and setting BCR4.4. BCR4.3 must remain set for the entire algorithm to properly increment the address pointer.



13. FUNCTIONAL TIMING

13.1 Delays

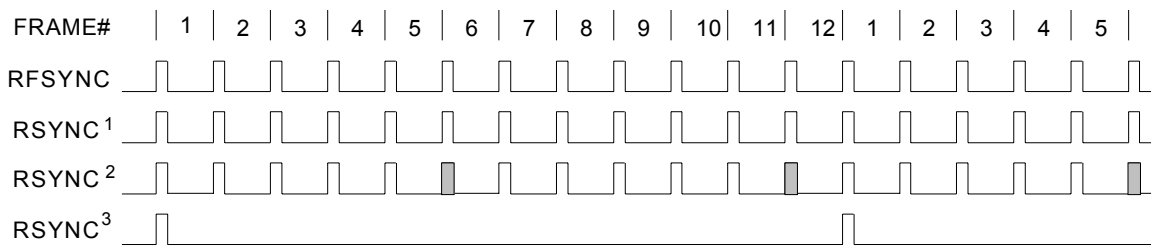
Table 13-1 shows the delay through the framer with the elastic disabled. With the elastic stores enabled, the delay will be what is shown in the table, plus a variable amount depending on the pointer positions in the elastic store.

Table 13-1. Throughput Delays

MODE	DELAY
T1 Receive Path	11 RCLKs
T1 Transmit Path	16 TCLKs
E1 Receive Path	6 RCLKs
E1 Transmit Path	12 TCLKs

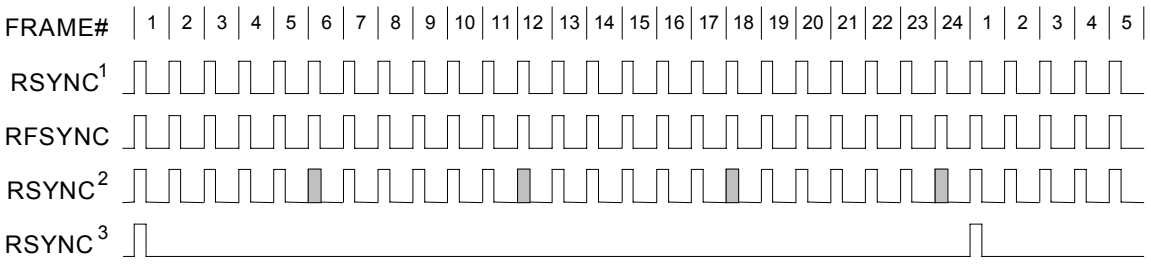
13.2 T1 Receiver Functional Timing Diagrams

Figure 13-1. T1 Receive-Side D4 Timing



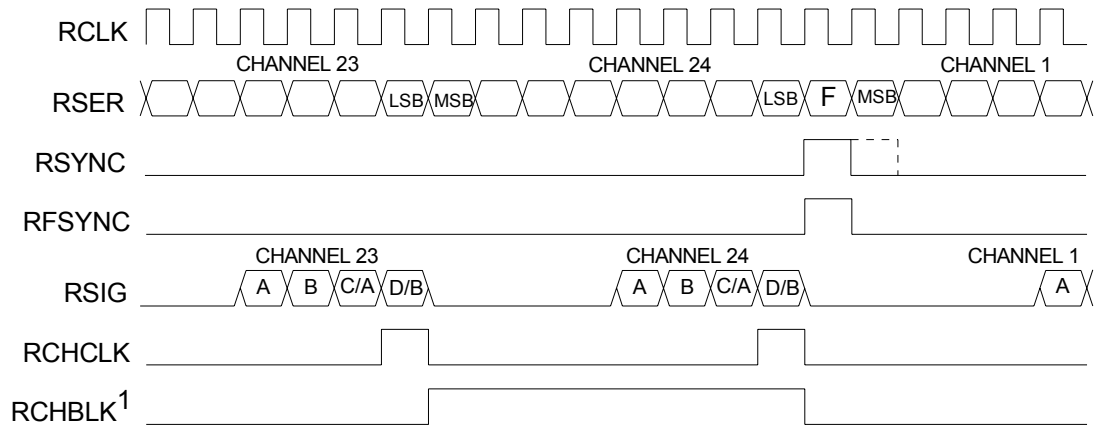
NOTE 1: RSYNC IN THE FRAME MODE (RIOCR.0 = 0) AND DOUBLEWIDE FRAME SYNC IS NOT ENABLED (RIOCR.1 = 0).
NOTE 2: RSYNC IN THE FRAME MODE (RIOCR.0 = 0) AND DOUBLEWIDE FRAME SYNC IS ENABLED (RIOCR.1 = 1).
NOTE 3: RSYNC IN THE MULTIFRAME MODE (RIOCR.0 = 1).

Figure 13-2. T1 Receive-Side ESF Timing



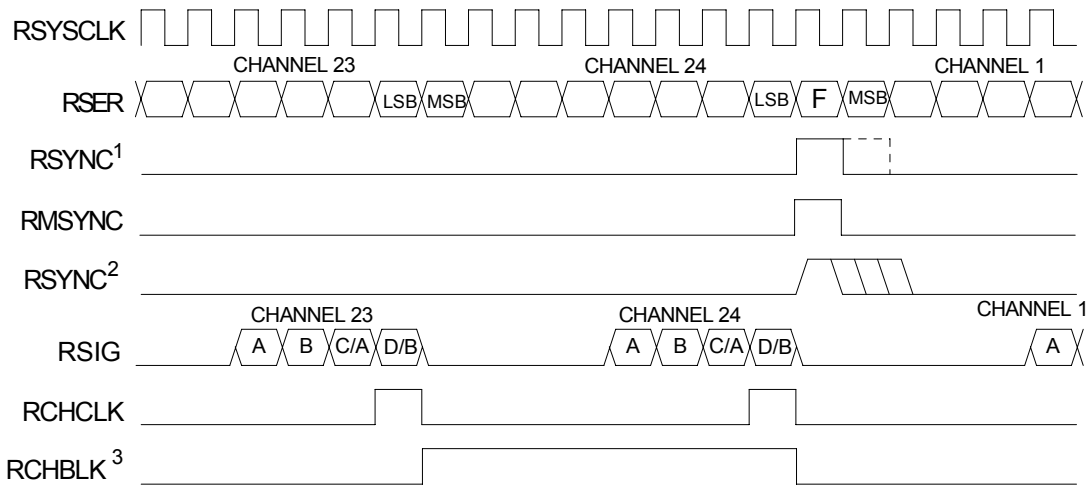
NOTE 1: RSYNC IN FRAME MODE (RIOCR.0 = 0) AND DOUBLE -WIDE FRAME SYNC IS NOT ENABLED (RIOCR.1 = 0).
NOTE 2: RSYNC IN FRAME MODE (RIOCR.0 = 0) AND DOUBLE- WIDE FRAME SYNC IS ENABLED (RIOCR.1 = 1).
NOTE 3: RSYNC IN MULTIFRAME MODE (RIOCR.0 = 1).

Figure 13-3. T1 Receive-Side Boundary Timing (Elastic Store Disabled)



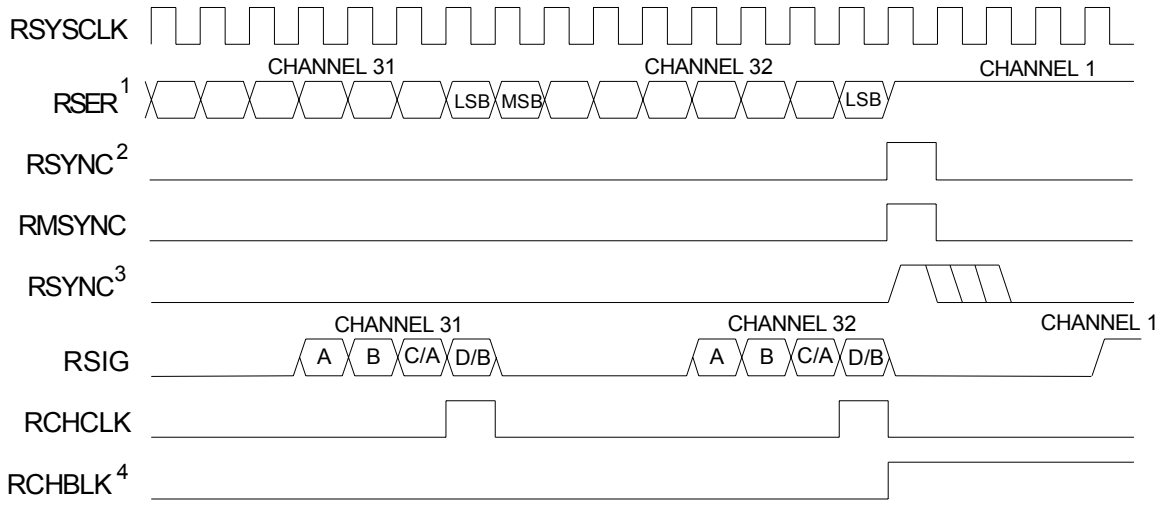
NOTE 1: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 24.

Figure 13-4. T1 Receive-Side 1.544MHz Boundary Timing (Elastic Store Enabled)



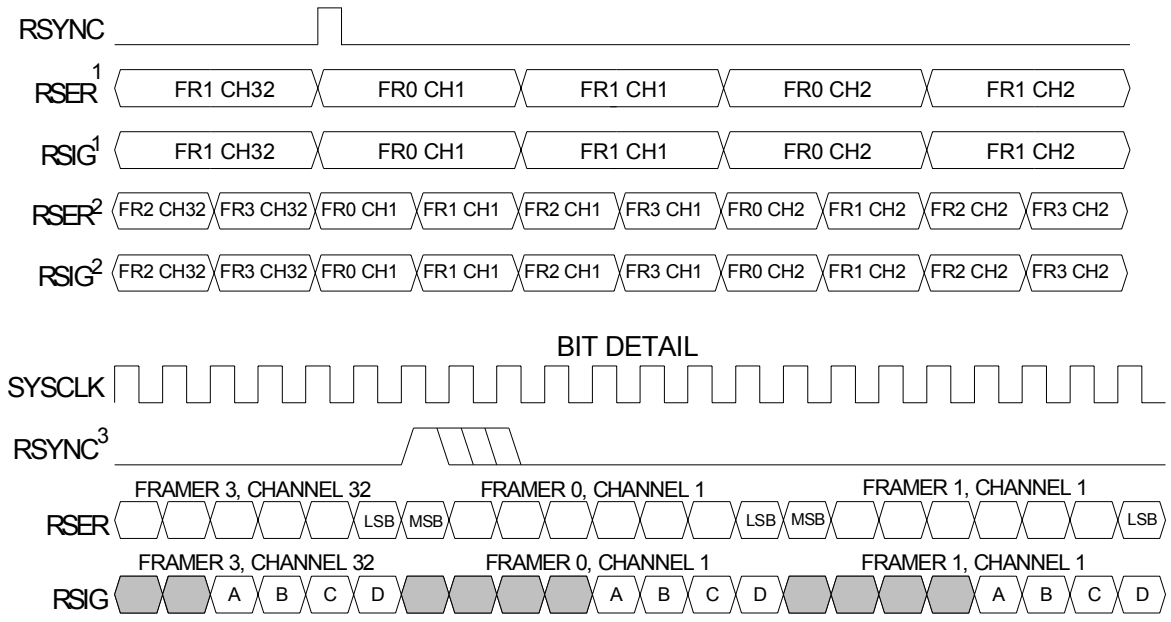
NOTE 1: RSYNC IS IN OUTPUT MODE (RIOCR.2 = 0).
NOTE 2: RSYNC IS IN INPUT MODE (RIOCR.2 = 1).
NOTE 3: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 24.

Figure 13-5. T1 Receive-Side 2.048MHz Boundary Timing (Elastic Store Enabled)



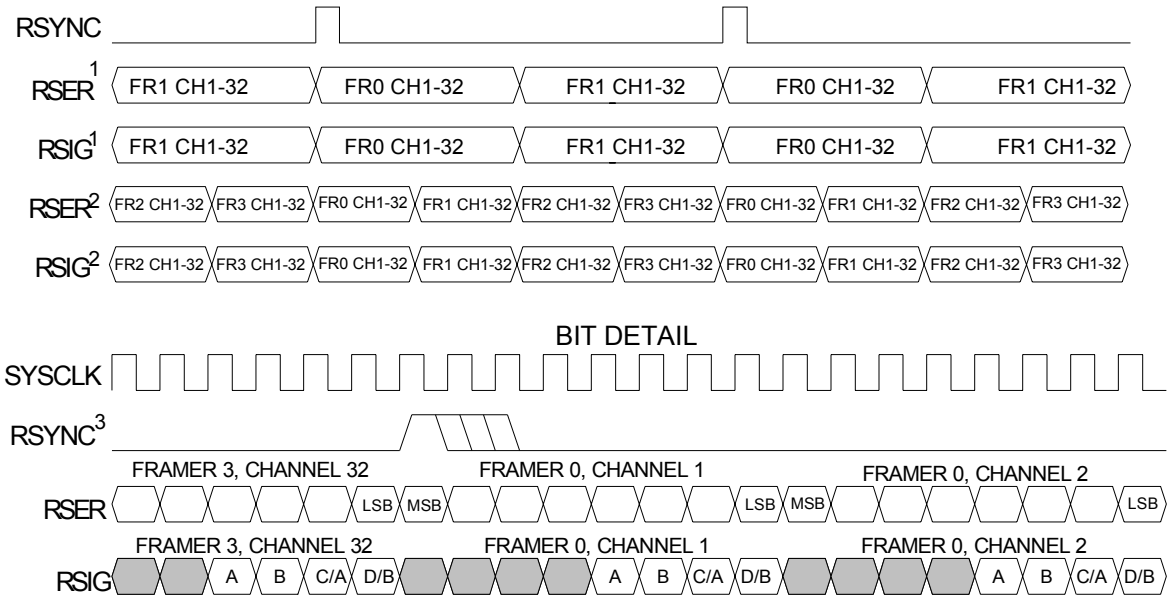
NOTE 1: RSER DATA IN CHANNELS 1, 5, 9, 13, 17, 21, 25, AND 29 ARE FORCED TO 1.
NOTE 2: RSYNC IS IN OUTPUT MODE (RIOCR.2 = 0).
NOTE 3: RSYNC IS IN INPUT MODE (RIOCR.2 = 1).
NOTE 4: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 1.
NOTE 5: THE F-BIT POSITION IS PASSED THROUGH THE RECEIVE-SIDE ELASTIC STORE.

Figure 13-6. T1 Receive-Side Interleave Bus Operation, BYTE Mode



NOTE 1: 4.096MHz BUS CONFIGURATION.
NOTE 2: 8.192MHz BUS CONFIGURATION.
NOTE 3: RSYNC IS IN INPUT MODE (RIOCR.2 = 0).
NOTE 4: SHOWS SYSTEM IMPLEMENTATION WITH MULTIPLE 31IP02 CORES DRIVING BACKPLANE.
NOTE 5: THOUGH NOT SHOWN, TCHCLK CONTINUES TO MARK THE CHANNEL LSB FOR THE FRAMER'S ACTIVE PERIOD.
NOTE 6: THOUGH NOT SHOWN, TCHBLK CONTINUES TO MARK THE BLOCKED CHANNELS FOR THE FRAMERS ACTIVE PERIOD.

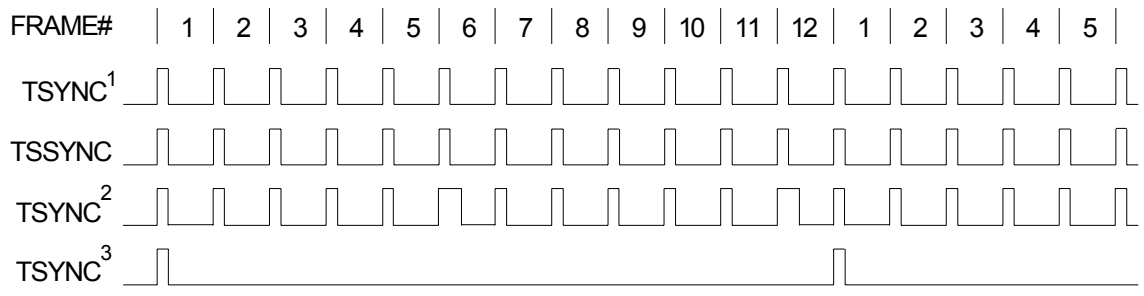
Figure 13-7. T1 Receive-Side Interleave Bus Operation, FRAME Mode



NOTE 1: 4.096MHz BUS CONFIGURATION.
NOTE 2: 8.192MHz BUS CONFIGURATION.
NOTE 3: RSYNC IS IN THE INPUT MODE (RIOCR.2 = 0).
NOTE 4: SHOWS SYSTEM IMPLEMENTATION WITH MULTIPLE 31IP02 CORES DRIVING BACKPLANE.
NOTE 5: THOUGH NOT SHOWN, RCHCLK CONTINUES TO MARK THE CHANNEL LSB FOR THE FRAMER'S ACTIVE PERIOD.
NOTE 6: THOUGH NOT SHOWN, RCHBLK CONTINUES TO MARK THE BLOCKED CHANNELS FOR THE FRAMERS ACTIVE PERIOD.

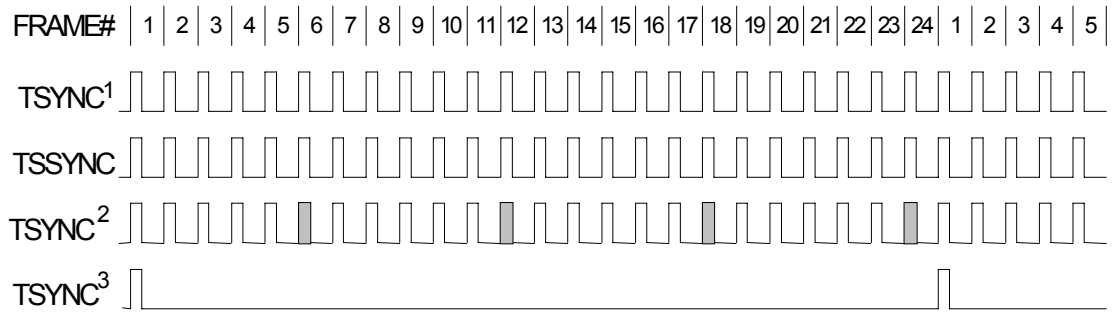
13.3 T1 Transmitter Functional Timing Diagrams

Figure 13-8. T1 Transmit-Side D4 Timing



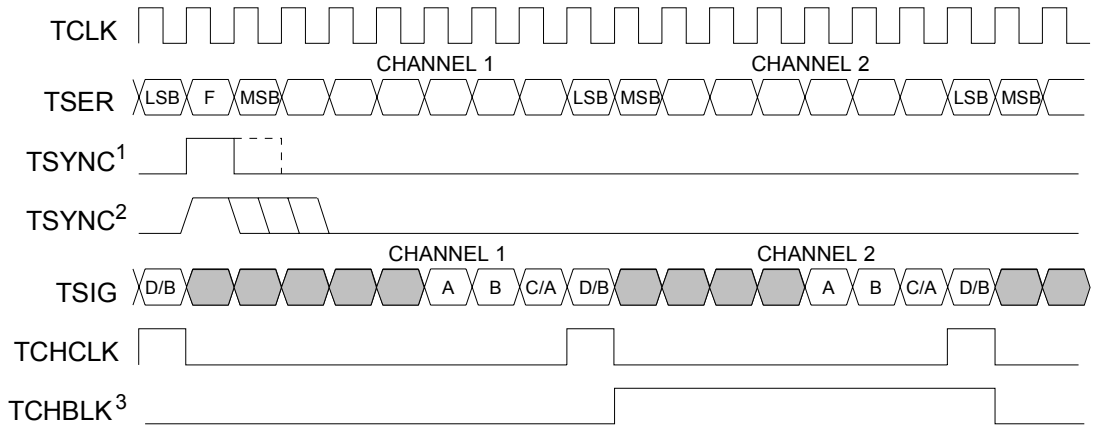
NOTE 1: TSYNC IN THE FRAME MODE (TIOCR.0 = 0) AND DOUBLEWIDE FRAME SYNC IS NOT ENABLED (TIOCR.1 = 0).
NOTE 2: TSYNC IN THE FRAME MODE (TIOCR.0 = 0) AND DOUBLEWIDE FRAME SYNC IS ENABLED (TIOCR.1 = 1).
NOTE 3: TSYNC IN THE MULTIFRAME MODE (TIOCR.0 = 1).

Figure 13-9. T1 Transmit-Side ESF Timing



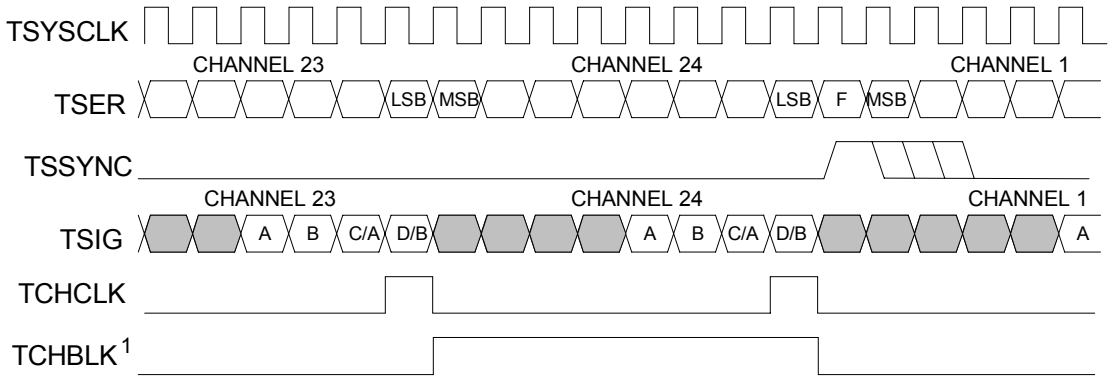
NOTE 1: TSYNC IN FRAME MODE (TIOCR.0 = 0) AND DOUBLEWIDE FRAME SYNC IS NOT ENABLED (TIOCR.1 = 0).
NOTE 2: TSYNC IN FRAME MODE (TIOCR.0 = 0) AND DOUBLEWIDE FRAME SYNC IS ENABLED (TIOCR.1 = 1).
NOTE 3: TSYNC IN MULTIFRAME MODE (TIOCR.0 = 1).

Figure 13-10. T1 Transmit-Side Boundary Timing (Elastic Store Disabled)



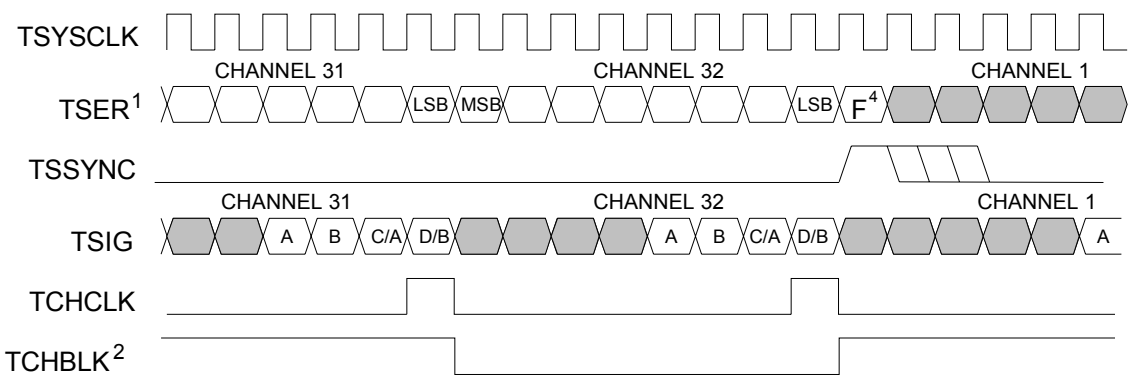
NOTE 1: TSYNC IS IN THE OUTPUT MODE (TIOCR.2 = 1).
NOTE 2: TSYNC IS IN THE INPUT MODE (TIOCR.2 = 0).
NOTE 3: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 2.

Figure 13-11. T1 Transmit-Side 1.544MHz Boundary Timing (Elastic Store Enabled)



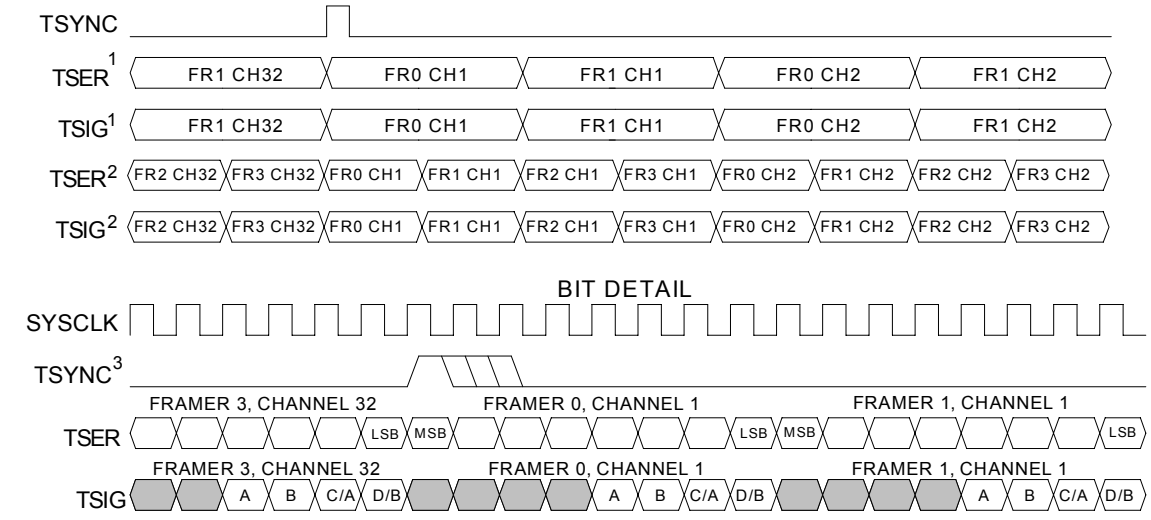
NOTE 1: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 24.

Figure 13-12. T1 Transmit-Side 2.048MHz Boundary Timing (Elastic Store Enabled)



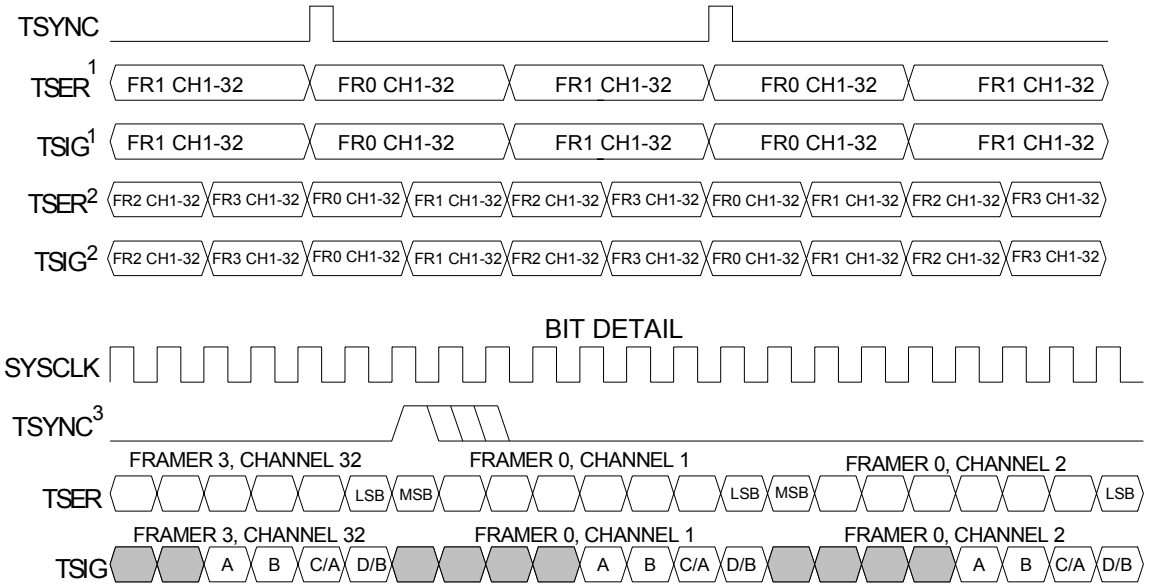
NOTE 1: TSER DATA IN CHANNELS 1, 5, 9, 13, 17, 21, 25, AND 29 IS IGNORED.
NOTE 2: TCHBLK IS PROGRAMMED TO BLOCK CHANNELS 31 AND 1.
NOTE 3: THE F-BIT POSITION FOR THE T1 FRAME IS SAMPLED AND PASSED THROUGH THE TRANSMIT-SIDE ELASTIC STORE INTO THE MSB BIT POSITION OF CHANNEL 1. (NORMALLY, THE TRANSMIT-SIDE FORMATTER OVERWRITES THE F-BIT POSITION UNLESS THE FORMATTER IS PROGRAMMED TO PASS-THROUGH THE F-BIT POSITION.)

Figure 13-13. T1 Transmit-Side Interleave Bus Operation, BYTE Mode



NOTE 1: 4.096MHz BUS CONFIGURATION.
NOTE 2: 8.192MHz BUS CONFIGURATION.
NOTE 3: TSYNC IS IN THE INPUT MODE (TIOCR.2 = 0).
NOTE 4: THOUGH NOT SHOWN, TCHCLK CONTINUES TO MARK THE CHANNEL LSB FOR THE FRAMER'S ACTIVE PERIOD.
NOTE 5: THOUGH NOT SHOWN, TCHBLK CONTINUES TO MARK THE BLOCKED CHANNELS FOR THE FRAMERS ACTIVE PERIOD.

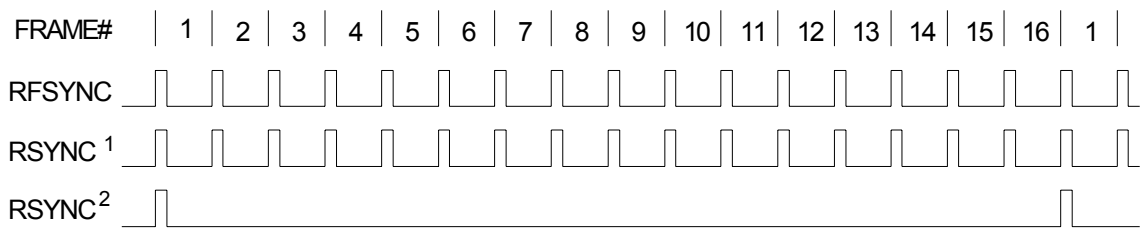
Figure 13-14. T1 Transmit Interleave Bus Operation, FRAME Mode



NOTE 1: 4.096MHz BUS CONFIGURATION.
NOTE 2: 8.192MHz BUS CONFIGURATION.
NOTE 3: TSYNC IS IN THE INPUT MODE (TIOCR.2 = 0).
NOTE 4: THOUGH NOT SHOWN, TCHCLK CONTINUES TO MARK THE CHANNEL LSB FOR THE FRAMER'S ACTIVE PERIOD.
NOTE 5: THOUGH NOT SHOWN, TCHBLK CONTINUES TO MARK THE BLOCKED CHANNELS FOR THE FRAMERS ACTIVE PERIOD.

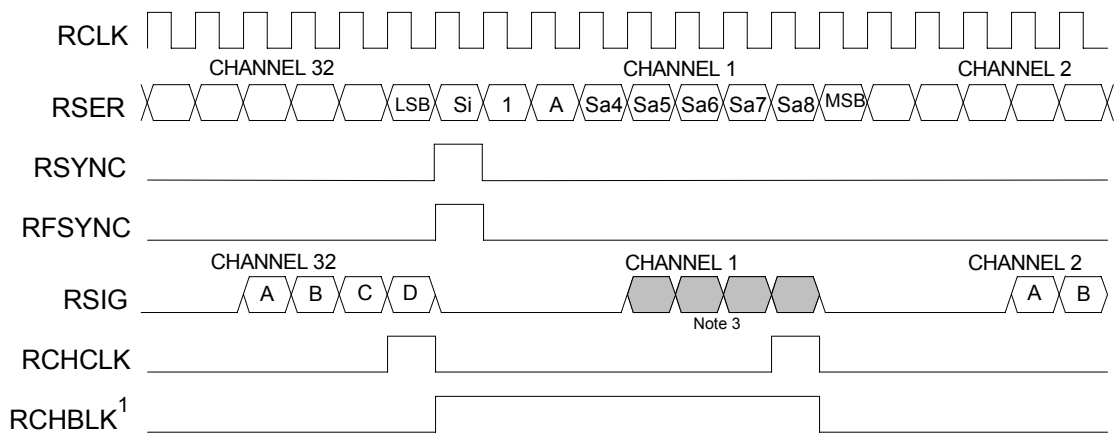
13.4 E1 Receiver Functional Timing Diagrams

Figure 13-15. E1 Receive-Side Timing



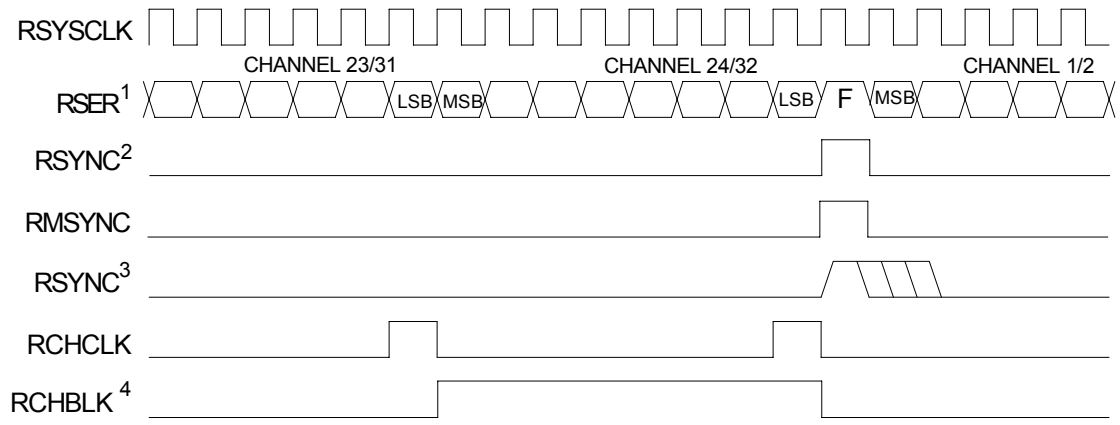
NOTE 1: RSYNC IN FRAME MODE (RIOCR.0 = 0).
NOTE 2: RSYNC IN MULTIFRAME MODE (RIOCR.0 = 1).
NOTE 3: THIS DIAGRAM ASSUMES THE CAS MF BEGINS IN THE RAF FRAME.

Figure 13-16. E1 Receive-Side Boundary Timing (Elastic Store Disabled)



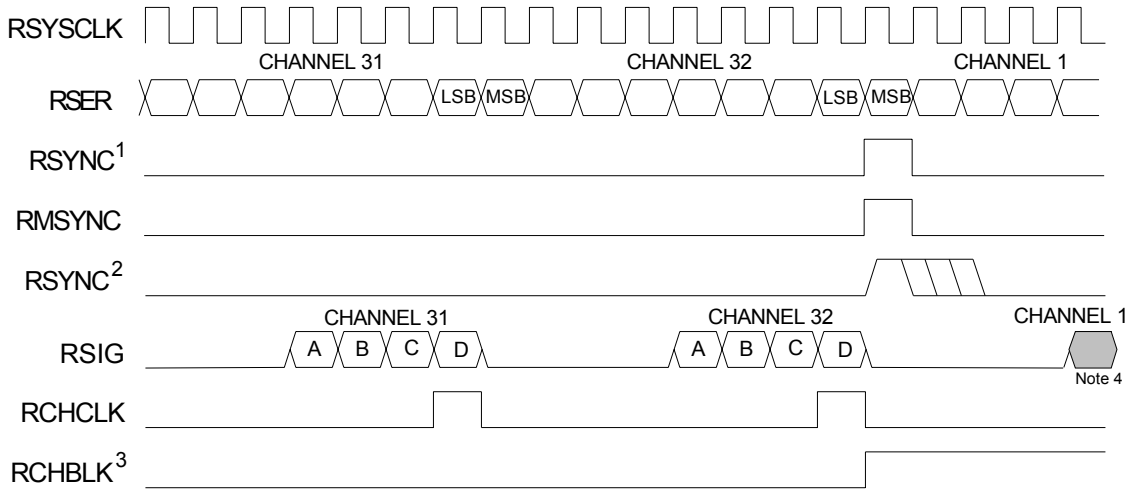
NOTE 1: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 1.
NOTE 2: SHOWN IS A RNAF FRAME BOUNDARY.
NOTE 3: RSIG NORMALLY CONTAINS THE CAS MULTIFRAME ALIGNMENT NIBBLE (0000) IN CHANNEL 1.

Figure 13-17. E1 Receive-Side 1.544MHz Boundary Timing (Elastic Store Enabled)



NOTE 1: DATA FROM THE E1 CHANNELS 1. 5. 9, 13, 17, 21, 25, AND 29 IS DROPPED (CHANNEL 2 FROM THE E1 LINK IS (MAPPED TO CHANNEL 1 OF THE T1 LINK, ETC.) AND THE F-BIT POSITION IS ADDED (FORCED TO 1).
NOTE 2: RSYNC IS IN OUTPUT MODE (RIOCR.2 = 0).
NOTE 3: RSYNC IS IN INPUT MODE (RIOCR.2 = 1).
NOTE 4: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 24.

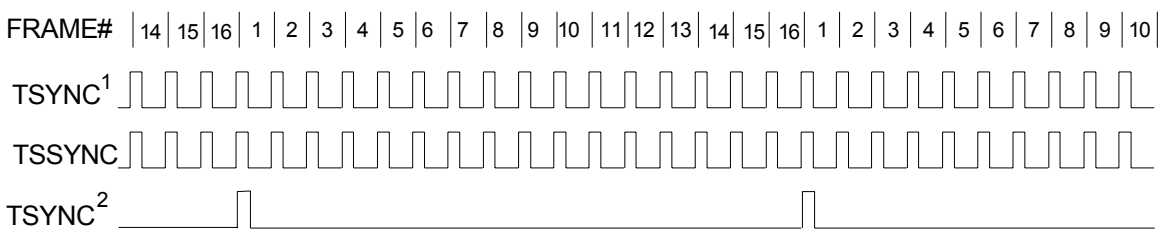
Figure 13-18. E1 Receive-Side 2.048MHz Boundary Timing (Elastic Store Enabled)



NOTE 1: RSYNC IS IN OUTPUT MODE (RIOCR.2 = 0).
NOTE 2: RSYNC IS IN INPUT MODE (RIOCR.2 = 1).
NOTE 3: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 1.
NOTE 4: RSIG NORMALLY CONTAINS THE CAS MULTIFRAME ALIGNMENT NIBBLE (0000) IN CHANNEL 1.

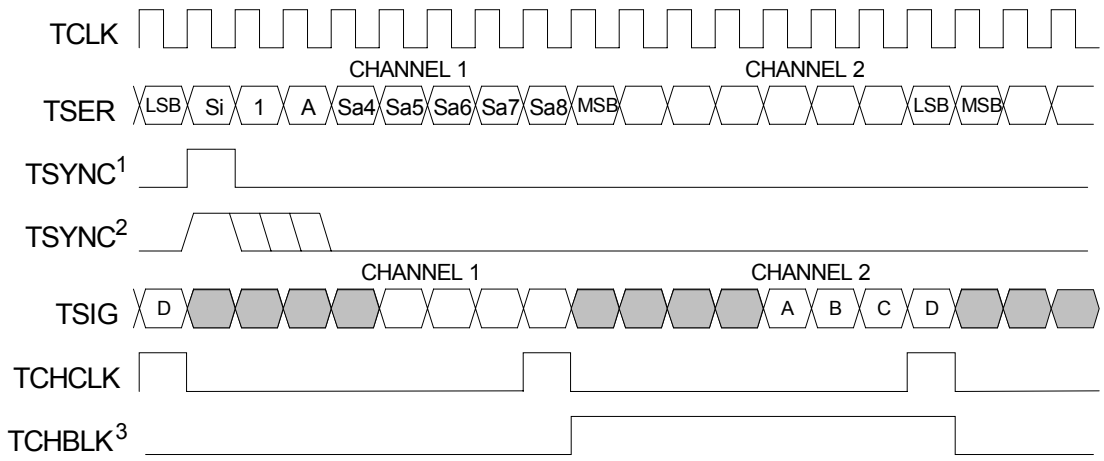
13.5 E1 Transmitter Functional Timing Diagrams

Figure 13-19. E1 Transmit-Side Timing



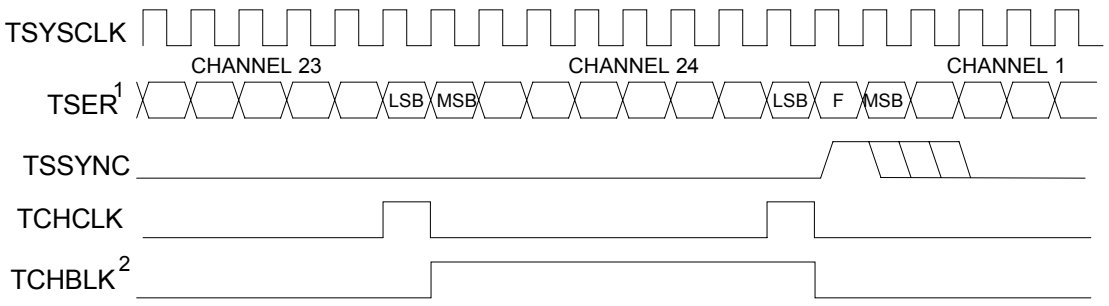
NOTE 1: TSYNC IS IN FRAME MODE (TIOCR.0 = 0).
NOTE 2: TSYNC IS IN MULTIFRAME MODE (TIOCR.0 = 1).
NOTE 3: THIS DIAGRAM ASSUMES BOTH THE CAS MF AND THE CRC4 MF BEGIN WITH THE TAF FRAME.

Figure 13-20. E1 Transmit-Side Boundary Timing (Elastic Store Disabled)



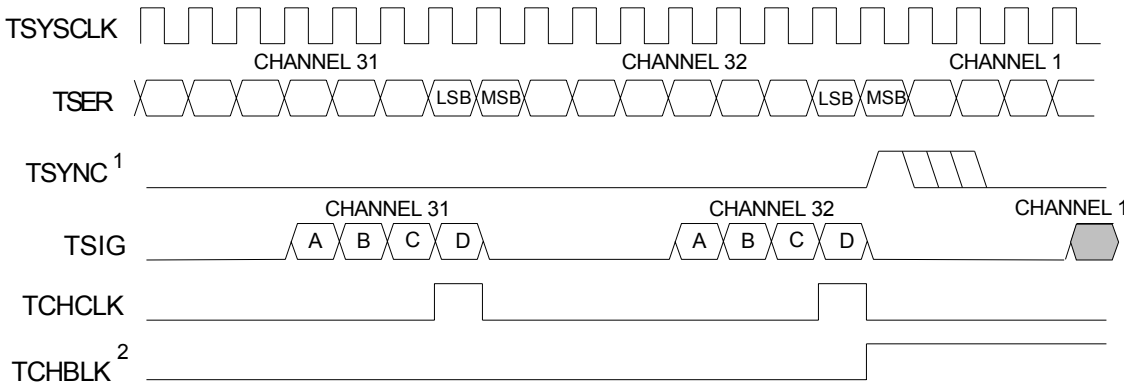
NOTE 1: TSYNC IS IN OUTPUT MODE (TIOCR.2 = 1).
NOTE 2: TSYNC IS IN INPUT MODE (TIOCR.2 = 0).
NOTE 3: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 2.
NOTE 4: THE SIGNALING DATA AT TSIG DURING CHANNEL 1 IS NORMALLY OVERWRITTEN IN THE TRANSMIT FORMATTER WITH THE CAS MF ALIGNMENT NIBBLE (0000).
NOTE 5: SHOWN IS A TNAF FRAME BOUNDARY.

Figure 13-21. E1 Transmit-Side 1.544MHz Boundary Timing (Elastic Store Enabled)



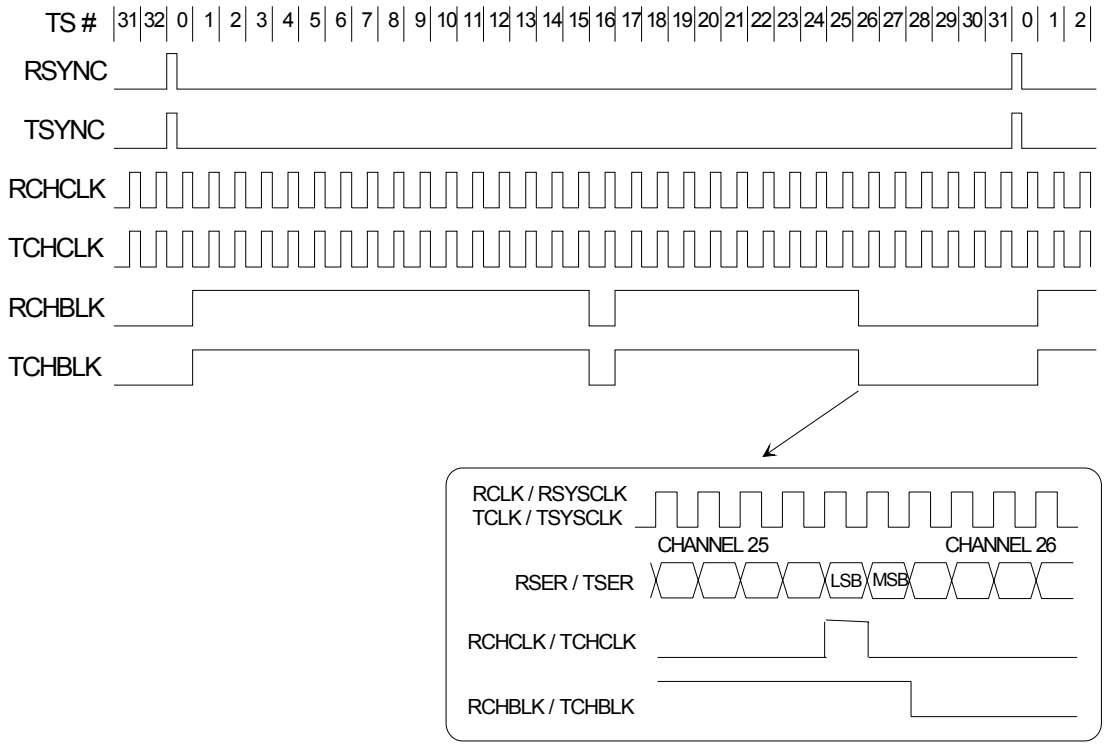
NOTE 1: THE F-BIT POSITION IN THE TSER DATA IS IGNORED.
NOTE 2: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 24.

Figure 13-22. E1 Transmit-Side 2.048MHz Boundary Timing (Elastic Store Enabled)



NOTE 1: TSYNC IS IN INPUT MODE (TIOCR.2 = 0).
NOTE 2: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 1.

Figure 13-23. E1 G.802 Timing



NOTE: RCHBLK OR TCHBLK PROGRAMMED TO PULSE HIGH DURING TIME SLOTS 1 THROUGH 15, 17 THROUGH 25, AND BIT 1 OF TIME SLOT 26.

14. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Lead with Respect to V_{SS} (except V_{DD})	-0.3V to +5.5V
Supply Voltage (V_{DD}) Range with Respect to V_{SS}	-0.3V to +3.63V
Operating Temperature Range for DS26401	0°C to +70°C
Operating Temperature Range for DS26401N	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C for DS26401N.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}		2.0		5.5	V
Logic 0	V_{IL}		-0.3		+0.8	V
Supply	V_{DD}		3.135	3.3	3.465	V

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}			7		pF
Output Capacitance	C_{OUT}			7		pF

DC CHARACTERISTICS

(V_{DD} = 3.135V to 3.465V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current at 3.3V	I_{DD}	(Note 1)		275	330	mA
Input Leakage	I_{IL}		-10.0		+10.0	µA
Input Leakage on Pins with Pullups	I_L		-500		+500	µA
Tri-State Output Leakage	I_{OL}		-10.0		+10.0	µA
Output Voltage	V_{OH}	I_o = -4.0mA	2.4			V
	V_{OL}	I_o = +4.0mA			0.4	

Note 1: RCLK1-n = TCLK1-n = 2.048MHz, GCLK = 45MHz.

15. TIMING

Unless otherwise noted, all timing numbers assume 20pF test load on output signals, 40pF test load on bus signals.

15.1 Microprocessor Bus AC Characteristics

AC CHARACTERISTICS—MICROPROCESSOR BUS TIMING

(V_{DD} = 3.3V ±5%, T_A = 0°C to +70°C for DS26401; V_{DD} = 3.3V ± 5%, T_A = -40°C to +85°C for DS26401N.)
(Figure 15-1, Figure 15-2, Figure 15-3, and Figure 15-4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for A[11:0] Valid to $\overline{CS}$ Active	t1	(Note 1)	0			ns
Setup Time for $\overline{CS}$ Active to Either $\overline{RD}$ or $\overline{WR}$ Active	t2	(Note 1)	0			ns
Delay Time from Either $\overline{RD}$ or $\overline{DS}$ Active to D[7:0] Valid	t3				115	ns
Hold Time from Either $\overline{RD}$ or $\overline{WR}$ Inactive to $\overline{CS}$ Inactive	t4		0			ns
Hold Time from $\overline{CS}$ or $\overline{RD}$ or $\overline{DS}$ Inactive to D[7:0] Tri-State	t5		2.5		20	ns
Wait Time from $\overline{WR}$ Active to Latch Data	t6		35			ns
Data Set Up Time to $\overline{WR}$ Inactive	t7		10			ns
Data Hold Time from $\overline{WR}$ Inactive	t8		2			ns
Address Hold from $\overline{WR}$ Inactive	t9		3			ns
Write Access to Subsequent Write/Read Access Delay Time	t10		80			ns

Note 1: Guaranteed by design.

Figure 15-1. Intel Bus Read Timing (BTS = 0)

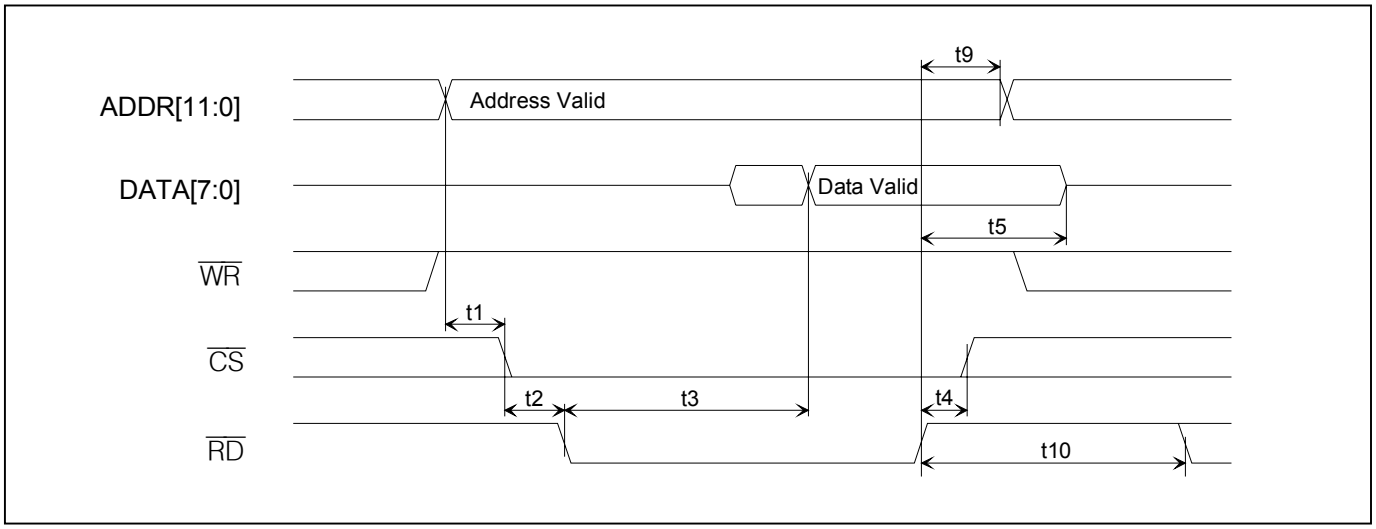


Figure 15-2. Intel Bus Write Timing (BTS = 0)

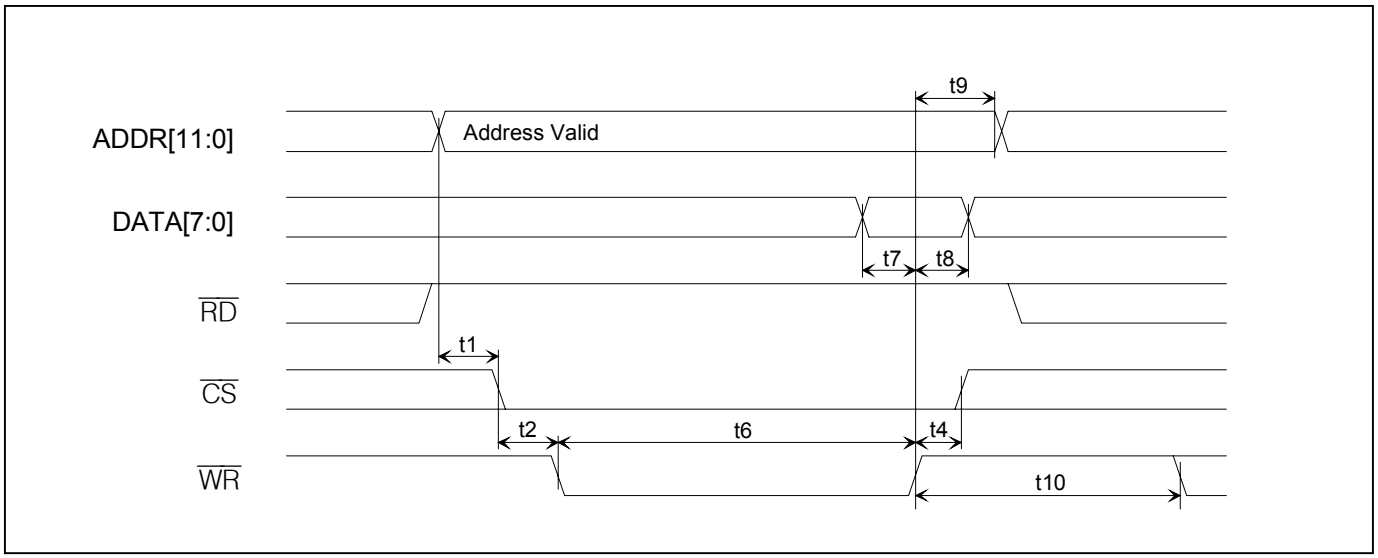


Figure 15-3. Motorola Bus Read Timing (BTS = 1)

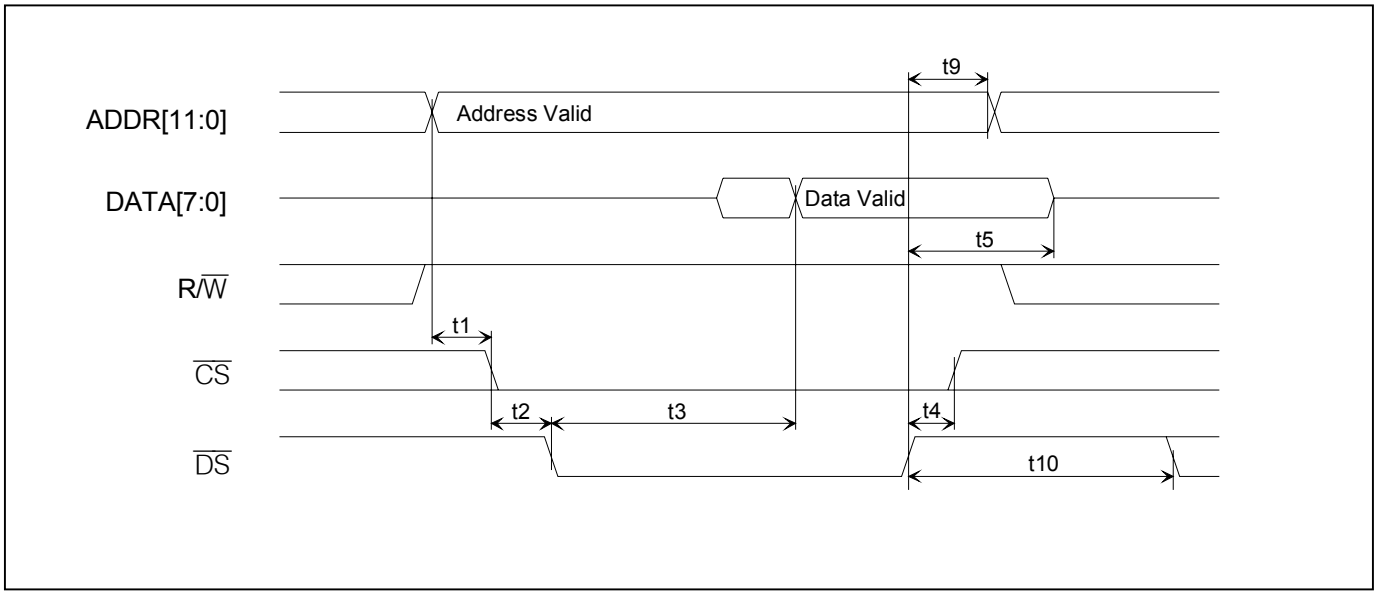
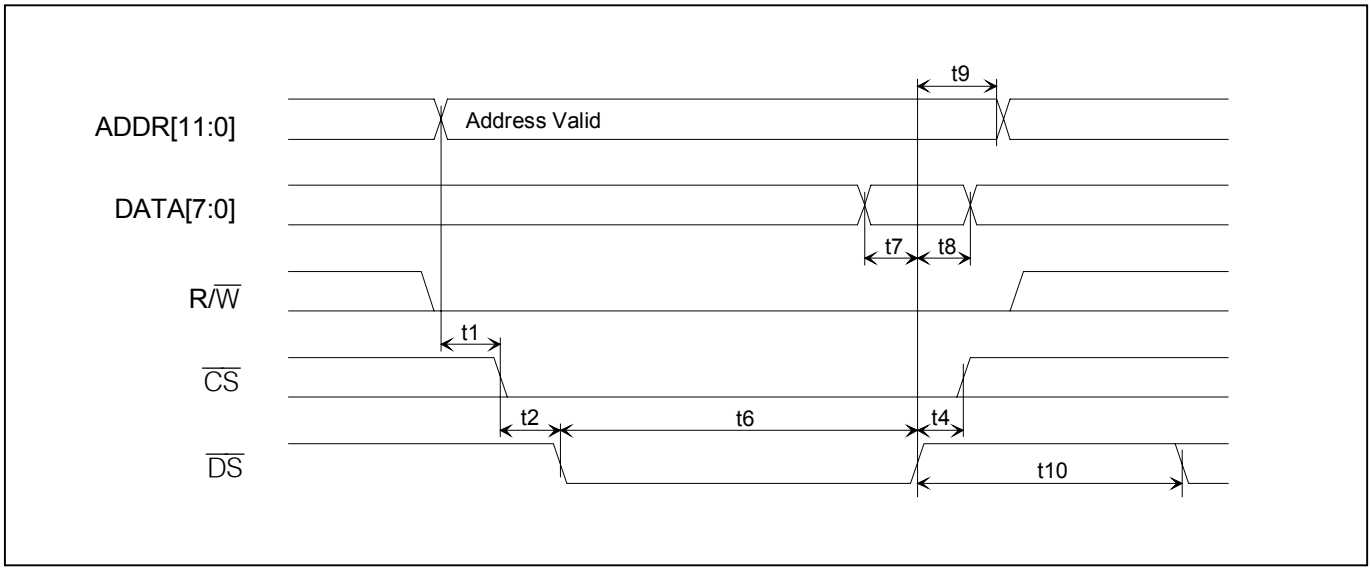


Figure 15-4. Motorola Bus Write Timing (BTS = 1)



15.2 Receiver AC Characteristics

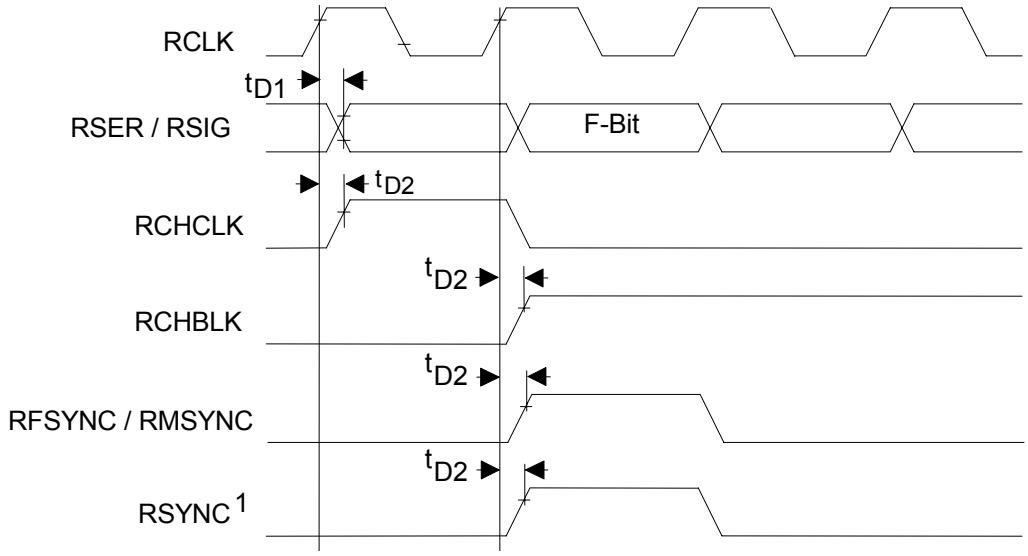
RECEIVER AC CHARACTERISTICS

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (Note 1: Guaranteed by design.
Figure 15-5, Figure 15-6, and Figure 15-7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RCLK Period	t_{CP}	T1 mode		648		ns
	t_{CP}	E1 mode		488		
RCLK Pulse Width	t_{CH}		85			ns
	t_{CL}		85			
RSYSCLK Period (Note 1)	t_{SP}	RSYSCLK = 1.544MHz	60	648		ns
	t_{SP}	RSYSCLK = 2.048MHz	60	488		
RSYSCLK Pulse Width	t_{SH}		30			ns
	t_{SL}		30			
RSYNC Setup to RSYSCLK Falling	t_{SU}		20		t_{SH} - 5	ns
RSYNC Pulse Width	t_{PW}		50			ns
RPOS/RNEG Setup to RCLK Falling	t_{SU}		20			ns
RPOS/RNEG Hold From RCLK Falling	t_{HD}		20			ns
Delay RCLK to RSER, RSIG Valid	t_{D1}				50	ns
Delay RCLK to RCHCLK, RSYNC, RCHBLK, RFSYNC	t_{D2}				50	ns
Delay RSYSCLK to RSER, RSIG Valid	t_{D3}				50	ns
Delay RSYSCLK to RCHCLK, RCHBLK, RMSYNC, RSYNC	t_{D4}				50	ns

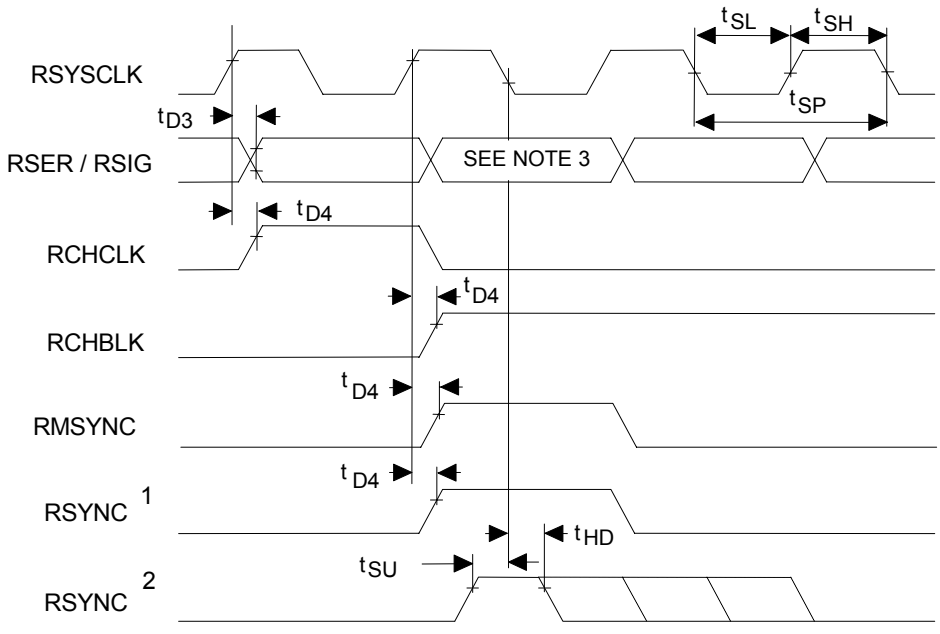
Note 1: Guaranteed by design.

Figure 15-5. Receive Framer Timing—Backplane (T1 Mode)



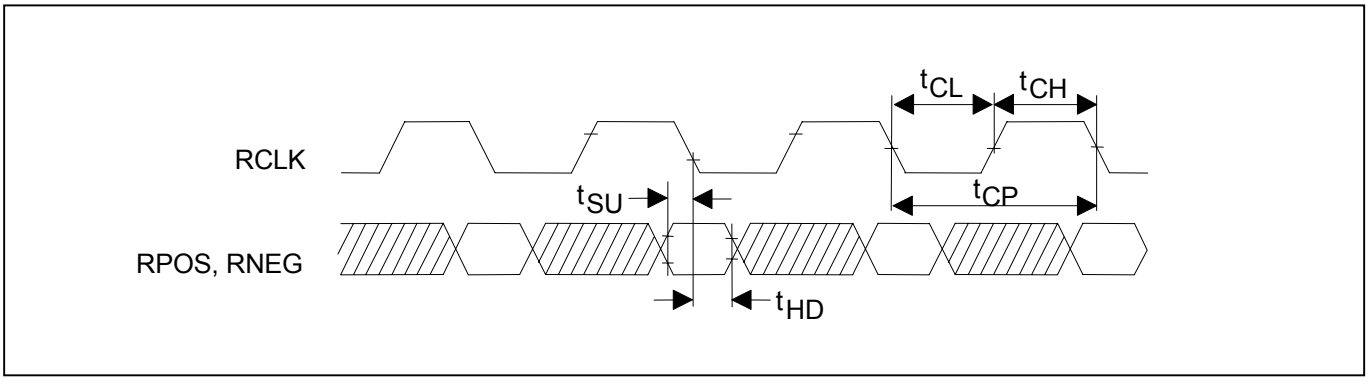
NOTE 1: RSYNC IS IN OUTPUT MODE.
NOTE 2: NO RELATIONSHIP BETWEEN RCHCLK AND RCHBLK AND OTHER SIGNALS IS IMPLIED.

Figure 15-6. Receive-Side Timing—Elastic Store Enabled (T1 Mode)



NOTE 1: RSYNC IS IN OUTPUT MODE.
NOTE 2: RSYNC IS IN INPUT MODE.
NOTE 3: F-BIT WHEN RIOCR.4 = 0, MSB OF TS0 WHEN RIOCR.4 = 1.

Figure 15-7. Receive Framer Timing—Line Side



15.3 Transmit AC Characteristics

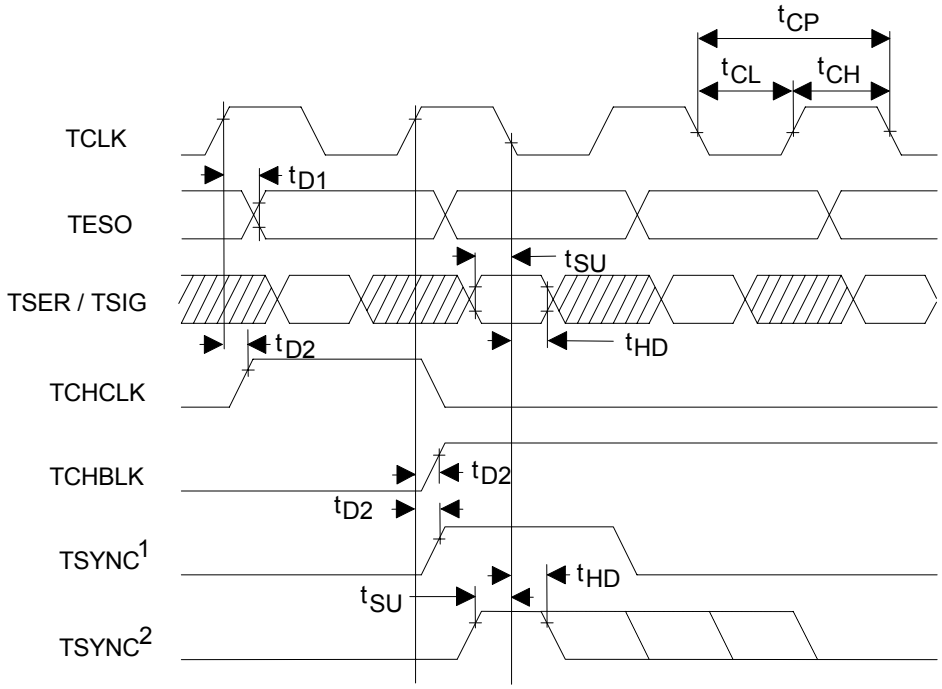
TRANSMIT AC CHARACTERISTICS

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (Figure 15-8, Figure 15-9, and Figure 15-10)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TCLK Period	t_{CP}	T1 mode		648		ns
	t_{CP}	E1 mode		488		
TCLK Pulse Width	t_{CH}		85			ns
	t_{CL}		85			
TSYSCLK Period (Note 1)	t_{SP}	RSYSCLK = 1.544MHz	60	648		ns
	t_{SP}	RSYSCLK = 2.048MHz	60	448		
TSYSCLK Pulse Width	t_{SH}		30			ns
	t_{SL}		30			
TSYNC or TSSYNC Setup to TCLK or TSYSCLK falling	t_{SU}		20		t_{CH} - 5 or t_{SH} - 5	ns
TSYNC or TSSYNC Pulse Width	t_{PW}		50			ns
TSER, TSIG, Setup to TCLK, TSYSCLK Falling	t_{SU}		20			ns
TSER, TSIG, Hold from TCLK, TSYSCLK Falling	t_{HD}		20			ns
Delay TCLK to TCHBLK, TCHCLK, TSYNC	t_{D2}				50	ns
Delay TSYSCLK to TCHCLK, TCHBLK	t_{D3}				50	ns
Delay TCLK to TPOS, TNEG	t_{D4}				50	ns

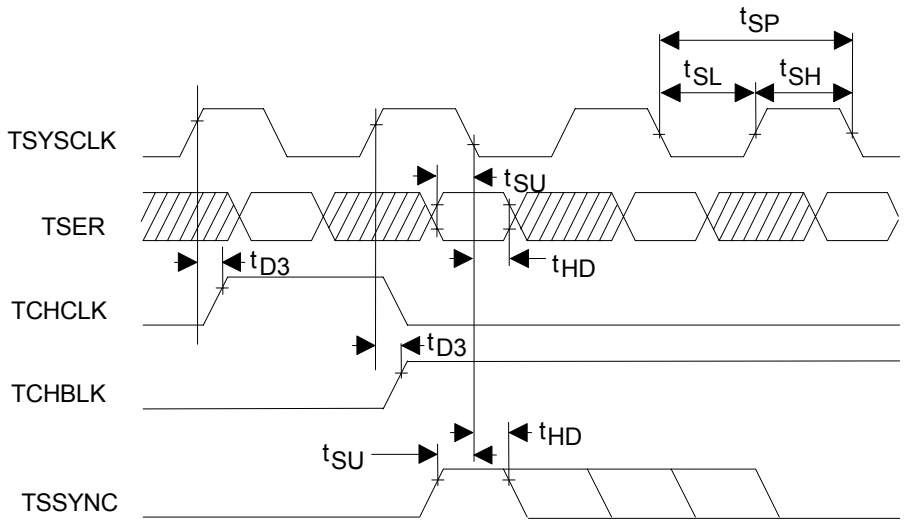
Note 1: Guaranteed by design.

Figure 15-8. Transmit Formatter Timing—Backplane



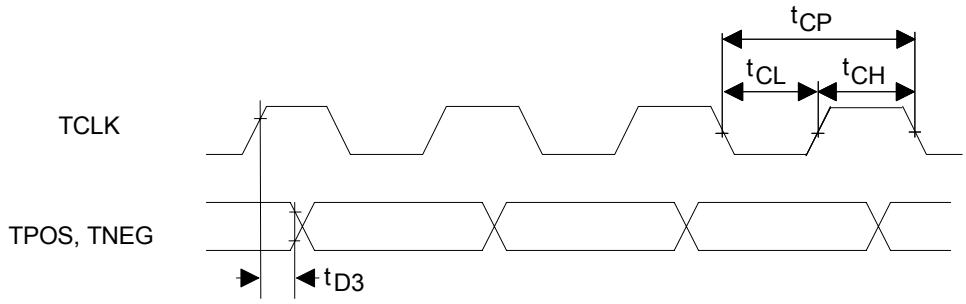
NOTE 1: TSYNC IS IN OUTPUT MODE.
NOTE 2: TSYNC IS IN INPUT MODE.
NOTE 3: TSER IS SAMPLED ON THE FALLING EDGE OF TCLK WHEN THE TRANSMIT-SIDE ELASTIC STORE IS DISABLED.
NOTE 4: TCHCLK AND TCHBLK ARE SYNCHRONOUS WITH TCLK WHEN THE TRANSMIT-SIDE ELASTIC STORE IS DISABLED.
NOTE 5: NO RELATIONSHIP BETWEEN TCHCLK AND TCHBLK AND THE OTHER SIGNALS IS IMPLIED.

Figure 15-9. Transmit Formatter Timing, Elastic Store Enabled



NOTE 1: TSER IS ONLY SAMPLED ON THE FALLING EDGE OF TSYSCLK WHEN THE TRANSMIT-SIDE ELASTIC STORE IS ENABLED.
NOTE 2: TCHCLK AND TCHBLK ARE SYNCHRONOUS WITH TSYSCLK WHEN THE TRANSMIT-SIDE ELASTIC STORE IS ENABLED.

Figure 15-10. Transmit Formatter Timing—Line Side



15.4 JTAG Interface Timing

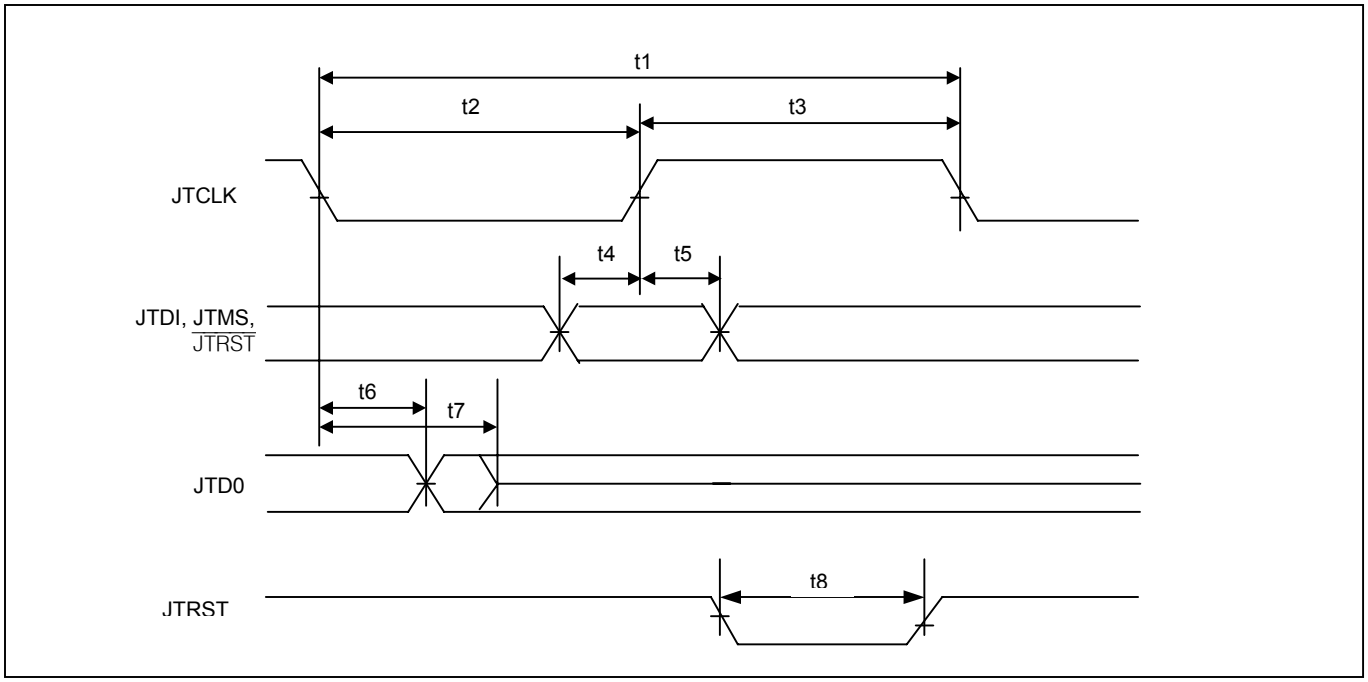
JTAG INTERFACE TIMING

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (Figure 15-11)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1			1000		ns
JTCLK Clock High/Low Time	t2/t3	(Note 1)	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4		3			ns
JTCLK to JTDI, JTMS Hold Time	t5		2			ns
JTCLK to JTDO Delay	t6		2		50	ns
JTCLK to JTDO High-Z Delay	t7		2		50	ns
$\overline{\text{JTRST}}$ Width Low Time	t8		100			ns

Note 1: Clock can be stopped high or low.

Figure 15-11. JTAG Interface Timing Diagram



15.5 System Clock AC Characteristics

SYSTEM CLOCK AC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REF_CLK Frequency				1.544		MHz
				2.048		
REF_CLK Duty Cycle		(Note 1)	40		60	%
GCLK Frequency		(Note 1)	43	45	49	MHz
GCLK Duty Cycle			40		60	%

Note 1: Guaranteed by design.

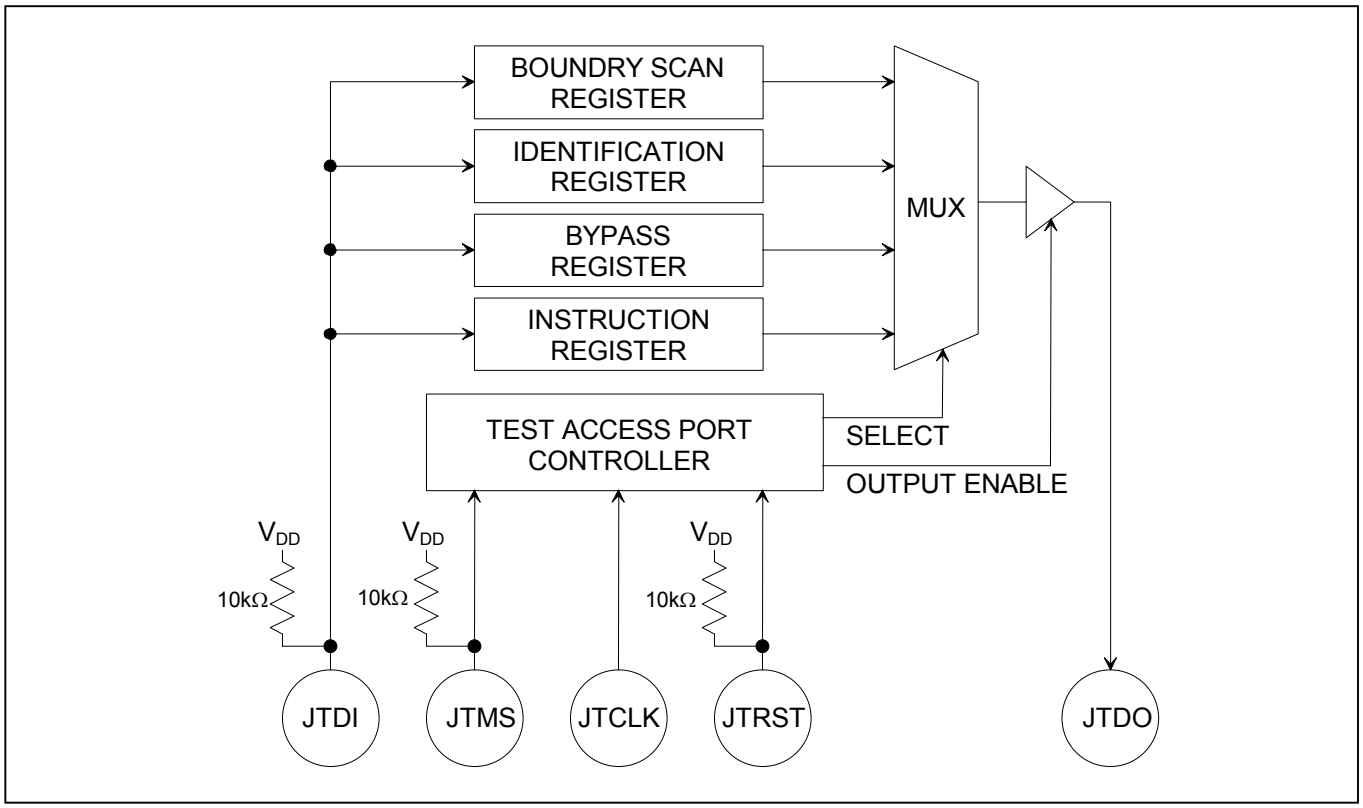
16. JTAG BOUNDARY SCAN ARCHITECTURE AND TEST ACCESS PORT

The DS26401 IEEE 1149.1 design supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE (see Table 16-1). The DS26401 contains the following, as required by IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register
- Bypass Register
- Boundary Scan Register
- Device Identification Register

The Test Access Port has the necessary interface pins JTRST, JTCLK, JTMS, JTDI, and JTDO. See the pin descriptions for details.

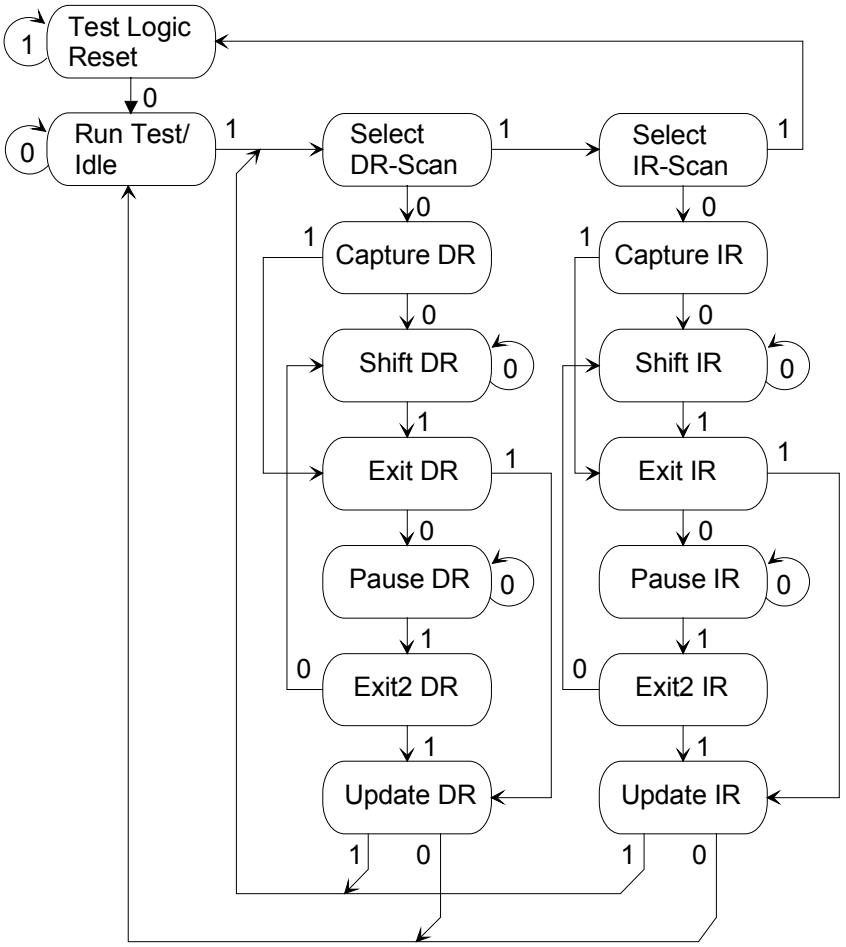
Figure 16-1. JTAG Functional Block Diagram



16.1 TAP Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. See Figure 16-2.

Figure 16-2. Tap Controller State Diagram



Test-Logic-Reset
Upon power up, the TAP Controller will be in the Test-Logic-Reset state. The Instruction register will contain the IDCODE instruction. All system logic of the device will operate normally.

Run-Test-Idle
The Run-Test-Idle is used between scan operations or during specific tests. The Instruction register and test registers will remain idle.

Select-DR-Scan
All test registers retain their previous state. With JTMS LOW, a rising edge of JTCLK moves the controller into the Capture-DR state and will initiate a scan sequence. JTMS HIGH during a rising edge on JTCLK moves the controller to the Select-IR-Scan state.

Capture-DR
Data may be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register will remain at its current value. On the rising edge of JTCLK, the controller will go to the Shift-DR state if JTMS is LOW or it will go to the Exit1-DR state if JTMS is HIGH.

Shift-DR
The test data register selected by the current instruction will be connected between JTDI and JTDO and will shift data one stage towards its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it will maintain its previous state.

Exit1-DR
While in this state, a rising edge on JTCLK will put the controller in the Update-DR state, which terminates the scanning process, if JTMS is HIGH. A rising edge on JTCLK with JTMS LOW will put the controller in the Pause-DR state.

Pause-DR
Shifting of the test registers is halted while in this state. All test registers selected by the current instruction will retain their previous state. The controller will remain in this state while JTMS is LOW. A rising edge on JTCLK with JTMS HIGH will put the controller in the Exit2-DR state.

Exit2-DR
A rising edge on JTCLK with JTMS HIGH while in this state will put the controller in the Update-DR state and terminate the scanning process. A rising edge on JTCLK with JTMS LOW will enter the Shift-DR state.

Update-DR
A falling edge on JTCLK while in the Update-DR state will latch the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register.

Select-IR-Scan
All test registers retain their previous state. The instruction register will remain unchanged during this state. With JTMS LOW, a rising edge on JTCLK moves the controller into the Capture-IR state and will initiate a scan sequence for the instruction register. JTMS HIGH during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR
The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the Exit1-IR state. If JTMS is LOW on the rising edge of JTCLK, the controller will enter the Shift-IR state.

Shift-IR
In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register and all test registers remain at their previous states. A rising edge on JTCLK with JTMS HIGH will move the controller to the Exit1-IR state. A

rising edge on JTCLK with JTMS LOW will keep the controller in the Shift-IR state while moving data one stage thorough the instruction shift register.

Exit1-IR
A rising edge on JTCLK with JTMS LOW will put the controller in the Pause-IR state. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the Update-IR state and terminate the scanning process.

Pause-IR
Shifting of the instruction shift register is halted temporarily. With JTMS HIGH, a rising edge on JTCLK will put the controller in the Exit2-IR state. The controller will remain in the Pause-IR state if JTMS is LOW during a rising edge on JTCLK.

Exit2-IR
A rising edge on JTCLK with JTMS LOW will put the controller in the Update-IR state. The controller will loop back to Shift-IR if JTMS is HIGH during a rising edge of JTCLK in this state.

Update-IR
The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS LOW puts the controller in the Run-Test-Idle state. With JTMS HIGH, the controller enters the Select-DR-Scan state.

16.2 Instruction Register

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register will be connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS LOW will shift the data one stage towards the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS HIGH will move the controller to the Update-IR state. The falling edge of that same JTCLK will latch the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS26401 and its respective operational binary codes are shown in Table 16-1.

Table 16-1. Instruction Codes for IEEE 1149.1 Architecture

INSTRUCTION	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD
This is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE/PRELOAD also allows the device to shift data into the boundary scan register via JTDI using the Shift-DR state.

BYPASS
When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the one-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation.

EXTEST
This allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins will be driven. The boundary scan register will be connected between JTDI and JTDO. The Capture-DR will sample all digital inputs into the boundary scan register.

CLAMP
All digital outputs of the device will output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs will not change during the CLAMP instruction.

HIGHZ
All digital outputs of the device will be placed in a high impedance state. The BYPASS register will be connected between JTDI and JTDO.

IDCODE
When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code will be loaded into the identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The ID code will always have a '1' in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version.

Table 16-2. ID Code Structure

MSB			LSB (Must be '1')
Version (contact factory)	Device ID (0025h)	JEDEC	1
4 bits	0000000000100101	00010100001	1

16.3 Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included with the DS26401 design. The identification register is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

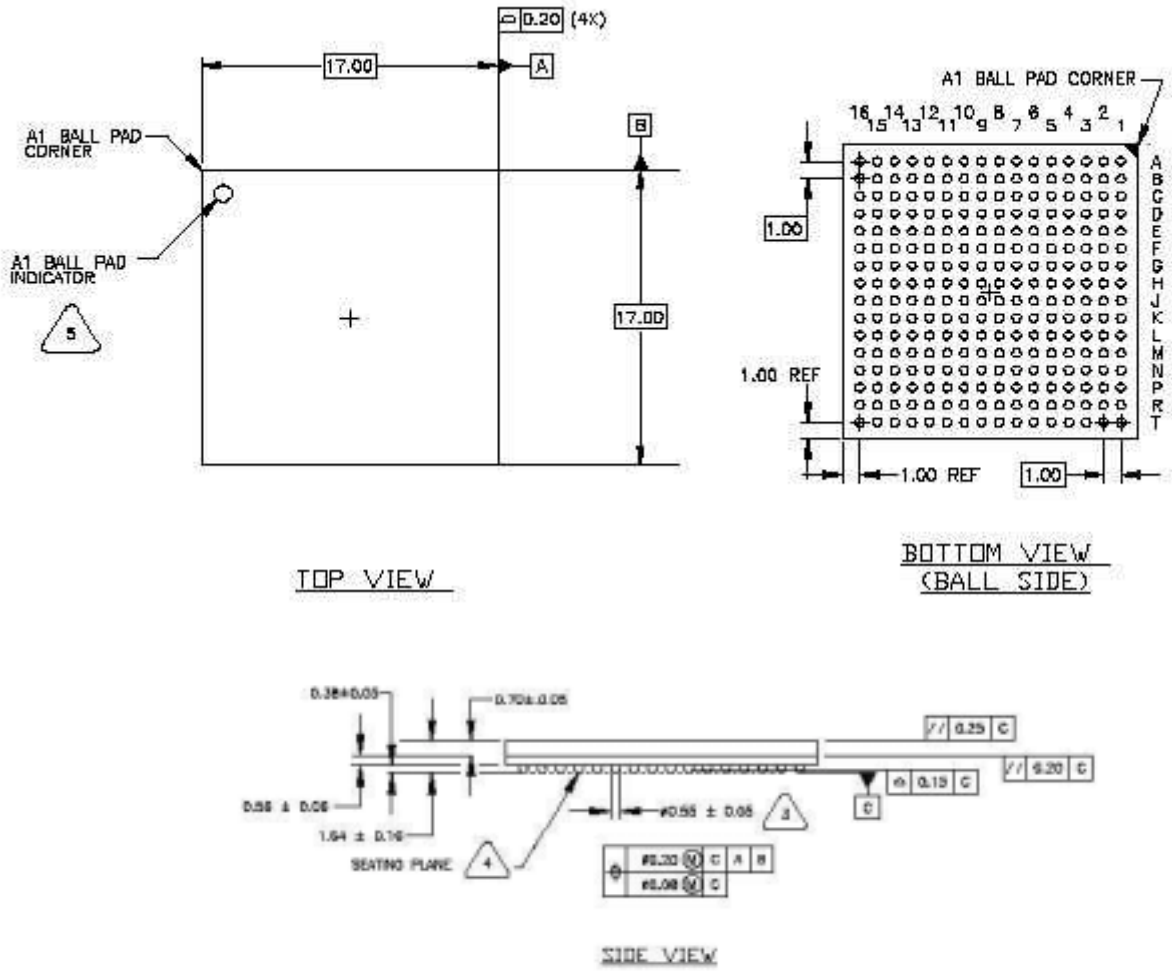
Boundary Scan Register
This register contains a shift register path and a latched parallel output for all control cells and digital I/O cells. It is n bits in length.

Bypass Register
The bypass register is a single one-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions, which provides a short path between JTDI and JTDO.

Identification Register
The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

17. PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)



NOTES:

1. DIMENSION IS MM.
2. THE BASIC SOLDER BALL GRID PITCH IS 1.00 MM.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. A1 BALL PAD CORNER ID

18. THERMAL INFORMATION

PARAMETER	VALUE
Target Ambient Temperature Range	-40°C to +85°C
Die Junction Temperature Range	-40°C to +125°C

19. REVISION HISTORY

REVISION	DESCRIPTION
072403	New product release.

Maxim/Dallas Semiconductor cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim/Dallas Semiconductor product. No circuit patent licenses are implied. Maxim/Dallas Semiconductor reserves the right to change the circuitry and specifications without notice at any time.

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