

MSP430F543xA, MSP430F541xA Mixed-Signal Microcontrollers

1 Features

- Low supply voltage range: 3.6 V down to 1.8 V
- Ultra-low power consumption
 - Active mode (AM): all system clocks active
230 μ A/MHz at 8 MHz, 3.0 V, flash program execution (typical)
110 μ A/MHz at 8 MHz, 3.0 V, RAM program execution (typical)
 - Standby mode (LPM3): real-time clock (RTC) with crystal, watchdog, and supply supervisor operational, full RAM retention, fast wakeup:
1.7 μ A at 2.2 V, 2.1 μ A at 3.0 V (typical)
low-power oscillator (VLO), general-purpose counter, watchdog, and supply supervisor operational, full RAM retention, fast wakeup:
1.2 μ A at 3.0 V (typical)
 - Off mode (LPM4): full RAM retention, supply supervisor operational, fast wakeup:
1.2 μ A at 3.0 V (typical)
 - Shutdown mode (LPM4.5): 0.1 μ A at 3.0 V (typical)
- Wake up from standby mode in 3.5 μ s (typical)
- 16-bit RISC architecture
 - Extended memory
 - Up to 25-MHz system clock
- Flexible power-management system
 - Fully integrated LDO with programmable regulated core supply voltage
 - Supply voltage supervision, monitoring, and brownout
- Unified clock system
 - FLL control loop for frequency stabilization
 - Low-power low-frequency internal clock source (VLO)
 - Low-frequency trimmed internal reference source (REFO)
- 32-kHz crystals
- High-frequency crystals up to 32 MHz
- 16-bit timer TA0, Timer_A with five capture/compare registers
- 16-bit timer TA1, Timer_A with three capture/compare registers
- 16-bit timer TB0, Timer_B with seven capture/compare shadow registers
- Up to four universal serial communication interfaces (USCIs)
 - USCI_A0, USCI_A1, USCI_A2, and USCI_A3 each support:
 - Enhanced UART supports automatic baud-rate detection
 - IrDA encoder and decoder
 - Synchronous SPI
 - USCI_B0, USCI_B1, USCI_B2, and USCI_B3 each support:
 - I²C
 - Synchronous SPI
- 12-bit analog-to-digital converter (ADC)
 - Internal reference
 - Sample-and-hold
 - Autoscan feature
 - 14 external channels, 2 internal channels
- Hardware multiplier supports 32-bit operations
- Serial onboard programming, no external programming voltage needed
- 3-channel internal DMA
- Basic timer with RTC feature
- [Device Comparison](#) summarizes the available family members

2 Applications

- Analog and Digital Sensor Systems
- Digital Motor Controls
- Remote Controls
- Thermostats
- Digital Timers
- Hand-Held Meters

3 Description

The TI MSP family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3.5 μ s (typical).



The MSP430F543xA and MSP430F541xA series are microcontroller configurations with three 16-bit timers, a high-performance 12-bit ADC, up to four USCIs, a hardware multiplier, DMA, an RTC module with alarm capabilities, and up to 87 I/O pins.

For complete module descriptions, see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

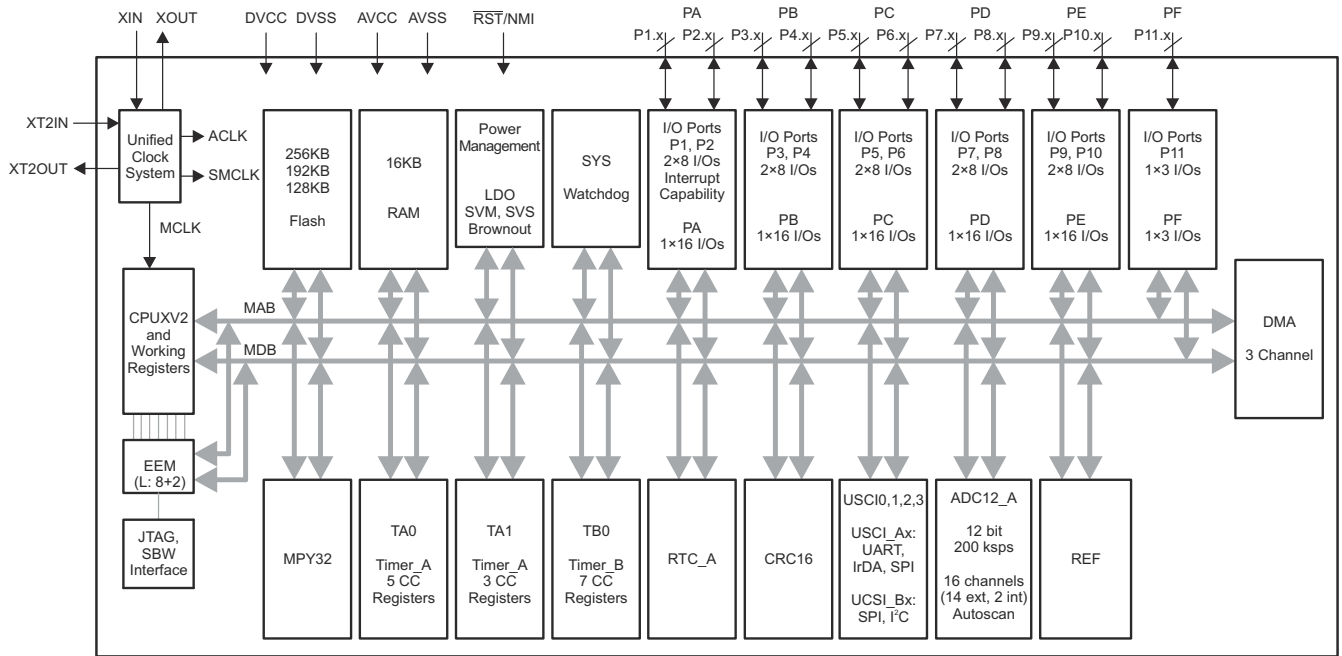
Device Information

| PART NUMBER ⁽¹⁾ | PACKAGE | BODY SIZE ⁽²⁾ |
|---------------------------------|-----------------------------|--------------------------|
| MSP430F5438AIPZ | LQFP (100) | 14 mm × 14 mm |
| MSP430F5437AIPN | LQFP (80) | 12 mm × 12 mm |
| MSP430F5438AIZCA | nFBGA (113) | 7 mm × 7 mm |
| MSP430F5438AIZQW ⁽³⁾ | MicroStar Junior™ BGA (113) | 7 mm × 7 mm |

- (1) For the most current part, package, and ordering information, see the *Package Option Addendum* in [Section 11](#), or see the TI website at www.ti.com.
- (2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 11](#).
- (3) All orderable part numbers in the ZQW (MicroStar Junior BGA) package have been changed to a status of Last Time Buy. Visit the [Product life cycle](#) page for details on this status.

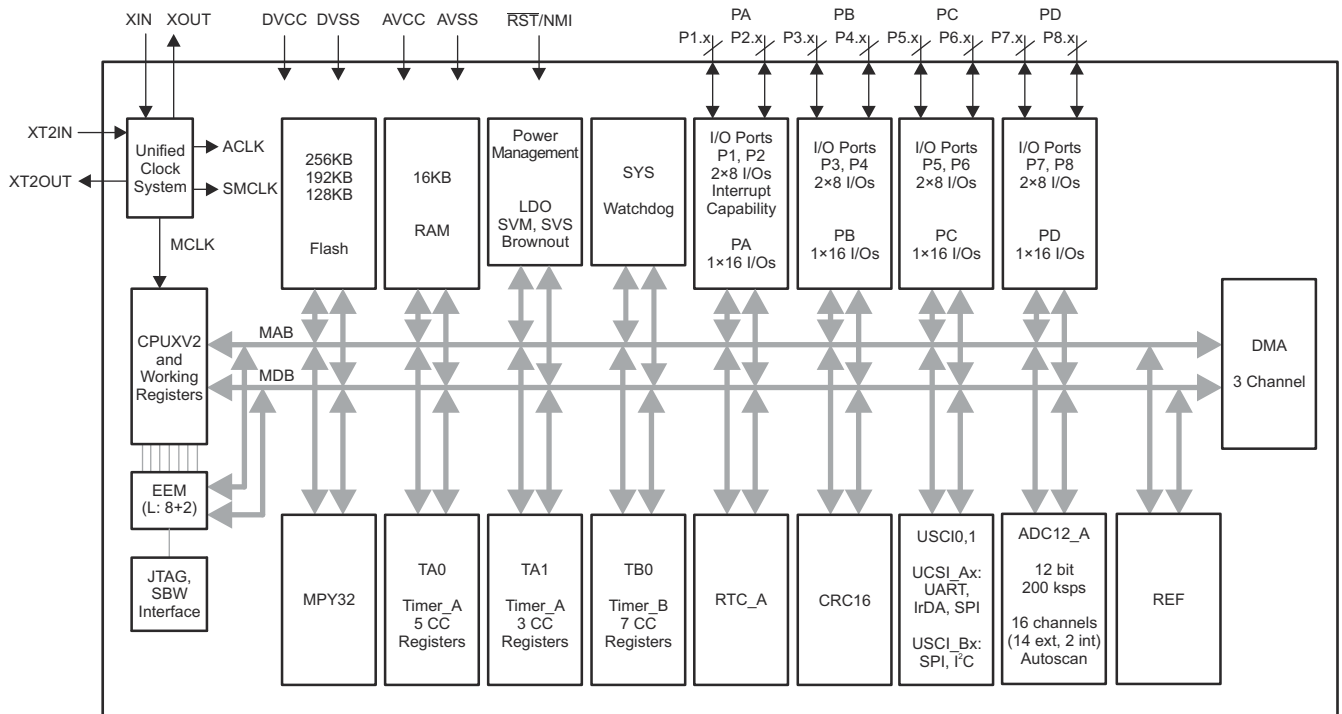
4 Functional Block Diagrams

Figure 4-1 and Figure 4-2 show the functional block diagrams.



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Figure 4-1. Functional Block Diagram – MSP430F5438AIPZ, MSP430F5436AIPZ, MSP430F5419AIPZ, MSP430F5438AIZCAW, MSP430F5436AIZCA, MSP430F5419AIZCA, MSP430F5438AIZQW, MSP430F5436AIZQW, MSP430F5419AIZQW



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Functional Block Diagram – MSP430F5437AIPN, MSP430F5435AIPN, MSP430F5418AIPN

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from September 12, 2020 to May 10, 2021 | Page |
|---|-------------|
| • Added nFBGA package (ZCA) thermal resistance characteristics..... | 18 |

6 Device Comparison

Table 6-1 summarizes the available family members.

Table 6-1. Device Characteristics

| DEVICE ⁽¹⁾ | FLASH (KB) ⁽²⁾ | SRAM (KB) | Timer_A ⁽³⁾ | Timer_B ⁽⁴⁾ | USCI | | ADC12_A (Ch) | I/O | PACKAGE |
|-----------------------|---------------------------|-----------|------------------------|------------------------|----------------------------|----------------------------------|---------------|-----|--------------------------|
| | | | | | CHANNEL A: UART, IrDA, SPI | CHANNEL B: SPI, I ² C | | | |
| MSP430F5438A | 256 | 16 | 5, 3 | 7 | 4 | 4 | 14 ext, 2 int | 87 | 100 PZ, 113 ZCA, 113 ZQW |
| MSP430F5437A | 256 | 16 | 5, 3 | 7 | 2 | 2 | 14 ext, 2 int | 67 | 80 PN |
| MSP430F5436A | 192 | 16 | 5, 3 | 7 | 4 | 4 | 14 ext, 2 int | 87 | 100 PZ, 113 ZCA, 113 ZQW |
| MSP430F5435A | 192 | 16 | 5, 3 | 7 | 2 | 2 | 14 ext, 2 int | 67 | 80 PN |
| MSP430F5419A | 128 | 16 | 5, 3 | 7 | 4 | 4 | 14 ext, 2 int | 87 | 100 PZ, 113 ZCA, 113 ZQW |
| MSP430F5418A | 128 | 16 | 5, 3 | 7 | 2 | 2 | 14 ext, 2 int | 67 | 80 PN |

- (1) For the most current part, package, and ordering information, see the *Package Option Addendum* in [Section 11](#), or see the TI website at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators.

6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

[Products for TI Microcontrollers](#)

TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

[Products for MSP430 Ultra-Low-Power Microcontrollers](#)

One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

[Companion Products for MSP430F5438A](#)

Review products that are frequently purchased or used with this product.

[Reference Designs for MSP430F5438A](#)

Find reference designs that leverage the best in TI technology to solve your system-level challenges.

7 Terminal Configuration and Functions

7.1 Pin Diagrams

Figure 7-1 shows the pinout of the 100-pin PZ package for the MSP430F5438A, MSP430F5436A, and MSP430F5419A devices.

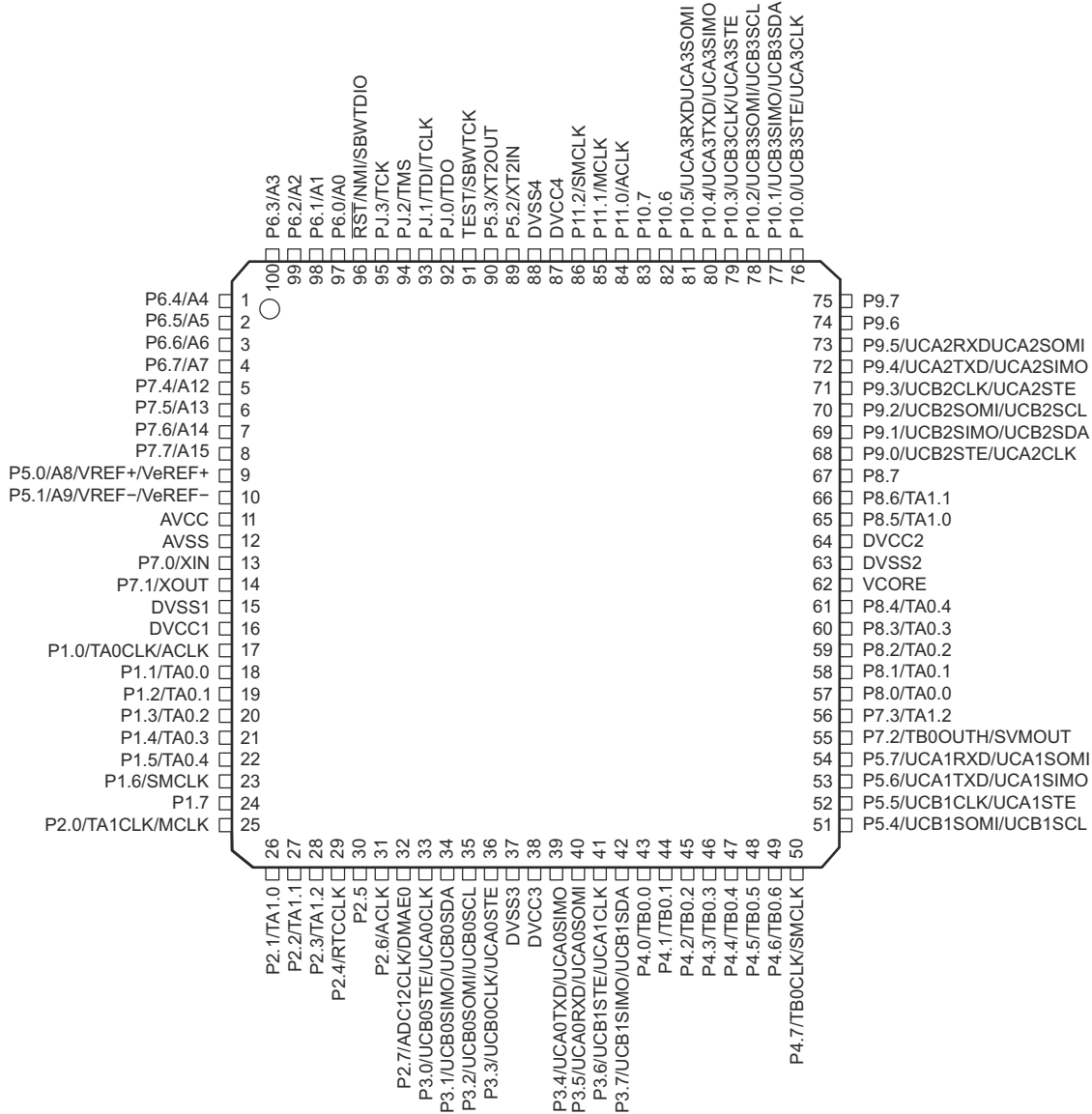


Figure 7-1. 100-Pin PZ Package (Top View) – MSP430F5438AIPZ, MSP430F5436AIPZ, MSP430F5419AIPZ

Figure 7-2 shows the pinout of the 80-pin PN package for the MSP430F5437A, MSP430F5435A, and MSP430F5418A devices.

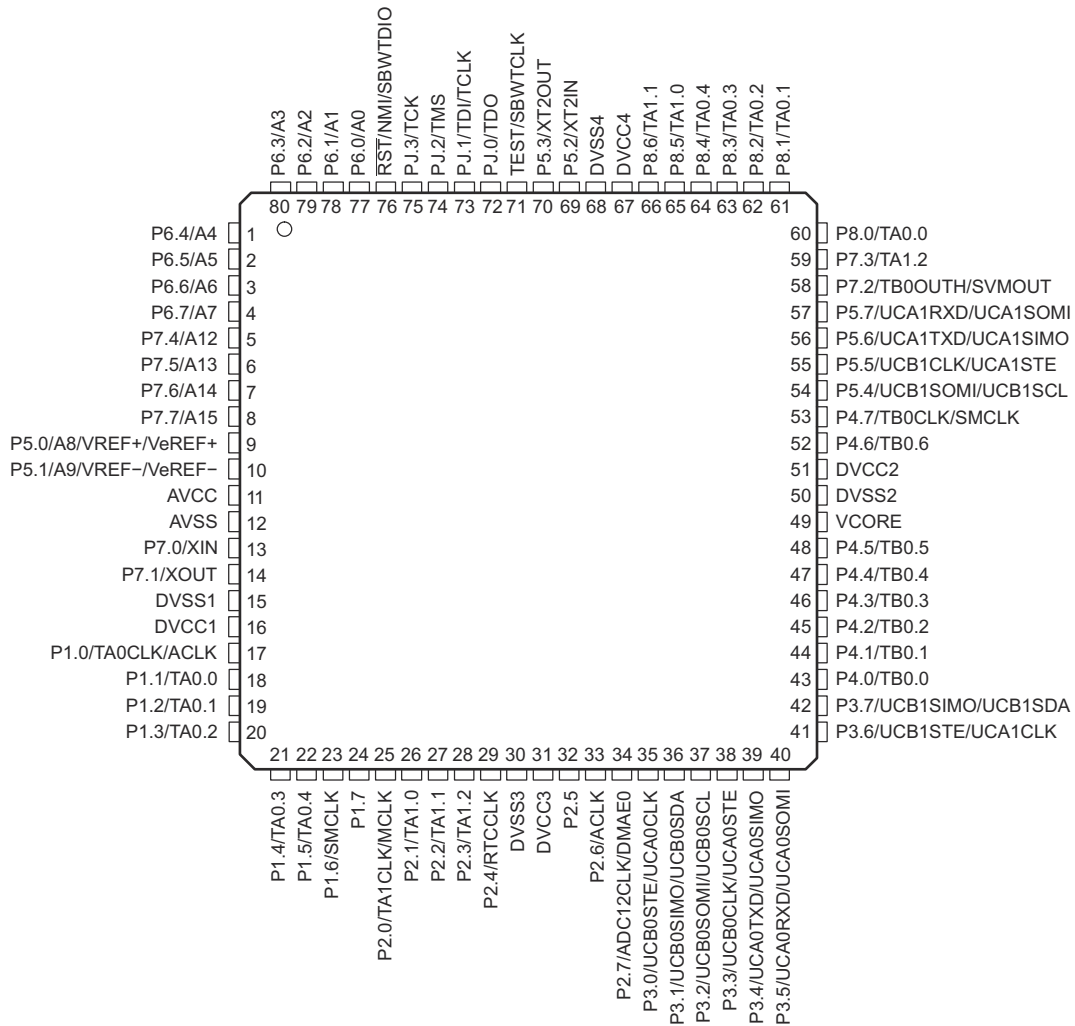


Figure 7-2. 80-Pin PN Package (Top View) – MSP430F5437AIPN, MSP430F5435AIPN, MSP430F5418AIPN

Figure 7-3 shows the pinout of the 113-pin ZCA or ZQW package for the MSP430F5438A, MSP430F5436A, and MSP430F5419A devices.

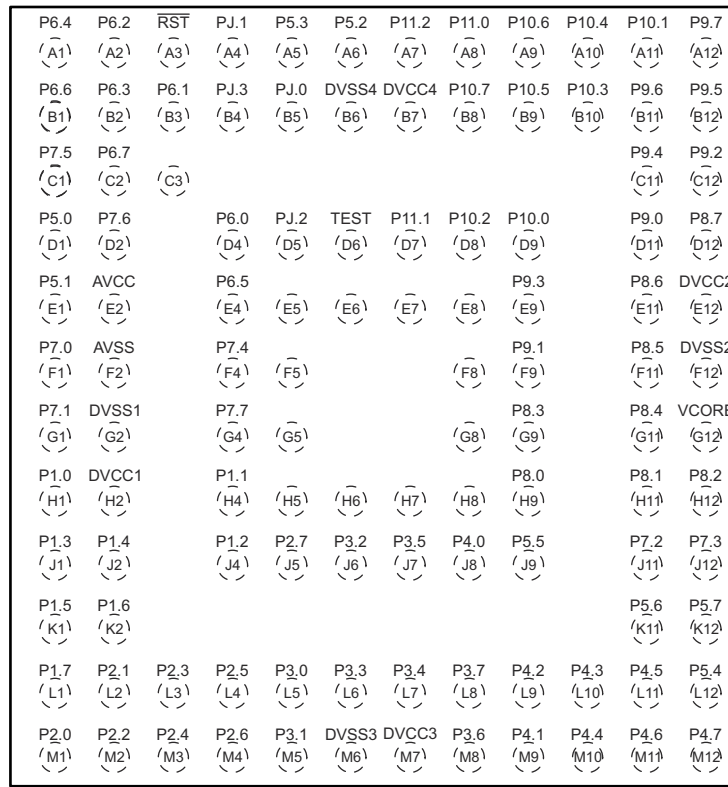


Figure 7-3. 113-Pin ZCA or ZQW Package (Top View) – MSP430F5438AIZCA, MSP430F5436AIZCA, MSP430F5419AIZCA, MSP430F5438AIZQW, MSP430F5436AIZQW, MSP430F5419AIZQW

7.2 Signal Descriptions

Section 7.2 describes the signals for all device variants and package options.

Table 7-1. Signal Descriptions

| TERMINAL | | | | I/O ⁽¹⁾ | DESCRIPTION |
|----------------------|-----|----|-------------|--------------------|--|
| NAME | NO. | | | | |
| | PZ | PN | ZCA, ZQW | | |
| P6.4/A4 | 1 | 1 | A1 | I/O | General-purpose digital I/O Analog input A4 for the ADC |
| P6.5/A5 | 2 | 2 | E4 | I/O | General-purpose digital I/O Analog input A5 for the ADC |
| P6.6/A6 | 3 | 3 | B1 | I/O | General-purpose digital I/O Analog input A6 for the ADC |
| P6.7/A7 | 4 | 4 | C2 | I/O | General-purpose digital I/O Analog input A7 for the ADC |
| P7.4/A12 | 5 | 5 | F4 | I/O | General-purpose digital I/O Analog input A12 for the ADC |
| P7.5/A13 | 6 | 6 | C1 | I/O | General-purpose digital I/O Analog input A13 for the ADC |
| P7.6/A14 | 7 | 7 | D2 | I/O | General-purpose digital I/O Analog input A14 for the ADC |
| P7.7/A15 | 8 | 8 | G4 | I/O | General-purpose digital I/O Analog input A15 for the ADC |
| P5.0/A8/VREF+/VeREF+ | 9 | 9 | D1 | I/O | General-purpose digital I/O Analog input A8 for the ADC Output of reference voltage to the ADC Input for an external reference voltage to the ADC |
| P5.1/A9/VREF-/VeREF- | 10 | 10 | E1 | I/O | General-purpose digital I/O Analog input A9 for the ADC Negative terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage |
| AVCC | 11 | 11 | E2 | | Analog power supply |
| AVSS | 12 | 12 | F2 | | Analog ground supply |
| P7.0/XIN | 13 | 13 | F1 | I/O | General-purpose digital I/O Input terminal for crystal oscillator XT1 |
| P7.1/XOUT | 14 | 14 | G1 | I/O | General-purpose digital I/O Output terminal of crystal oscillator XT1 |
| DVSS1 | 15 | 15 | G2 | | Digital ground supply |
| DVCC1 | 16 | 16 | H2 | | Digital power supply |
| P1.0/TA0CLK/ACLK | 17 | 17 | H1 | I/O | General-purpose digital I/O with port interrupt TA0 clock signal TACLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32) |
| P1.1/TA0.0 | 18 | 18 | H4 | I/O | General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output |
| P1.2/TA0.1 | 19 | 19 | J4 | I/O | General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input |
| P1.3/TA0.2 | 20 | 20 | J1 | I/O | General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output |
| P1.4/TA0.3 | 21 | 21 | J2 | I/O | General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output |
| P1.5/TA0.4 | 22 | 22 | K1 | I/O | General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output |

Table 7-1. Signal Descriptions (continued)

| TERMINAL | | | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------------------|-----|----|-------------|--------------------|---|
| NAME | NO. | | | | |
| | PZ | PN | ZCA, ZQW | | |
| P1.6/SMCLK | 23 | 23 | K2 | I/O | General-purpose digital I/O with port interrupt SMCLK output |
| P1.7 | 24 | 24 | L1 | I/O | General-purpose digital I/O with port interrupt |
| P2.0/TA1CLK/MCLK | 25 | 25 | M1 | I/O | General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input MCLK output |
| P2.1/TA1.0 | 26 | 26 | L2 | I/O | General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output |
| P2.2/TA1.1 | 27 | 27 | M2 | I/O | General-purpose digital I/O with port interrupt TA1 CCR1 capture: CCI1A input, compare: Out1 output |
| P2.3/TA1.2 | 28 | 28 | L3 | I/O | General-purpose digital I/O with port interrupt TA1 CCR2 capture: CCI2A input, compare: Out2 output |
| P2.4/RTCCLK | 29 | 29 | M3 | I/O | General-purpose digital I/O with port interrupt RTCCLK output |
| P2.5 | 30 | 32 | L4 | I/O | General-purpose digital I/O with port interrupt |
| P2.6/ACLK | 31 | 33 | M4 | I/O | General-purpose digital I/O with port interrupt ACLK output (divided by 1, 2, 4, 8, 16, or 32) |
| P2.7/ADC12CLK/DMAE0 | 32 | 34 | J5 | I/O | General-purpose digital I/O with port interrupt Conversion clock output for the ADC DMA external trigger input |
| P3.0/UCB0STE/UCA0CLK | 33 | 35 | L5 | I/O | General-purpose digital I/O Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode |
| P3.1/UCB0SIMO/UCB0SDA | 34 | 36 | M5 | I/O | General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I ² C data – USCI_B0 I ² C mode |
| P3.2/UCB0SOMI/UCB0SCL | 35 | 37 | J6 | I/O | General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I ² C clock – USCI_B0 I ² C mode |
| P3.3/UCB0CLK/UCA0STE | 36 | 38 | L6 | I/O | General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode |
| DVSS3 | 37 | 30 | M6 | | Digital ground supply |
| DVCC3 | 38 | 31 | M7 | | Digital power supply |
| P3.4/UCA0TXD/UCA0SIMO | 39 | 39 | L7 | I/O | General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode |
| P3.5/UCA0RXD/UCA0SOMI | 40 | 40 | J7 | I/O | General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode |
| P3.6/UCB1STE/UCA1CLK | 41 | 41 | M8 | I/O | General-purpose digital I/O Slave transmit enable – USCI_B1 SPI mode Clock signal input – USCI_A1 SPI slave mode Clock signal output – USCI_A1 SPI master mode |
| P3.7/UCB1SIMO/UCB1SDA | 42 | 42 | L8 | I/O | General-purpose digital I/O Slave in, master out – USCI_B1 SPI mode I ² C data – USCI_B1 I ² C mode |
| P4.0/TB0.0 | 43 | 43 | J8 | I/O | General-purpose digital I/O TB0 capture CCR0: CCI0A/CCI0B input, compare: Out0 output |

Table 7-1. Signal Descriptions (continued)

| TERMINAL | | | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------------------|-----|----|-------------|--------------------|---|
| NAME | NO. | | | | |
| | PZ | PN | ZCA, ZQW | | |
| P4.1/TB0.1 | 44 | 44 | M9 | I/O | General-purpose digital I/O TB0 capture CCR1: CCI1A/CCI1B input, compare: Out1 output |
| P4.2/TB0.2 | 45 | 45 | L9 | I/O | General-purpose digital I/O TB0 capture CCR2: CCI2A/CCI2B input, compare: Out2 output |
| P4.3/TB0.3 | 46 | 46 | L10 | I/O | General-purpose digital I/O TB0 capture CCR3: CCI3A/CCI3B input, compare: Out3 output |
| P4.4/TB0.4 | 47 | 47 | M10 | I/O | General-purpose digital I/O TB0 capture CCR4: CCI4A/CCI4B input, compare: Out4 output |
| P4.5/TB0.5 | 48 | 48 | L11 | I/O | General-purpose digital I/O TB0 capture CCR5: CCI5A/CCI5B input, compare: Out5 output |
| P4.6/TB0.6 | 49 | 52 | M11 | I/O | General-purpose digital I/O TB0 capture CCR6: CCI6A/CCI6B input, compare: Out6 output |
| P4.7/TB0CLK/SMCLK | 50 | 53 | M12 | I/O | General-purpose digital I/O TB0 clock input SMCLK output |
| P5.4/UCB1SOMI/UCB1SCL | 51 | 54 | L12 | I/O | General-purpose digital I/O Slave out, master in – USCI_B1 SPI mode I ² C clock – USCI_B1 I ² C mode |
| P5.5/UCB1CLK/UCA1STE | 52 | 55 | J9 | I/O | General-purpose digital I/O Clock signal input – USCI_B1 SPI slave mode Clock signal output – USCI_B1 SPI master mode Slave transmit enable – USCI_A1 SPI mode |
| P5.6/UCA1TXD/UCA1SIMO | 53 | 56 | K11 | I/O | General-purpose digital I/O Transmit data – USCI_A1 UART mode Slave in, master out – USCI_A1 SPI mode |
| P5.7/UCA1RXD/UCA1SOMI | 54 | 57 | K12 | I/O | General-purpose digital I/O Receive data – USCI_A1 UART mode Slave out, master in – USCI_A1 SPI mode |
| P7.2/TB0OUTH/SVMOUT | 55 | 58 | J11 | I/O | General-purpose digital I/O Switch all PWM outputs to high impedance – Timer TB0 SVM output |
| P7.3/TA1.2 | 56 | 59 | J12 | I/O | General-purpose digital I/O TA1 CCR2 capture: CCI2B input, compare: Out2 output |
| P8.0/TA0.0 | 57 | 60 | H9 | I/O | General-purpose digital I/O TA0 CCR0 capture: CCI0B input, compare: Out0 output |
| P8.1/TA0.1 | 58 | 61 | H11 | I/O | General-purpose digital I/O TA0 CCR1 capture: CCI1B input, compare: Out1 output |
| P8.2/TA0.2 | 59 | 62 | H12 | I/O | General-purpose digital I/O TA0 CCR2 capture: CCI2B input, compare: Out2 output |
| P8.3/TA0.3 | 60 | 63 | G9 | I/O | General-purpose digital I/O TA0 CCR3 capture: CCI3B input, compare: Out3 output |
| P8.4/TA0.4 | 61 | 64 | G11 | I/O | General-purpose digital I/O TA0 CCR4 capture: CCI4B input, compare: Out4 output |
| VCORE ⁽³⁾ | 62 | 49 | G12 | | Regulated core power supply output (internal use only, no external current loading) |
| DVSS2 | 63 | 50 | F12 | | Digital ground supply |
| DVCC2 | 64 | 51 | E12 | | Digital power supply |
| P8.5/TA1.0 | 65 | 65 | F11 | I/O | General-purpose digital I/O TA1 CCR0 capture: CCI0B input, compare: Out0 output |
| P8.6/TA1.1 | 66 | 66 | E11 | I/O | General-purpose digital I/O TA1 CCR1 capture: CCI1B input, compare: Out1 output |

Table 7-1. Signal Descriptions (continued)

| TERMINAL | | | | I/O ⁽¹⁾ | DESCRIPTION |
|------------------------|-----|-----|-------------|--------------------|---|
| NAME | NO. | | | | |
| | PZ | PN | ZCA, ZQW | | |
| P8.7 | 67 | N/A | D12 | I/O | General-purpose digital I/O |
| P9.0/UCB2STE/UCA2CLK | 68 | N/A | D11 | I/O | General-purpose digital I/O Slave transmit enable – USCI_B2 SPI mode Clock signal input – USCI_A2 SPI slave mode Clock signal output – USCI_A2 SPI master mode |
| P9.1/UCB2SIMO/UCB2SDA | 69 | N/A | F9 | I/O | General-purpose digital I/O Slave in, master out – USCI_B2 SPI mode I ² C data – USCI_B2 I ² C mode |
| P9.2/UCB2SOMI/UCB2SCL | 70 | N/A | C12 | I/O | General-purpose digital I/O Slave out, master in – USCI_B2 SPI mode I ² C clock – USCI_B2 I ² C mode |
| P9.3/UCB2CLK/UCA2STE | 71 | N/A | E9 | I/O | General-purpose digital I/O Clock signal input – USCI_B2 SPI slave mode Clock signal output – USCI_B2 SPI master mode Slave transmit enable – USCI_A2 SPI mode |
| P9.4/UCA2TXD/UCA2SIMO | 72 | N/A | C11 | I/O | General-purpose digital I/O Transmit data – USCI_A2 UART mode Slave in, master out – USCI_A2 SPI mode |
| P9.5/UCA2RXD/UCA2SOMI | 73 | N/A | B12 | I/O | General-purpose digital I/O Receive data – USCI_A2 UART mode Slave out, master in – USCI_A2 SPI mode |
| P9.6 | 74 | N/A | B11 | I/O | General-purpose digital I/O |
| P9.7 | 75 | N/A | A12 | I/O | General-purpose digital I/O |
| P10.0/UCB3STE/UCA3CLK | 76 | N/A | D9 | I/O | General-purpose digital I/O Slave transmit enable – USCI_B3 SPI mode Clock signal input – USCI_A3 SPI slave mode Clock signal output – USCI_A3 SPI master mode |
| P10.1/UCB3SIMO/UCB3SDA | 77 | N/A | A11 | I/O | General-purpose digital I/O Slave in, master out – USCI_B3 SPI mode I ² C data – USCI_B3 I ² C mode |
| P10.2/UCB3SOMI/UCB3SCL | 78 | N/A | D8 | I/O | General-purpose digital I/O Slave out, master in – USCI_B3 SPI mode I ² C clock – USCI_B3 I ² C mode |
| P10.3/UCB3CLK/UCA3STE | 79 | N/A | B10 | I/O | General-purpose digital I/O Clock signal input – USCI_B3 SPI slave mode Clock signal output – USCI_B3 SPI master mode Slave transmit enable – USCI_A3 SPI mode |
| P10.4/UCA3TXD/UCA3SIMO | 80 | N/A | A10 | I/O | General-purpose digital I/O Transmit data – USCI_A3 UART mode Slave in, master out – USCI_A3 SPI mode |
| P10.5/UCA3RXD/UCA3SOMI | 81 | N/A | B9 | I/O | General-purpose digital I/O Receive data – USCI_A3 UART mode Slave out, master in – USCI_A3 SPI mode |
| P10.6 | 82 | N/A | A9 | I/O | General-purpose digital I/O |
| P10.7 | 83 | N/A | B8 | I/O | General-purpose digital I/O |
| P11.0/ACLK | 84 | N/A | A8 | I/O | General-purpose digital I/O ACLK output (divided by 1, 2, 4, 8, 16, or 32) |
| P11.1/MCLK | 85 | N/A | D7 | I/O | General-purpose digital I/O MCLK output |
| P11.2/SMCLK | 86 | N/A | A7 | I/O | General-purpose digital I/O SMCLK output |
| DVCC4 | 87 | 67 | B7 | | Digital power supply |

Table 7-1. Signal Descriptions (continued)

| TERMINAL | | | | I/O ⁽¹⁾ | DESCRIPTION |
|-------------------------------|-----|-----|-------------|--------------------|---|
| NAME | NO. | | | | |
| | PZ | PN | ZCA, ZQW | | |
| DVSS4 | 88 | 68 | B6 | | Digital ground supply |
| P5.2/XT2IN | 89 | 69 | A6 | I/O | General-purpose digital I/O Input terminal for crystal oscillator XT2 |
| P5.3/XT2OUT | 90 | 70 | A5 | I/O | General-purpose digital I/O Output terminal of crystal oscillator XT2 |
| TEST/SBWTCK ⁽⁴⁾ | 91 | 71 | D6 | I | Test mode pin – Selects four wire JTAG operation. Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated |
| PJ.0/TDO ⁽⁵⁾ | 92 | 72 | B5 | I/O | General-purpose digital I/O JTAG test data output port |
| PJ.1/TDI/TCLK ⁽⁵⁾ | 93 | 73 | A4 | I/O | General-purpose digital I/O JTAG test data input or test clock input |
| PJ.2/TMS ⁽⁵⁾ | 94 | 74 | D5 | I/O | General-purpose digital I/O JTAG test mode select |
| PJ.3/TCK ⁽⁵⁾ | 95 | 75 | B4 | I/O | General-purpose digital I/O JTAG test clock |
| RST/NMI/SBWDIO ⁽⁴⁾ | 96 | 76 | A3 | I/O | Reset input active low ⁽⁶⁾ Nonmaskable interrupt input Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated. |
| P6.0/A0 | 97 | 77 | D4 | I/O | General-purpose digital I/O Analog input A0 for the ADC |
| P6.1/A1 | 98 | 78 | B3 | I/O | General-purpose digital I/O Analog input A1 for the ADC |
| P6.2/A2 | 99 | 79 | A2 | I/O | General-purpose digital I/O Analog input A2 for the ADC |
| P6.3/A3 | 100 | 80 | B2 | I/O | General-purpose digital I/O Analog input A3 for the ADC |
| Reserved | N/A | N/A | (2) | | |

- (1) I = input, O = output, N/A = not available on this package offering
(2) C3, E5, E6, E7, E8, F5, F8, G5, G8, H5, H6, H7, H8 are reserved and should be connected to ground.
(3) V_{CORE} is for internal use only. No external current loading is possible. V_{CORE} should be connected to only the recommended capacitor value, C_{V_{CORE}}.
(4) See [Section 9.5](#) and [Section 9.6](#) for use with BSL and JTAG functions, respectively.
(5) See [Section 9.6](#) for use with JTAG function.
(6) When this pin is configured as reset, the internal pullup resistor is enabled by default.

8 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|--|------|----------------|------|
| Voltage applied at V_{CC} to V_{SS} ⁽¹⁾ | -0.3 | 4.1 | V |
| Voltage applied to any pin (excluding V _{CORE}) ⁽²⁾ | -0.3 | $V_{CC} + 0.3$ | V |
| Diode current at any device pin | | ±2 | mA |
| Storage temperature, T_{stg} ⁽³⁾ | -55 | 105 | °C |
| Maximum junction temperature, T_J | | 95 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . V_{CORE} is for internal device use only. No external DC loading or voltage should be applied.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

8.2 ESD Ratings

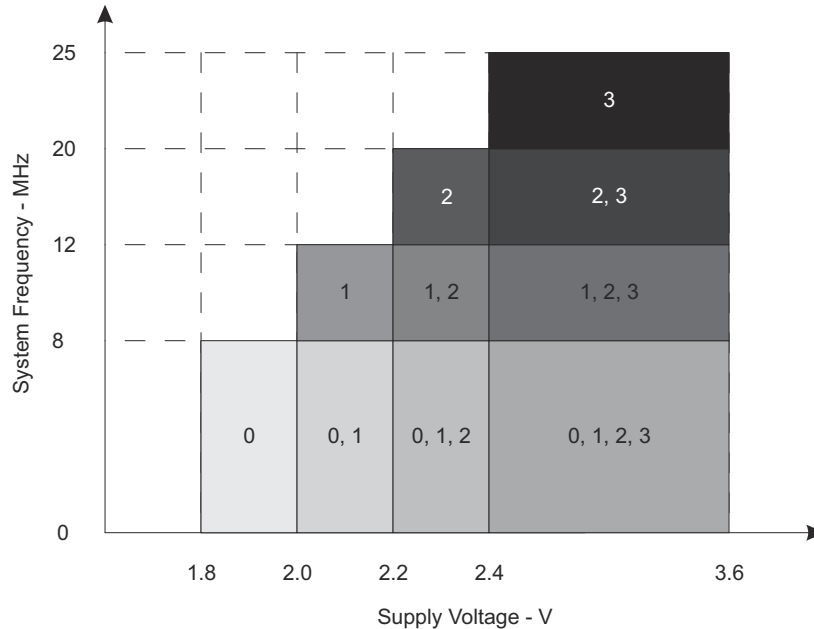
| | | VALUE | UNIT |
|-------------------------------------|--|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±1000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±250 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

8.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT | |
|----------------------------|---|---|-----|-----|------|-----|
| V_{CC} | Supply voltage during program execution and flash programming ($AV_{CC} = DV_{CC1/2/3/4} = DV_{CC}$) ^{(1) (2)} | 1.8 | | 3.6 | V | |
| V_{SS} | Supply voltage ($AV_{SS} = DV_{SS1/2/3/4} = DV_{SS}$) | | 0 | | V | |
| T_A | Operating free-air temperature | -40 | | 85 | °C | |
| T_J | Operating junction temperature | -40 | | 85 | °C | |
| $C_{V_{CORE}}$ | Recommended capacitor at V _{CORE} ⁽³⁾ | | 470 | | nF | |
| $C_{DV_{CC}}/C_{V_{CORE}}$ | Capacitor ratio of DV _{CC} to V _{CORE} | 10 | | | | |
| f_{SYSTEM} | Processor frequency (maximum MCLK frequency) ^{(4) (5)} (see Figure 8-1) | PMMCOREVx = 0, $1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | | 0 | 8 | MHz |
| | | PMMCOREVx = 1, $2.0\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | | 0 | 12 | |
| | | PMMCOREVx = 2, $2.2\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | | 0 | 20 | |
| | | PMMCOREVx = 3, $2.4\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | | 0 | 25 | |

- (1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
- (2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the [Section 8.23](#) threshold parameters for the exact values and further details.
- (3) A capacitor tolerance of ±20% or better is required.
- (4) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
- (5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

Figure 8-1. Frequency vs Supply Voltage

8.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾ ⁽³⁾

| PARAMETER | EXECUTION MEMORY | V_{CC} | PMMCOREVx | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | UNIT | | |
|-----------------|------------------|----------|-----------|--|------|-------|------|--------|------|--------|------|------|--------|-----|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 20 MHz | | | 25 MHz | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | | TYP | MAX |
| $I_{AM, Flash}$ | Flash | 3.0 V | 0 | 0.29 | 0.33 | 1.84 | 2.08 | | | | | | | mA |
| | | | 1 | 0.32 | | 2.08 | | 3.10 | | | | | | |
| | | | 2 | 0.33 | | 2.24 | | 3.50 | 6.37 | | | | | |
| | | | 3 | 0.35 | | 2.36 | | 3.70 | 6.75 | 8.90 | 9.60 | | | |
| $I_{AM, RAM}$ | RAM | 3.0 V | 0 | 0.17 | 0.19 | 0.88 | 0.99 | | | | | | | mA |
| | | | 1 | 0.18 | | 1.00 | | 1.47 | | | | | | |
| | | | 2 | 0.19 | | 1.13 | | 1.68 | 2.82 | | | | | |
| | | | 3 | 0.20 | | 1.20 | | 1.78 | 3.00 | 4.50 | 4.90 | | | |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Characterized with program executing typical data processing.
 $f_{ACLK} = 32768$ Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

8.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | V_{CC} | PMMCOREVx | -40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|--|----------|-----------|-------|------|------|------|------|------|------|------|---------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ Low-power mode 0 ^{(3) (9)} | 2.2 V | 0 | 69 | 93 | 69 | 93 | 69 | 93 | 69 | 93 | μA |
| | 3.0 V | 3 | 73 | 100 | 73 | 100 | 73 | 100 | 73 | 100 | |
| I_{LPM2} Low-power mode 2 ^{(4) (9)} | 2.2 V | 0 | 11 | 15.5 | 11 | 15.5 | 11 | 15.5 | 11 | 15.5 | μA |
| | 3.0 V | 3 | 11.7 | 17.5 | 11.7 | 17.5 | 11.7 | 17.5 | 11.7 | 17.5 | |
| $I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode ^{(5) (9)} | 2.2 V | 0 | 1.4 | | 1.7 | | 2.6 | | 6.6 | | μA |
| | | 1 | 1.5 | | 1.8 | | 2.9 | | 9.9 | | |
| | | 2 | 1.5 | | 2.0 | | 3.3 | | 10.1 | | |
| | 3.0 V | 0 | 1.8 | | 2.1 | 2.4 | 2.8 | | 7.1 | 13.6 | |
| | | 1 | 1.8 | | 2.3 | | 3.1 | | 10.5 | | |
| | | 2 | 1.9 | | 2.4 | | 3.5 | | 10.6 | | |
| $I_{LPM3,VLO}$ Low-power mode 3, VLO mode ^{(6) (9)} | 3.0 V | 3 | 2.0 | | 2.3 | 2.6 | 3.9 | | 11.8 | 14.8 | |
| | | 0 | 1.0 | | 1.2 | 1.42 | 2.0 | | 5.8 | 12.9 | |
| | | 1 | 1.0 | | 1.3 | | 2.3 | | 6.0 | | |
| | | 2 | 1.1 | | 1.4 | | 2.8 | | 6.2 | | |
| I_{LPM4} Low-power mode 4 ^{(7) (9)} | 3.0 V | 3 | 1.2 | | 1.4 | 1.62 | 3.0 | | 6.2 | 13.9 | |
| | | 0 | 1.1 | | 1.2 | 1.35 | 1.9 | | 5.7 | 12.9 | |
| | | 1 | 1.2 | | 1.2 | | 2.2 | | 5.9 | | |
| | | 2 | 1.3 | | 1.3 | | 2.6 | | 6.1 | | |
| $I_{LPM4.5}$ Low-power mode 4.5 ⁽⁸⁾ | 3.0 V | 3 | 1.3 | | 1.3 | 1.52 | 2.9 | | 6.2 | 13.9 | |
| | | 0 | 0.10 | | 0.10 | 0.13 | 0.20 | | 0.50 | 1.14 | |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
- (4) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz, DCO setting = 1 MHz operation, DCO bias generator enabled.
- (5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
- (6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = f_{VLO} , f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
- (7) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
- (8) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
- (9) Current for brownout, high side supervisor (SVSH) normal mode included. Low-side supervisor (SVSL) and low-side monitor (SVM_L) disabled. High-side monitor (SVM_H) disabled. RAM retention enabled.

8.6 Thermal Resistance Characteristics

| THERMAL METRIC | | | VALUE | UNIT | |
|--------------------|--|------------------------|-----------|------|------|
| R θ_{JA} | Junction-to-ambient thermal resistance, still air | Low-K board (JESD51-3) | LQFP (PZ) | 50.1 | °C/W |
| | | | LQFP (PN) | 57.9 | |
| | | | BGA (ZQW) | 60 | |
| | High-K board (JESD51-7) | LQFP (PZ) | 40.8 | | |
| | | LQFP (PN) | 37.9 | | |
| | | BGA (ZQW) | 42 | | |
| See (1) and (2) | nFBGA (ZCA) | 36.2 | | | |
| R θ_{JC} | Junction-to-case thermal resistance (1) (2) | LQFP (PZ) | 8.9 | °C/W | |
| | | LQFP (PN) | 10.3 | | |
| | | BGA (ZQW) | 8 | | |
| R θ_{JcTop} | Junction-to-case (top) thermal resistance (1) (2) | | 13.5 | °C/W | |
| R θ_{JB} | Junction-to-board thermal resistance (1) (2) | | 14.5 | °C/W | |
| Ψ_{JT} | Junction-to-top characterization parameter (1) (2) | | 0.3 | °C/W | |
| Ψ_{JB} | Junction-to-board characterization parameter (1) (2) | | 14.3 | °C/W | |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).
(2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).

8.7 Schmitt-Trigger Inputs – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER ⁽¹⁾ | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------|---|--|------|-----|------|------------|
| V _{IT+} | Positive-going input threshold voltage | 1.8 V | 0.80 | | 1.40 | V |
| | | 3 V | 1.50 | | 2.10 | |
| V _{IT-} | Negative-going input threshold voltage | 1.8 V | 0.45 | | 1.00 | V |
| | | 3 V | 0.75 | | 1.65 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | 1.8 V | 0.3 | | 0.85 | V |
| | | 3 V | 0.4 | | 1.0 | |
| R _{Pull} | Pullup or pulldown resistor ⁽²⁾ | For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC} | 20 | 35 | 50 | k Ω |
| C _I | Input capacitance | V _{IN} = V _{SS} or V _{CC} | | 5 | | pF |

- (1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).
(2) Also applies to the \overline{RST} pin when the pullup or pulldown resistor is enabled.

8.8 Inputs – Ports P1 and P2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER ⁽¹⁾ | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--------------------------|--|--|------------|-----|------|
| t _(int) | External interrupt timing ⁽²⁾ | Port P1, P2: P1.x to P2.x, external trigger pulse duration to set interrupt flag | 2.2 V, 3 V | 20 | ns |

- (1) Some devices may contain additional ports with interrupts. See the block diagram (see [Section 4](#)) and signal descriptions (see [Section 7.2](#)).
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

8.9 Leakage Current – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|------------------------|--------------------------------|-----------------|-----------------|-----|-----|------|
| I _{lkg(Px,y)} | High-impedance leakage current | See (1) (2) | 1.8 V, 3 V | | ±50 | nA |

- (1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
 (2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

8.10 Outputs – General-Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|--|-----------------|------------------------|------------------------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = -3 mA ⁽¹⁾ | 1.8 V | V _{CC} - 0.25 | V _{CC} | V |
| | | I _(OHmax) = -10 mA ⁽²⁾ | | V _{CC} - 0.60 | V _{CC} | |
| | | I _(OHmax) = -5 mA ⁽¹⁾ | 3 V | V _{CC} - 0.25 | V _{CC} | |
| | | I _(OHmax) = -15 mA ⁽²⁾ | | V _{CC} - 0.60 | V _{CC} | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 3 mA ⁽¹⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | | I _(OLmax) = 10 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | | I _(OLmax) = 5 mA ⁽¹⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | |
| | | I _(OLmax) = 15 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |

- (1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

8.11 Outputs – General-Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|---|-----------------|------------------------|------------------------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = -1 mA ⁽¹⁾ | 1.8 V | V _{CC} - 0.25 | V _{CC} | V |
| | | I _(OHmax) = -3 mA ⁽²⁾ | | V _{CC} - 0.60 | V _{CC} | |
| | | I _(OHmax) = -2 mA ⁽¹⁾ | 3.0 V | V _{CC} - 0.25 | V _{CC} | |
| | | I _(OHmax) = -6 mA ⁽²⁾ | | V _{CC} - 0.60 | V _{CC} | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 1 mA ⁽¹⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | | I _(OLmax) = 3 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | | I _(OLmax) = 2 mA ⁽¹⁾ | 3.0 V | V _{SS} | V _{SS} + 0.25 | |
| | | I _(OLmax) = 6 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |

- (1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.
- (3) Selecting reduced drive strength may reduce EMI.

8.12 Output Frequency – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------------|-----------------------------------|---|--|-----|------|
| f _{Px.y} | Port output frequency (with load) | P1.6/SMCLK ⁽¹⁾ ⁽²⁾ | V _{CC} = 1.8 V, PMMCOREV _x = 0 | 16 | MHz |
| | | | V _{CC} = 3 V, PMMCOREV _x = 3 | 25 | |
| f _{Port_CLK} | Clock output frequency | P1.0/TA0CLK/ACLK P1.6/SMCLK P2.0/TA1CLK/MCLK C _L = 20 pF ⁽²⁾ | V _{CC} = 1.8 V, PMMCOREV _x = 0 | 16 | MHz |
| | | | V _{CC} = 3 V, PMMCOREV _x = 3 | 25 | |

- (1) A resistive divider with 2 × R₁ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R₁ = 550 Ω. For reduced drive strength, R₁ = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

8.13 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

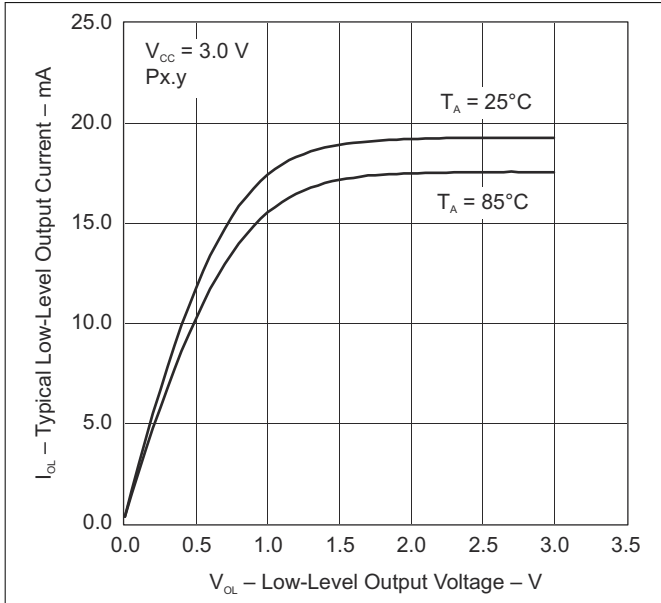


Figure 8-2. Typical Low-Level Output Current vs Low-Level Output Voltage

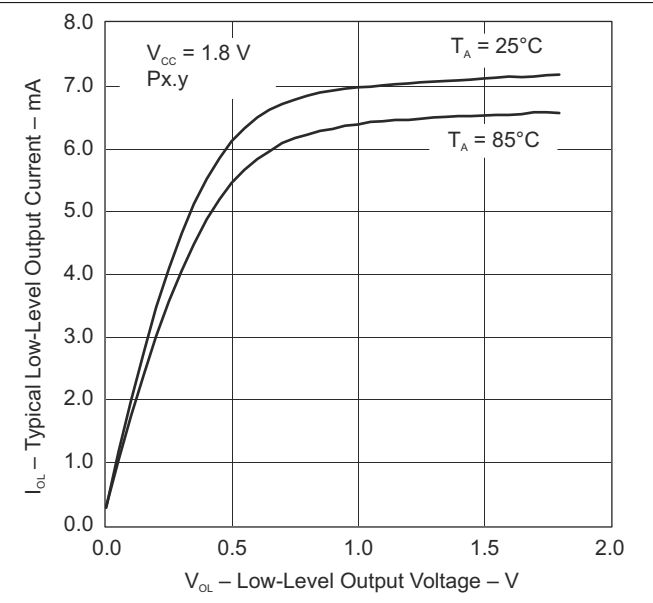


Figure 8-3. Typical Low-Level Output Current vs Low-Level Output Voltage

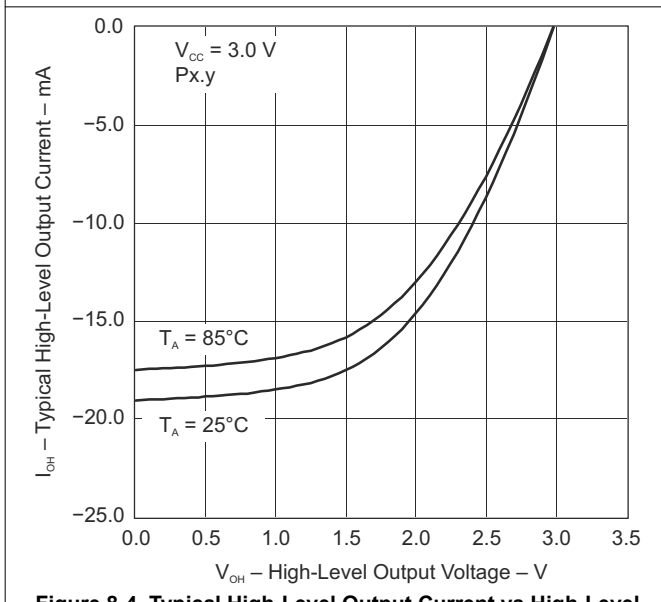


Figure 8-4. Typical High-Level Output Current vs High-Level Output Voltage

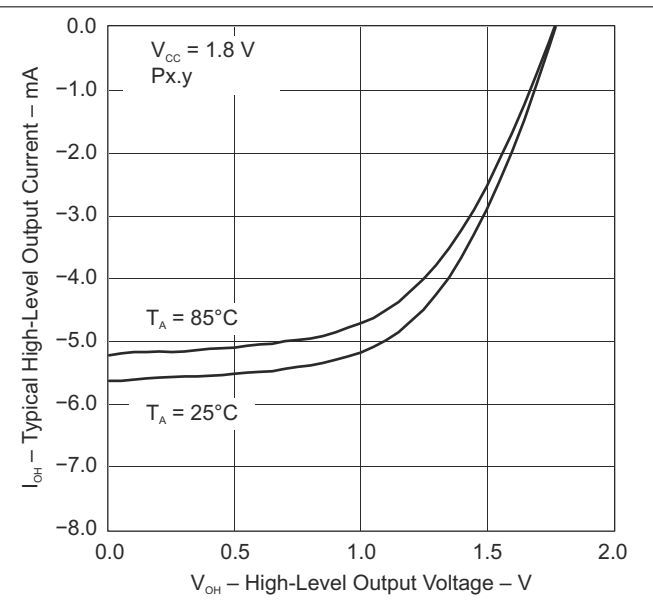


Figure 8-5. Typical High-Level Output Current vs High-Level Output Voltage

8.14 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

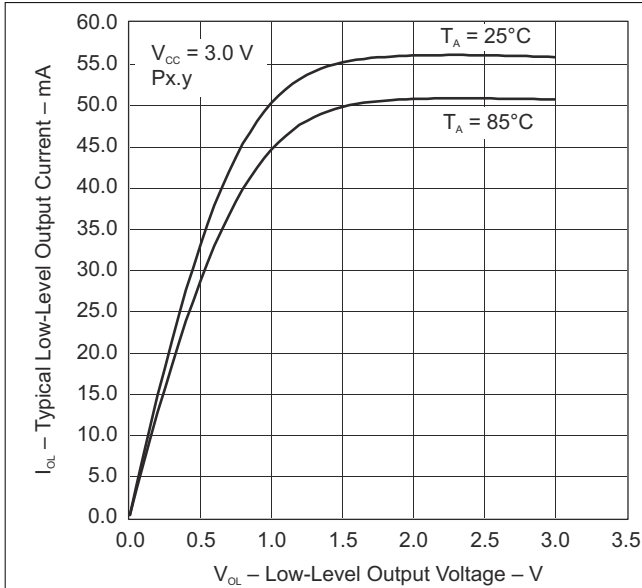


Figure 8-6. Typical Low-Level Output Current vs Low-Level Output Voltage

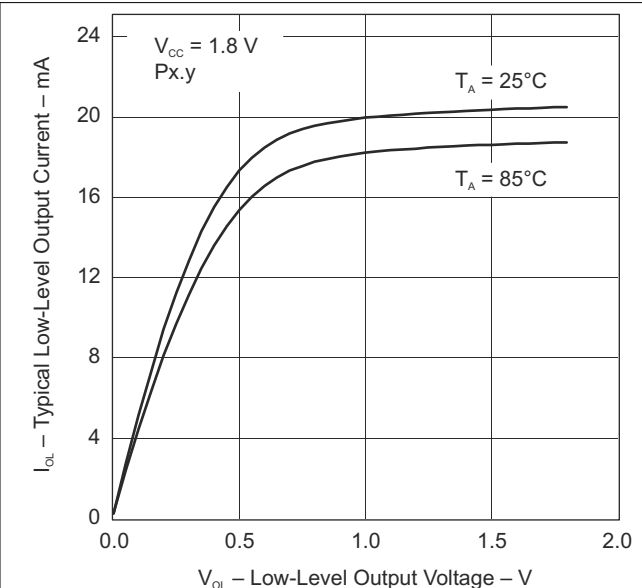


Figure 8-7. Typical Low-Level Output Current vs Low-Level Output Voltage

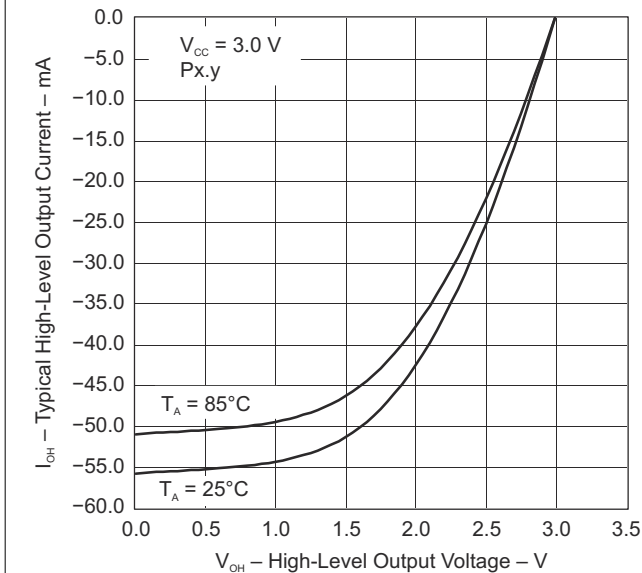


Figure 8-8. Typical High-Level Output Current vs High-Level Output Voltage

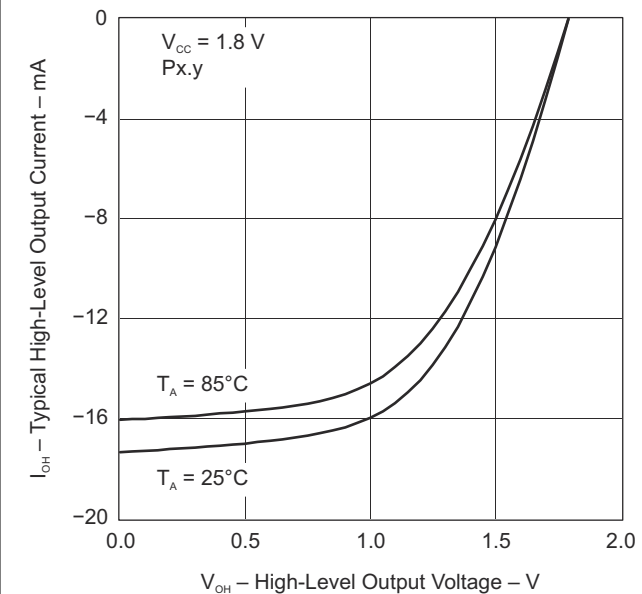


Figure 8-9. Typical High-Level Output Current vs High-Level Output Voltage

8.15 Crystal Oscillator, XT1, Low-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------|--|--|-----------------|-------|--------|------------|------|
| $\Delta I_{DVCC,LF}$ | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C | 3.0 V | 0.075 | | μ A | |
| | | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C | | 0.170 | | | |
| | | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C | | 0.290 | | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | XTS = 0, XT1BYPASS = 0 | | 32768 | | Hz | |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, XT1BYPASS = 1 ⁽²⁾ ⁽³⁾ | | 10 | 32.768 | 50 | kHz |
| OA_{LF} | Oscillation allowance for LF crystals ⁽⁴⁾ | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 6 pF | | 210 | | k Ω | |
| | | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 12 pF | | 300 | | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode ⁽⁵⁾ | XTS = 0, XCAP _x = 0 ⁽⁶⁾ | | 1 | | pF | |
| | | XTS = 0, XCAP _x = 1 | | 5.5 | | | |
| | | XTS = 0, XCAP _x = 2 | | 8.5 | | | |
| | | XTS = 0, XCAP _x = 3 | | 12.0 | | | |
| | Duty cycle, LF mode | XTS = 0, Measured at ACLK, $f_{XT1,LF} = 32768$ Hz | | 30% | | 70% | |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode ⁽⁷⁾ | XTS = 0 ⁽⁸⁾ | | 10 | | 10000 | Hz |
| $t_{START,LF}$ | Start-up time, LF mode | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 6 pF | 3.0 V | 1000 | | ms | |
| | | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C, C _{L,eff} = 12 pF | | 500 | | | |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE_x settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVE_x = 0, C_{L,eff} ≤ 6 pF.
 - For XT1DRIVE_x = 1, 6 pF ≤ C_{L,eff} ≤ 9 pF.
 - For XT1DRIVE_x = 2, 6 pF ≤ C_{L,eff} ≤ 10 pF.
 - For XT1DRIVE_x = 3, C_{L,eff} ≥ 6 pF.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

8.16 Crystal Oscillator, XT1, High-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------|---|---|-----------------|-----|-----|-----|------|
| I _{DVCC,HF} | XT1 oscillator crystal current, HF mode | f _{OSC} = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C | 3.0 V | | 200 | | μA |
| | | f _{OSC} = 12 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C | | | 260 | | |
| | | f _{OSC} = 20 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C | | | 325 | | |
| | | f _{OSC} = 32 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C | | | 450 | | |
| f _{XT1,HF0} | XT1 oscillator crystal frequency, HF mode 0 | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 0 ⁽²⁾ | | 4 | | 8 | MHz |
| f _{XT1,HF1} | XT1 oscillator crystal frequency, HF mode 1 | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 1 ⁽²⁾ | | 8 | | 16 | MHz |
| f _{XT1,HF2} | XT1 oscillator crystal frequency, HF mode 2 | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 2 ⁽²⁾ | | 16 | | 24 | MHz |
| f _{XT1,HF3} | XT1 oscillator crystal frequency, HF mode 3 | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 3 ⁽²⁾ | | 24 | | 32 | MHz |
| f _{XT1,HF,SW} | XT1 oscillator logic-level square-wave input frequency, HF mode, bypass mode | XTS = 1, XT1BYPASS = 1 ⁽³⁾ ⁽²⁾ | | 0.7 | | 32 | MHz |
| O _{AHF} | Oscillation allowance for HF crystals ⁽⁴⁾ | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 0, f _{XT1,HF} = 6 MHz, C _{L,eff} = 15 pF | | | 450 | | Ω |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 1, f _{XT1,HF} = 12 MHz, C _{L,eff} = 15 pF | | | 320 | | |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 2, f _{XT1,HF} = 20 MHz, C _{L,eff} = 15 pF | | | 200 | | |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 3, f _{XT1,HF} = 32 MHz, C _{L,eff} = 15 pF | | | 200 | | |
| t _{START,HF} | Start-up time, HF mode | f _{OSC} = 6 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 15 pF | 3.0 V | | 0.5 | | ms |
| | | f _{OSC} = 20 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C, C _{L,eff} = 15 pF | | | 0.3 | | |
| C _{L,eff} | Integrated effective load capacitance, HF mode ⁽⁵⁾ ⁽⁶⁾ | XTS = 1 | | | 1 | | pF |
| | Duty cycle, HF mode | XTS = 1, Measured at ACLK, f _{XT1,HF2} = 20 MHz | | 40% | 50% | 60% | |
| f _{FAULT,HF} | Oscillator fault frequency, HF mode ⁽⁷⁾ | XTS = 1 ⁽⁸⁾ | | 30 | | 300 | kHz |

(1) To improve EMI on the XT1 oscillator the following guidelines should be observed.

- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceeded for a given range of operation.

- (3) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. In general, an effective load capacitance of up to 18 pF can be supported.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

8.17 Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|---|--|-----------------|-----|-----|-----|------|
| I _{DVCC,XT2} | XT2 oscillator crystal current consumption | f _{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C | 3.0 V | | 200 | | μA |
| | | f _{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 1, T _A = 25°C | | | 260 | | |
| | | f _{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C | | | 325 | | |
| | | f _{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 3, T _A = 25°C | | | 450 | | |
| f _{XT2,HF0} | XT2 oscillator crystal frequency, mode 0 | XT2DRIVE _x = 0, XT2BYPASS = 0 ⁽³⁾ | | 4 | | 8 | MHz |
| f _{XT2,HF1} | XT2 oscillator crystal frequency, mode 1 | XT2DRIVE _x = 1, XT2BYPASS = 0 ⁽³⁾ | | 8 | | 16 | MHz |
| f _{XT2,HF2} | XT2 oscillator crystal frequency, mode 2 | XT2DRIVE _x = 2, XT2BYPASS = 0 ⁽³⁾ | | 16 | | 24 | MHz |
| f _{XT2,HF3} | XT2 oscillator crystal frequency, mode 3 | XT2DRIVE _x = 3, XT2BYPASS = 0 ⁽³⁾ | | 24 | | 32 | MHz |
| f _{XT2,HF,SW} | XT2 oscillator logic-level square-wave input frequency, bypass mode | XT2BYPASS = 1 ^{(4) (3)} | | 0.7 | | 32 | MHz |
| O _{A,HF} | Oscillation allowance for HF crystals ⁽⁵⁾ | XT2DRIVE _x = 0, XT2BYPASS = 0, f _{XT2,HF0} = 6 MHz, C _{L,eff} = 15 pF | | | 450 | | Ω |
| | | XT2DRIVE _x = 1, XT2BYPASS = 0, f _{XT2,HF1} = 12 MHz, C _{L,eff} = 15 pF | | | 320 | | |
| | | XT2DRIVE _x = 2, XT2BYPASS = 0, f _{XT2,HF2} = 20 MHz, C _{L,eff} = 15 pF | | | 200 | | |
| | | XT2DRIVE _x = 3, XT2BYPASS = 0, f _{XT2,HF3} = 32 MHz, C _{L,eff} = 15 pF | | | 200 | | |
| t _{START,HF} | Start-up time | f _{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 15 pF | 3.0 V | | 0.5 | | ms |
| | | f _{OSC} = 20 MHz, XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C, C _{L,eff} = 15 pF | | | 0.3 | | |
| C _{L,eff} | Integrated effective load capacitance, HF mode ^{(6) (1)} | | | | 1 | | pF |
| | Duty cycle | Measured at ACLK, f _{XT2,HF2} = 20 MHz | | 40% | 50% | 60% | |
| f _{Fault,HF} | Oscillator fault frequency ⁽⁷⁾ | XT2BYPASS = 1 ⁽⁸⁾ | | 30 | | 300 | kHz |

- (1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. In general, an effective load capacitance of up to 18 pF can be supported.
- (2) To improve EMI on the XT2 oscillator the following guidelines should be observed.

- Keep the traces between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
 - Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.
 - (4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
 - (5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
 - (6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
 - (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
 - (8) Measured with logic-level input frequency but also applies to operation with crystals.

8.18 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.4 | 14 | kHz |
| df _{VLO} /dT | VLO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 4 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

8.19 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------------------|-------------------------------------|---------------------------------|-----------------|-----|-------|-------|------|
| I _{REFO} | REFO oscillator current consumption | T _A = 25°C | 1.8 V to 3.6 V | | 3 | | μA |
| f _{REFO} | REFO frequency calibrated | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance calibrated | Full temperature range | 1.8 V to 3.6 V | | | ±3.5% | |
| | | T _A = 25°C | 3 V | | | ±1.5% | |
| df _{REFO} /dT | REFO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| df _{REFO} /dV _{CC} | REFO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 1.0 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| t _{START} | REFO start-up time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | μs |

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

8.20 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|--|------|------|-------|
| $f_{DCO(0,0)}$ | DCO frequency (0, 0) ⁽¹⁾ | DCORSELx = 0, DCOx = 0, MODx = 0 | 0.07 | 0.20 | MHz |
| $f_{DCO(0,31)}$ | DCO frequency (0, 31) ⁽¹⁾ | DCORSELx = 0, DCOx = 31, MODx = 0 | 0.70 | 1.70 | MHz |
| $f_{DCO(1,0)}$ | DCO frequency (1, 0) ⁽¹⁾ | DCORSELx = 1, DCOx = 0, MODx = 0 | 0.15 | 0.36 | MHz |
| $f_{DCO(1,31)}$ | DCO frequency (1, 31) ⁽¹⁾ | DCORSELx = 1, DCOx = 31, MODx = 0 | 1.47 | 3.45 | MHz |
| $f_{DCO(2,0)}$ | DCO frequency (2, 0) ⁽¹⁾ | DCORSELx = 2, DCOx = 0, MODx = 0 | 0.32 | 0.75 | MHz |
| $f_{DCO(2,31)}$ | DCO frequency (2, 31) ⁽¹⁾ | DCORSELx = 2, DCOx = 31, MODx = 0 | 3.17 | 7.38 | MHz |
| $f_{DCO(3,0)}$ | DCO frequency (3, 0) ⁽¹⁾ | DCORSELx = 3, DCOx = 0, MODx = 0 | 0.64 | 1.51 | MHz |
| $f_{DCO(3,31)}$ | DCO frequency (3, 31) ⁽¹⁾ | DCORSELx = 3, DCOx = 31, MODx = 0 | 6.07 | 14.0 | MHz |
| $f_{DCO(4,0)}$ | DCO frequency (4, 0) ⁽¹⁾ | DCORSELx = 4, DCOx = 0, MODx = 0 | 1.3 | 3.2 | MHz |
| $f_{DCO(4,31)}$ | DCO frequency (4, 31) ⁽¹⁾ | DCORSELx = 4, DCOx = 31, MODx = 0 | 12.3 | 28.2 | MHz |
| $f_{DCO(5,0)}$ | DCO frequency (5, 0) ⁽¹⁾ | DCORSELx = 5, DCOx = 0, MODx = 0 | 2.5 | 6.0 | MHz |
| $f_{DCO(5,31)}$ | DCO frequency (5, 31) ⁽¹⁾ | DCORSELx = 5, DCOx = 31, MODx = 0 | 23.7 | 54.1 | MHz |
| $f_{DCO(6,0)}$ | DCO frequency (6, 0) ⁽¹⁾ | DCORSELx = 6, DCOx = 0, MODx = 0 | 4.6 | 10.7 | MHz |
| $f_{DCO(6,31)}$ | DCO frequency (6, 31) ⁽¹⁾ | DCORSELx = 6, DCOx = 31, MODx = 0 | 39.0 | 88.0 | MHz |
| $f_{DCO(7,0)}$ | DCO frequency (7, 0) ⁽¹⁾ | DCORSELx = 7, DCOx = 0, MODx = 0 | 8.5 | 19.6 | MHz |
| $f_{DCO(7,31)}$ | DCO frequency (7, 31) ⁽¹⁾ | DCORSELx = 7, DCOx = 31, MODx = 0 | 60 | 135 | MHz |
| $S_{DCORSEL}$ | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{RSEL} = f_{DCO(DCORSEL+1,DCO)} / f_{DCO(DCORSEL,DCO)}$ | 1.2 | 2.3 | ratio |
| S_{DCO} | Frequency step between tap DCO and DCO + 1 | $S_{DCO} = f_{DCO(DCORSEL,DCO+1)} / f_{DCO(DCORSEL,DCO)}$ | 1.02 | 1.12 | ratio |
| | Duty cycle | Measured at SMCLK | 40% | 50% | 60% |
| df_{DCO}/dT | DCO frequency temperature drift ⁽²⁾ | $f_{DCO} = 1$ MHz | | 0.1 | %/°C |
| df_{DCO}/dV_{CC} | DCO frequency voltage drift ⁽³⁾ | $f_{DCO} = 1$ MHz | | 1.9 | %/V |

- (1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO} , should be set to reside within the range of $f_{DCO(n,0),MAX} \leq f_{DCO} \leq f_{DCO(n,31),MIN}$, where $f_{DCO(n,0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.
- (2) Calculated using the box method: $(MAX(-40^{\circ}C \text{ to } 85^{\circ}C) - MIN(-40^{\circ}C \text{ to } 85^{\circ}C)) / MIN(-40^{\circ}C \text{ to } 85^{\circ}C) / (85^{\circ}C - (-40^{\circ}C))$
- (3) Calculated using the box method: $(MAX(1.8 \text{ V to } 3.6 \text{ V}) - MIN(1.8 \text{ V to } 3.6 \text{ V})) / MIN(1.8 \text{ V to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$

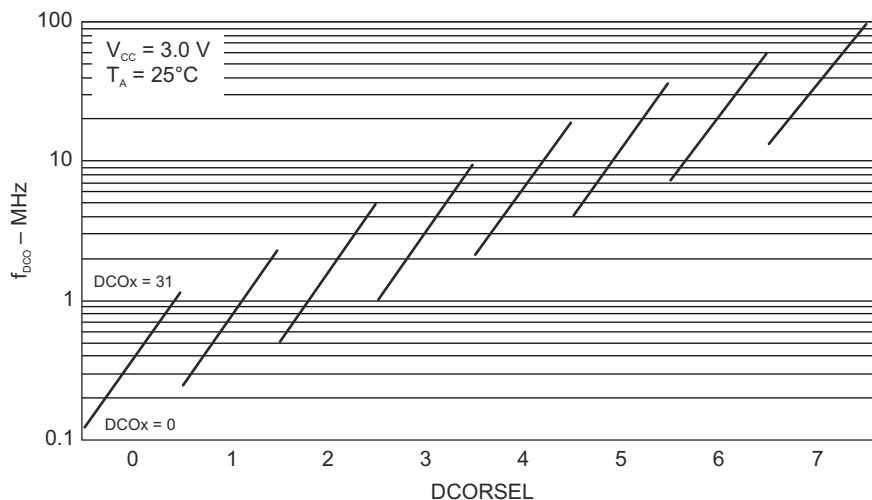


Figure 8-10. Typical DCO Frequency

8.21 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|---------------------------------|------|------|------|------|
| $V_{(DVCC_BOR_IT-)}$ | BOR _H on voltage, DV _{CC} falling level | $ dDV_{CC}/dt < 3 \text{ V/s}$ | | | 1.45 | V |
| $V_{(DVCC_BOR_IT+)}$ | BOR _H off voltage, DV _{CC} rising level | $ dDV_{CC}/dt < 3 \text{ V/s}$ | 0.80 | 1.30 | 1.50 | V |
| $V_{(DVCC_BOR_hys)}$ | BOR _H hysteresis | | 50 | | 250 | mV |
| t_{RESET} | Pulse duration required at RST/NMI pin to accept a reset | | 2 | | | μs |

8.22 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|---|-----|------|-----|------|
| $V_{\text{CORE3(AM)}}$ | Core voltage, active mode, PMMCOREV = 3 | $2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.90 | | V |
| $V_{\text{CORE2(AM)}}$ | Core voltage, active mode, PMMCOREV = 2 | $2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.80 | | V |
| $V_{\text{CORE1(AM)}}$ | Core voltage, active mode, PMMCOREV = 1 | $2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.60 | | V |
| $V_{\text{CORE0(AM)}}$ | Core voltage, active mode, PMMCOREV = 0 | $1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.40 | | V |
| $V_{\text{CORE3(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 3 | $2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.94 | | V |
| $V_{\text{CORE2(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 2 | $2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.84 | | V |
| $V_{\text{CORE1(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 1 | $2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.64 | | V |
| $V_{\text{CORE0(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 0 | $1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.44 | | V |

8.23 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|------|------|------|---------------|
| $I_{(SVSH)}$ SVS current consumption | SVSHE = 0, $DV_{CC} = 3.6\text{ V}$ | | 0 | | nA |
| | SVSHE = 1, $DV_{CC} = 3.6\text{ V}$, SVSHFP = 0 | | 200 | | |
| | SVSHE = 1, $DV_{CC} = 3.6\text{ V}$, SVSHFP = 1 | | 1.5 | | μA |
| $V_{(SVSH_IT-)}$ SVS _H on voltage level ⁽¹⁾ | SVSHE = 1, SVSHRVL = 0 | 1.57 | 1.68 | 1.78 | V |
| | SVSHE = 1, SVSHRVL = 1 | 1.79 | 1.88 | 1.98 | |
| | SVSHE = 1, SVSHRVL = 2 | 1.98 | 2.08 | 2.21 | |
| | SVSHE = 1, SVSHRVL = 3 | 2.10 | 2.18 | 2.31 | |
| $V_{(SVSH_IT+)}$ SVS _H off voltage level ⁽¹⁾ | SVSHE = 1, SVSMHRRRL = 0 | 1.62 | 1.74 | 1.85 | V |
| | SVSHE = 1, SVSMHRRRL = 1 | 1.88 | 1.94 | 2.07 | |
| | SVSHE = 1, SVSMHRRRL = 2 | 2.07 | 2.14 | 2.28 | |
| | SVSHE = 1, SVSMHRRRL = 3 | 2.20 | 2.30 | 2.42 | |
| | SVSHE = 1, SVSMHRRRL = 4 | 2.32 | 2.40 | 2.55 | |
| | SVSHE = 1, SVSMHRRRL = 5 | 2.52 | 2.70 | 2.88 | |
| | SVSHE = 1, SVSMHRRRL = 6 | 2.90 | 3.10 | 3.23 | |
| | SVSHE = 1, SVSMHRRRL = 7 | 2.90 | 3.10 | 3.23 | |
| $t_{pd(SVSH)}$ SVS _H propagation delay | SVSHE = 1, $dV_{DVCC}/dt = 10\text{ mV}/\mu\text{s}$, SVSHFP = 1 | | 2.5 | | μs |
| | SVSHE = 1, $dV_{DVCC}/dt = 1\text{ mV}/\mu\text{s}$, SVSHFP = 0 | | 20 | | |
| $t_{(SVSH)}$ SVS _H on or off delay time | SVSHE = 0 → 1, SVSHFP = 1 | | 12.5 | | μs |
| | SVSHE = 0 → 1, SVSHFP = 0 | | 100 | | |
| dV_{DVCC}/dt DV_{CC} rise time | | 0 | | 1000 | V/s |

(1) The SVS_H settings available depend on the VCore (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* on recommended settings and use.

8.24 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|------|------|---------------|
| $I_{(SVMH)}$ SVM _H current consumption | SVMHE = 0, $DV_{CC} = 3.6\text{ V}$ | | 0 | | nA |
| | SVMHE = 1, $DV_{CC} = 3.6\text{ V}$, SVMHFP = 0 | | 200 | | |
| | SVMHE = 1, $DV_{CC} = 3.6\text{ V}$, SVMHFP = 1 | | 1.5 | | μA |
| $V_{(SVMH)}$ SVM _H on or off voltage level ⁽¹⁾ | SVMHE = 1, SVSMHRRRL = 0 | 1.62 | 1.74 | 1.85 | V |
| | SVMHE = 1, SVSMHRRRL = 1 | 1.88 | 1.94 | 2.07 | |
| | SVMHE = 1, SVSMHRRRL = 2 | 2.07 | 2.14 | 2.28 | |
| | SVMHE = 1, SVSMHRRRL = 3 | 2.20 | 2.30 | 2.42 | |
| | SVMHE = 1, SVSMHRRRL = 4 | 2.32 | 2.40 | 2.55 | |
| | SVMHE = 1, SVSMHRRRL = 5 | 2.52 | 2.70 | 2.88 | |
| | SVMHE = 1, SVSMHRRRL = 6 | 2.90 | 3.10 | 3.23 | |
| | SVMHE = 1, SVSMHRRRL = 7 | 2.90 | 3.10 | 3.23 | |
| | SVMHE = 1, SVMHOVPE = 1 | | 3.75 | | |
| | $t_{pd(SVMH)}$ SVM _H propagation delay | SVMHE = 1, $dV_{DVCC}/dt = 10\text{ mV}/\mu\text{s}$, SVMHFP = 1 | | 2.5 | |
| SVMHE = 1, $dV_{DVCC}/dt = 1\text{ mV}/\mu\text{s}$, SVMHFP = 0 | | | 20 | | |
| $t_{(SVMH)}$ SVM _H on or off delay time | SVMHE = 0 → 1, SVMHFP = 1 | | 12.5 | | μs |
| | SVMHE = 0 → 1, SVMHFP = 0 | | 100 | | |

(1) The SVM_H settings available depend on the VCore (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* on recommended settings and use.

8.25 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------------|--|-----|------|-----|------|
| $I_{(SVSL)}$ | SVS _L current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0 | | 200 | | |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1 | | 1.5 | | μA |
| $t_{pd(SVSL)}$ | SVS _L propagation delay | SVSLE = 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$, SVSLFP = 1 | | 2.5 | | μs |
| | | SVSLE = 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$, SVSLFP = 0 | | 20 | | |
| $t_{(SVSL)}$ | SVS _L on or off delay time | SVSLE = 0 → 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$, SVSLFP = 1 | | 12.5 | | μs |
| | | SVSLE = 0 → 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$, SVSLFP = 0 | | 100 | | |

8.26 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------------------|---|-----|------|-----|------|
| $I_{(SVM_L)}$ | SVM _L current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVM_LFP = 0 | | 200 | | |
| | | SVMLE = 1, PMMCOREV = 2, SVM_LFP = 1 | | 1.5 | | μA |
| $t_{pd(SVM_L)}$ | SVM _L propagation delay | SVMLE = 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$, SVM_LFP = 1 | | 2.5 | | μs |
| | | SVMLE = 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$, SVM_LFP = 0 | | 20 | | |
| $t_{(SVM_L)}$ | SVM _L on or off delay time | SVMLE = 0 → 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$, SVM_LFP = 1 | | 12.5 | | μs |
| | | SVMLE = 0 → 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$, SVM_LFP = 0 | | 100 | | |

8.27 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|--|--|-----|-----|-----|------|
| $t_{\text{WAKE-UP-FAST}}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽¹⁾ | PMMCOREV = SVSMLRRL = n, $f_{\text{MCLK}} \geq 4.0 \text{ MHz}$ | | 3.5 | 7.5 | μs |
| | | (where n = 0, 1, 2, or 3), SVSLFP = 1, $1.0 \text{ MHz} < f_{\text{MCLK}} < 4.0 \text{ MHz}$ | | 4.5 | 9 | |
| $t_{\text{WAKE-UP-SLOW}}$ | Wake-up time from LPM2, LPM3 or LPM4 to active mode ^{(2) (3)} | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | 150 | 165 | μs |
| $t_{\text{WAKE-UP-LPM5}}$ | Wake-up time from LPM4.5 to active mode ⁽⁴⁾ | | | 2 | 3 | ms |
| $t_{\text{WAKE-UP-RESET}}$ | Wake-up time from RST or BOR event to active mode ⁽⁴⁾ | | | 2 | 3 | ms |

- (1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{\text{WAKE-UP-FAST}}$ is possible with SVS_L and SVM_L in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide*.
- (2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{\text{WAKE-UP-SLOW}}$ is set with SVS_L and SVM_L in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide*.
- (3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.
- (4) This value represents the time from the wake-up event to the reset vector execution.

8.28 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---------------------|-------------------------------|---|-----------------|-----|-----|------|
| f _{TA} | Timer_A input clock frequency | Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10% | 1.8 V, 3.0 V | | 25 | MHz |
| t _{TA,cap} | Timer_A capture timing | All capture inputs, Minimum pulse duration required for capture | 1.8 V, 3.0 V | 20 | | ns |

8.29 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---------------------|-------------------------------|---|-----------------|-----|-----|------|
| f _{TB} | Timer_B input clock frequency | Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10% | 1.8 V, 3.0 V | | 25 | MHz |
| t _{TB,cap} | Timer_B capture timing | All capture inputs, minimum pulse duration required for capture | 1.8 V, 3.0 V | 20 | | ns |

8.30 USCI (UART Mode) Clock Frequency

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|--|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10% | | f _{SYSTEM} | MHz |
| f _{BITCLK} | BITCLK clock frequency (equals baud rate in MBaud) | | | 1 | MHz |

8.31 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V _{CC} | MIN | MAX | UNIT |
|----------------|---|-----------------|-----|-----|------|
| t _r | UART receive deglitch time ⁽¹⁾ | 2.2 V | 50 | 600 | ns |
| | | 3 V | 50 | 600 | |

- (1) Pulses on the UART receive input (UCxRX) that are shorter than the UART receive deglitch time are suppressed. To make sure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

8.32 USCI (SPI Master Mode) Clock Frequency

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-------------------|----------------------------|---|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK or ACLK, Duty cycle = 50% ±10% | | f _{SYSTEM} | MHz |

8.33 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾
(see [Figure 8-11](#) and [Figure 8-12](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|--|--|-----------------|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | SMCLK or ACLK, Duty cycle = 50% ±10% | | | f _{SYSTEM} | MHz |
| t _{SU,MI} | SOMI input data setup time | PMMCOREV = 0 | 1.8 V | 55 | ns | |
| | | | 3.0 V | 38 | | |
| | | PMMCOREV = 3 | 2.4 V | 30 | | |
| | | | 3.0 V | 25 | | |
| t _{HD,MI} | SOMI input data hold time | PMMCOREV = 0 | 1.8 V | 0 | ns | |
| | | | 3.0 V | 0 | | |
| | | PMMCOREV = 3 | 2.4 V | 0 | | |
| | | | 3.0 V | 0 | | |
| t _{VALID,MO} | SIMO output data valid time ⁽²⁾ | UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 0 | 1.8 V | 20 | ns | |
| | | | 3.0 V | 18 | | |
| | | UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 3 | 2.4 V | 16 | | |
| | | | 3.0 V | 15 | | |
| t _{HD,MO} | SIMO output data hold time ⁽³⁾ | C _L = 20 pF, PMMCOREV = 0 | 1.8 V | -10 | ns | |
| | | | 3.0 V | -8 | | |
| | | C _L = 20 pF, PMMCOREV = 3 | 2.4 V | -10 | | |
| | | | 3.0 V | -8 | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave))$
For the slave parameters $t_{SU,SI}(Slave)$ and $t_{VALID,SO}(Slave)$, see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 8-11](#) and [Figure 8-12](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 8-11](#) and [Figure 8-12](#).

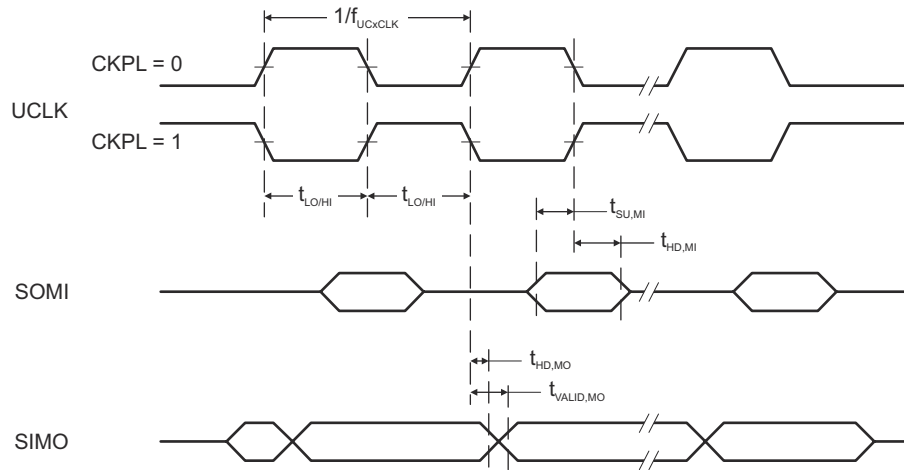


Figure 8-11. SPI Master Mode, CKPH = 0

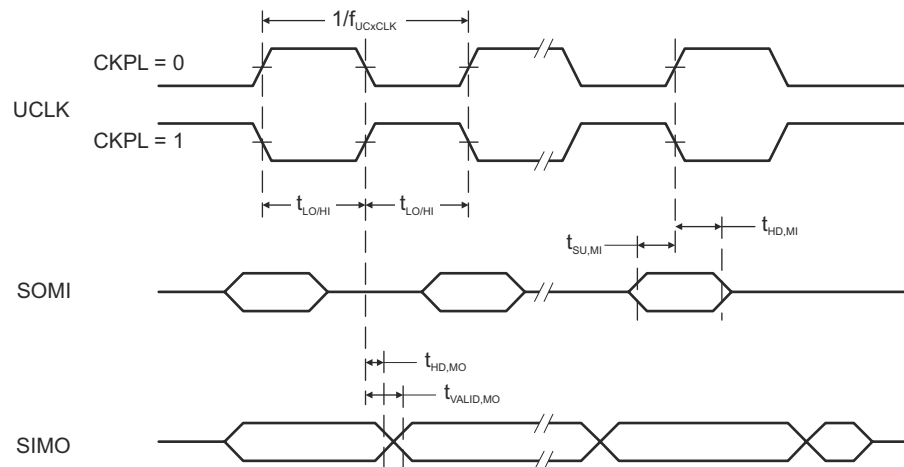


Figure 8-12. SPI Master Mode, CKPH = 1

8.34 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾
(see [Figure 8-13](#) and [Figure 8-14](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|---|--|-----------------|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE low to clock | PMMCOREV = 0 | 1.8 V | 11 | ns | |
| | | | 3.0 V | 8 | | |
| | | PMMCOREV = 3 | 2.4 V | 7 | | |
| | | | 3.0 V | 6 | | |
| t _{STE,LAG} | STE lag time, Last clock to STE high | PMMCOREV = 0 | 1.8 V | 3 | ns | |
| | | | 3.0 V | 3 | | |
| | | PMMCOREV = 3 | 2.4 V | 3 | | |
| | | | 3.0 V | 3 | | |
| t _{STE,ACC} | STE access time, STE low to SOMI data out | PMMCOREV = 0 | 1.8 V | 66 | ns | |
| | | | 3.0 V | 50 | | |
| | | PMMCOREV = 3 | 2.4 V | 36 | | |
| | | | 3.0 V | 30 | | |
| t _{STE,DIS} | STE disable time, STE high to SOMI high impedance | PMMCOREV = 0 | 1.8 V | 30 | ns | |
| | | | 3.0 V | 23 | | |
| | | PMMCOREV = 3 | 2.4 V | 16 | | |
| | | | 3.0 V | 13 | | |
| t _{SU,SI} | SIMO input data setup time | PMMCOREV = 0 | 1.8 V | 5 | ns | |
| | | | 3.0 V | 5 | | |
| | | PMMCOREV = 3 | 2.4 V | 2 | | |
| | | | 3.0 V | 2 | | |
| t _{HD,SI} | SIMO input data hold time | PMMCOREV = 0 | 1.8 V | 5 | ns | |
| | | | 3.0 V | 5 | | |
| | | PMMCOREV = 3 | 2.4 V | 5 | | |
| | | | 3.0 V | 5 | | |
| t _{VALID,SO} | SOMI output data valid time ⁽²⁾ | UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 0 | 1.8 V | 76 | ns | |
| | | | 3.0 V | 60 | | |
| | | UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 3 | 2.4 V | 44 | | |
| | | | 3.0 V | 40 | | |
| t _{HD,SO} | SOMI output data hold time ⁽³⁾ | C _L = 20 pF, PMMCOREV = 0 | 1.8 V | 18 | ns | |
| | | | 3.0 V | 12 | | |
| | | C _L = 20 pF, PMMCOREV = 3 | 2.4 V | 10 | | |
| | | | 3.0 V | 8 | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 8-13](#) and [Figure 8-14](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 8-13](#) and [Figure 8-14](#).

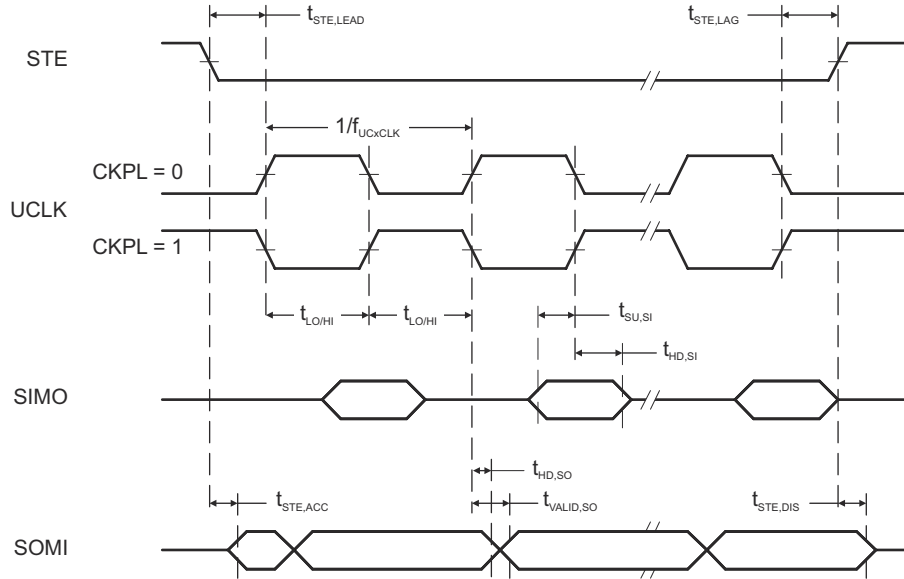


Figure 8-13. SPI Slave Mode, CKPH = 0

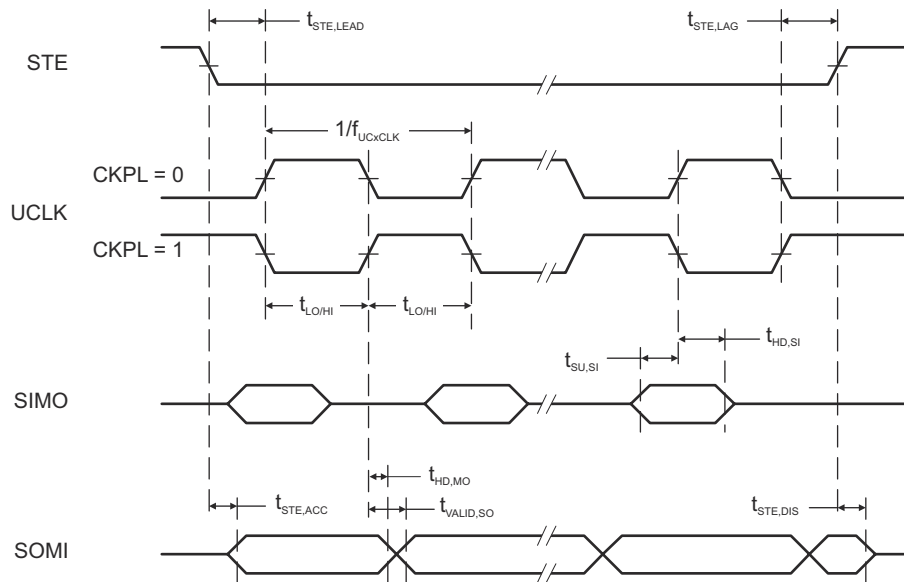


Figure 8-14. SPI Slave Mode, CKPH = 1

8.35 USCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 8-15](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---------------------|---|--|-----------------|---------------------|-----|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10% | | f _{SYSTEM} | | MHz |
| f _{SCL} | SCL clock frequency | | 2.2 V, 3 V | 0 | 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START | f _{SCL} ≤ 100 kHz | 2.2 V, 3 V | 4.0 | | μs |
| | | f _{SCL} > 100 kHz | | 0.6 | | |
| t _{SU,STA} | Setup time for a repeated START | f _{SCL} ≤ 100 kHz | 2.2 V, 3 V | 4.7 | | μs |
| | | f _{SCL} > 100 kHz | | 0.6 | | |
| t _{HD,DAT} | Data hold time | | 2.2 V, 3 V | 0 | | ns |
| t _{SU,DAT} | Data setup time | | 2.2 V, 3 V | 250 | | ns |
| t _{SU,STO} | Setup time for STOP | f _{SCL} ≤ 100 kHz | 2.2 V, 3 V | 4.0 | | μs |
| | | f _{SCL} > 100 kHz | | 0.6 | | |
| t _{SP} | Pulse duration of spikes suppressed by input filter | | 2.2 V | 50 | 600 | ns |
| | | | 3 V | 50 | 600 | |

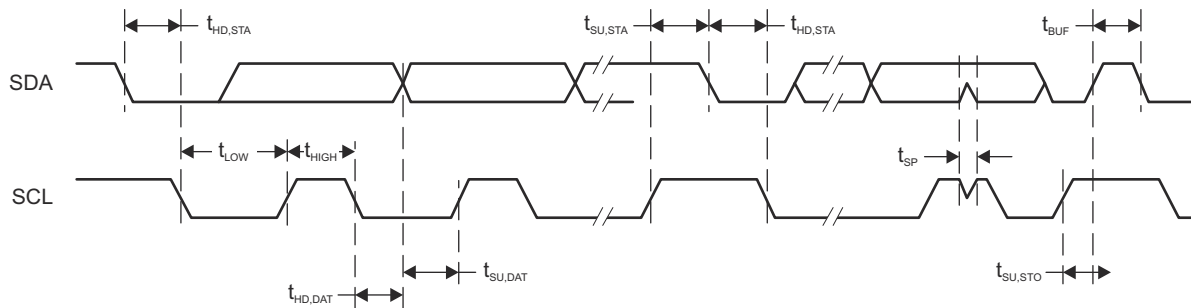


Figure 8-15. I²C Mode Timing

8.36 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|--|---|-----------------|-----|-----|------------------|------|
| AV _{CC} | Analog supply voltage | AV _{CC} and DV _{CC} are connected together, AV _{SS} and DV _{SS} are connected together, V _(AVSS) = V _(DVSS) = 0 V | | 2.2 | | 3.6 | V |
| V _(Ax) | Analog input voltage range ⁽²⁾ | All ADC12 analog input pins Ax | | 0 | | AV _{CC} | V |
| I _{ADC12_A} | Operating supply current into AV _{CC} terminal ⁽³⁾ | f _{ADC12CLK} = 5.0 MHz ⁽⁴⁾ | 2.2 V | | 125 | 155 | μA |
| | | | 3 V | | 150 | 220 | |
| C _I | Input capacitance | Only one terminal Ax can be selected at one time | 2.2 V | | 20 | 25 | pF |
| R _I | Input MUX ON-resistance | 0 V ≤ V _{Ax} ≤ AV _{CC} | | 10 | 200 | 1900 | Ω |

- (1) The leakage current is specified by the digital I/O input leakage.
- (2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See Section 8.41 and Section 8.42.
- (3) The internal reference supply current is not included in current consumption parameter I_{ADC12_A}.
- (4) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0.

8.37 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|-----------------|------|-----------------------------------|-----|------|
| f _{ADC12CLK} | ADC conversion clock | For specified performance of ADC12 linearity parameters using an external reference voltage or AV _{CC} as reference ⁽¹⁾ | 2.2 V, 3 V | 0.45 | 4.8 | 5.0 | MHz |
| | | For specified performance of ADC12 linearity parameters using the internal reference ⁽²⁾ | | 0.45 | 2.4 | 4.0 | |
| | | For specified performance of ADC12 linearity parameters using the internal reference ⁽³⁾ | | 0.45 | 2.4 | 2.7 | |
| f _{ADC12OSC} | Internal ADC12 oscillator ⁽⁴⁾ | ADC12DIV = 0, f _{ADC12CLK} = f _{ADC12OSC} | 2.2 V, 3 V | 4.2 | 4.8 | 5.4 | MHz |
| t _{CONVERT} | Conversion time | REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock | 2.2 V, 3 V | 2.4 | | 3.1 | μs |
| | | External f _{ADC12CLK} from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0 | | | 13 × 1 / f _{ADC12CLK} | | |
| t _{Sample} | Sampling time | R _S = 400 Ω, R _I = 1000 Ω, C _I = 20 pF, τ = (R _S + R _I) × C _I ⁽⁵⁾ | 2.2 V, 3 V | 1000 | | | ns |

- (1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AV_{CC} as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with f_{ADC12CLK} maximum of 5.0 MHz.
- (2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1
- (3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.
- (4) The ADC12OSC is sourced directly from MODOSC inside the UCS.
- (5) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB:
t_{sample} = ln(2ⁿ⁺¹) × (R_S + R_I) × C_I + 800 ns, where n = ADC resolution = 12, R_S = external source resistance

8.38 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|---|--------------------------------------|-----------------|-----|------|------|------|
| E _I | Integral linearity error ⁽¹⁾ | 1.4 V ≤ dVREF ≤ 1.6 V ⁽²⁾ | 2.2 V, 3 V | | | ±2.0 | LSB |
| | | 1.6 V < dVREF ⁽²⁾ | | | | ±1.7 | |
| E _D | Differential linearity error ⁽¹⁾ | ⁽²⁾ | 2.2 V, 3 V | | | ±1.0 | LSB |
| E _O | Offset error ⁽³⁾ | dVREF ≤ 2.2 V ⁽²⁾ | 2.2 V, 3 V | | ±1.0 | ±2.0 | LSB |
| | | dVREF > 2.2 V ⁽²⁾ | 2.2 V, 3 V | | ±1.0 | ±2.0 | |
| E _G | Gain error ⁽³⁾ | ⁽²⁾ | 2.2 V, 3 V | | ±1.0 | ±2.0 | LSB |
| E _T | Total unadjusted error | dVREF ≤ 2.2 V ⁽²⁾ | 2.2 V, 3 V | | ±1.4 | ±3.5 | LSB |
| | | dVREF > 2.2 V ⁽²⁾ | 2.2 V, 3 V | | ±1.4 | ±3.5 | |

- (1) Parameters are derived using the histogram method.
- (2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = V_{R+} – V_{R-}, V_{R+} < AVCC, V_{R-} > AVSS. Unless otherwise mentioned, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω, and two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current. See also the [MSP430x6xx Family User's Guide](#).
- (3) Parameters are derived using a best fit curve.

8.39 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|---|--------------------------------|---------------------------------|-----------------|-----|------|----------------------|------|
| E _I | Integral linearity error ⁽²⁾ | ADC12SR = 0, REFOUT = 1 | f _{ADC12CLK} ≤ 4.0 MHz | 2.2 V, 3 V | | | ±1.7 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | f _{ADC12CLK} ≤ 2.7 MHz | | | | ±2.5 | |
| E _D | Differential linearity error ⁽²⁾ | ADC12SR = 0, REFOUT = 1 | f _{ADC12CLK} ≤ 4.0 MHz | 2.2 V, 3 V | | -1.0 | +1.5 | LSB |
| | | ADC12SR = 0, REFOUT = 1 | f _{ADC12CLK} ≤ 2.7 MHz | | | -1.0 | +1.0 | |
| | | ADC12SR = 0, REFOUT = 0 | f _{ADC12CLK} ≤ 2.7 MHz | | | -1.0 | +2.5 | |
| E _O | Offset error ⁽³⁾ | ADC12SR = 0, REFOUT = 1 | f _{ADC12CLK} ≤ 4.0 MHz | 2.2 V, 3 V | | ±2.0 | ±4.0 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | f _{ADC12CLK} ≤ 2.7 MHz | | | ±2.0 | ±4.0 | |
| E _G | Gain error ⁽³⁾ | ADC12SR = 0, REFOUT = 1 | f _{ADC12CLK} ≤ 4.0 MHz | 2.2 V, 3 V | | ±1.0 | ±2.5 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | f _{ADC12CLK} ≤ 2.7 MHz | | | | ±1.5% ⁽⁴⁾ | VREF |
| E _T | Total unadjusted error | ADC12SR = 0, REFOUT = 1 | f _{ADC12CLK} ≤ 4.0 MHz | 2.2 V, 3 V | | ±2 | ±5 | LSB |
| | | ADC12SR = 0, REFOUT = 0 | f _{ADC12CLK} ≤ 2.7 MHz | | | | ±1.5% ⁽⁴⁾ | VREF |

- (1) The internal reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 1. dVREF = V_{R+} – V_{R-}.
- (2) Parameters are derived using the histogram method.
- (3) Parameters are derived using a best fit curve.
- (4) The gain error and total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode the reference voltage used by the ADC12_A is not available on a pin.

8.40 12-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|--------------------------|---|---|------------|------|-----|------|----------------------|
| V_{SENSOR} | See (2) | ADC12ON = 1, INCH = 0Ah, $T_A = 0^\circ\text{C}$ | 2.2 V | 680 | | | mV |
| | | | 3 V | 680 | | | |
| TC_{SENSOR} | | ADC12ON = 1, INCH = 0Ah | 2.2 V | 2.25 | | | mV/ $^\circ\text{C}$ |
| | | | 3 V | 2.25 | | | |
| $t_{SENSOR(sample)}$ | Sample time required if channel 10 is selected ⁽³⁾ | ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | 2.2 V | 100 | | | μs |
| | | | 3 V | 100 | | | |
| V_{MID} | AV _{CC} divider at channel 11, V _{AVCC} factor | ADC12ON = 1, INCH = 0Bh | | 0.48 | 0.5 | 0.52 | V _{AVCC} |
| | | | 2.2 V | 1.06 | 1.1 | 1.14 | V |
| | | | 3 V | 1.44 | 1.5 | 1.56 | |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected ⁽⁴⁾ | ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | 2.2 V, 3 V | 1000 | | | ns |

- (1) The temperature sensor is provided by the REF module. See the REF module parametric I_{REF+} regarding the current consumption of the temperature sensor.
- (2) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor. The TLV structure contains calibration values for $30^\circ\text{C} \pm 3^\circ\text{C}$ and $85^\circ\text{C} \pm 3^\circ\text{C}$ for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, } ^\circ\text{C}) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy. See also the [MSP430x5xx and MSP430x6xx Family User's Guide](#).
- (3) The typical equivalent impedance of the sensor is 51 k Ω . The sample time required includes the sensor on time, $t_{SENSOR(on)}$.
- (4) The on time ($t_{VMID(on)}$) is included in the sampling time ($t_{VMID(sample)}$); no additional on time is needed.

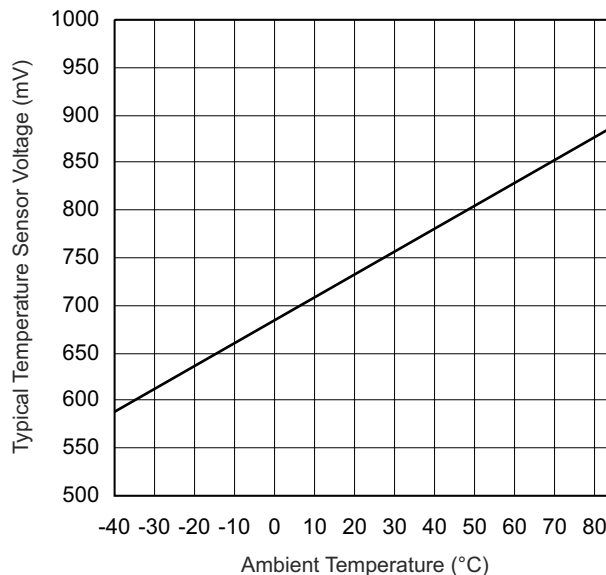


Figure 8-16. Typical Temperature Sensor Voltage

8.41 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|--|-----------------|-----|-----|------------------|------|
| V _{eREF+} | Positive external reference voltage input | V _{eREF+} > V _{REF-} /V _{eREF-} ⁽²⁾ | | 1.4 | | AV _{CC} | V |
| V _{REF-} /V _{eREF-} | Negative external reference voltage input | V _{eREF+} > V _{REF-} /V _{eREF-} ⁽³⁾ | | 0 | | 1.2 | V |
| (V _{eREF+} – V _{REF-} /V _{eREF-}) | Differential external reference voltage input | V _{eREF+} > V _{REF-} /V _{eREF-} ⁽⁴⁾ | | 1.4 | | AV _{CC} | V |
| I _{VeREF+} , I _{VREF-/VeREF-} | Static input current | 1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF-} = 0 V, f _{ADC12CLK} = 5 MHz, ADC12SHTx = 1h, Conversion rate 200 ksp/s | 2.2 V, 3 V | -26 | | 26 | μA |
| | | 1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF-} = 0 V, f _{ADC12CLK} = 5 MHz, ADC12SHTx = 8h, Conversion rate 20 ksp/s | 2.2 V, 3 V | -1 | | 1 | |
| C _{VREF+/-} | Capacitance at VREF+ or VREF- terminals | See ⁽⁵⁾ | | 10 | | | μF |

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- (5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the [MSP430x5xx and MSP430x6xx Family User's Guide](#).

8.42 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|-----------------|-----|------|-------|------------|
| V _{REF+} | REFVSEL = {2} for 2.5 V, REFON = REFOUT = 1, I _{VREF+} = 0 A | 3 V | | 2.50 | ±1.5% | V |
| | REFVSEL = {1} for 2.0 V, REFON = REFOUT = 1, I _{VREF+} = 0 A | 3 V | | 1.98 | ±1.5% | |
| | REFVSEL = {0} for 1.5 V, REFON = REFOUT = 1, I _{VREF+} = 0 A | 2.2 V, 3 V | | 1.49 | ±1.5% | |
| AV _{CC(min)} | REFVSEL = {0} for 1.5 V | | | 2.2 | | V |
| | REFVSEL = {1} for 2.0 V | | | 2.3 | | |
| | REFVSEL = {2} for 2.5 V | | | 2.8 | | |
| I _{REF+} | ADC12SR = 1, REFON = 1, REFOUT = 0, REFBURST = 0 | 3 V | | 70 | 100 | μA |
| | ADC12SR = 1, REFON = 1, REFOUT = 1, REFBURST = 0 | 3 V | | 0.45 | 0.75 | mA |
| | ADC12SR = 0, REFON = 1, REFOUT = 0, REFBURST = 0 | 3 V | | 210 | 310 | μA |
| | ADC12SR = 0, REFON = 1, REFOUT = 1, REFBURST = 0 | 3 V | | 0.95 | 1.7 | mA |
| I _{L(VREF+)} | REFVSEL = {0, 1, 2} I _{VREF+} = +10 μA or –1000 μA AV _{CC} = AV _{CC(min)} for each reference level, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1 | | | | 2500 | μV/mA |
| C _{VREF+} | REFON = REFOUT = 1 | | | 20 | 100 | pF |
| TC _{REF+} | I _{VREF+} = 0 A, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1 | | | 30 | 50 | ppm/ °C |
| PSRR _{DC} | AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1 | | | 120 | 300 | μV/V |
| PSRR _{AC} | AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, f = 1 kHz, ΔV _{pp} = 100 mV, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1 | | | 6.4 | | mV/V |
| t _{SETTLE} | AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , REFVSEL = {0, 1, 2}, REFOUT = 0, REFON = 0 → 1 | | | 75 | | μs |
| | AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , C _{VREF} = C _{VREF(max)} , REFVSEL = {0, 1, 2}, REFOUT = 1, REFON = 0 → 1 | | | 75 | | |

- The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger for driving the VREF+ terminal. When REFOUT = 1, the reference is available at the VREF+ terminal and is used as the reference for the conversion and uses the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and uses the smaller buffer.
- The internal reference current is supplied from the AVCC terminal. Consumption is independent of the ADC12ON control bit, unless a conversion is active. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.
- The temperature sensor is provided by the REF module. Its current is supplied from the AVCC terminal and is equivalent to I_{REF+} with REFON = 1 and REFOUT = 0.
- Contribution only due to the reference and buffer including package. This does not include resistance due to the PCB traces or other application factors.
- Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
- The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.

8.43 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | T _J | MIN | TYP | MAX | UNIT |
|-----------------------------|--|----------------|-----------------|-----------------|-----|--------|
| DV _{CC(PGM/ERASE)} | Program and erase supply voltage | | 1.8 | | 3.6 | V |
| I _{PGM} | Average supply current from DVCC during program | | | 3 | 5 | mA |
| I _{ERASE} | Average supply current from DVCC during erase | | | 6 | 15 | mA |
| I _{MERASE, IBANK} | Average supply current from DVCC during mass erase or bank erase | | | 6 | 15 | mA |
| t _{CPT} | Cumulative program time ⁽¹⁾ | | | | 16 | ms |
| | Program and erase endurance | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | 25°C | 100 | | | years |
| t _{Word} | Word or byte program time ⁽²⁾ | | 64 | | 85 | µs |
| t _{Block, 0} | Block program time for first byte or word ⁽²⁾ | | 49 | | 65 | µs |
| t _{Block, 1–(N–1)} | Block program time for each additional byte or word, except for last byte or word ⁽²⁾ | | 37 | | 49 | µs |
| t _{Block, N} | Block program time for last byte or word ⁽²⁾ | | 55 | | 73 | µs |
| t _{Erase} | Erase time for segment, mass erase, and bank erase when available ⁽²⁾ | | 23 | | 32 | ms |
| f _{MCLK,MGR} | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1) | | 0 | | 1 | MHz |

- (1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.
- (2) These values are hardwired into the state machine of the flash controller.

8.44 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse duration | 2.2 V, 3 V | 0.025 | | 15 | µs |
| t _{SBW,En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾ | 2.2 V, 3 V | | | 1 | µs |
| t _{SBW,Rst} | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | µs |
| f _{TCK} | TCK input frequency, 4-wire JTAG ⁽²⁾ | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | MHz |
| R _{internal} | Internal pulldown resistance on TEST | 2.2 V, 3 V | 45 | 60 | 80 | kΩ |

- (1) Tools that access the Spy-Bi-Wire interface must wait for the t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
- (2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

9 Detailed Description

9.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see [Figure 9-1](#)).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

Figure 9-1. Integrated CPU Registers

9.2 Operating Modes

These microcontrollers have one active mode and six software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active
 - MCLK is disabled
 - FLL loop control remains active
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - FLL loop control is disabled
 - ACLK and SMCLK remain active
 - MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO is disabled
 - Crystal oscillator is stopped
 - Complete data retention
- Low-power mode 4.5 (LPM4.5)
 - Internal regulator disabled
 - No data retention
 - Wake-up input from $\overline{\text{RST}}$ or digital I/O

9.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see [Table 9-1](#)). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 9-1. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|--|------------------|--------------|-------------|
| System Reset Power up External reset Watchdog time-out, password violation Flash memory password violation PMM password violation | WDTIFG, KEYV (SYSRSTIV) ^{(1) (3)} | Reset | 0FFFEh | 63, highest |
| System NMI PMM Vacant memory access JTAG mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) ⁽¹⁾ | (Non)maskable | 0FFFCh | 62 |
| User NMI NMI Oscillator fault Flash memory access violation | NMIIFG, OFIFG, ACCVIFG (SYSUNIV) ^{(1) (3)} | (Non)maskable | 0FFFAh | 61 |
| TB0 | TBCCR0 CCIFG0 ⁽²⁾ | Maskable | 0FFF8h | 60 |
| TB0 | TBCCR1 CCIFG1 to TBCCR6 CCIFG6, TBIFG (TBIV) ^{(1) (2)} | Maskable | 0FFF6h | 59 |
| Watchdog timer interval timer mode | WDTIFG | Maskable | 0FFF4h | 58 |
| USCI_A0 receive and transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV) ^{(1) (2)} | Maskable | 0FFF2h | 57 |
| USCI_B0 receive and transmit | UCB0RXIFG, UCB0TXIFG (UCB0IV) ^{(1) (2)} | Maskable | 0FFF0h | 56 |
| ADC12_A | ADC12IFG0 to ADC12IFG15 (ADC12IV) ^{(1) (2)} | Maskable | 0FFEEh | 55 |
| TA0 | TA0CCR0 CCIFG0 ⁽²⁾ | Maskable | 0FFECCh | 54 |
| TA0 | TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV) ^{(1) (2)} | Maskable | 0FFEAh | 53 |
| USCI_A2 receive and transmit | UCA2RXIFG, UCA2TXIFG (UCA2IV) ^{(1) (2)} | Maskable | 0FFE8h | 52 |
| USCI_B2 receive and transmit | UCB2RXIFG, UCB2TXIFG (UCB2IV) ^{(1) (2)} | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ^{(1) (2)} | Maskable | 0FFE4h | 50 |
| TA1 | TA1CCR0 CCIFG0 ⁽²⁾ | Maskable | 0FFE2h | 49 |
| TA1 | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) ^{(1) (2)} | Maskable | 0FFE0h | 48 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) ^{(1) (2)} | Maskable | 0FFDEh | 47 |
| USCI_A1 receive and transmit | UCA1RXIFG, UCA1TXIFG (UCA1IV) ^{(1) (2)} | Maskable | 0FFDCh | 46 |
| USCI_B1 receive and transmit | UCB1RXIFG, UCB1TXIFG (UCB1IV) ^{(1) (2)} | Maskable | 0FFDAh | 45 |
| USCI_A3 receive and transmit | UCA3RXIFG, UCA3TXIFG (UCA3IV) ^{(1) (2)} | Maskable | 0FFD8h | 44 |
| USCI_B3 receive and transmit | UCB3RXIFG, UCB3TXIFG (UCB3IV) ^{(1) (2)} | Maskable | 0FFD6h | 43 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV) ^{(1) (2)} | Maskable | 0FFD4h | 42 |
| RTC_A | RTC RDYIFG, RTC TEVIFG, RTC AIFG, RTC PSIFG, RTC PSIFG (RTCIV) ^{(1) (2)} | Maskable | 0FFD2h | 41 |
| Reserved | Reserved ⁽⁴⁾ | | 0FFD0h | 40 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

- (1) Multiple source flags
- (2) Interrupt flags are in the module.
- (3) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.
(Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot disable it.
- (4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

9.4 Memory Organization

Table 9-2 summarizes the memory map for all devices.

Table 9-2. Memory Organization

| | | MSP430F5419A MSP430F5418A | MSP430F5436A MSP430F5435A | MSP430F5438A MSP430F5437A |
|---|------------------------------|---|---|---|
| Memory (flash) Main: interrupt vector Main: code memory | Total Size Flash Flash | 128KB 00FFFFh to 00FF80h 025BFFh to 005C00h | 192KB 00FFFFh to 00FF80h 035BFFh to 005C00h | 256KB 00FFFFh to 00FF80h 045BFFh to 005C00h |
| Main: code memory | Bank D | N/A | 23KB 035BFFh to 030000h | 64KB 03FFFFh to 030000h |
| | Bank C | 23KB 025BFFh to 020000h | 64KB 02FFFFh to 020000h | 64KB 02FFFFh to 020000h |
| | Bank B | 64KB 01FFFFh to 010000h | 64KB 01FFFFh to 010000h | 64KB 01FFFFh to 010000h |
| | Bank A | 41KB 00FFFFh to 005C00h | 41KB 00FFFFh to 005C00h | 64KB 045BFFh to 040000h 00FFFFh to 005C00h |
| RAM | Size | 16 KB | 16KB | 16KB |
| | Sector 3 | 4KB 005BFFh to 004C00h | 4KB 005BFFh to 004C00h | 4KB 005BFFh to 004C00h |
| | Sector 2 | 4KB 004BFFh to 003C00h | 4KB 004BFFh to 003C00h | 4KB 004BFFh to 003C00h |
| | Sector 1 | 4KB 003BFFh to 002C00h | 4KB 003BFFh to 002C00h | 4KB 003BFFh to 002C00h |
| | Sector 0 | 4KB 002BFFh to 001C00h | 4KB 002BFFh to 001C00h | 4KB 002BFFh to 001C00h |
| Information memory (flash) | Info A | 128 B 0019FFh to 001980h | 128 B 0019FFh to 001980h | 128 B 0019FFh to 001980h |
| | Info B | 128 B 00197Fh to 001900h | 128 B 00197Fh to 001900h | 128 B 00197Fh to 001900h |
| | Info C | 128 B 0018FFh to 001880h | 128 B 0018FFh to 001880h | 128 B 0018FFh to 001880h |
| | Info D | 128 B 00187Fh to 001800h | 128 B 00187Fh to 001800h | 128 B 00187Fh to 001800h |
| Bootloader (BSL) memory (flash) | BSL 3 | 512 B 0017FFh to 001600h | 512 B 0017FFh to 001600h | 512 B 0017FFh to 001600h |
| | BSL 2 | 512 B 0015FFh to 001400h | 512 B 0015FFh to 001400h | 512 B 0015FFh to 001400h |
| | BSL 1 | 512 B 0013FFh to 001200h | 512 B 0013FFh to 001200h | 512 B 0013FFh to 001200h |
| | BSL 0 | 512 B 0011FFh to 001000h | 512 B 0011FFh to 001000h | 512 B 0011FFh to 001000h |
| Peripherals | Size | 4KB 000FFFh to 000000h | 4KB 000FFFh to 000000h | 4KB 000FFFh to 000000h |

9.5 Bootloader (BSL)

The BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the device memory through the BSL is protected by a user-defined password. Table 9-3 lists the BSL pin requirements. BSL entry requires a specific entry sequence on the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ and $\text{TEST}/\text{SBWTCK}$ pins. For complete description of the features of the BSL and its implementation, see [MSP430 Memory Programming With the Bootloader \(BSL\)](#).

Table 9-3. BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|----------------|-----------------------|
| RST/NMI/SBWDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P1.1 | Data transmit |
| P1.2 | Data receive |
| VCC | Power supply |
| VSS | Ground supply |

9.6 JTAG Operation

9.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the RST/NMI/SBWDIO is required to interface with MSP430 development tools and device programmers. [Table 9-4](#) lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For complete description of the features of the JTAG interface and its implementation, see [MSP430 Memory Programming With the JTAG Interface](#).

Table 9-4. JTAG Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|----------------|-----------|-----------------------------|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| RST/NMI/SBWDIO | IN | External reset |
| VCC | | Power supply |
| VSS | | Ground supply |

9.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 microcontrollers support the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. [Table 9-5](#) lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For the description of the Spy-Bi-Wire interface and its implementation, see the [MSP430 Memory Programming With the JTAG Interface](#).

Table 9-5. Spy-Bi-Wire Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|----------------|-----------|-----------------------------------|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| RST/NMI/SBWDIO | IN, OUT | Spy-Bi-Wire data input and output |
| VCC | | Power supply |
| VSS | | Ground supply |

9.7 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

9.8 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data are lost. Features of the RAM include:

- RAM has n sectors. The size of a sector can be found in [Section 9.4](#).
- Each sector 0 to n can be completely disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.
- For devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

9.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be handled using all instructions. For complete module descriptions, see the [MSP430x5xx and MSP430x6xx Family User's Guide](#).

9.9.1 Digital I/O

Up to ten 8-bit I/O ports are implemented: For 100- and 113-pin options, P1 through P10 are complete, and P11 contains three individual I/O ports. For 80-pin options, P1 through P7 are complete, P8 contains seven individual I/O ports, and P9 through P11 do not exist. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wake-up input capability is available for all bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P11) or word-wise in pairs (PA through PF).

9.9.2 Oscillator and System Clock

The clock system is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (XT1 LF mode), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT1 HF mode or XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turnon clock source and stabilizes in less than 5 μ s. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal, a high-frequency crystal, the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally controlled oscillator (DCO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

9.9.3 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

9.9.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

9.9.5 Real-Time Clock (RTC_A)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

9.9.6 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

9.9.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These functions include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. [Table 9-6](#) summarizes the SYS module interrupt vector registers.

Table 9-6. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---------------------------|------------|-------------------------------------|------------|----------------------|
| SYSRSTIV, System Reset | 019Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RST/NMI (POR) | 04h | |
| | | PMMSWBOR (BOR) | 06h | |
| | | Wake up from LPMx.5 | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | SVSL (POR) | 0Ch | |
| | | SVSH (POR) | 0Eh | |
| | | SVML_OVP (POR) | 10h | |
| | | SVMH_OVP (POR) | 12h | |
| | | PMMSWPOR (POR) | 14h | |
| | | WDT time-out (PUC) | 16h | |
| | | WDT password violation (PUC) | 18h | |
| | | KEYV flash password violation (PUC) | 1Ah | |
| | | Reserved | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMM password violation (PUC) | 20h | |
| Reserved | 22h to 3Eh | Lowest | | |
| SYSSNIV, System NMI | 019Ch | No interrupt pending | 00h | |
| | | SVMLIFG | 02h | Highest |
| | | SVMHIFG | 04h | |
| | | SVSMLDLYIFG | 06h | |
| | | SVSMHDLYIFG | 08h | |
| | | VMAIFG | 0Ah | |
| | | JMBINIFG | 0Ch | |
| | | JMBOUTIFG | 0Eh | |
| | | SVMLVLRIFG | 10h | |
| | | SVMHVLRFIFG | 12h | |
| | | Reserved | 14h to 1Eh | Lowest |
| | | SYSUNIV, User NMI | 019Ah | No interrupt pending |
| NMIIFG | 02h | | | Highest |
| OFIFG | 04h | | | |
| ACCVIFG | 06h | | | |
| Reserved | 08h | | | |
| Reserved | 0Ah to 1Eh | | | Lowest |

9.9.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. [Table 9-7](#) lists the available DMA triggers.

Table 9-7. DMA Trigger Assignments

| TRIGGER ⁽¹⁾ | CHANNEL | | |
|------------------------|---------------|---------------|---------------|
| | 0 | 1 | 2 |
| 0 | DMAREQ | DMAREQ | DMAREQ |
| 1 | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2 | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3 | TA1CCR0 CCIFG | TA1CCR0 CCIFG | TA1CCR0 CCIFG |
| 4 | TA1CCR2 CCIFG | TA1CCR2 CCIFG | TA1CCR2 CCIFG |
| 5 | TB0CCR0 CCIFG | TB0CCR0 CCIFG | TB0CCR0 CCIFG |
| 6 | TB0CCR2 CCIFG | TB0CCR2 CCIFG | TB0CCR2 CCIFG |
| 7 | Reserved | Reserved | Reserved |
| 8 | Reserved | Reserved | Reserved |
| 9 | Reserved | Reserved | Reserved |
| 10 | Reserved | Reserved | Reserved |
| 11 | Reserved | Reserved | Reserved |
| 12 | Reserved | Reserved | Reserved |
| 13 | Reserved | Reserved | Reserved |
| 14 | Reserved | Reserved | Reserved |
| 15 | Reserved | Reserved | Reserved |
| 16 | UCA0RXIFG | UCA0RXIFG | UCA0RXIFG |
| 17 | UCA0TXIFG | UCA0TXIFG | UCA0TXIFG |
| 18 | UCB0RXIFG | UCB0RXIFG | UCB0RXIFG |
| 19 | UCB0TXIFG | UCB0TXIFG | UCB0TXIFG |
| 20 | UCA1RXIFG | UCA1RXIFG | UCA1RXIFG |
| 21 | UCA1TXIFG | UCA1TXIFG | UCA1TXIFG |
| 22 | UCB1RXIFG | UCB1RXIFG | UCB1RXIFG |
| 23 | UCB1TXIFG | UCB1TXIFG | UCB1TXIFG |
| 24 | ADC12IFGx | ADC12IFGx | ADC12IFGx |
| 25 | Reserved | Reserved | Reserved |
| 26 | Reserved | Reserved | Reserved |
| 27 | Reserved | Reserved | Reserved |
| 28 | Reserved | Reserved | Reserved |
| 29 | MPY ready | MPY ready | MPY ready |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | DMAE0 | DMAE0 | DMAE0 |

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.

9.9.9 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3-pin or 4-pin) or I²C.

The MSP430F5438A, MSP430F5436A, and MSP430F5419A include four complete USCI modules (n = 0 to 3). The MSP430F5437A, MSP430F5435A, and MSP430F5418A include two complete USCI modules (n = 0 or 1).

9.9.10 TAO

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing (see Table 9-8). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. Table 9-8 lists the available signal connections.

Table 9-8. TAO Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|---------|---------------------|---------------------|--------------|----------------------|----------------------|-------------------------------------|-------------------------------------|
| PZ, ZCA, ZQW | PN | | | | | | PZ, ZCA, ZQW | PN |
| 17, H1-P1.0 | 17-P1.0 | TA0CLK | TACLK | Timer | N/A | N/A | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 17, H1-P1.0 | 17-P1.0 | TA0CLK | \overline{TACLK} | | | | | |
| 18, H4-P1.1 | 18-P1.1 | TA0.0 | CCI0A | CCR0 | TA0 | TA0.0 | 18, H4-P1.1 | 18-P1.1 |
| 57, H9-P8.0 | 60-P8.0 | TA0.0 | CCI0B | | | | 57, H9-P8.0 | 60-P8.0 |
| | | DV _{SS} | GND | | | | ADC12 (internal) ADC12SHSx = {1} | ADC12 (internal) ADC12SHSx = {1} |
| | | DV _{CC} | V _{CC} | | | | | |
| 19, J4-P1.2 | 19-P1.2 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | 19, J4-P1.2 | 19-P1.2 |
| 58, H11-P8.1 | 61-P8.1 | TA0.1 | CCI1B | | | | 58, H11-P8.1 | 61-P8.1 |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 20, J1-P1.3 | 20-P1.3 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | 20, J1-P1.3 | 20-P1.3 |
| 59, H12-P8.2 | 62-P8.2 | TA0.2 | CCI2B | | | | 59, H12-P8.2 | 62-P8.2 |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 21, J2-P1.4 | 21-P1.4 | TA0.3 | CCI3A | CCR3 | TA3 | TA0.3 | 21, J2-P1.4 | 21-P1.4 |
| 60, G9-P8.3 | 63-P8.3 | TA0.3 | CCI3B | | | | 60, G9-P8.3 | 63-P8.3 |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 22, K1-P1.5 | 22-P1.5 | TA0.4 | CCI4A | CCR4 | TA4 | TA0.4 | 22, K1-P1.5 | 22-P1.5 |
| 61, G11-P8.4 | 64-P8.4 | TA0.4 | CCI4B | | | | 61, G11-P8.4 | 64-P8.4 |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |

9.9.11 TA1

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 can support multiple capture/comparers, PWM outputs, and interval timing (see [Table 9-9](#)). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. [Table 9-9](#) lists the available signal connections.

Table 9-9. TA1 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|---------|---------------------|---------------------------|--------------|----------------------|----------------------|-------------------|---------|
| PZ, ZCA, ZQW | PN | | | | | | PZ, ZCA, ZQW | PN |
| 25, M1-P2.0 | 25-P2.0 | TA1CLK | TACLK | Timer | N/A | N/A | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 25, M1-P2.0 | 25-P2.0 | TA1CLK | $\overline{\text{TACLK}}$ | | | | | |
| 26, L2-P2.1 | 26-P2.1 | TA1.0 | CCI0A | CCR0 | TA0 | TA1.0 | 26, L2-P2.1 | 26-P2.1 |
| 65, F11-P8.5 | 65-P8.5 | TA1.0 | CCI0B | | | | 65, F11-P8.5 | 65-P8.5 |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 27, M2-P2.2 | 27-P2.2 | TA1.1 | CCI1A | CCR1 | TA1 | TA1.1 | 27, M2-P2.2 | 27-P2.2 |
| 66, E11-P8.6 | 66-P8.6 | TA1.1 | CCI1B | | | | 66, E11-P8.6 | 66-P8.6 |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 28, L3-P2.3 | 28-P2.3 | TA1.2 | CCI2A | CCR2 | TA2 | TA1.2 | 28, L3-P2.3 | 28-P2.3 |
| 56, J12-P7.3 | 59-P7.3 | TA1.2 | CCI2B | | | | 56, J12-P7.3 | 59-P7.3 |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |

9.9.12 TB0

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. TB0 can support multiple capture/compares, PWM outputs, and interval timing (see [Table 9-10](#)). TB0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. [Table 9-10](#) lists the available signal connections.

Table 9-10. TB0 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|---------|---------------------|---------------------|--------------|----------------------|----------------------|-------------------------------------|-------------------------------------|
| PZ, ZCA, ZQW | PN | | | | | | PZ, ZCA, ZQW | PN |
| 50, M12-P4.7 | 53-P4.7 | TB0CLK | TBCLK | Timer | N/A | N/A | | |
| | | ACLK | ACLK | | | | | |
| | | SMCLK | SMCLK | | | | | |
| 50, M12-P4.7 | 53-P4.7 | TB0CLK | TBCLK | | | | | |
| 43, J8-P4.0 | 43-P4.0 | TB0.0 | CCI0A | CCR0 | TB0 | TB0.0 | 43, J8-P4.0 | 43-P4.0 |
| 43, J8-P4.0 | 43-P4.0 | TB0.0 | CCI0B | | | | ADC12 (internal) ADC12SHSx = {2} | ADC12 (internal) ADC12SHSx = {2} |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 44, M9-P4.1 | 44-P4.1 | TB0.1 | CCI1A | CCR1 | TB1 | TB0.1 | 44, M9-P4.1 | 44-P4.1 |
| 44, M9-P4.1 | 44-P4.1 | TB0.1 | CCI1B | | | | ADC12 (internal) ADC12SHSx = {3} | ADC12 (internal) ADC12SHSx = {3} |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 45, L9-P4.2 | 45-P4.2 | TB0.2 | CCI2A | CCR2 | TB2 | TB0.2 | 45, L9-P4.2 | 45-P4.2 |
| 45, L9-P4.2 | 45-P4.2 | TB0.2 | CCI2B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 46, L10-P4.3 | 46-P4.3 | TB0.3 | CCI3A | CCR3 | TB3 | TB0.3 | 46, L10-P4.3 | 46-P4.3 |
| 46, L10-P4.3 | 46-P4.3 | TB0.3 | CCI3B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 47, M10-P4.4 | 47-P4.4 | TB0.4 | CCI4A | CCR4 | TB4 | TB0.4 | 47, M10-P4.4 | 47-P4.4 |
| 47, M10-P4.4 | 47-P4.4 | TB0.4 | CCI4B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 48, L11-P4.5 | 48-P4.5 | TB0.5 | CCI5A | CCR5 | TB5 | TB0.5 | 48, L11-P4.5 | 48-P4.5 |
| 48, L11-P4.5 | 48-P4.5 | TB0.5 | CCI5B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |
| 49, M11-P4.6 | 52-P4.6 | TB0.6 | CCI6A | CCR6 | TB6 | TB0.6 | 49, M11-P4.6 | 52-P4.6 |
| | | ACLK (internal) | CCI6B | | | | | |
| | | DV _{SS} | GND | | | | | |
| | | DV _{CC} | V _{CC} | | | | | |

9.9.13 ADC12_A

The ADC12_A module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

9.9.14 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

9.9.15 Reference (REF) Module Voltage Reference

The REF is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

9.9.16 Embedded Emulation Module (EEM) (L Version)

The EEM supports real-time in-system debugging. The L version of the EEM has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware trigger or breakpoint on CPU register write access
- Up to 10 hardware triggers that can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

9.9.17 Peripheral File Map

Table 9-11 lists the base address of the registers for each peripheral.

Table 9-11. Peripherals

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|---|--------------|----------------------|
| Special Functions (see Table 9-12) | 0100h | 000h to 01Fh |
| PMM (see Table 9-13) | 0120h | 000h to 010h |
| Flash Control (see Table 9-14) | 0140h | 000h to 00Fh |
| CRC16 (see Table 9-15) | 0150h | 000h to 007h |
| RAM Control (see Table 9-16) | 0158h | 000h to 001h |
| Watchdog (see Table 9-17) | 015Ch | 000h to 001h |
| UCS (see Table 9-18) | 0160h | 000h to 01Fh |
| SYS (see Table 9-19) | 0180h | 000h to 01Fh |
| Shared Reference (see Table 9-20) | 01B0h | 000h to 001h |
| Port P1, P2 (see Table 9-21) | 0200h | 000h to 01Fh |
| Port P3, P4 (see Table 9-22) | 0220h | 000h to 00Bh |
| Port P5, P6 (see Table 9-23) | 0240h | 000h to 00Bh |
| Port P7, P8 (see Table 9-24) | 0260h | 000h to 00Bh |
| Port P9, P10 (see Table 9-25) | 0280h | 000h to 00Bh |
| Port P11 (see Table 9-26) | 02A0h | 000h to 00Ah |
| Port PJ (see Table 9-27) | 0320h | 000h to 01Fh |
| TA0 (see Table 9-28) | 0340h | 000h to 02Eh |
| TA1 (see Table 9-29) | 0380h | 000h to 02Eh |
| TB0 (see Table 9-30) | 03C0h | 000h to 02Eh |
| Real Timer Clock (RTC_A) (see Table 9-31) | 04A0h | 000h to 01Bh |
| 32-Bit Hardware Multiplier (see Table 9-32) | 04C0h | 000h to 02Fh |
| DMA General Control (see Table 9-33) | 0500h | 000h to 00Fh |
| DMA Channel 0 (see Table 9-33) | 0510h | 000h to 00Ah |
| DMA Channel 1 (see Table 9-33) | 0520h | 000h to 00Ah |
| DMA Channel 2 (see Table 9-33) | 0530h | 000h to 00Ah |
| USCI_A0 (see Table 9-34) | 05C0h | 000h to 01Fh |
| USCI_B0 (see Table 9-35) | 05E0h | 000h to 01Fh |
| USCI_A1 (see Table 9-36) | 0600h | 000h to 01Fh |
| USCI_B1 (see Table 9-37) | 0620h | 000h to 01Fh |
| USCI_A2 (see Table 9-38) | 0640h | 000h to 01Fh |
| USCI_B2 (see Table 9-39) | 0660h | 000h to 01Fh |
| USCI_A3 (see Table 9-40) | 0680h | 000h to 01Fh |
| USCI_B3 (see Table 9-41) | 06A0h | 000h to 01Fh |
| ADC12_A (see Table 9-42) | 0700h | 000h to 03Eh |

Table 9-12. Special Function Registers (Base Address: 0100h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

Table 9-13. PMM Registers (Base Address: 0120h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| PMM control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high-side control | SVSMHCTL | 04h |
| SVS low-side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM power mode 5 control | PM5CTL0 | 10h |

Table 9-14. Flash Control Registers (Base Address: 0140h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

Table 9-15. CRC16 Registers (Base Address: 0150h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

Table 9-16. RAM Control Registers (Base Address: 0158h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RAM control 0 | RCCTL0 | 00h |

Table 9-17. Watchdog Registers (Base Address: 015Ch)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL | 00h |

Table 9-18. UCS Registers (Base Address: 0160h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |
| UCS control 8 | UCSCTL8 | 10h |

Table 9-19. SYS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|-----------|--------|
| System control | SYSCTL | 00h |
| Bootloader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus Error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

Table 9-20. Shared Reference Registers (Base Address: 01B0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL | 00h |

Table 9-21. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 resistor enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |
| Port P1 selection | P1SEL | 0Ah |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 resistor enable | P2REN | 07h |
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection | P2SEL | 0Bh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

Table 9-22. Port P3, P4 Registers (Base Address: 0220h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 resistor enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection | P3SEL | 0Ah |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 resistor enable | P4REN | 07h |
| Port P4 drive strength | P4DS | 09h |
| Port P4 selection | P4SEL | 0Bh |

Table 9-23. Port P5, P6 Registers (Base Address: 0240h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 resistor enable | P5REN | 06h |
| Port P5 drive strength | P5DS | 08h |
| Port P5 selection | P5SEL | 0Ah |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 resistor enable | P6REN | 07h |
| Port P6 drive strength | P6DS | 09h |
| Port P6 selection | P6SEL | 0Bh |

Table 9-24. Port P7, P8 Registers (Base Address: 0260h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P7 input | P7IN | 00h |
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |
| Port P7 resistor enable | P7REN | 06h |
| Port P7 drive strength | P7DS | 08h |
| Port P7 selection | P7SEL | 0Ah |
| Port P8 input | P8IN | 01h |
| Port P8 output | P8OUT | 03h |
| Port P8 direction | P8DIR | 05h |
| Port P8 resistor enable | P8REN | 07h |
| Port P8 drive strength | P8DS | 09h |
| Port P8 selection | P8SEL | 0Bh |

Table 9-25. Port P9, P10 Registers (Base Address: 0280h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Port P9 input | P9IN | 00h |
| Port P9 output | P9OUT | 02h |
| Port P9 direction | P9DIR | 04h |
| Port P9 resistor enable | P9REN | 06h |
| Port P9 drive strength | P9DS | 08h |
| Port P9 selection | P9SEL | 0Ah |
| Port P10 input | P10IN | 01h |
| Port P10 output | P10OUT | 03h |
| Port P10 direction | P10DIR | 05h |
| Port P10 resistor enable | P10REN | 07h |
| Port P10 drive strength | P10DS | 09h |
| Port P10 selection | P10SEL | 0Bh |

Table 9-26. Port P11 Registers (Base Address: 02A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Port P11 input | P11IN | 00h |
| Port P11 output | P11OUT | 02h |
| Port P11 direction | P11DIR | 04h |
| Port P11 resistor enable | P11REN | 06h |
| Port P11 drive strength | P11DS | 08h |
| Port P11 selection | P11SEL | 0Ah |

Table 9-27. Port J Registers (Base Address: 0320h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ resistor enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |

Table 9-28. TA0 Registers (Base Address: 0340h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| Capture/compare control 3 | TA0CCTL3 | 08h |
| Capture/compare control 4 | TA0CCTL4 | 0Ah |
| TA0 counter | TA0R | 10h |
| Capture/compare 0 | TA0CCR0 | 12h |
| Capture/compare 1 | TA0CCR1 | 14h |
| Capture/compare 2 | TA0CCR2 | 16h |
| Capture/compare 3 | TA0CCR3 | 18h |
| Capture/compare 4 | TA0CCR4 | 1Ah |
| TA0 expansion 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

Table 9-29. TA1 Registers (Base Address: 0380h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| Capture/compare 2 | TA1CCR2 | 16h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

Table 9-30. TB0 Registers (Base Address: 03C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TB0 control | TB0CTL | 00h |
| Capture/compare control 0 | TB0CCTL0 | 02h |
| Capture/compare control 1 | TB0CCTL1 | 04h |
| Capture/compare control 2 | TB0CCTL2 | 06h |
| Capture/compare control 3 | TB0CCTL3 | 08h |
| Capture/compare control 4 | TB0CCTL4 | 0Ah |
| Capture/compare control 5 | TB0CCTL5 | 0Ch |
| Capture/compare control 6 | TB0CCTL6 | 0Eh |
| TB0 counter | TB0R | 10h |
| Capture/compare 0 | TB0CCR0 | 12h |
| Capture/compare 1 | TB0CCR1 | 14h |
| Capture/compare 2 | TB0CCR2 | 16h |
| Capture/compare 3 | TB0CCR3 | 18h |
| Capture/compare 4 | TB0CCR4 | 1Ah |
| Capture/compare 5 | TB0CCR5 | 1Ch |
| Capture/compare 6 | TB0CCR6 | 1Eh |
| TB0 expansion 0 | TB0EX0 | 20h |
| TB0 interrupt vector | TB0IV | 2Eh |

Table 9-31. Real Time Clock Registers (Base Address: 04A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------------|--------|
| RTC control 0 | RTCCTL0 | 00h |
| RTC control 1 | RTCCTL1 | 01h |
| RTC control 2 | RTCCTL2 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds/counter 1 | RTCSEC/RTCNT1 | 10h |
| RTC minutes/counter 2 | RTCMIN/RTCNT2 | 11h |
| RTC hours/counter 3 | RTCHOUR/RTCNT3 | 12h |
| RTC day of week/counter 4 | RTCADOW/RTCNT4 | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year low | RTCYEARL | 16h |
| RTC year high | RTCYEARH | 17h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |

Table 9-32. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-----------|--------|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

**Table 9-33. DMA Registers (Base Address DMA General Control: 0500h,
DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 0 control | DMA0CTL | 00h |
| DMA channel 0 source address low | DMA0SAL | 02h |
| DMA channel 0 source address high | DMA0SAH | 04h |
| DMA channel 0 destination address low | DMA0DAL | 06h |
| DMA channel 0 destination address high | DMA0DAH | 08h |
| DMA channel 0 transfer size | DMA0SZ | 0Ah |
| DMA channel 1 control | DMA1CTL | 00h |
| DMA channel 1 source address low | DMA1SAL | 02h |
| DMA channel 1 source address high | DMA1SAH | 04h |
| DMA channel 1 destination address low | DMA1DAL | 06h |
| DMA channel 1 destination address high | DMA1DAH | 08h |
| DMA channel 1 transfer size | DMA1SZ | 0Ah |
| DMA channel 2 control | DMA2CTL | 00h |
| DMA channel 2 source address low | DMA2SAL | 02h |
| DMA channel 2 source address high | DMA2SAH | 04h |
| DMA channel 2 destination address low | DMA2DAL | 06h |
| DMA channel 2 destination address high | DMA2DAH | 08h |
| DMA channel 2 transfer size | DMA2SZ | 0Ah |
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Eh |

Table 9-34. USCI_A0 Registers (Base Address: 05C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|------------|--------|
| USCI control 1 | UCA0CTL1 | 00h |
| USCI control 0 | UCA0CTL0 | 01h |
| USCI baud rate 0 | UCA0BR0 | 06h |
| USCI baud rate 1 | UCA0BR1 | 07h |
| USCI modulation control | UCA0MCTL | 08h |
| USCI status | UCA0STAT | 0Ah |
| USCI receive buffer | UCA0RXBUF | 0Ch |
| USCI transmit buffer | UCA0TXBUF | 0Eh |
| USCI LIN control | UCA0ABCTL | 10h |
| USCI IrDA transmit control | UCA0IRTCTL | 12h |
| USCI IrDA receive control | UCA0IRRCTL | 13h |
| USCI interrupt enable | UCA0IE | 1Ch |
| USCI interrupt flags | UCA0IFG | 1Dh |
| USCI interrupt vector word | UCA0IV | 1Eh |

Table 9-35. USCI_B0 Registers (Base Address: 05E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1 | UCB0CTL1 | 00h |
| USCI synchronous control 0 | UCB0CTL0 | 01h |
| USCI synchronous bit rate 0 | UCB0BR0 | 06h |
| USCI synchronous bit rate 1 | UCB0BR1 | 07h |
| USCI synchronous status | UCB0STAT | 0Ah |
| USCI synchronous receive buffer | UCB0RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB0TXBUF | 0Eh |
| USCI I2C own address | UCB0I2COA | 10h |
| USCI I2C slave address | UCB0I2CSA | 12h |
| USCI interrupt enable | UCB0IE | 1Ch |
| USCI interrupt flags | UCB0IFG | 1Dh |
| USCI interrupt vector word | UCB0IV | 1Eh |

Table 9-36. USCI_A1 Registers (Base Address: 0600h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|------------|--------|
| USCI control 1 | UCA1CTL1 | 00h |
| USCI control 0 | UCA1CTL0 | 01h |
| USCI baud rate 0 | UCA1BR0 | 06h |
| USCI baud rate 1 | UCA1BR1 | 07h |
| USCI modulation control | UCA1MCTL | 08h |
| USCI status | UCA1STAT | 0Ah |
| USCI receive buffer | UCA1RXBUF | 0Ch |
| USCI transmit buffer | UCA1TXBUF | 0Eh |
| USCI LIN control | UCA1ABCTL | 10h |
| USCI IrDA transmit control | UCA1IRTCTL | 12h |
| USCI IrDA receive control | UCA1IRRCTL | 13h |
| USCI interrupt enable | UCA1IE | 1Ch |
| USCI interrupt flags | UCA1IFG | 1Dh |
| USCI interrupt vector word | UCA1IV | 1Eh |

Table 9-37. USCI_B1 Registers (Base Address: 0620h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1 | UCB1CTL1 | 00h |
| USCI synchronous control 0 | UCB1CTL0 | 01h |
| USCI synchronous bit rate 0 | UCB1BR0 | 06h |
| USCI synchronous bit rate 1 | UCB1BR1 | 07h |
| USCI synchronous status | UCB1STAT | 0Ah |
| USCI synchronous receive buffer | UCB1RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB1TXBUF | 0Eh |
| USCI I2C own address | UCB1I2COA | 10h |
| USCI I2C slave address | UCB1I2CSA | 12h |
| USCI interrupt enable | UCB1IE | 1Ch |
| USCI interrupt flags | UCB1IFG | 1Dh |
| USCI interrupt vector word | UCB1IV | 1Eh |

Table 9-38. USCI_A2 Registers (Base Address: 0640h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|------------|--------|
| USCI control 1 | UCA2CTL1 | 00h |
| USCI control 0 | UCA2CTL0 | 01h |
| USCI baud rate 0 | UCA2BR0 | 06h |
| USCI baud rate 1 | UCA2BR1 | 07h |
| USCI modulation control | UCA2MCTL | 08h |
| USCI status | UCA2STAT | 0Ah |
| USCI receive buffer | UCA2RXBUF | 0Ch |
| USCI transmit buffer | UCA2TXBUF | 0Eh |
| USCI LIN control | UCA2ABCTL | 10h |
| USCI IrDA transmit control | UCA2IRTCTL | 12h |
| USCI IrDA receive control | UCA2IRRCTL | 13h |
| USCI interrupt enable | UCA2IE | 1Ch |
| USCI interrupt flags | UCA2IFG | 1Dh |
| USCI interrupt vector word | UCA2IV | 1Eh |

Table 9-39. USCI_B2 Registers (Base Address: 0660h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1 | UCB2CTL1 | 00h |
| USCI synchronous control 0 | UCB2CTL0 | 01h |
| USCI synchronous bit rate 0 | UCB2BR0 | 06h |
| USCI synchronous bit rate 1 | UCB2BR1 | 07h |
| USCI synchronous status | UCB2STAT | 0Ah |
| USCI synchronous receive buffer | UCB2RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB2TXBUF | 0Eh |
| USCI I2C own address | UCB2I2COA | 10h |
| USCI I2C slave address | UCB2I2CSA | 12h |
| USCI interrupt enable | UCB2IE | 1Ch |
| USCI interrupt flags | UCB2IFG | 1Dh |
| USCI interrupt vector word | UCB2IV | 1Eh |

Table 9-40. USCI_A3 Registers (Base Address: 0680h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|------------|--------|
| USCI control 1 | UCA3CTL1 | 00h |
| USCI control 0 | UCA3CTL0 | 01h |
| USCI baud rate 0 | UCA3BR0 | 06h |
| USCI baud rate 1 | UCA3BR1 | 07h |
| USCI modulation control | UCA3MCTL | 08h |
| USCI status | UCA3STAT | 0Ah |
| USCI receive buffer | UCA3RXBUF | 0Ch |
| USCI transmit buffer | UCA3TXBUF | 0Eh |
| USCI LIN control | UCA3ABCTL | 10h |
| USCI IrDA transmit control | UCA3IRTCTL | 12h |
| USCI IrDA receive control | UCA3IRRCTL | 13h |
| USCI interrupt enable | UCA3IE | 1Ch |
| USCI interrupt flags | UCA3IFG | 1Dh |
| USCI interrupt vector word | UCA3IV | 1Eh |

Table 9-41. USCI_B3 Registers (Base Address: 06A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1 | UCB3CTL1 | 00h |
| USCI synchronous control 0 | UCB3CTL0 | 01h |
| USCI synchronous bit rate 0 | UCB3BR0 | 06h |
| USCI synchronous bit rate 1 | UCB3BR1 | 07h |
| USCI synchronous status | UCB3STAT | 0Ah |
| USCI synchronous receive buffer | UCB3RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB3TXBUF | 0Eh |
| USCI I2C own address | UCB3I2COA | 10h |
| USCI I2C slave address | UCB3I2CSA | 12h |
| USCI interrupt enable | UCB3IE | 1Ch |
| USCI interrupt flags | UCB3IFG | 1Dh |
| USCI interrupt vector word | UCB3IV | 1Eh |

Table 9-42. ADC12_A Registers (Base Address: 0700h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|-------------|--------|
| Control 0 | ADC12CTL0 | 00h |
| Control 1 | ADC12CTL1 | 02h |
| Control 2 | ADC12CTL2 | 04h |
| Interrupt flag | ADC12IFG | 0Ah |
| Interrupt enable | ADC12IE | 0Ch |
| Interrupt vector word | ADC12IV | 0Eh |
| ADC memory control 0 | ADC12MCTL0 | 10h |
| ADC memory control 1 | ADC12MCTL1 | 11h |
| ADC memory control 2 | ADC12MCTL2 | 12h |
| ADC memory control 3 | ADC12MCTL3 | 13h |
| ADC memory control 4 | ADC12MCTL4 | 14h |
| ADC memory control 5 | ADC12MCTL5 | 15h |
| ADC memory control 6 | ADC12MCTL6 | 16h |
| ADC memory control 7 | ADC12MCTL7 | 17h |
| ADC memory control 8 | ADC12MCTL8 | 18h |
| ADC memory control 9 | ADC12MCTL9 | 19h |
| ADC memory control 10 | ADC12MCTL10 | 1Ah |
| ADC memory control 11 | ADC12MCTL11 | 1Bh |
| ADC memory control 12 | ADC12MCTL12 | 1Ch |
| ADC memory control 13 | ADC12MCTL13 | 1Dh |
| ADC memory control 14 | ADC12MCTL14 | 1Eh |
| ADC memory control 15 | ADC12MCTL15 | 1Fh |
| Conversion memory 0 | ADC12MEM0 | 20h |
| Conversion memory 1 | ADC12MEM1 | 22h |
| Conversion memory 2 | ADC12MEM2 | 24h |
| Conversion memory 3 | ADC12MEM3 | 26h |
| Conversion memory 4 | ADC12MEM4 | 28h |
| Conversion memory 5 | ADC12MEM5 | 2Ah |
| Conversion memory 6 | ADC12MEM6 | 2Ch |
| Conversion memory 7 | ADC12MEM7 | 2Eh |
| Conversion memory 8 | ADC12MEM8 | 30h |
| Conversion memory 9 | ADC12MEM9 | 32h |
| Conversion memory 10 | ADC12MEM10 | 34h |
| Conversion memory 11 | ADC12MEM11 | 36h |
| Conversion memory 12 | ADC12MEM12 | 38h |
| Conversion memory 13 | ADC12MEM13 | 3Ah |
| Conversion memory 14 | ADC12MEM14 | 3Ch |
| Conversion memory 15 | ADC12MEM15 | 3Eh |

9.10 Input/Output Diagrams

9.10.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Figure 9-2 shows the port diagram. Table 9-43 summarizes the selection of the pin functions.

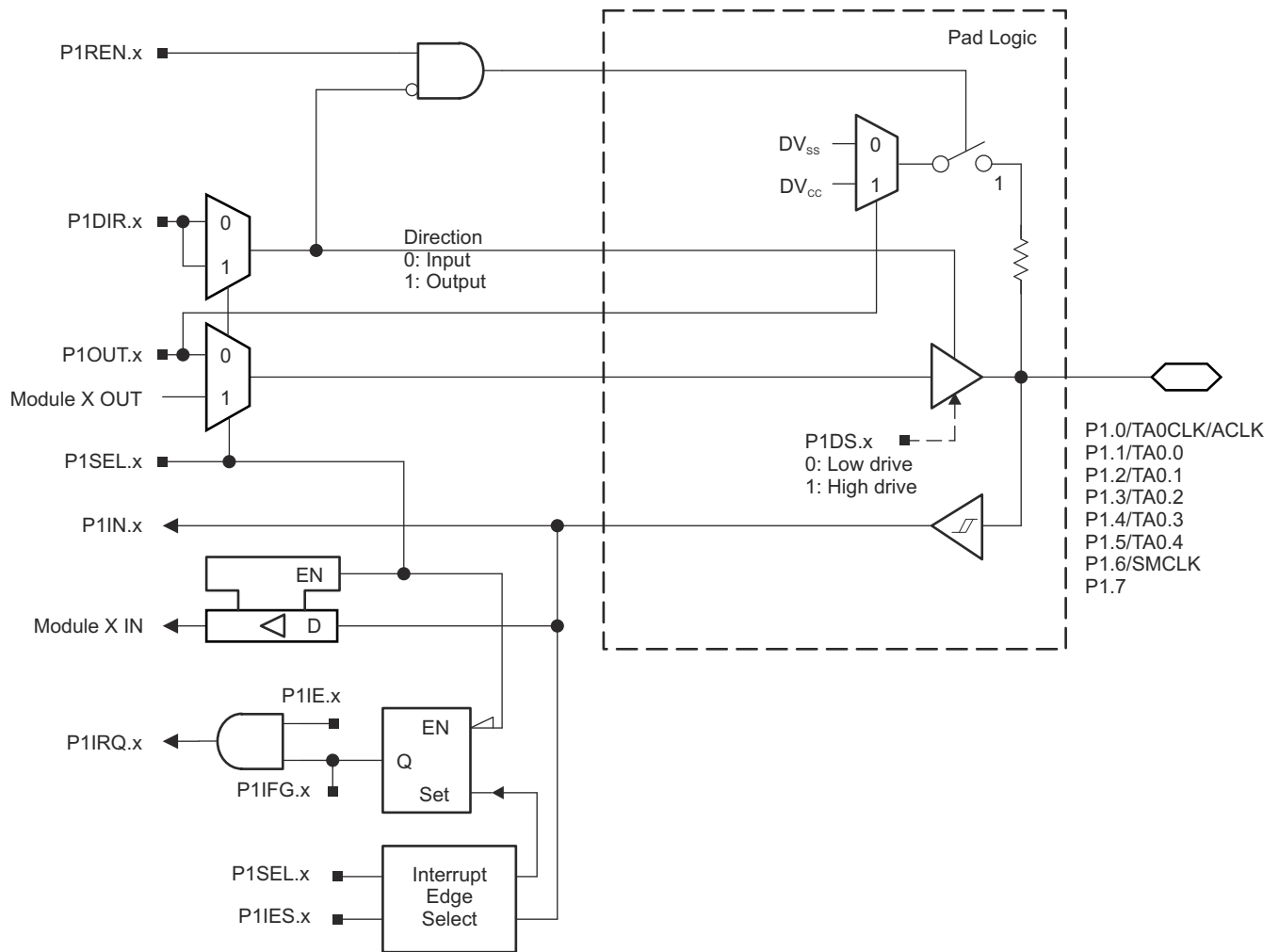


Figure 9-2. Port P1 (P1.0 to P1.7) Diagram

Table 9-43. Port P1 (P1.0 to P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|------------------|---|------------|-------------------------|---------|
| | | | P1DIR.x | P1SEL.x |
| P1.0/TA0CLK/ACLK | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.TA0CLK | 0 | 1 |
| | | ACLK | 1 | 1 |
| P1.1/TA0.0 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI0A | 0 | 1 |
| | | TA0.0 | 1 | 1 |
| P1.2/TA0.1 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI1A | 0 | 1 |
| | | TA0.1 | 1 | 1 |
| P1.3/TA0.2 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI2A | 0 | 1 |
| | | TA0.2 | 1 | 1 |
| P1.4/TA0.3 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI3A | 0 | 1 |
| | | TA0.3 | 1 | 1 |
| P1.5/TA0.4 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI4A | 0 | 1 |
| | | TA0.4 | 1 | 1 |
| P1.6/SMCLK | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 |
| | | SMCLK | 1 | 1 |
| P1.7 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 |

9.10.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

Figure 9-3 shows the port diagram. Table 9-44 summarizes the selection of the pin functions.

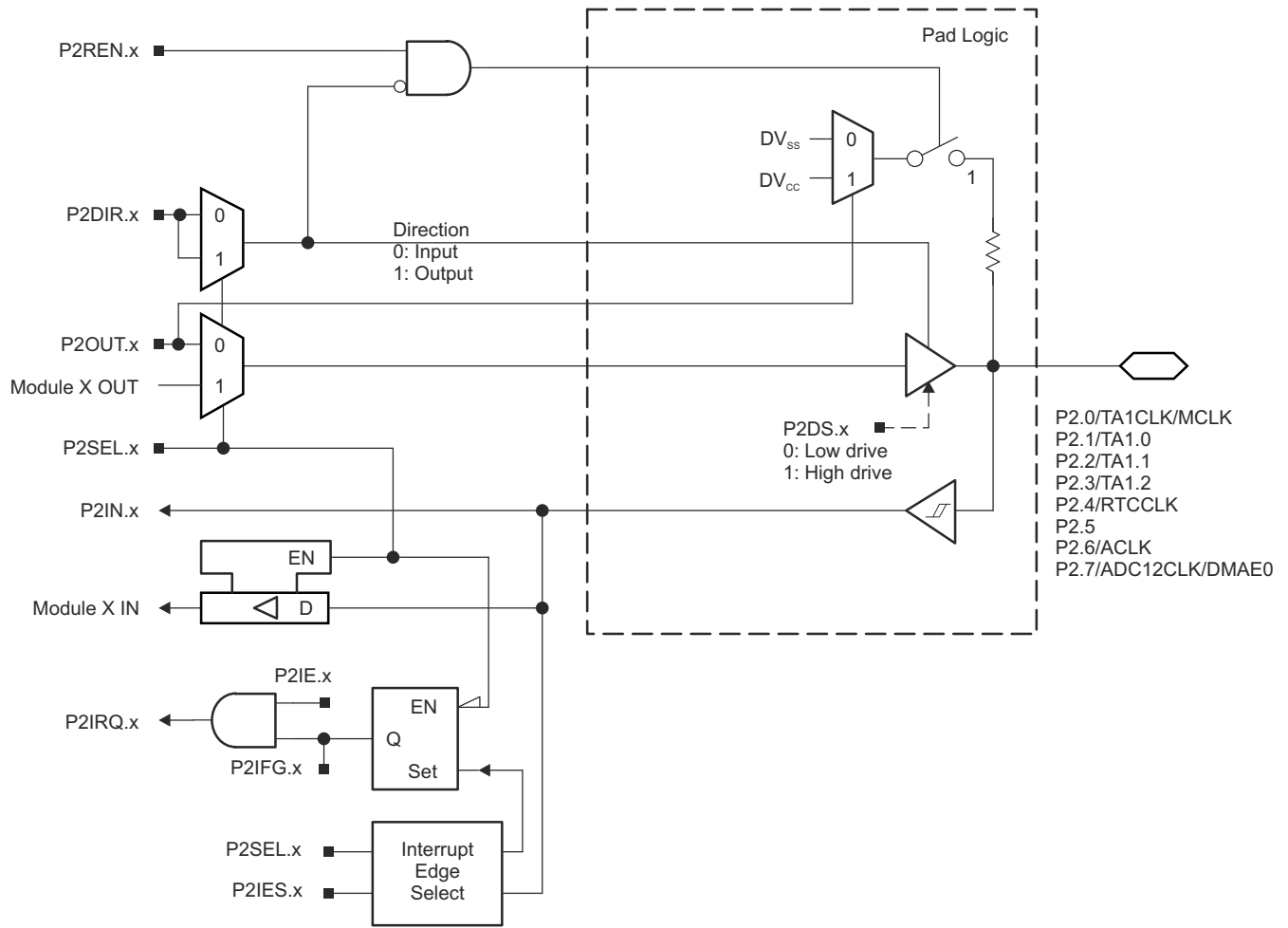


Figure 9-3. Port P2 (P2.0 to P2.7) Diagram

Table 9-44. Port P2 (P2.0 to P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---------------------|---|------------|-------------------------|---------|
| | | | P2DIR.x | P2SEL.x |
| P2.0/TA1CLK/MCLK | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 |
| | | TA1CLK | 0 | 1 |
| | | MCLK | 1 | 1 |
| P2.1/TA1.0 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI0A | 0 | 1 |
| | | TA1.0 | 1 | 1 |
| P2.2/TA1.1 | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI1A | 0 | 1 |
| | | TA1.1 | 1 | 1 |
| P2.3/TA1.2 | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI2A | 0 | 1 |
| | | TA1.2 | 1 | 1 |
| P2.4/RTCCLK | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 |
| | | RTCCLK | 1 | 1 |
| P2.5 | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 |
| P2.6/ACLK | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 |
| | | ACLK | 1 | 1 |
| P2.7/ADC12CLK/DMAE0 | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 |
| | | DMAE0 | 0 | 1 |
| | | ADC12CLK | 1 | 1 |

9.10.3 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

Figure 9-4 shows the port diagram. Table 9-45 summarizes the selection of the pin functions.

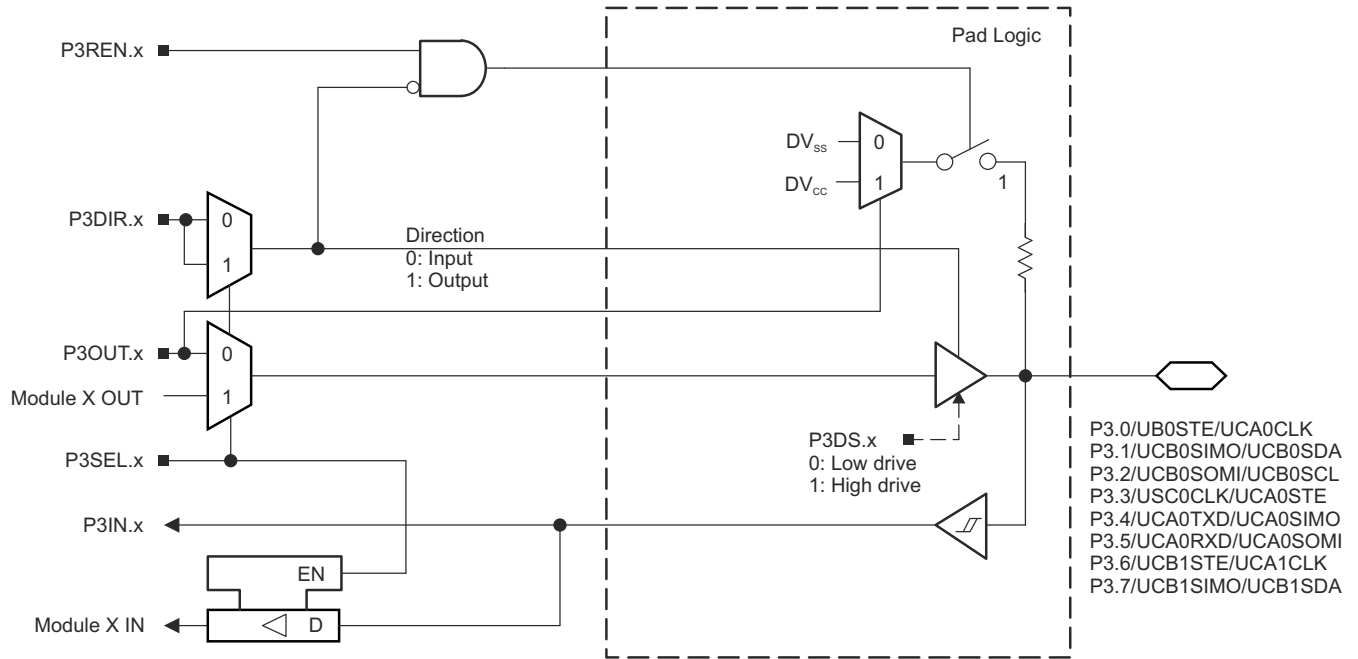


Figure 9-4. Port P3 (P3.0 to P3.7) Diagram

Table 9-45. Port P3 (P3.0 to P3.7) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | |
|-----------------------|---|-------------------------------------|--|---------|
| | | | P3DIR.x | P3SEL.x |
| P3.0/UCB0STE/UCA0CLK | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0STE/UCA0CLK ^{(2) (4)} | X | 1 |
| P3.1/UCB0SIMO/UCB0SDA | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0SIMO/UCB0SDA ^{(2) (3)} | X | 1 |
| P3.2/UCB0SOMI/UCB0SCL | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0SOMI/UCB0SCL ^{(2) (3)} | X | 1 |
| P3.3/UCB0CLK/UCA0STE | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0CLK/UCA0STE ^{(2) (5)} | X | 1 |
| P3.4/UCA0TXD/UCA0SIMO | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 |
| | | UCA0TXD/UCA0SIMO ⁽²⁾ | X | 1 |
| P3.5/UCA0RXD/UCA0SOMI | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 |
| | | UCA0RXD/UCA0SOMI ⁽²⁾ | X | 1 |
| P3.6/UCB1STE/UCA1CLK | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1STE/UCA1CLK ^{(2) (6)} | X | 1 |
| P3.7/UCB1SIMO/UCB1SDA | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1SIMO/UCB1SDA ^{(2) (3)} | X | 1 |

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) If the I²C functionality is selected, the output drives only the logical 0 to V_{SS} level.

(4) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

(5) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

(6) UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output, USCI_B1 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

9.10.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Figure 9-5 shows the port diagram. Table 9-46 summarizes the selection of the pin functions.

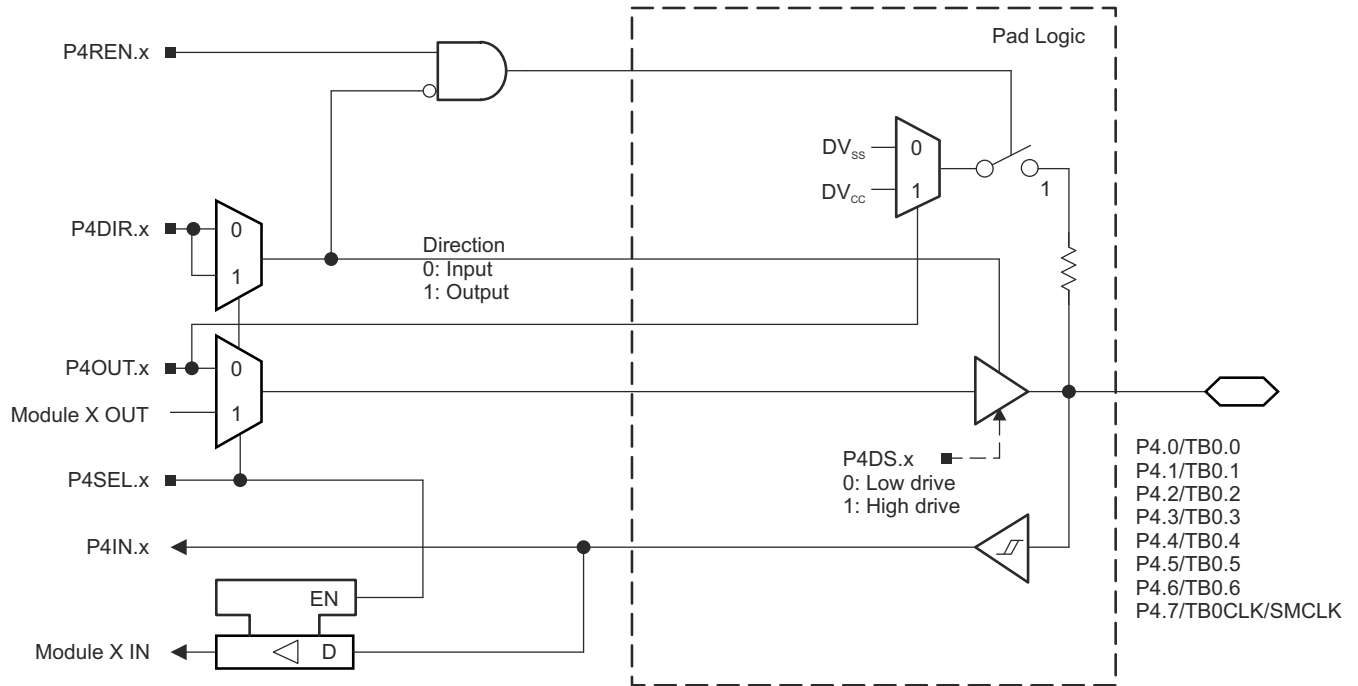


Figure 9-5. Port P4 (P4.0 to P4.7) Diagram

Table 9-46. Port P4 (P4.0 to P4.7) Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|-------------------|---|-------------------------|-------------------------|---------|
| | | | P4DIR.x | P4SEL.x |
| P4.0/TB0.0 | 0 | 4.0 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI0A and TB0.CCI0B | 0 | 1 |
| | | TB0.0 ⁽¹⁾ | 1 | 1 |
| P4.1/TB0.1 | 1 | 4.1 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI1A and TB0.CCI1B | 0 | 1 |
| | | TB0.1 ⁽¹⁾ | 1 | 1 |
| P4.2/TB0.2 | 2 | 4.2 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI2A and TB0.CCI2B | 0 | 1 |
| | | TB0.2 ⁽¹⁾ | 1 | 1 |
| P4.3/TB0.3 | 3 | 4.3 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI3A and TB0.CCI3B | 0 | 1 |
| | | TB0.3 ⁽¹⁾ | 1 | 1 |
| P4.4/TB0.5 | 4 | 4.4 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI4A and TB0.CCI4B | 0 | 1 |
| | | TB0.4 ⁽¹⁾ | 1 | 1 |
| P4.5/TB0.5 | 5 | 4.5 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI5A and TB0.CCI5B | 0 | 1 |
| | | TB0.5 ⁽¹⁾ | 1 | 1 |
| P4.6/TB0.6 | 6 | 4.6 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI6A and TB0.CCI6B | 0 | 1 |
| | | TB0.6 ⁽¹⁾ | 1 | 1 |
| P4.7/TB0CLK/SMCLK | 7 | 4.7 (I/O) | I: 0; O: 1 | 0 |
| | | TB0CLK | 0 | 1 |
| | | SMCLK | 1 | 1 |

(1) Setting TBOUTH causes all Timer_B configured outputs to be set to high impedance.

9.10.5 Port P5 (P5.0 and P5.1) Input/Output With Schmitt Trigger

Figure 9-6 shows the port diagram. Table 9-47 summarizes the selection of the pin functions.

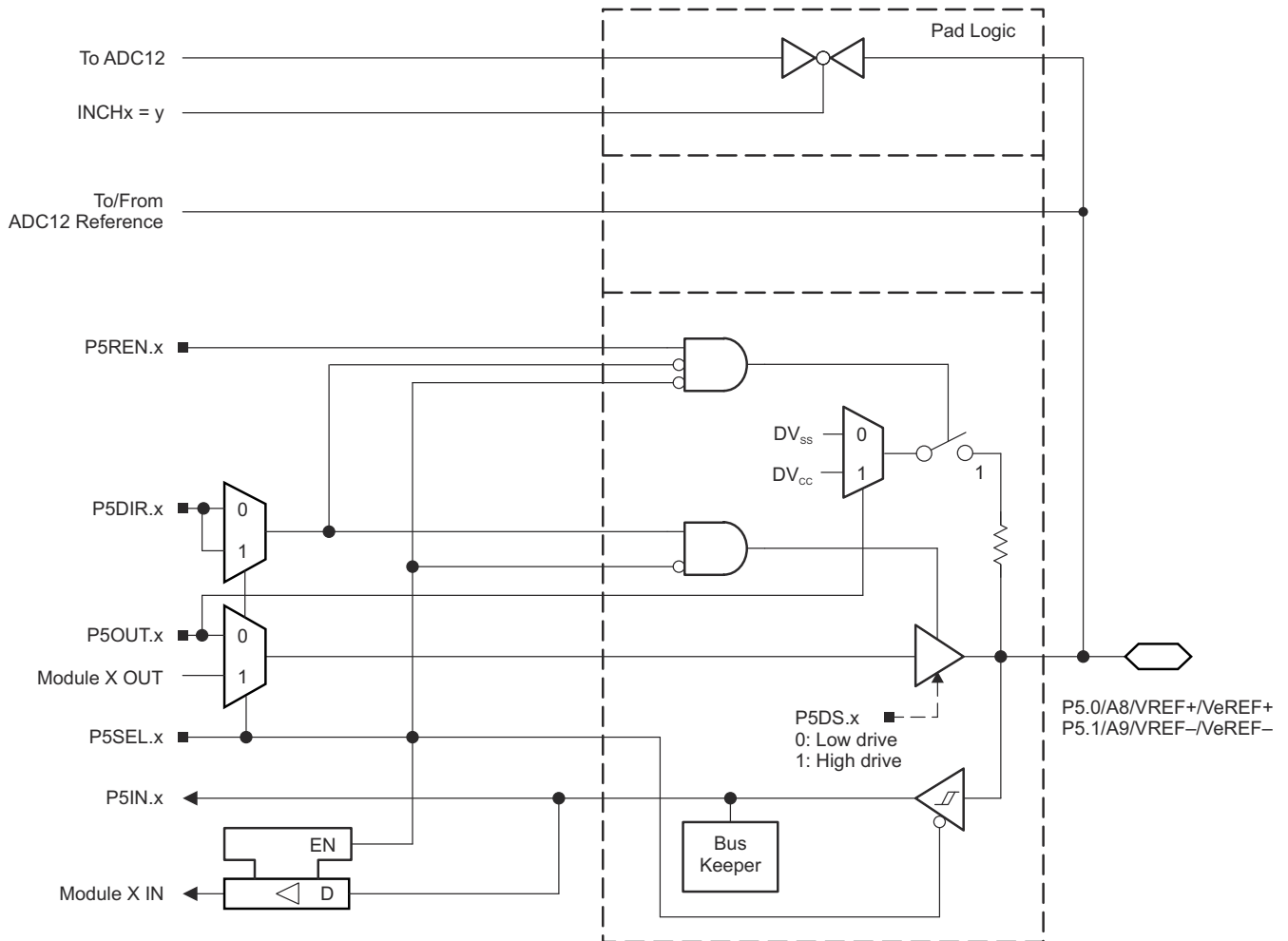


Figure 9-6. Port P5 (P5.0 and P5.1) Diagram

Table 9-47. Port P5 (P5.0 and P5.1) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|----------------------|---|---------------------------|--|---------|--------|
| | | | P5DIR.x | P5SEL.x | REFOUT |
| P5.0/A8/VREF+/VeREF+ | 0 | P5.0 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | X |
| | | A8/VeREF+ ⁽³⁾ | X | 1 | 0 |
| | | A8/VREF+ ⁽⁴⁾ | X | 1 | 1 |
| P5.1/A9/VREF-/VeREF- | 1 | P5.1 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | X |
| | | A9/VeREF- ⁽⁵⁾ | X | 1 | 0 |
| | | A9/VREF- ⁽⁶⁾ | X | 1 | 1 |

- (1) X = Don't care
- (2) Default condition
- (3) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12_A. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.
- (4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF+ reference is available at the pin. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.
- (5) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12_A. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.
- (6) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF- reference is available at the pin. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.

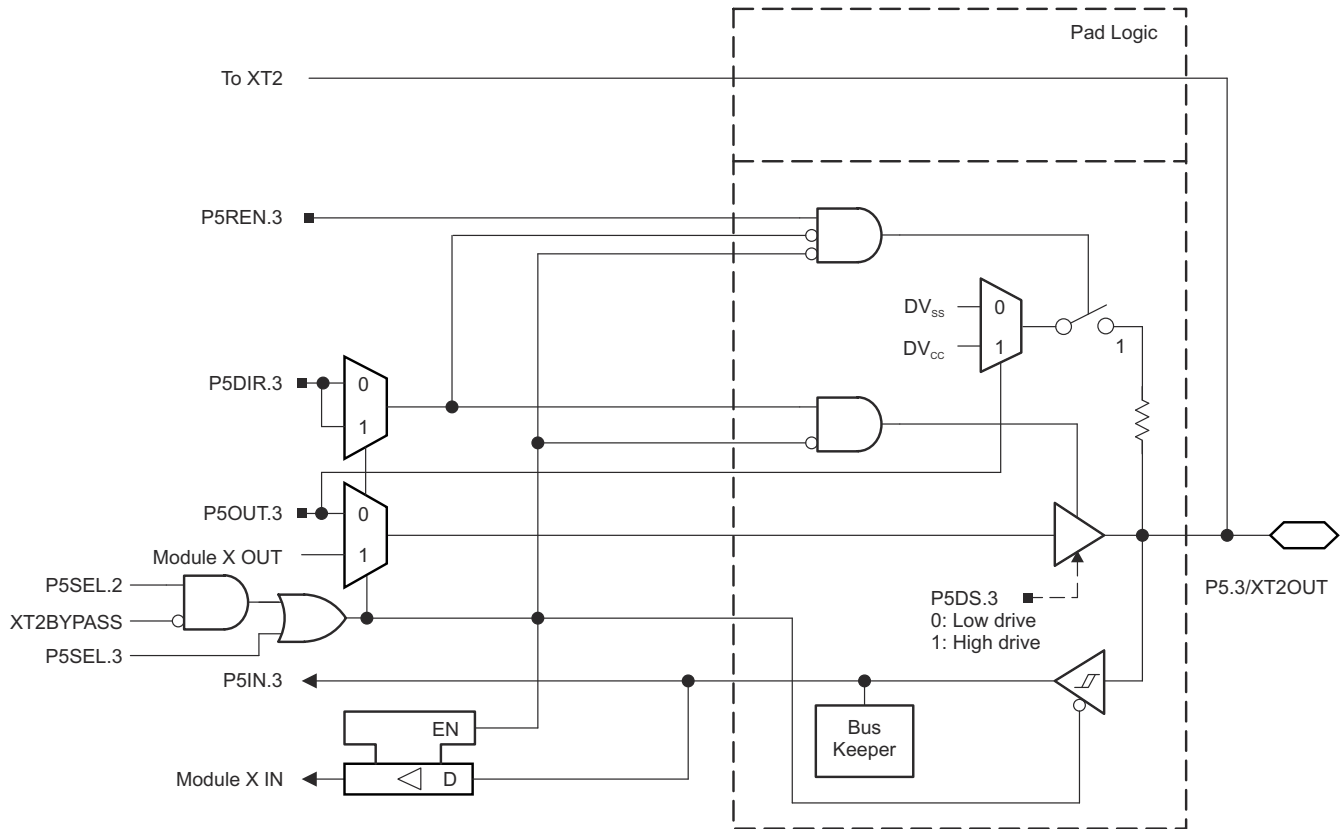


Figure 9-8. Port P5 (P5.3) Diagram

Table 9-48. Port P5 (P5.2 and P5.3) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------|---|------------------------------------|--|---------|---------|-----------|
| | | | P5DIR.x | P5SEL.2 | P5SEL.3 | XT2BYPASS |
| P5.2/XT2IN | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | X | X |
| | | XT2IN crystal mode ⁽²⁾ | X | 1 | X | 0 |
| | | XT2IN bypass mode ⁽²⁾ | X | 1 | X | 1 |
| P5.3/XT2OUT | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | XT2OUT crystal mode ⁽³⁾ | X | 1 | X | 0 |
| | | P5.3 (I/O) ⁽³⁾ | X | 1 | 0 | 1 |

- (1) X = Don't care
- (2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.
- (3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

9.10.7 Port P5 (P5.4 to P5.7) Input/Output With Schmitt Trigger

Figure 9-9 shows the port diagram. Table 9-49 summarizes the selection of the pin functions.

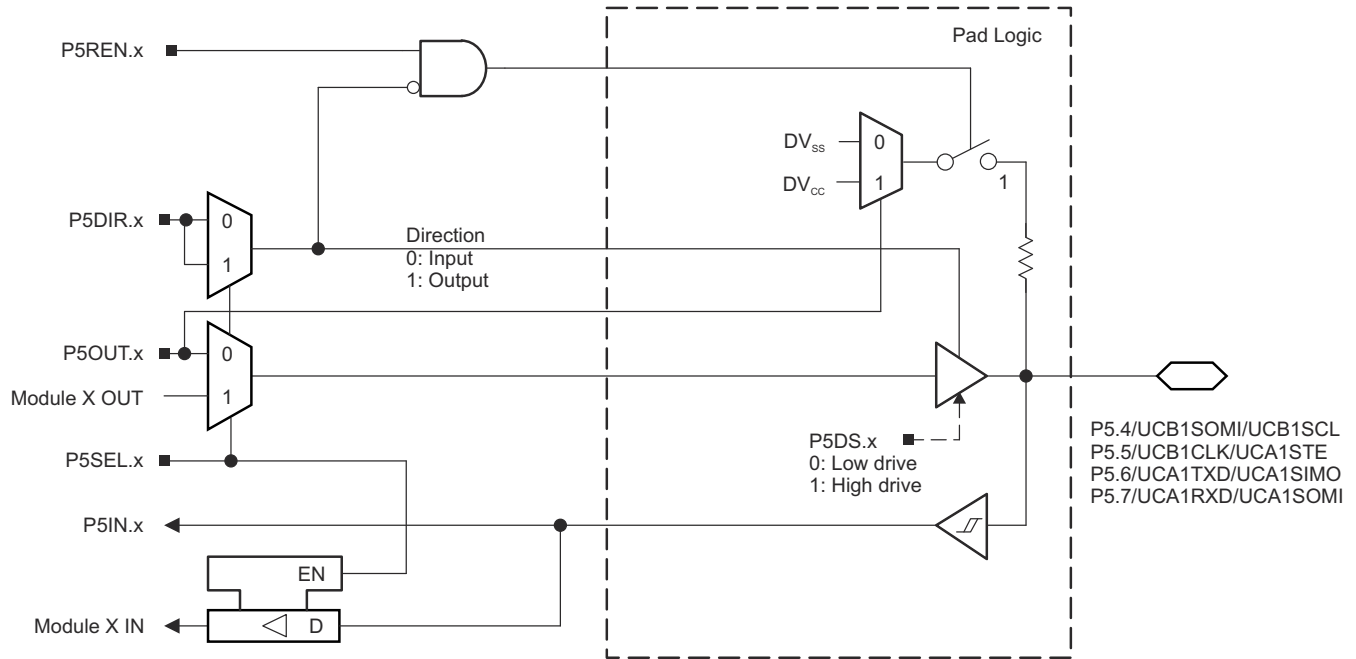


Figure 9-9. Port P5 (P5.4 to P5.7) Diagram

Table 9-49. Port P5 (P5.4 to P5.7) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | |
|-----------------------|---|-------------------------------------|--|---------|
| | | | P5DIR.x | P5SEL.x |
| P5.4/UCB1SOMI/UCB1SCL | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1SOMI/UCB1SCL ^{(2) (3)} | X | 1 |
| P5.5/UCB1CLK/UCA1STE | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 |
| | | UCB1CLK/UCA1STE ^{(2) (4)} | X | 1 |
| P5.6/UCA1TXD/UCA1SIMO | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 |
| | | UCA1TXD/UCA1SIMO ⁽²⁾ | X | 1 |
| P5.7/UCA1RXD/UCA1SOMI | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 |
| | | UCA1RXD/UCA1SOMI ⁽²⁾ | X | 1 |

- (1) X = Don't care
- (2) The pin direction is controlled by the USCI module.
- (3) If the I²C functionality is selected, the output drives only the logical 0 to V_{SS} level.
- (4) UCB1CLK function takes precedence over UCA1STE function. If the pin is required as UCB1CLK input or output, USCI_A1 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

9.10.8 Port P6 (P6.0 to P6.7) Input/Output With Schmitt Trigger

Figure 9-10 shows the port diagram. Table 9-50 summarizes the selection of the pin functions.

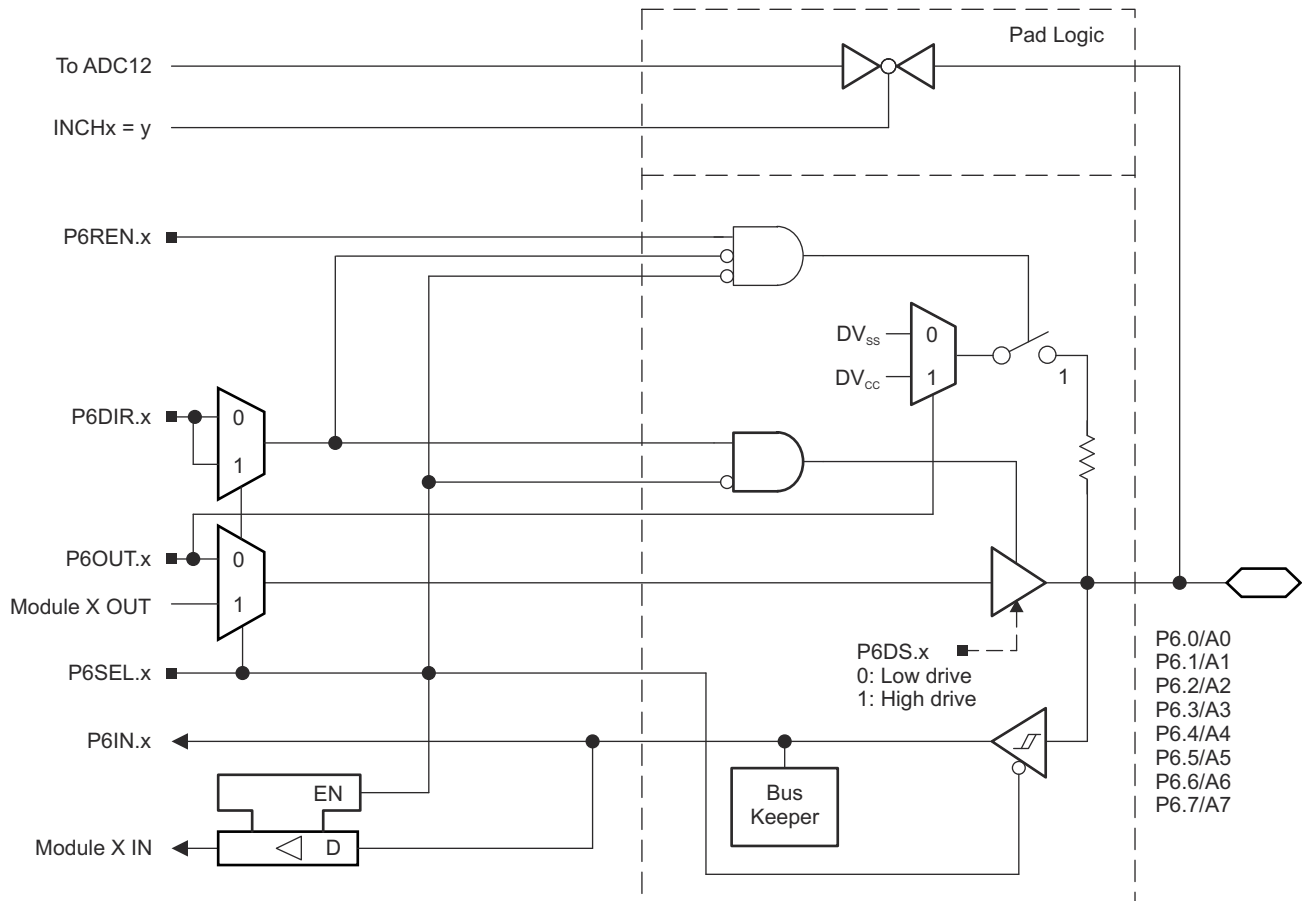


Figure 9-10. Port P6 (P6.0 to P6.7) Diagram

Table 9-50. Port P6 (P6.0 to P6.7) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|---------------------------|--|---------|-------|
| | | | P6DIR.x | P6SEL.x | INCHx |
| P6.0/A0 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | X |
| | | A0 ^{(2) (3)} | X | X | 0 |
| P6.1/A1 | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | X |
| | | A1 ^{(2) (3)} | X | X | 1 |
| P6.2/A2 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | X |
| | | A2 ^{(2) (3)} | X | X | 2 |
| P6.3/A3 | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | X |
| | | A3 ^{(2) (3)} | X | X | 3 |
| P6.4/A4 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | X |
| | | A4 ^{(2) (3)} | X | X | 4 |
| P6.5/A5 | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | X |
| | | A5 ^{(1) (2) (3)} | X | X | 5 |
| P6.6/A6 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | X |
| | | A6 ^{(2) (3)} | X | X | 6 |
| P6.7/A7 | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | X |
| | | A7 ^{(2) (3)} | X | X | 7 |

- (1) X = Don't care
- (2) Setting the P6SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

9.10.9 Port P7 (P7.0 and P7.1) Input/Output With Schmitt Trigger

Figure 9-11 and Figure 9-12 show the port diagrams. Table 9-51 summarizes the selection of the pin functions.

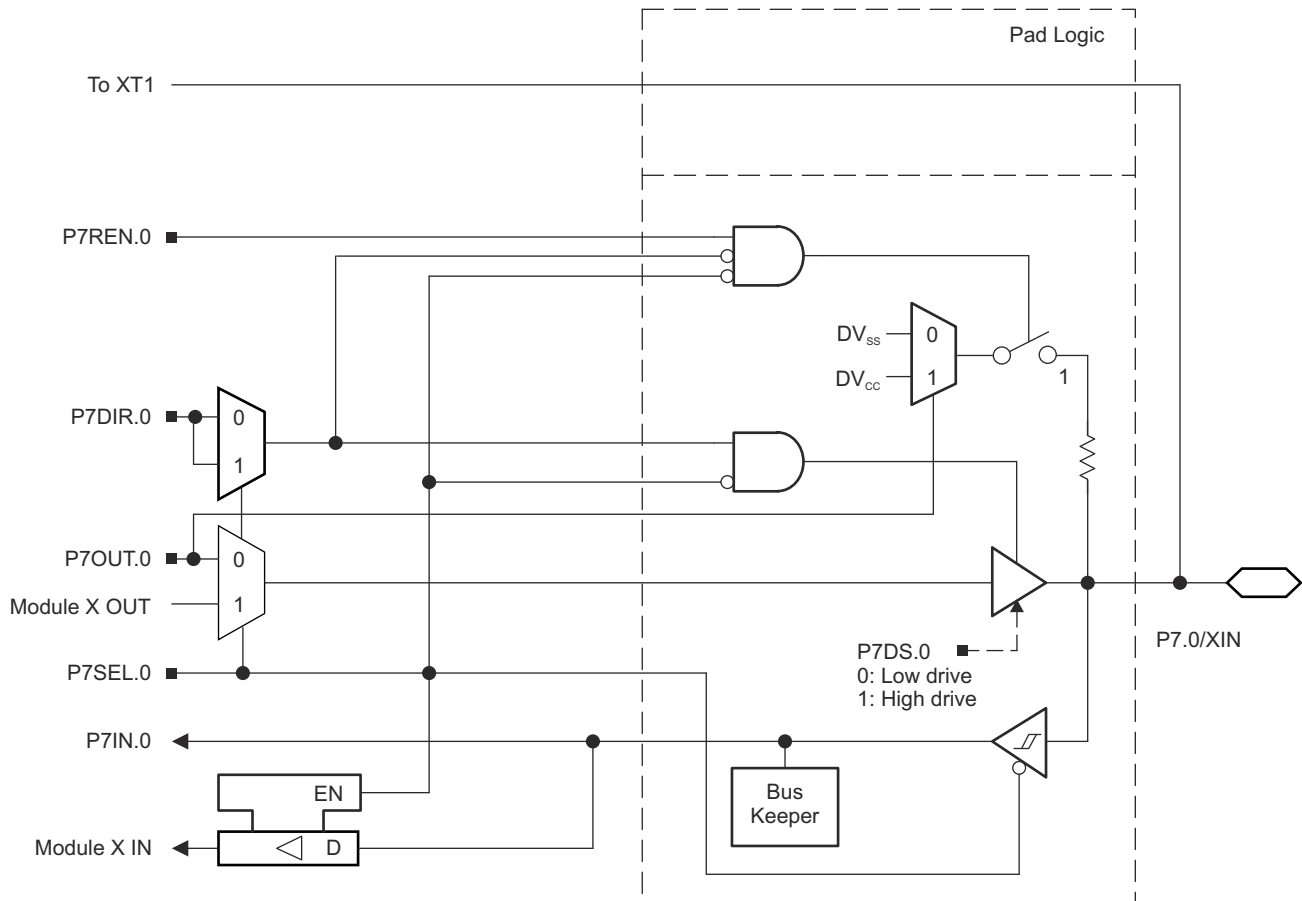


Figure 9-11. Port P7 (P7.0) Diagram

9.10.10 Port P7 (P7.2 and P7.3) Input/Output With Schmitt Trigger

Figure 9-13 shows the port diagram. Table 9-52 summarizes the selection of the pin functions.

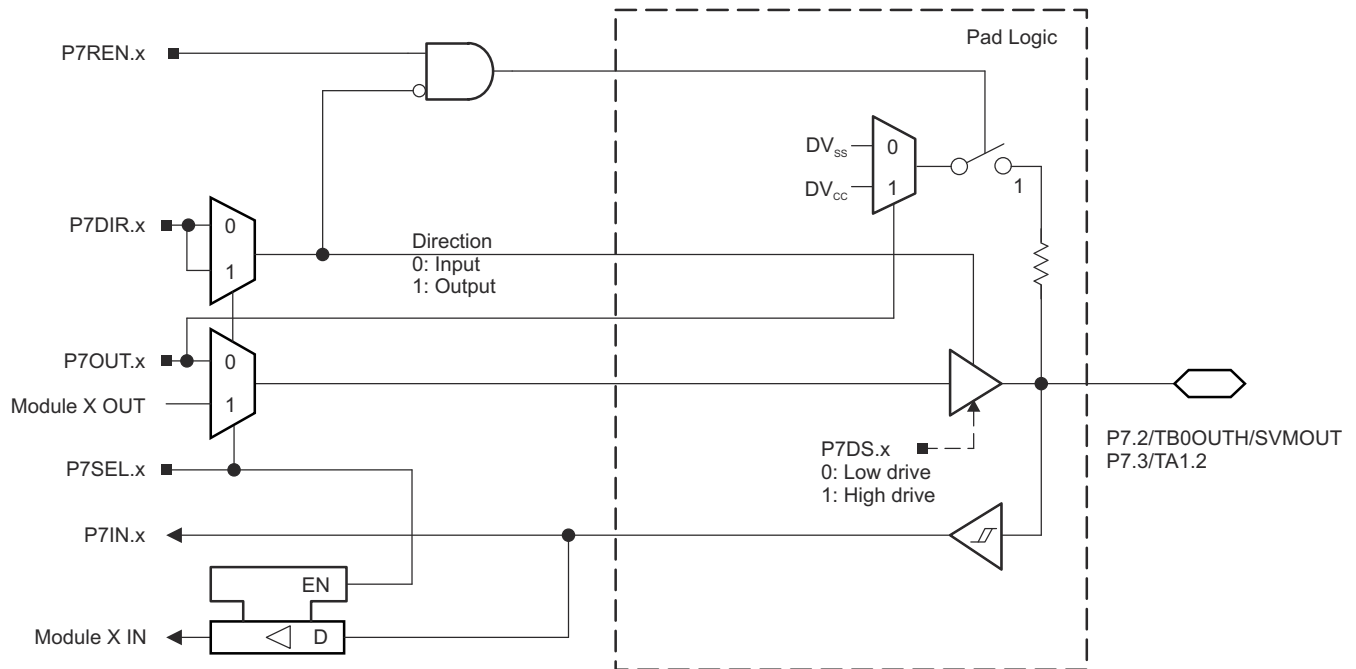


Figure 9-13. Port P7 (P7.2 and P7.3) Diagram

Table 9-52. Port P7 (P7.2 and P7.3) Pin Functions

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---------------------|---|------------|-------------------------|---------|
| | | | P7DIR.x | P7SEL.x |
| P7.2/TB0OUTH/SVMOUT | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 |
| | | TB0OUTH | 0 | 1 |
| | | SVMOUT | 1 | 1 |
| P7.3/TA1.2 | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI2B | 0 | 1 |
| | | TA1.2 | 1 | 1 |

9.10.11 Port P7 (P7.4 to P7.7) Input/Output With Schmitt Trigger

Figure 9-14 shows the port diagram. Table 9-53 summarizes the selection of the pin functions.

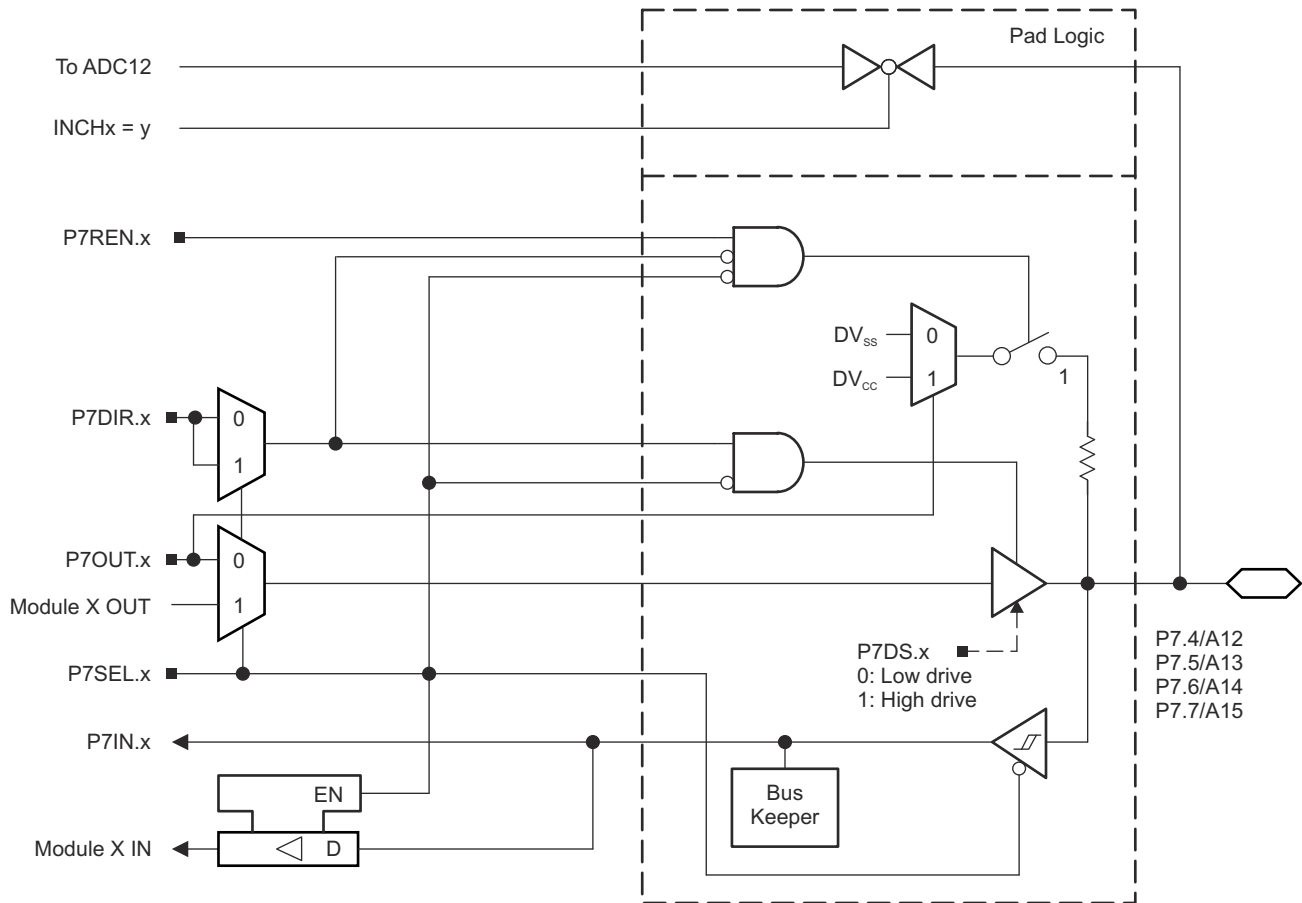


Figure 9-14. Port P7 (P7.4 to P7.7) Diagram

Table 9-53. Port P7 (P7.4 to P7.7) Pin Functions

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------------------|--|---------|-------|
| | | | P7DIR.x | P7SEL.x | INCHx |
| P7.4/A12 | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 | X |
| | | A12 ^{(2) (3)} | X | X | 12 |
| P7.5/A13 | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 | X |
| | | A13 ^{(2) (3)} | X | X | 13 |
| P7.6/A14 | 6 | P7.6 (I/O) | I: 0; O: 1 | 0 | X |
| | | A14 ^{(2) (3)} | X | X | 14 |
| P7.7/A15 | 7 | P7.7 (I/O) | I: 0; O: 1 | 0 | X |
| | | A15 ^{(2) (3)} | X | X | 15 |

- (1) X = Don't care
- (2) Setting the P7SEL.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected by the respective INCHx bits.

9.10.12 Port P8 (P8.0 to P8.7) Input/Output With Schmitt Trigger

Figure 9-15 shows the port diagram. Table 9-54 summarizes the selection of the pin functions.

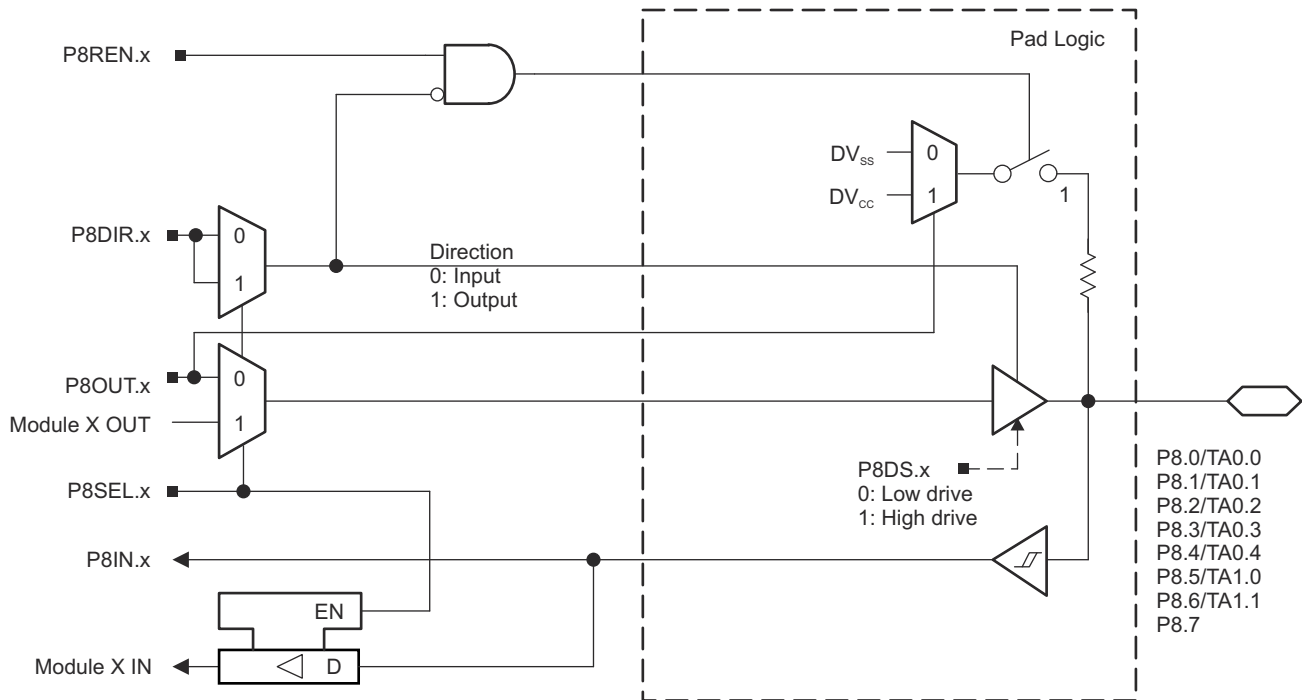


Figure 9-15. Port P8 (P8.0 to P8.7) Diagram

Table 9-54. Port P8 (P8.0 to P8.7) Pin Functions

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|-----------------|---|------------|-------------------------|---------|
| | | | P8DIR.x | P8SEL.x |
| P8.0/TA0.0 | 0 | P8.0 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI0B | 0 | 1 |
| | | TA0.0 | 1 | 1 |
| P8.1/TA0.1 | 1 | P8.1 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI1B | 0 | 1 |
| | | TA0.1 | 1 | 1 |
| P8.2/TA0.2 | 2 | P8.2 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI2B | 0 | 1 |
| | | TA0.2 | 1 | 1 |
| P8.3/TA0.3 | 3 | P8.3 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI3B | 0 | 1 |
| | | TA0.3 | 1 | 1 |
| P8.4/TA0.4 | 4 | P8.4 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI4B | 0 | 1 |
| | | TA0.4 | 1 | 1 |
| P8.5/TA1.0 | 5 | P8.5 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI0B | 0 | 1 |
| | | TA1.0 | 1 | 1 |
| P8.6/TA1.1 | 6 | P8.6 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI1B | 0 | 1 |
| | | TA1.1 | 1 | 1 |
| P8.7 | 7 | P8.7 (I/O) | I: 0; O: 1 | 0 |

9.10.13 Port P9 (P9.0 to P9.7) Input/Output With Schmitt Trigger

Figure 9-16 shows the port diagram. Table 9-55 summarizes the selection of the pin functions.

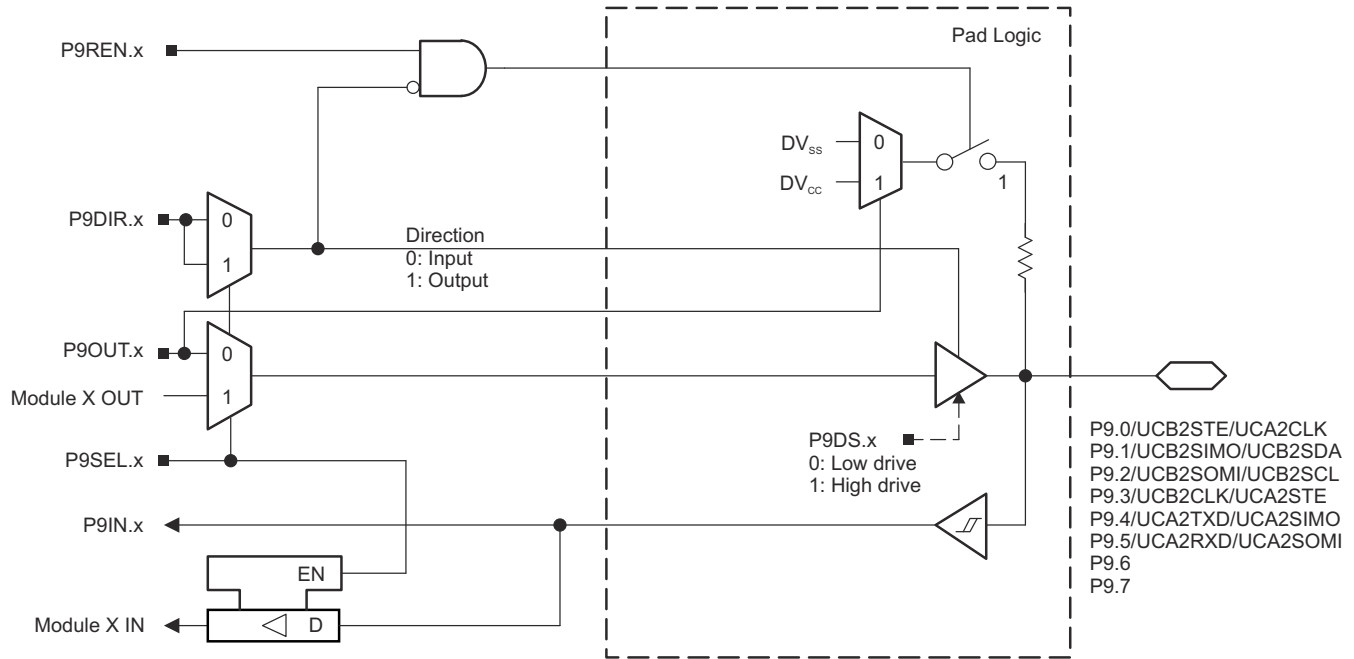


Figure 9-16. Port P9 (P9.0 to P9.7) Diagram

Table 9-55. Port P9 (P9.0 to P9.7) Pin Functions

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | |
|-----------------------|---|-------------------------------------|--|---------|
| | | | P9DIR.x | P9SEL.x |
| P9.0/UCB2STE/UCA2CLK | 0 | P9.0 (I/O) | I: 0; O: 1 | 0 |
| | | UCB2STE/UCA2CLK ^{(2) (4)} | X | 1 |
| P9.1/UCB2SIMO/UCB2SDA | 1 | P9.1 (I/O) | I: 0; O: 1 | 0 |
| | | UCB2SIMO/UCB2SDA ^{(2) (3)} | X | 1 |
| P9.2/UCB2SOMI/UCB2SCL | 2 | P9.2 (I/O) | I: 0; O: 1 | 0 |
| | | UCB2SOMI/UCB2SCL ^{(2) (3)} | X | 1 |
| P9.3/UCB2CLK/UCA2STE | 3 | P9.3 (I/O) | I: 0; O: 1 | 0 |
| | | UCB2CLK/UCA2STE ^{(2) (5)} | X | 1 |
| P9.4/UCA2TXD/UCA2SIMO | 4 | P9.4 (I/O) | I: 0; O: 1 | 0 |
| | | UCA2TXD/UCA2SIMO ⁽²⁾ | X | 1 |
| P9.5/UCA2RXD/UCA2SOMI | 5 | P9.5 (I/O) | I: 0; O: 1 | 0 |
| | | UCA2RXD/UCA2SOMI ⁽²⁾ | X | 1 |
| P9.6 | 6 | P9.6 (I/O) | I: 0; O: 1 | 0 |
| P9.7 | 7 | P9.7 (I/O) | I: 0; O: 1 | 0 |

- (1) X = Don't care
- (2) The pin direction is controlled by the USCI module.
- (3) If the I²C functionality is selected, the output drives only the logical 0 to V_{SS} level.
- (4) UCA2CLK function takes precedence over UCB2STE function. If the pin is required as UCA2CLK input or output, USCI_B2 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
- (5) UCB2CLK function takes precedence over UCA2STE function. If the pin is required as UCB2CLK input or output, USCI_A2 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

9.10.14 Port P10 (P10.0 to P10.7) Input/Output With Schmitt Trigger

Figure 9-17 shows the port diagram. Table 9-56 summarizes the selection of the pin functions.

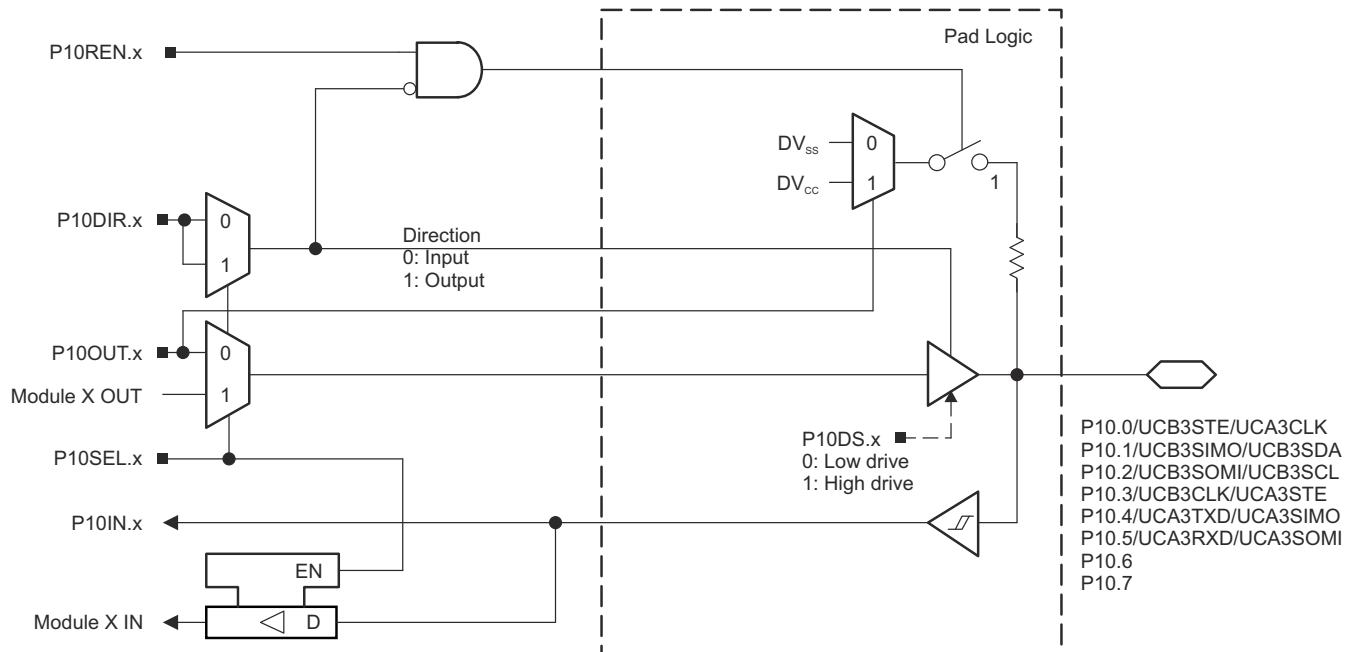


Figure 9-17. Port P10 (P10.0 to P10.7) Diagram

Table 9-56. Port P10 (P10.0 to P10.7) Pin Functions

| PIN NAME (P10.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | |
|------------------------|---|-------------------------------------|--|----------|
| | | | P10DIR.x | P10SEL.x |
| P10.0/UCB3STE/UCA3CLK | 0 | P10.0 (I/O) | I: 0; O: 1 | 0 |
| | | UCB3STE/UCA3CLK ^{(2) (4)} | X | 1 |
| P10.1/UCB3SIMO/UCB3SDA | 1 | P10.1 (I/O) | I: 0; O: 1 | 0 |
| | | UCB3SIMO/UCB3SDA ^{(2) (3)} | X | 1 |
| P10.2/UCB3SOMI/UCB3SCL | 2 | P10.2 (I/O) | I: 0; O: 1 | 0 |
| | | UCB3SOMI/UCB3SCL ^{(2) (3)} | X | 1 |
| P10.3/UCB3CLK/UCA3STE | 3 | P10.3 (I/O) | I: 0; O: 1 | 0 |
| | | UCB3CLK/UCA3STE ^{(2) (5)} | X | 1 |
| P10.4/UCA3TXD/UCA3SIMO | 4 | P10.4 (I/O) | I: 0; O: 1 | 0 |
| | | UCA3TXD/UCA3SIMO ⁽²⁾ | X | 1 |
| P10.5/UCA3RXD/UCA3SOMI | 5 | P10.5 (I/O) | I: 0; O: 1 | 0 |
| | | UCA3RXD/UCA3SOMI ⁽²⁾ | X | 1 |
| P10.6 | 6 | P10.6 (I/O) | I: 0; O: 1 | 0 |
| | | Reserved ⁽⁶⁾ | X | 1 |
| P10.7 | 7 | P10.7 (I/O) | I: 0; O: 1 | 0 |
| | | Reserved ⁽⁶⁾ | x | 1 |

- (1) X = Don't care
- (2) The pin direction is controlled by the USC1 module.
- (3) If the I²C functionality is selected, the output drives only the logical 0 to V_{SS} level.
- (4) UCA3CLK function takes precedence over UCB3STE function. If the pin is required as UCA3CLK input or output, USC1_B3 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
- (5) UCB3CLK function takes precedence over UCA3STE function. If the pin is required as UCB3CLK input or output, USC1_A3 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
- (6) The secondary function on these pins are reserved for factory test purposes. Application should keep the P10SEL.x of these ports cleared to prevent potential conflicts with the application.

9.10.15 Port P11 (P11.0 to P11.2) Input/Output With Schmitt Trigger

Figure 9-18 shows the port diagram. Table 9-57 summarizes the selection of the pin functions.

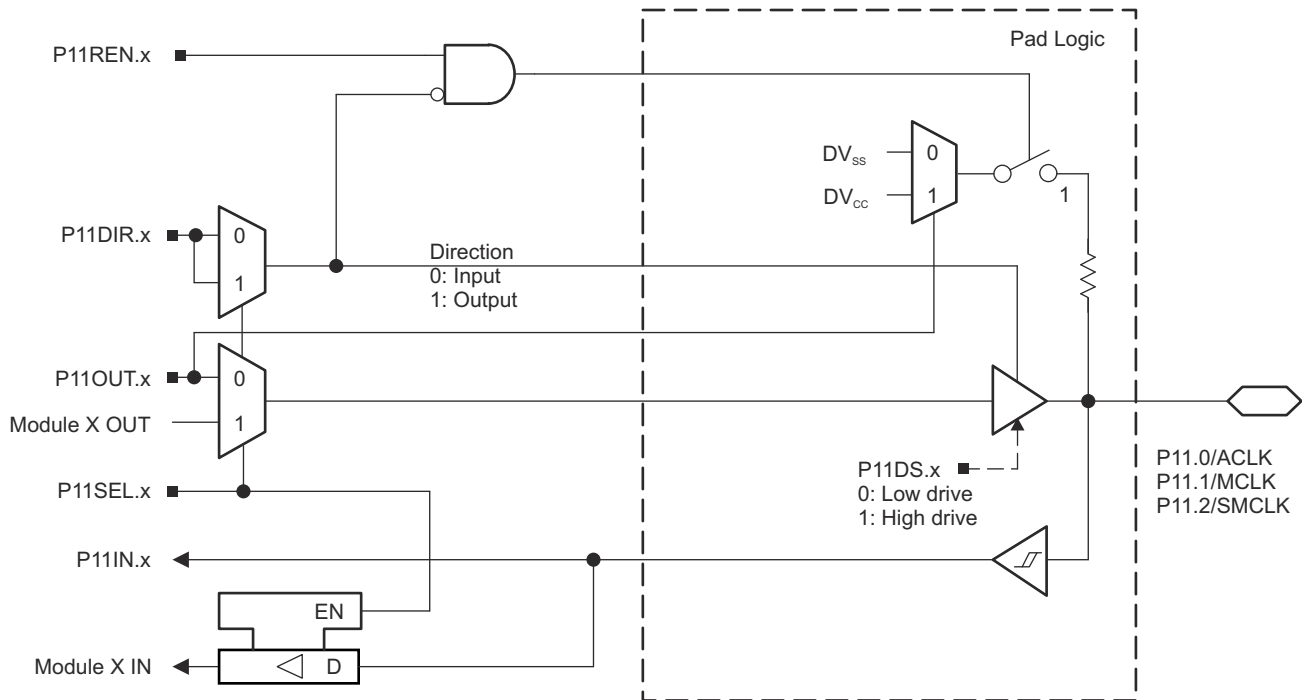


Figure 9-18. Port P11 (P11.0 to P11.2) Diagram

Table 9-57. Port P11 (P11.0 to P11.2) Pin Functions

| PIN NAME (P11.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|------------------|---|-------------|-------------------------|----------|
| | | | P11DIR.x | P11SEL.x |
| P11.0/ACLK | 0 | P11.0 (I/O) | I: 0; O: 1 | 0 |
| | | ACLK | 1 | 1 |
| P11.1/MCLK | 1 | P11.1 (I/O) | I: 0; O: 1 | 0 |
| | | MCLK | 1 | 1 |
| P11.2/SMCLK | 2 | P11.2 (I/O) | I: 0; O: 1 | 0 |
| | | SMCLK | 1 | 1 |

9.10.16 Port PJ (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 9-19 shows the port diagram. Table 9-58 summarizes the selection of the pin functions.

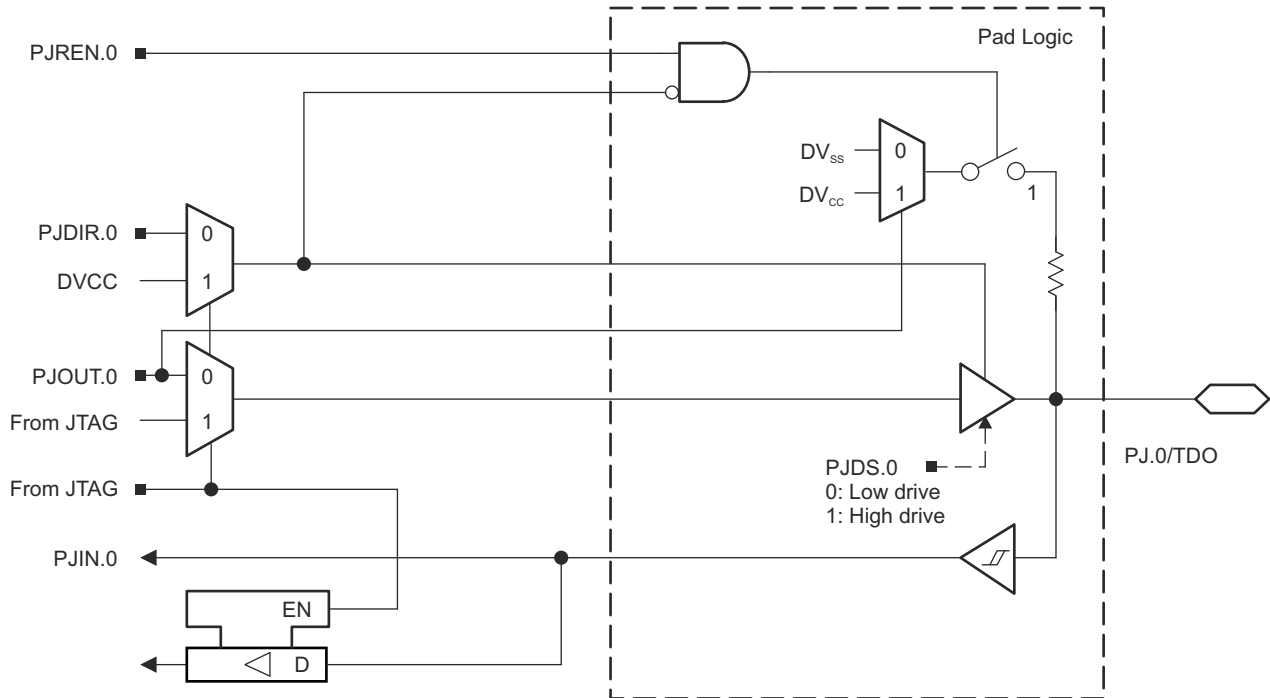


Figure 9-19. Port PJ (PJ.0) Diagram

9.10.17 Port PJ (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 9-20 shows the port diagram. Table 9-58 summarizes the selection of the pin functions.

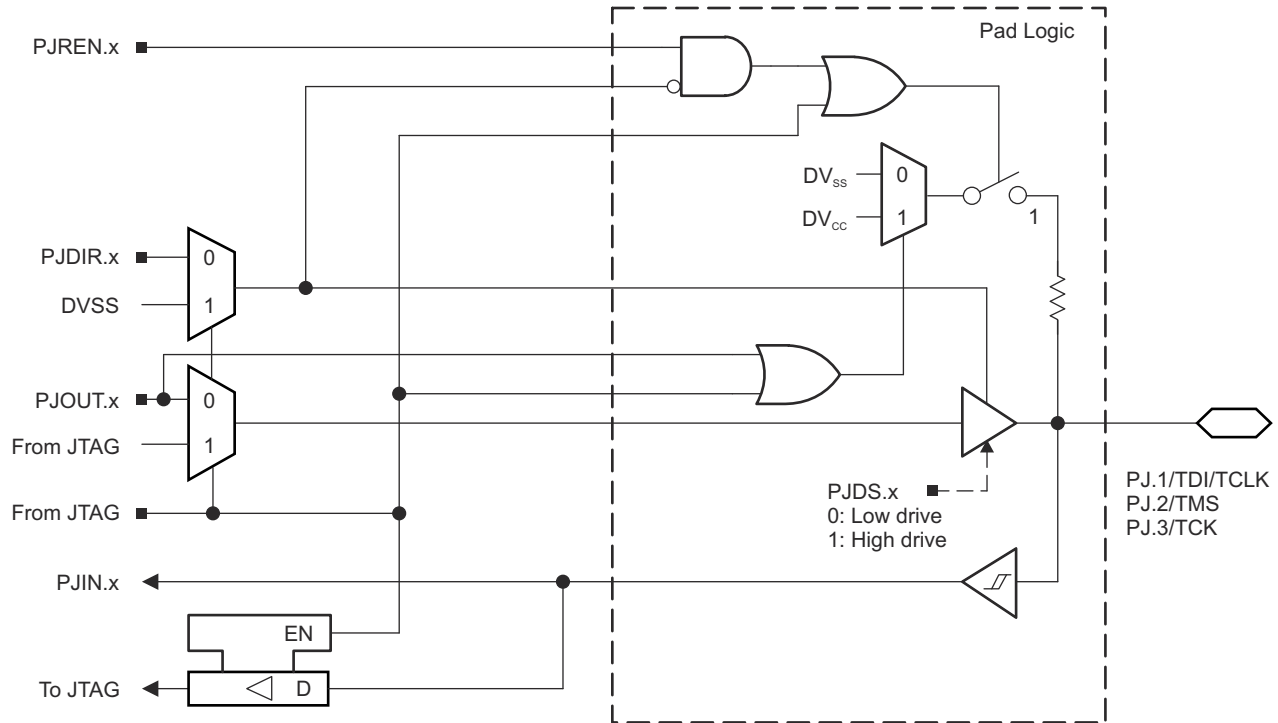


Figure 9-20. Port PJ (PJ.1 to PJ.3) Diagram

Table 9-58. Port PJ (PJ.0 to PJ.3) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ |
|-----------------|---|-----------------------------|--|
| | | | PJDIR.x |
| PJ.0/TDO | 0 | PJ.0 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TDO ⁽³⁾ | X |
| PJ.1/TDI/TCLK | 1 | PJ.1 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TDI/TCLK ^{(3) (4)} | X |
| PJ.2/TMS | 2 | PJ.2 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TMS ^{(3) (4)} | X |
| PJ.3/TCK | 3 | PJ.3 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TCK ^{(3) (4)} | X |

- (1) X = Don't care
- (2) Default condition
- (3) The pin direction is controlled by the JTAG module.
- (4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

9.11 Device Descriptors

Table 9-59 shows the contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 9-59. Device Descriptors

| DESCRIPTION ⁽¹⁾ | ADDRESS | SIZE (bytes) | VALUE | | | | | | |
|----------------------------|--|-----------------|--------|----------|----------|----------|----------|----------|----------|
| | | | F5438A | F5437A | F5436A | F5435A | F5419A | F5418A | |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 01A04h | 1 | 05h | 04h | 03h | 02h | 01h | 00h |
| | Device ID | 01A05h | 1 | 80h | 80h | 80h | 80h | 80h | 80h |
| | Hardware revision | 01A06h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 01A07h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 01A08h | 1 | 08h | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | 4 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die X position | 01A0Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die Y position | 01A10h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test results | 01A12h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| ADC12 Calibration | ADC12 calibration tag | 01A14h | 1 | 11h | 11h | 11h | 11h | 11h | 11h |
| | ADC12 calibration length | 01A15h | 1 | 10h | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC offset | 01A18h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 30°C | 01A1Ah | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 85°C | 01A1Ch | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 30°C | 01A1Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 85°C | 01A20h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 30°C | 01A22h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 85°C | 01A24h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| REF Calibration | REF calibration tag | 01A26h | 1 | 12h | 12h | 12h | 12h | 12h | 12h |
| | REF calibration length | 01A27h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | REF 1.5-V reference | 01A28h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | REF 2.0-V reference | 01A2Ah | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | REF 2.5-V reference | 01A2Ch | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |

Table 9-59. Device Descriptors (continued)

| DESCRIPTION ⁽¹⁾ | ADDRESS | SIZE (bytes) | VALUE | | | | | | |
|------------------------------|---------|-----------------|------------|------------|------------|------------|------------|------------|------------|
| | | | F5438A | F5437A | F5436A | F5435A | F5419A | F5418A | |
| Peripheral descriptor tag | 01A2Eh | 1 | 02h | 02h | 02h | 02h | 02h | 02h | 02h |
| Peripheral descriptor length | 01A2Fh | 1 | 61h | 059h | 62h | 5Ah | 61h | 59h | 59h |
| Memory 1 | | 2 | 08h 8Ah | 08h 8Ah | 08h 8Ah | 08h 8Ah | 08h 8Ah | 08h 8Ah | 08h 8Ah |
| Memory 2 | | 2 | 0Ch 86h | 0Ch 86h | 0Ch 86h | 0Ch 86h | 0Ch 86h | 0Ch 86h | 0Ch 86h |
| Memory 3 | | 2 | 0Eh 30h | 0Eh 30h | 0Eh 30h | 0Eh 30h | 0Eh 30h | 0Eh 30h | 0Eh 30h |
| Memory 4 | | 2 | 2Eh 98h | 2Eh 98h | 2Eh 97h | 2Eh 97h | 2Eh 96h | 2Eh 96h | 2Eh 96h |
| Memory 5 | | 0/1 | N/A | N/A | 94h | 94h | N/A | N/A | N/A |
| Delimiter | | 1 | 00h | 00h | 00h | 00h | 00h | 00h | 00h |
| Peripheral count | | 1 | 21h | 1Dh | 21h | 1Dh | 21h | 1Dh | 1Dh |
| MSP430CPUXV2 | | 2 | 00h 23h | 00h 23h | 00h 23h | 00h 23h | 00h 23h | 00h 23h | 00h 23h |
| SBW | | 2 | 00h 0Fh | 00h 0Fh | 00h 0Fh | 00h 0Fh | 00h 0Fh | 00h 0Fh | 00h 0Fh |
| EEM-8 | | 2 | 00h 05h | 00h 05h | 00h 05h | 00h 05h | 00h 05h | 00h 05h | 00h 05h |
| TI BSL | | 2 | 00h FCh | 00h FCh | 00h FCh | 00h FCh | 00h FCh | 00h FCh | 00h FCh |
| Package | | 2 | 00h 1Fh | 00h 1Fh | 00h 1Fh | 00h 1Fh | 00h 1Fh | 00h 1Fh | 00h 1Fh |
| SFR | | 2 | 10h 41h | 10h 41h | 10h 41h | 10h 41h | 10h 41h | 10h 41h | 10h 41h |
| PMM | | 2 | 02h 30h | 02h 30h | 02h 30h | 02h 30h | 02h 30h | 02h 30h | 02h 30h |
| FCTL | | 2 | 02h 38h | 02h 38h | 02h 38h | 02h 38h | 02h 38h | 02h 38h | 02h 38h |
| CRC16 straight | | 2 | 01h 3Ch | 01h 3Ch | 01h 3Ch | 01h 3Ch | 01h 3Ch | 01h 3Ch | 01h 3Ch |
| CRC16 bit reversed | | 2 | 00h 3Dh | 00h 3Dh | 00h 3Dh | 00h 3Dh | 00h 3Dh | 00h 3Dh | 00h 3Dh |
| RAMCTL | | 2 | 00h 44h | 00h 44h | 00h 44h | 00h 44h | 00h 44h | 00h 44h | 00h 44h |
| WDT_A | | 2 | 00h 40h | 00h 40h | 00h 40h | 00h 40h | 00h 40h | 00h 40h | 00h 40h |
| UCS | | 2 | 01h 48h | 01h 48h | 01h 48h | 01h 48h | 01h 48h | 01h 48h | 01h 48h |
| SYS | | 2 | 02h 42h | 02h 42h | 02h 42h | 02h 42h | 02h 42h | 02h 42h | 02h 42h |
| REF | | 2 | 03h A0h | 03h A0h | 03h A0h | 03h A0h | 03h A0h | 03h A0h | 03h A0h |
| Port 1 and 2 | | 2 | 05h 51h | 05h 51h | 05h 51h | 05h 51h | 05h 51h | 05h 51h | 05h 51h |
| Port 3 and 4 | | 2 | 02h 52h | 02h 52h | 02h 52h | 02h 52h | 02h 52h | 02h 52h | 02h 52h |
| Port 5 and 6 | | 2 | 02h 53h | 02h 53h | 02h 53h | 02h 53h | 02h 53h | 02h 53h | 02h 53h |
| Port 7 and 8 | | 2 | 02h 54h | 02h 54h | 02h 54h | 02h 54h | 02h 54h | 02h 54h | 02h 54h |
| Port 9 and 10 | | 2 | 02h 55h | N/A | 02h 55h | N/A | 02h 55h | N/A | N/A |
| Port 11 and 12 | | 2 | 02h 56h | N/A | 02h 56h | N/A | 02h 56h | N/A | N/A |

Peripheral
Descriptor

Table 9-59. Device Descriptors (continued)

| DESCRIPTION ⁽¹⁾ | ADDRESS | SIZE (bytes) | VALUE | | | | | | |
|---|-------------------|-----------------|--------|------------|------------|------------|------------|------------|------------|
| | | | F5438A | F5437A | F5436A | F5435A | F5419A | F5418A | |
| Peripheral Descriptor (continued) | JTAG | | 2 | 08h 5Fh | 0Ch 5Fh | 08h 5Fh | 0Ch 5Fh | 08h 5Fh | 0Ch 5Fh |
| | TA0 | | 2 | 02h 62h | 02h 62h | 02h 62h | 02h 62h | 02h 62h | 02h 62h |
| | TA1 | | 2 | 04h 61h | 04h 61h | 04h 61h | 04h 61h | 04h 61h | 04h 61h |
| | TB0 | | 2 | 04h 67h | 04h 67h | 04h 67h | 04h 67h | 04h 67h | 04h 67h |
| | RTC | | 2 | 0Eh 68h | 0Eh 68h | 0Eh 68h | 0Eh 68h | 0Eh 68h | 0Eh 68h |
| | MPY32 | | 2 | 02h 85h | 02h 85h | 02h 85h | 02h 85h | 02h 85h | 02h 85h |
| | DMA-3 | | 2 | 04h 47h | 04h 47h | 04h 47h | 04h 47h | 04h 47h | 04h 47h |
| | USCI_A and USCI_B | | 2 | 0Ch 90h | 0Ch 90h | 0Ch 90h | 0Ch 90h | 0Ch 90h | 0Ch 90h |
| | USCI_A and USCI_B | | 2 | 04h 90h | 04h 90h | 04h 90h | 04h 90h | 04h 90h | 04h 90h |
| | USCI_A and USCI_B | | 2 | 04h 90h | N/A | 04h 90h | N/A | 04h 90h | N/A |
| | USCI_A and USCI_B | | 2 | 04h 90h | N/A | 04h 90h | N/A | 04h 90h | N/A |
| | ADC12_A | | 2 | 08h D1h | 10h D1h | 08h D1h | 10h D1h | 08h D1h | 10h D1h |
| Interrupts | TB0.CCIFG0 | | 1 | 64h | 64h | 64h | 64h | 64h | 64h |
| | TB0.CCIFG1..6 | | 1 | 65h | 65h | 65h | 65h | 65h | 65h |
| | WDTIFG | | 1 | 40h | 40h | 40h | 40h | 40h | 40h |
| | USCI_A0 | | 1 | 90h | 90h | 90h | 90h | 90h | 90h |
| | USCI_B0 | | 1 | 91h | 91h | 91h | 91h | 91h | 91h |
| | ADC12_A | | 1 | D0h | D0h | D0h | D0h | D0h | D0h |
| | TA0.CCIFG0 | | 1 | 60h | 60h | 60h | 60h | 60h | 60h |
| | TA0.CCIFG1..4 | | 1 | 61h | 61h | 61h | 61h | 61h | 61h |
| | USCI_A2 | | 1 | 94h | 01h | 94h | 01h | 94h | 01h |
| | USCI_B2 | | 1 | 95h | 01h | 95h | 01h | 95h | 01h |
| | DMA | | 1 | 46h | 46h | 46h | 46h | 46h | 46h |
| | TA1.CCIFG0 | | 1 | 62h | 62h | 62h | 62h | 62h | 62h |
| | TA1.CCIFG1..2 | | 1 | 63h | 63h | 63h | 63h | 63h | 63h |
| | P1 | | 1 | 50h | 50h | 50h | 50h | 50h | 50h |
| | USCI_A1 | | 1 | 92h | 92h | 92h | 92h | 92h | 92h |
| | USCI_B1 | | 1 | 93h | 93h | 93h | 93h | 93h | 93h |
| | USCI_A3 | | 1 | 96h | 01h | 96h | 01h | 96h | 01h |
| | USCI_B3 | | 1 | 97h | 01h | 97h | 01h | 97h | 01h |
| | P2 | | 1 | 51h | 51h | 51h | 51h | 51h | 51h |
| | RTC_A | | 1 | 68h | 68h | 68h | 68h | 68h | 68h |
| Delimiter | | 1 | 00h | 00h | 00h | 00h | 00h | 00h | |

(1) N/A = Not applicable

10 Device and Documentation Support

10.1 Getting Started

For an introduction to the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the [MSP430 ultra-low-power sensing & measurement MCUs overview](#).

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

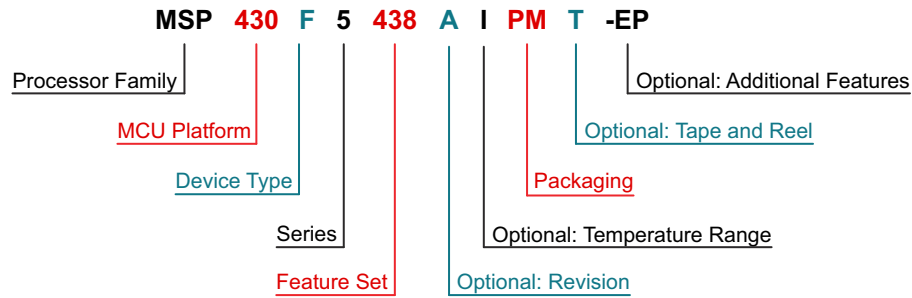
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [Figure 10-1](#) provides a legend for reading the complete device name.



| | | | |
|---|--|---|---|
| Processor Family | CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device | | |
| MCU Platform | 430 = MSP430 low-power microcontroller platform | | |
| Device Type | <table border="0" style="width: 100%;"> <tr> <td style="vertical-align: top;">Memory Type C = ROM F = Flash FR = FRAM G = Flash L = No nonvolatile memory</td> <td style="vertical-align: top;">Specialized Application AFE = Analog front end BQ = Contactless power CG = ROM medical FE = Flash energy meter FG = Flash medical FW = Flash electronic flow meter</td> </tr> </table> | Memory Type C = ROM F = Flash FR = FRAM G = Flash L = No nonvolatile memory | Specialized Application AFE = Analog front end BQ = Contactless power CG = ROM medical FE = Flash energy meter FG = Flash medical FW = Flash electronic flow meter |
| Memory Type C = ROM F = Flash FR = FRAM G = Flash L = No nonvolatile memory | Specialized Application AFE = Analog front end BQ = Contactless power CG = ROM medical FE = Flash energy meter FG = Flash medical FW = Flash electronic flow meter | | |
| Series | <table border="0" style="width: 100%;"> <tr> <td style="vertical-align: top;">1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD driver</td> <td style="vertical-align: top;">5 = Up to 25 MHz 6 = Up to 25 MHz with LCD driver 0 = Low-voltage series</td> </tr> </table> | 1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD driver | 5 = Up to 25 MHz 6 = Up to 25 MHz with LCD driver 0 = Low-voltage series |
| 1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD driver | 5 = Up to 25 MHz 6 = Up to 25 MHz with LCD driver 0 = Low-voltage series | | |
| Feature Set | Various levels of integration within a series | | |
| Optional: Revision | Updated version of the base part number | | |
| Optional: Temperature Range | S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105°C | | |
| Packaging | http://www.ti.com/packaging | | |
| Optional: Tape and Reel | T = Small reel R = Large reel No markings = Tube or tray | | |
| Optional: Additional Features | -EP = Enhanced product (-40°C to 105°C) -HT = Extreme temperature parts (-55°C to 150°C) -Q1 = Automotive Q100 qualified | | |

Figure 10-1. Device Nomenclature

10.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at [MSP430 Ultra-Low-Power MCUs – Tools & software](#).

Table 10-1 lists the debug features of the MSP430F543xA and MSP430F541xA MCUs. See the [Code Composer Studio IDE for MSP430 User's Guide](#) for details on the available features.

Table 10-1. Hardware Debug Features

| MSP430 ARCHITECTURE | 4-WIRE JTAG | 2-WIRE JTAG | BREAK-POINTS (N) | RANGE BREAK-POINTS | CLOCK CONTROL | STATE SEQUENCER | TRACE BUFFER | LPMx.5 DEBUGGING SUPPORT |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|
| MSP430Xv2 | Yes | Yes | 8 | Yes | Yes | Yes | Yes | No |

Design Kits and Evaluation Modules

[MSP-TS430PZ5x100 - 100-pin Target Development Board for MSP430F5x MCUs](#)

The MSP-TS430PZ5X100 is a stand-alone ZIF socket target board used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol.

[100-pin Target Development Board and MSP-FET Programmer Bundle for MSP430F5x MCUs](#)

The MSP-FET430U5x100 is a powerful flash emulation tool (FET) that includes the hardware and software required to quickly begin application development on the MSP430 MCU. It includes a ZIF socket target board (MSP-TS430PZ5x100) and a USB debugging interface (MSP-FET) used to program and debug the MSP430 in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol. The flash memory can be erased and programmed in seconds with only a few keystrokes, and since the MSP430 flash is ultra-low power, no external power supply is required.

[MSP430F5438 Experimenter Board](#)

The MSP430F5438 Experimenter Board (MSP-EXP430F5438) is a microcontroller development for highly integrated, high performance MSP430F5438 MCUs. It features a 100-pin socket which supports the MSP430F5438A and other devices with similar pinout. The socket allows for quick upgrades to newer devices or quick applications changes. It is compatible with many TI low-power RF wireless development kits such as the CC2520EMK. The Experimenter Board helps designers quickly learn and develop using the F5xx MCUs, which provide low power, more memory and leading integration for applications such as energy harvesting, wireless sensing and automatic metering infrastructure (AMI).

Software

[MSP430Ware™ Software](#)

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of Code Composer Studio™ IDE or as a stand-alone package.

[MSP430F543xA, MSP430F541xA Code Examples](#)

C Code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

[MSP Driver Library](#)

Driver Library's abstracted API keeps you above the bits and bytes of the MSP430 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

[MSP EnergyTrace™ Technology](#)

EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

[ULP \(Ultra-Low Power\) Advisor](#)

ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully utilize the unique ultra-low power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to squeeze every last nano amp out of your application. At build time, ULP Advisor will provide notifications and remarks to highlight areas of your code that can be further optimized for lower power.

[IEC60730 Software Package](#)

The IEC60730 MSP430 software package was developed to be useful in assisting customers in complying with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC60730 MSP430 software package can be embedded in customer applications running on MSP430s to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

[Fixed Point Math Library for MSP](#)

The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

[Floating Point Math Library for MSP430](#)

Continuing to innovate in the low power and low cost microcontroller space, TI brings you MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating point math library of scalar functions brings you up to 26x better performance. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio and IAR IDEs. Read the user's guide for an in depth look at the math library and relevant benchmarks.

Development Tools

[Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers](#)

Code Composer Studio is an integrated development environment (IDE) that supports all MSP microcontroller devices. Code Composer Studio comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar utilities and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers. When using CCS with an MSP MCU, a unique and powerful set of plugins and embedded software utilities are made available to fully leverage the MSP microcontroller.

[Command-Line Programmer](#)

MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) files directly to the MSP microcontroller without an IDE.

MSP MCU Programmer and Debugger

The MSP-FET is a powerful emulation development tool – often called a debug probe – which allows users to quickly begin application development on MSP low-power microcontrollers (MCU). Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging. The MSP-FET provides a debug communication pathway between a host computer and the target MSP. Furthermore, the MSP-FET also provides a Backchannel UART connection between the computer's USB interface and the MSP UART. This affords the MSP programmer a convenient method for communicating serially between the MSP and a terminal running on the computer. It also supports loading programs (often called firmware) to the MSP target using the BSL (bootloader) through the UART and I²C communication protocols.

MSP-GANG Production Programmer

The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 Flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process. The MSP Gang Programmer is provided with an expansion board, called the Gang Splitter, that implements the interconnections between the MSP Gang Programmer and multiple target devices. Eight cables are provided that connect the expansion board to eight target devices (through JTAG or Spy-Bi-Wire connectors). The programming can be done with a PC or as a stand-alone device. A PC-side graphical user interface is also available and is DLL-based.

10.4 Documentation Support

The following documents describe the MSP430F543xA and MSP430F541xA MCUs. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for example, [MSP430F5438A](http://ti.com)). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

[MSP430F5438A Device Erratasheet](#)

Describes the known exceptions to the functional specifications for all silicon revisions of this device.

[MSP430F5437A Device Erratasheet](#)

Describes the known exceptions to the functional specifications for all silicon revisions of this device.

[MSP430F5436A Device Erratasheet](#)

Describes the known exceptions to the functional specifications for all silicon revisions of this device.

[MSP430F5435A Device Erratasheet](#)

Describes the known exceptions to the functional specifications for all silicon revisions of this device.

[MSP430F5419A Device Erratasheet](#)

Describes the known exceptions to the functional specifications for all silicon revisions of this device.

[MSP430F5418A Device Erratasheet](#)

Describes the known exceptions to the functional specifications for all silicon revisions of this device.

User's Guides

[MSP430F5xx and MSP430F6xx Family User's Guide](#)

Detailed information on the modules and peripherals available in this device family.

[MSP430 Flash Device Bootloader \(BSL\) User's Guide](#)

The MSP430 bootloader (BSL) lets users communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

[MSP430 Programming With the JTAG Interface](#)

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

[MSP430 Hardware Tools User's Guide](#)

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

Application Reports

[MSP430 32-kHz Crystal Oscillators](#)

Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

[MSP430 System-Level ESD Considerations](#)

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three different ESD topics to help board designers and OEMs understand and design robust system-level designs.

10.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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10.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

10.9 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F5418AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5418A | Samples |
| MSP430F5418AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5418A | Samples |
| MSP430F5419AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5419A | Samples |
| MSP430F5419AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5419A | Samples |
| MSP430F5419AIZCAR | ACTIVE | NFBGA | ZCA | 113 | 2500 | RoHS & Green | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5419A | Samples |
| MSP430F5419AIZCAT | ACTIVE | NFBGA | ZCA | 113 | 250 | RoHS & Green | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5419A | Samples |
| MSP430F5435AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5435A | Samples |
| MSP430F5435AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5435A | Samples |
| MSP430F5436AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5436A | Samples |
| MSP430F5436AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5436A | Samples |
| MSP430F5436AIZCAR | ACTIVE | NFBGA | ZCA | 113 | 2500 | RoHS & Green | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5436A | Samples |
| MSP430F5436AIZCAT | ACTIVE | NFBGA | ZCA | 113 | 250 | RoHS & Green | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5436A | Samples |
| MSP430F5437AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5437A | Samples |
| MSP430F5437AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5437A | Samples |
| MSP430F5438AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5438A | Samples |
| MSP430F5438AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430F5438A | Samples |
| MSP430F5438AIZCAR | ACTIVE | NFBGA | ZCA | 113 | 2500 | RoHS & Green | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5438A | Samples |
| MSP430F5438AIZCAT | ACTIVE | NFBGA | ZCA | 113 | 250 | RoHS & Green | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5438A | Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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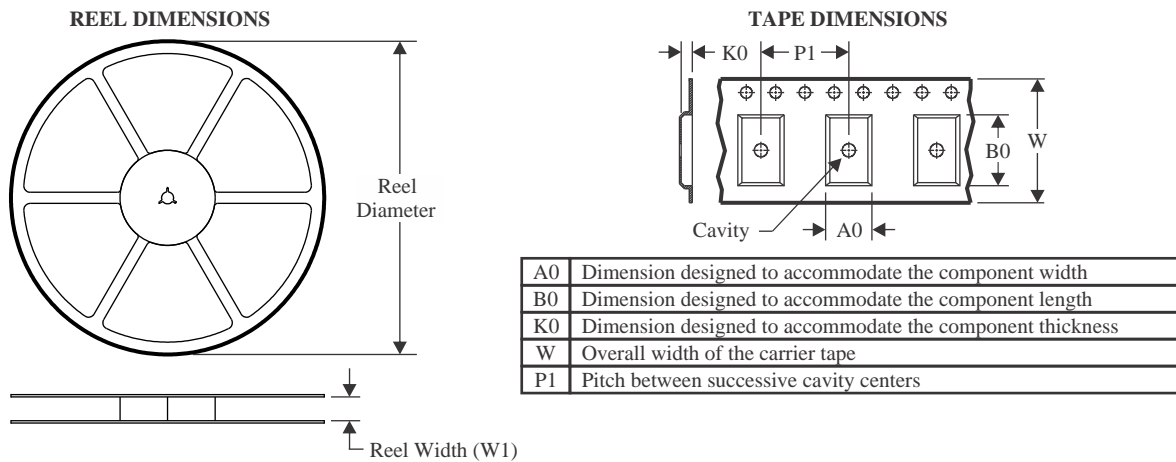
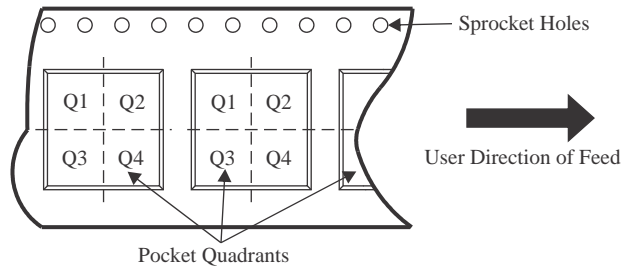
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430F5438A :

- Enhanced Product : [MSP430F5438A-EP](#)

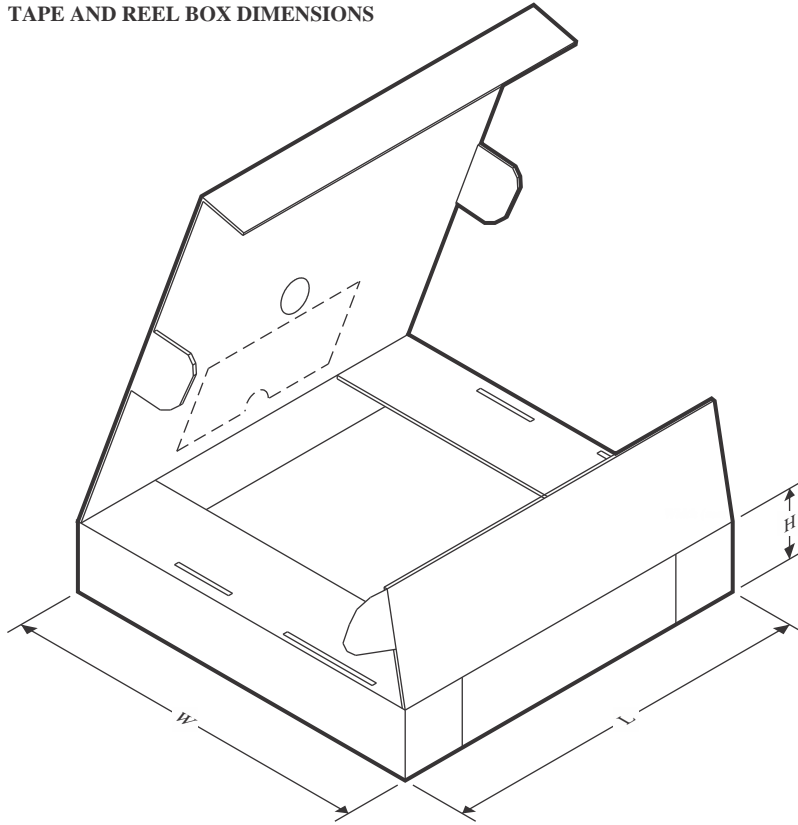
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


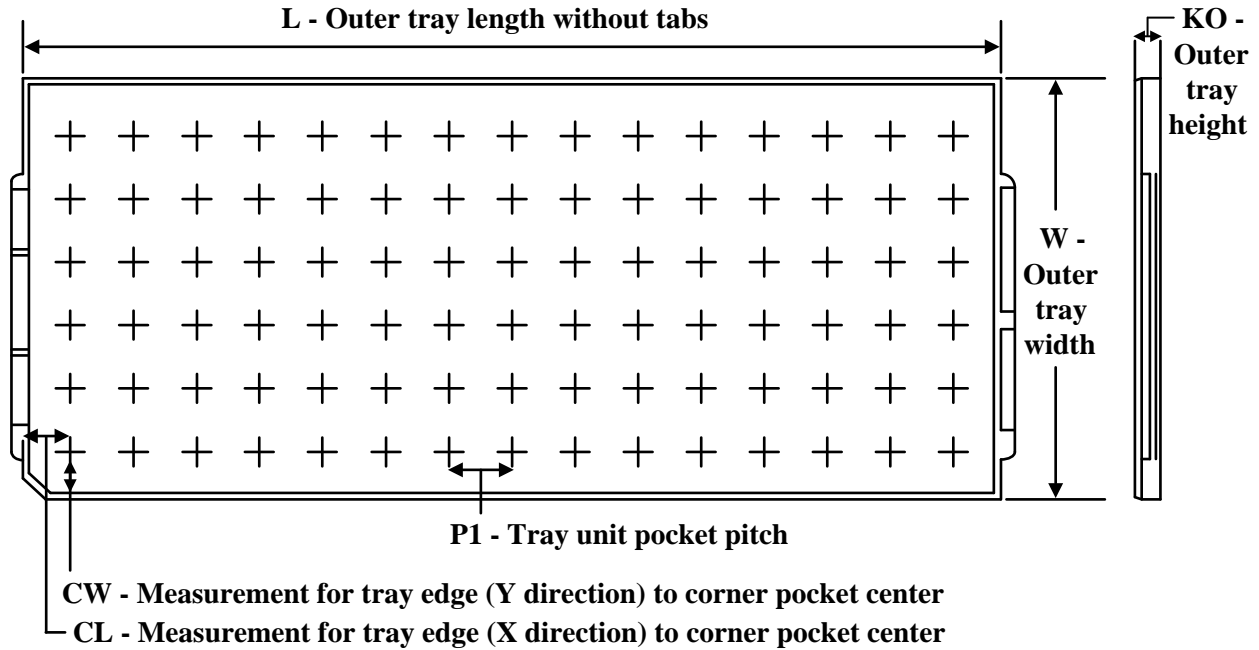
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F5418AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F5419AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F5435AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F5436AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F5437AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F5438AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F5418AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F5419AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F5435AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F5436AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F5437AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F5438AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |

TRAY


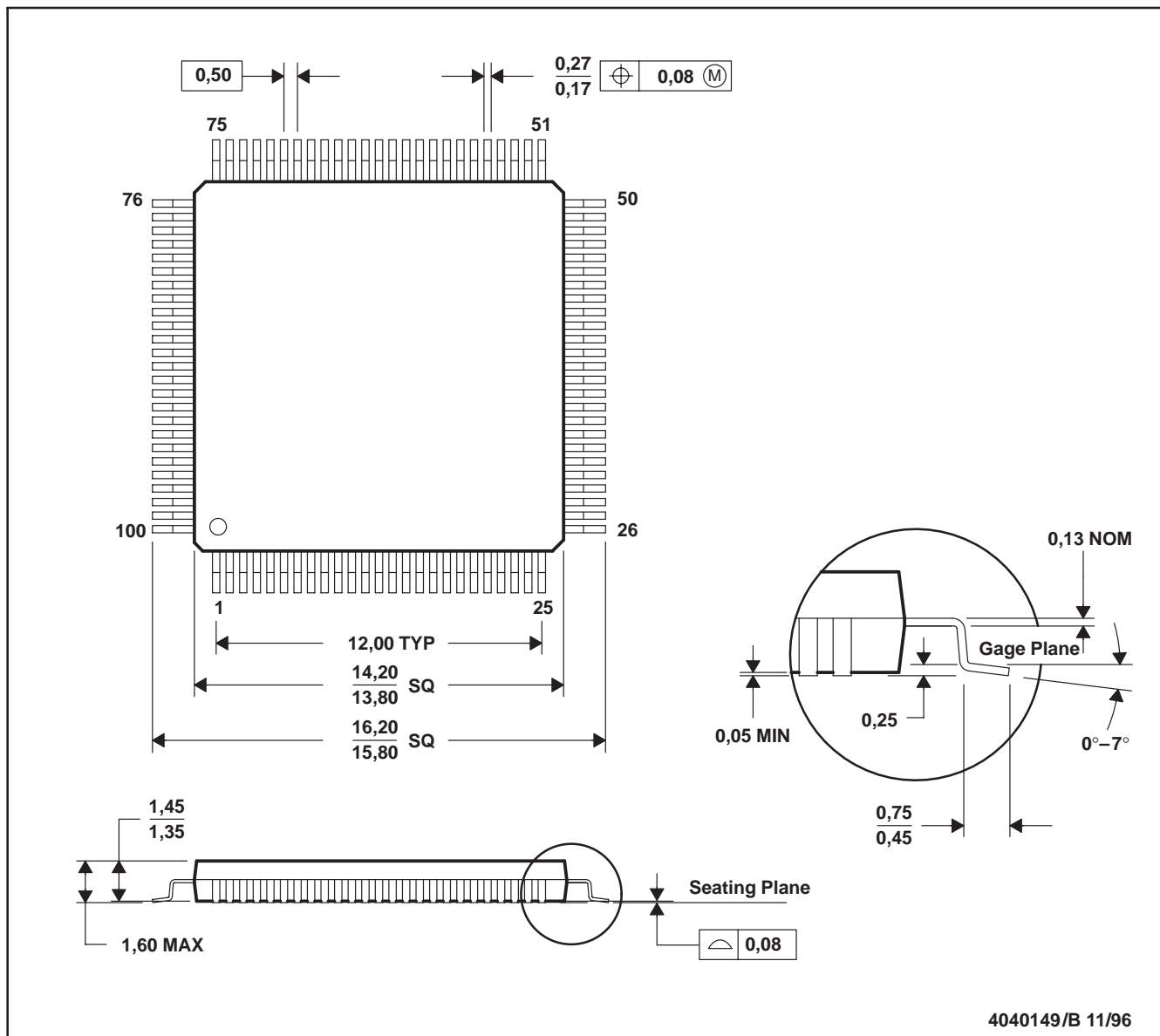
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|-------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| MSP430F5418AIPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F5419AIPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5419AIZCAT | ZCA | NFBGA | 113 | 250 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| MSP430F5435AIPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F5436AIPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5436AIZCAT | ZCA | NFBGA | 113 | 250 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| MSP430F5437AIPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F5438AIPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F5438AIZCAT | ZCA | NFBGA | 113 | 250 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |

PZ (S-PQFP-G100)

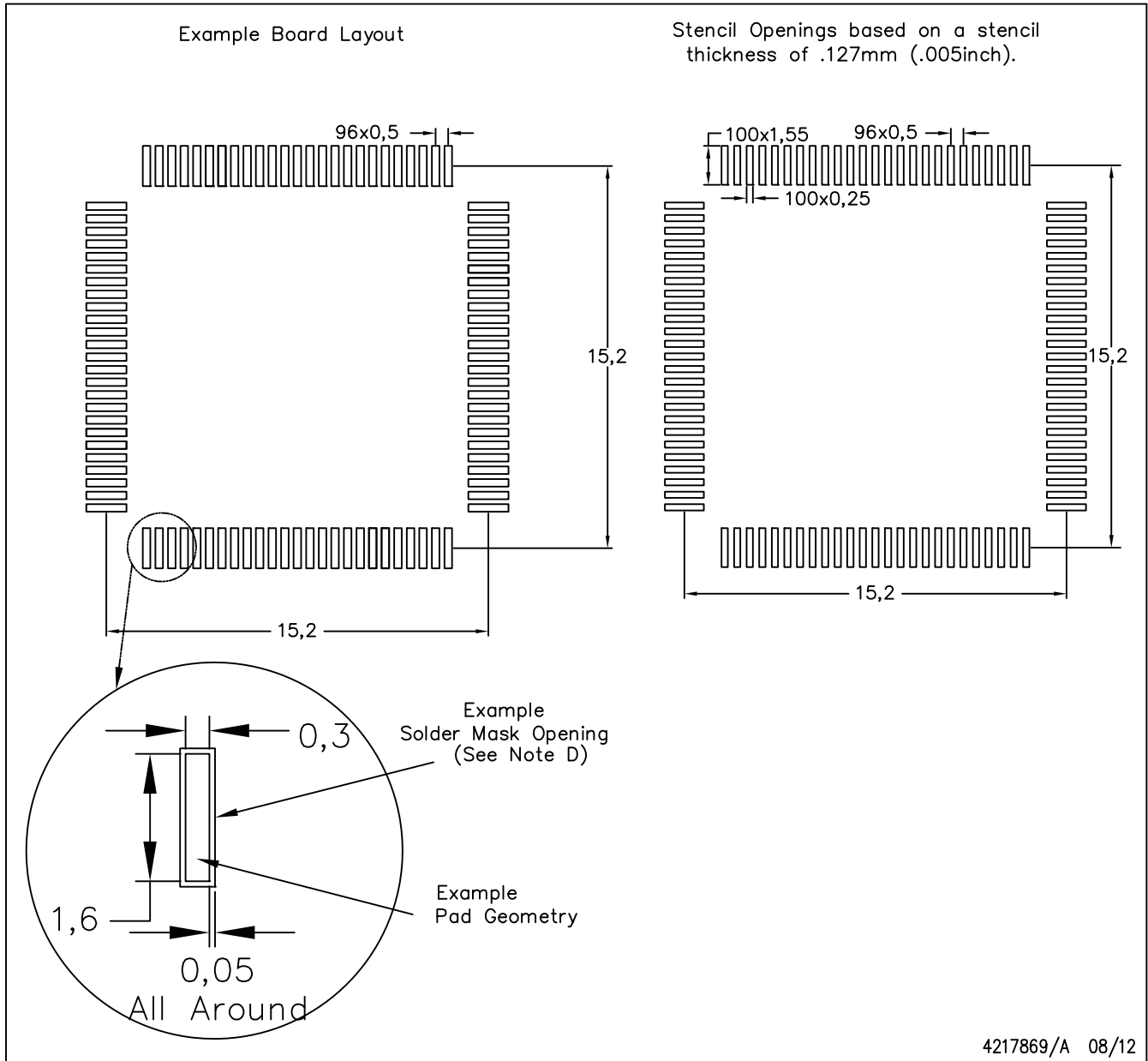
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

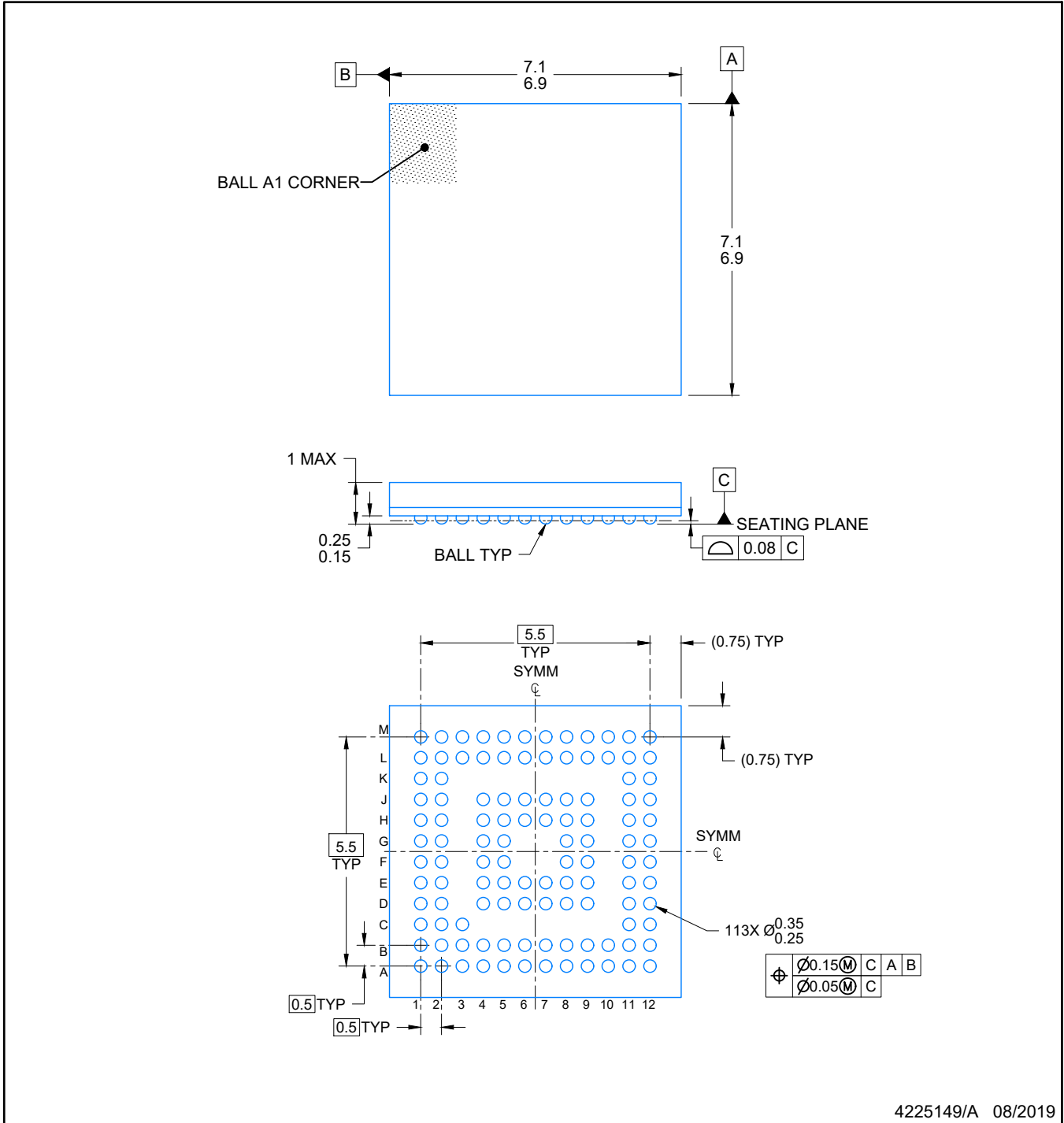
PZ (S-PQFP-G100)

PLASTIC QUAD FLAT PACK



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

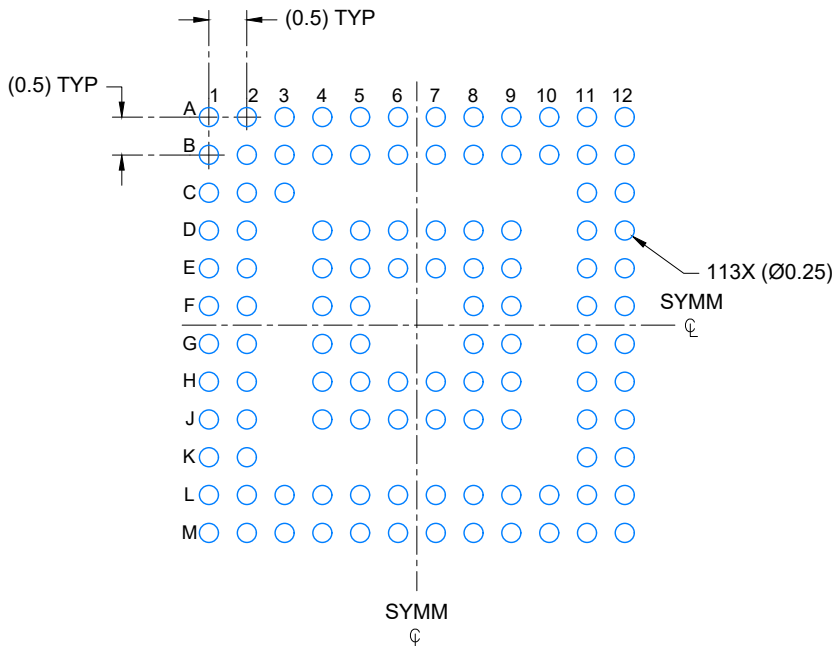


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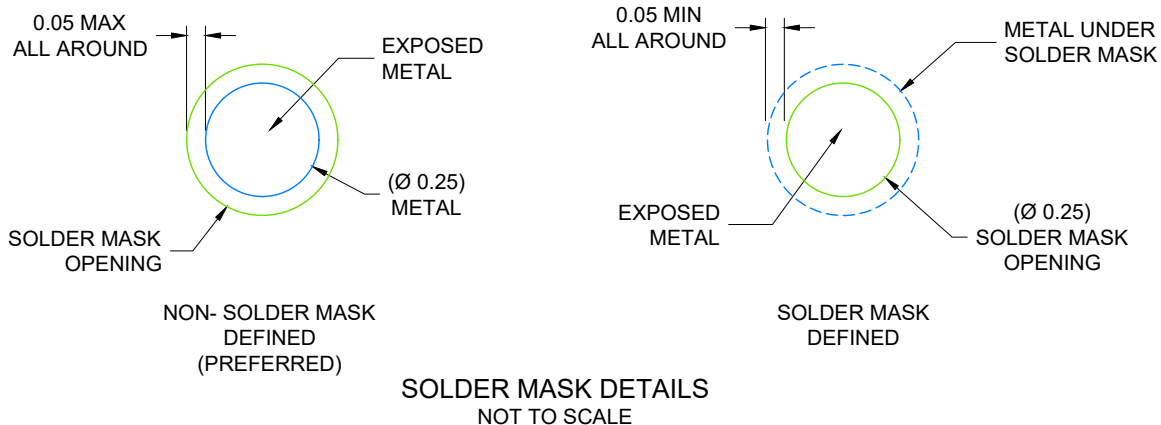
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 10X



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NOTES: (continued)

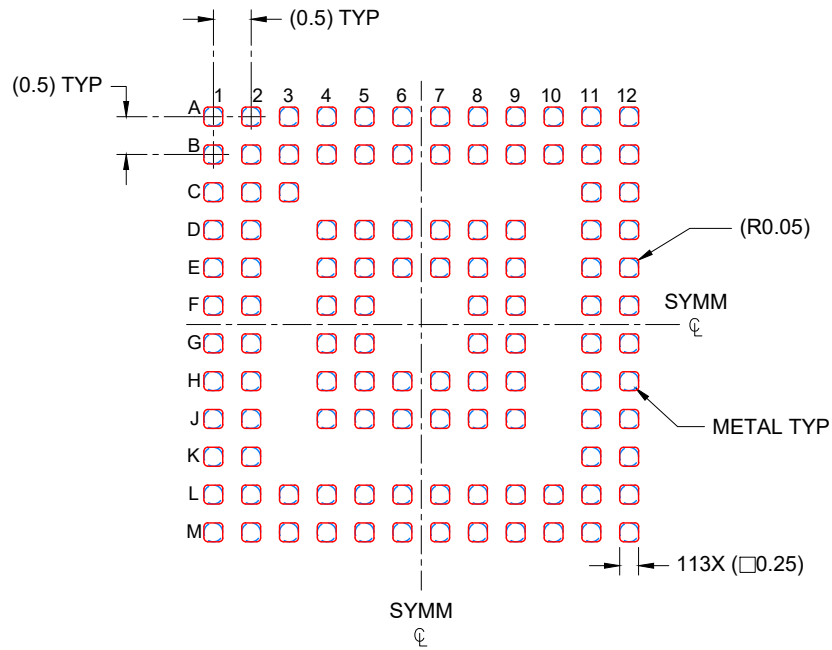
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

ZCA0113A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



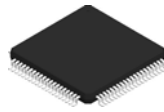
SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 10X

4225149/A 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

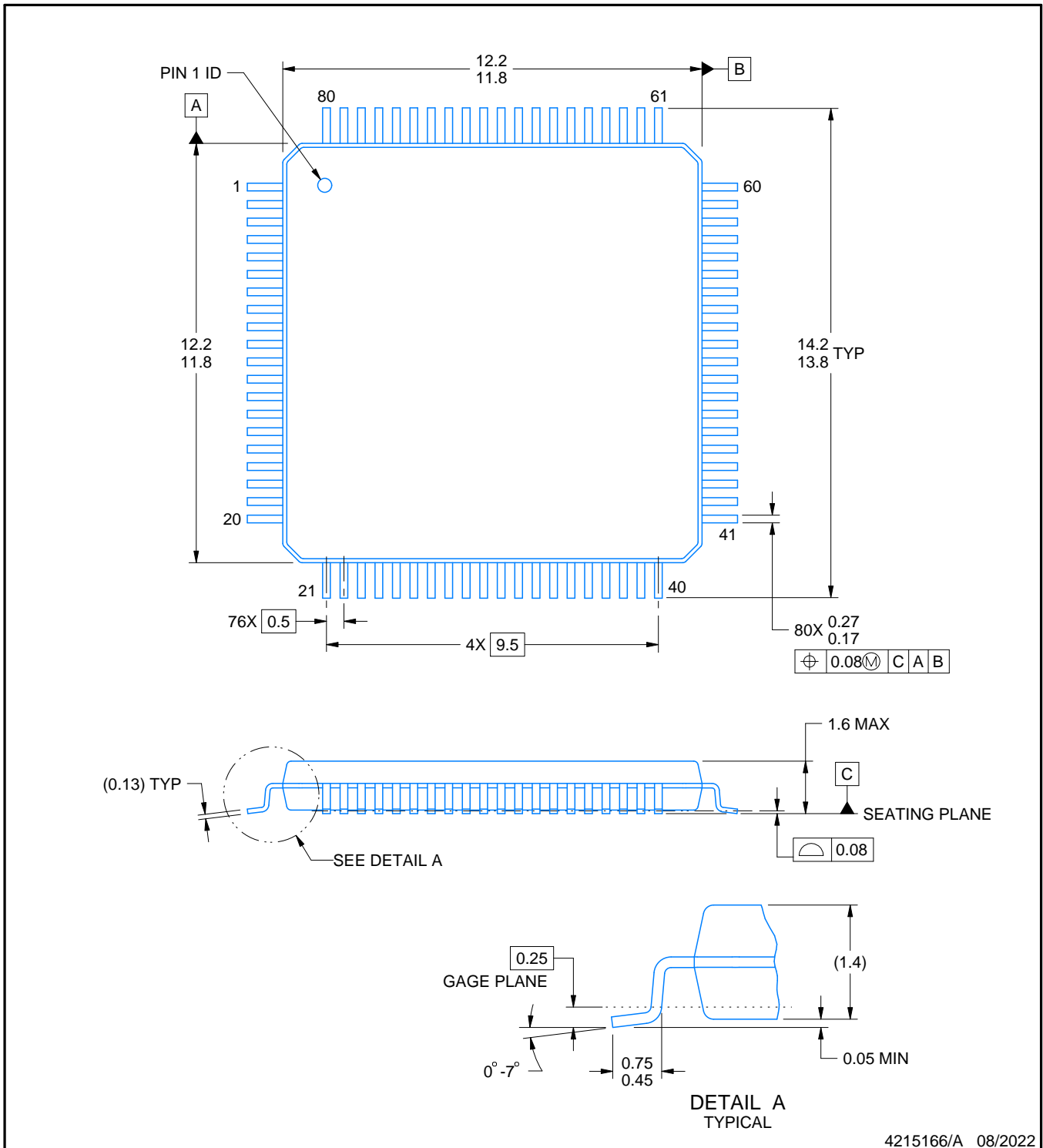
PN0080A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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NOTES:

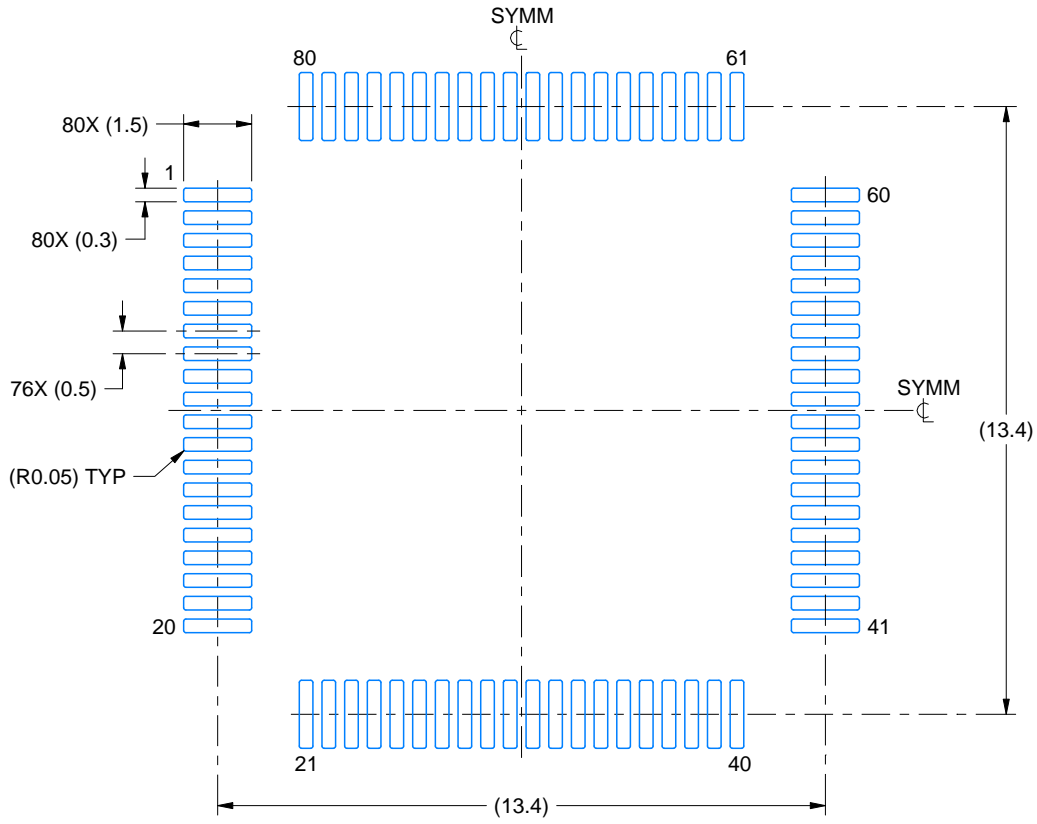
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

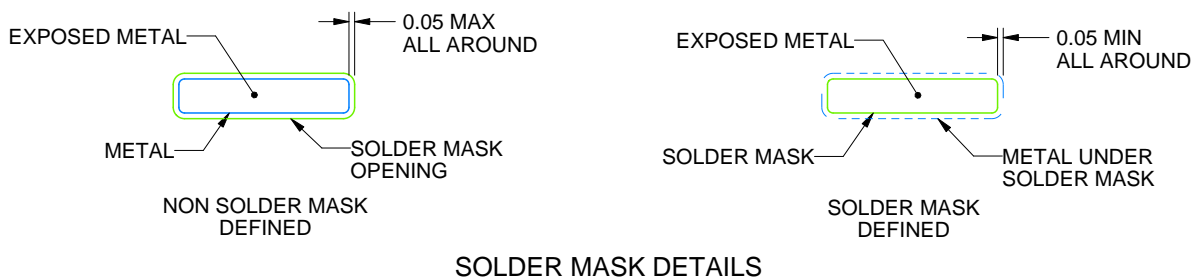
PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



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NOTES: (continued)

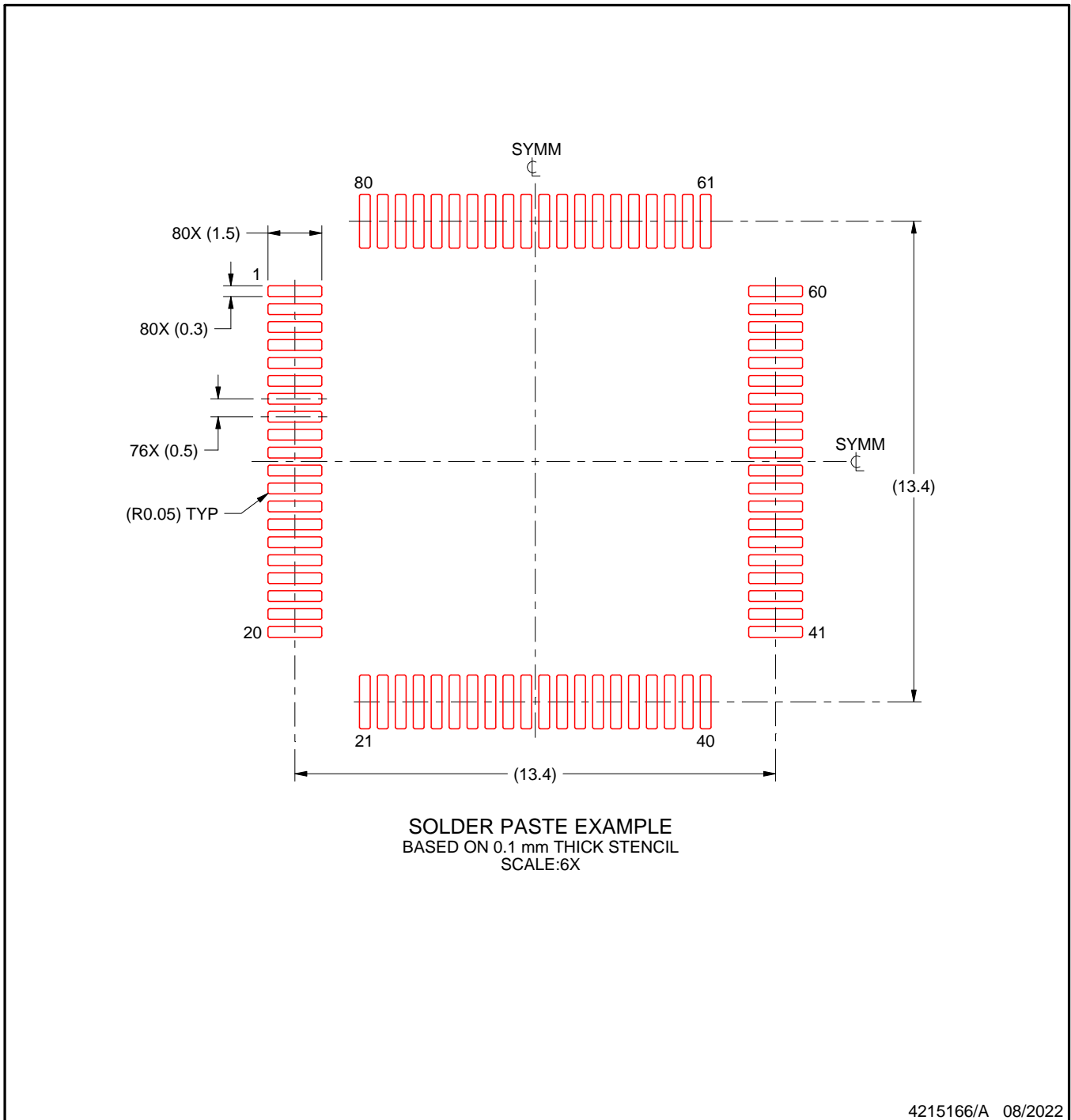
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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