



**THE DATASHEET OF
DS25MB200TSQ/NOPB**



DS25MB200 Dual 2.5 Gbps 2:1/1:2 CML Mux/Buffer with Transmit Pre-Emphasis and Receive Equalization

Check for Samples: [DS25MB200](#)

FEATURES

- 0.6–2.5 Gbps Low Jitter Operation
- Fixed Input Equalization
- Programmable Output Pre-Emphasis
- Independent Switch and Line Side Pre-Emphasis Controls
- Programmable Switch-Side Loopback Modes
- On-Chip Terminations
- HBM ESD Rating 6 kV on All Pins
- +3.3V Supply
- Lead-Less WQFN-48 Package (7mm x 7mm x 0.8mm, 0.5mm Pitch)
- -40°C to +85°C Operating Temperature Range

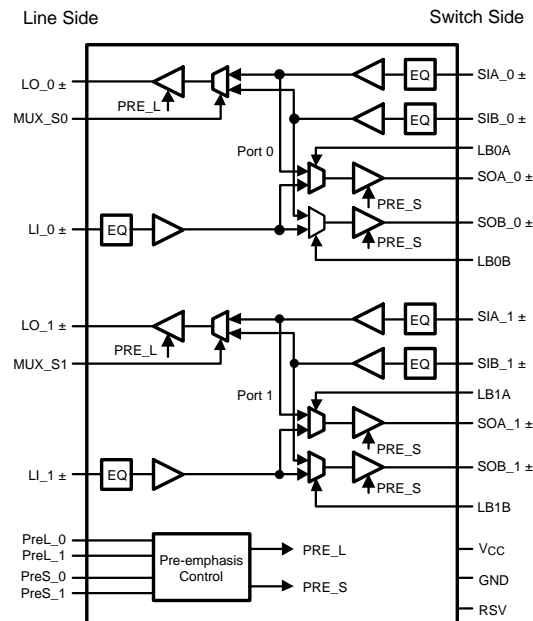
APPLICATIONS

- Backplane or Cable Driver
- Redundancy and Signal Conditioning Applications

DESCRIPTION

The DS25MB200 is a dual signal conditioning 2:1 multiplexer and 1:2 fan-out buffer designed for use in backplane redundancy applications. Signal conditioning features include input equalization and programmable output pre-emphasis that enable data communication in FR4 backplanes up to 2.5 Gbps. Each input stage has a fixed equalizer to reduce ISI distortion from board traces. All output drivers have 4 selectable steps of pre-emphasis to compensate for transmission losses from long FR4 backplanes and reduce deterministic jitter. The pre-emphasis levels can be independently controlled for the line-side and switch-side drivers. The internal loopback paths from switch-side input to switch-side output enable at-speed system testing. All receiver inputs are internally terminated with 100Ω differential terminating resistors. All drivers are internally terminated with 50Ω to V_{CC} .

Functional Block Diagram



All CML inputs and outputs must be AC coupled for optimal performance.



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Connection Diagram

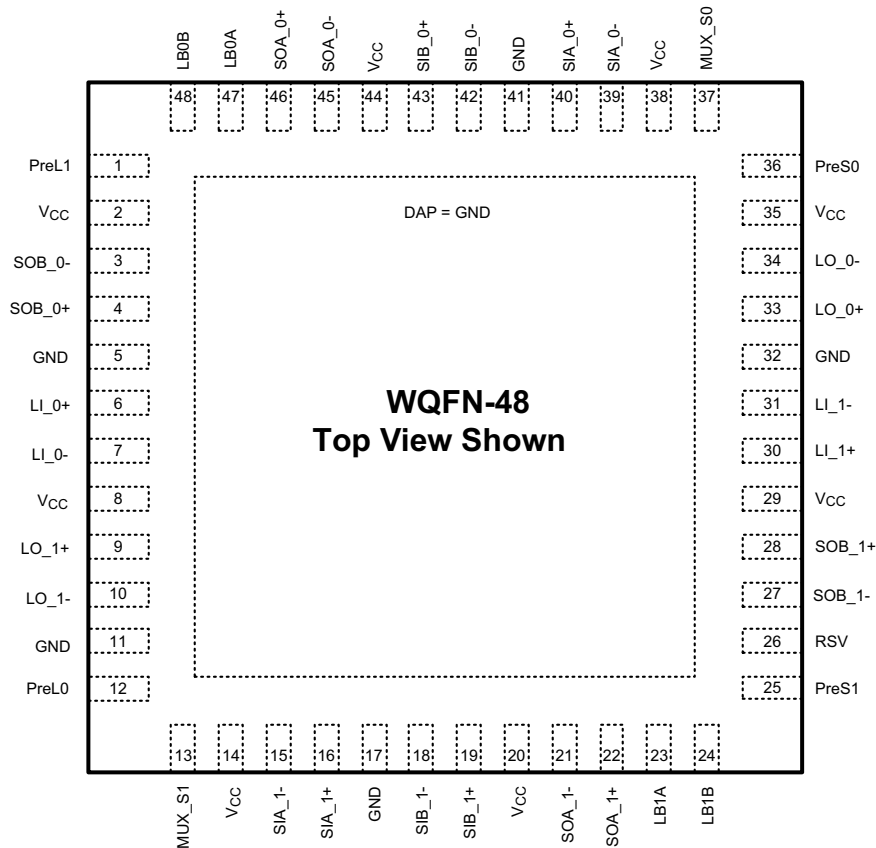


Figure 1. 48 Pin (Top View)
See Package Number NJU0048D

PIN DESCRIPTIONS⁽¹⁾

Pin Name	Pin Number	I/O ⁽²⁾	Description
LINE SIDE HIGH SPEED DIFFERENTIAL IO's			
LI_0+ LI_0-	6 7	I	Inverting and non-inverting differential inputs of port_0 at the line side. LI_0+ and LI_0- have an internal 50Ω connected to an internal reference voltage. See Figure 7 .
LO_0+ LO_0-	33 34	O	Inverting and non-inverting differential outputs of port_0 at the line side. LO_0+ and LO_0- have an internal 50Ω connected to V _{CC} .
LI_1+ LI_1-	30 31	I	Inverting and non-inverting differential inputs of port_1 at the line side. LI_1+ and LI_1- have an internal 50Ω connected to an internal reference voltage. See Figure 7 .
LO_1+ LO_1-	9 10	O	Inverting and non-inverting differential outputs of port_1 at the line side. LO_1+ and LO_1- have an internal 50Ω connected to V _{CC} .
SWITCH SIDE HIGH SPEED DIFFERENTIAL IO's			
SOA_0+ SOA_0-	46 45	O	Inverting and non-inverting differential outputs of mux_0 at the switch_A side. SOA_0+ and SOA_0- have an internal 50Ω connected to V _{CC} .
SOB_0+ SOB_0-	4 3	O	Inverting and non-inverting differential outputs of mux_0 at the switch_B side. SOB_0+ and SOB_0- have an internal 50Ω connected to V _{CC} .
SIA_0+ SIA_0-	40 39	I	Inverting and non-inverting differential inputs to the mux_0 at the switch_A side. SIA_0+ and SIA_0- have an internal 50Ω connected to an internal reference voltage. See Figure 7 .
SIB_0+ SIB_0-	43 42	I	Inverting and non-inverting differential inputs to the mux_0 at the switch_B side. SIB_0+ and SIB_0- have an internal 50Ω connected to an internal reference voltage. See Figure 7 .

(1) All CML Inputs or Outputs must be AC coupled.

(2) I = Input, O = Output, P = Power

PIN DESCRIPTIONS⁽¹⁾ (continued)

Pin Name	Pin Number	I/O ⁽²⁾	Description
SOA_1+ SOA_1-	22 21	O	Inverting and non-inverting differential outputs of mux_1 at the switch_A side. SOA_1+ and SOA_1- have an internal 50Ω connected to V _{CC} .
SOB_1+ SOB_1-	28 27	O	Inverting and non-inverting differential outputs of mux_1 at the switch_B side. SOB_1+ and SOB_1- have an internal 50Ω connected to V _{CC} .
SIA_1+ SIA_1-	16 15	I	Inverting and non-inverting differential inputs to the mux_1 at the switch_A side. SIA_1+ and SIA_1- have an internal 50Ω connected to an internal reference voltage. See Figure 7 .
SIB_1+ SIB_1-	19 18	I	Inverting and non-inverting differential inputs to the mux_1 at the switch_B side. SIB_1+ and SIB_1- have an internal 50Ω connected to an internal reference voltage. See Figure 7 .
CONTROL (3.3V LVC MOS)			
MUX_S0	37	I	A logic low at MUX_S0 selects mux_0 to switch B. MUX_S0 is internally pulled high. Default state for mux_0 is switch A.
MUX_S1	13	I	A logic low at MUX_S1 selects mux_1 to switch B. MUX_S0 is internally pulled high. Default state for mux_1 is switch A.
PREL_0 PREL_1	12 1	I	PREL_0 and PREL_1 select the output pre-emphasis of the line side drivers (LO_0± and LO_1±). PREL_0 and PREL_1 are internally pulled high. See Table 3 for line side pre-emphasis levels.
PRES_0 PRES_1	36 25	I	PRES_0 and PRES_1 select the output pre-emphasis of the switch side drivers (SOA_0±, SOB_0±, SOA_1± and SOB_1±). PRES_0 and PRES_1 are internally pulled high. See Table 4 for switch side pre-emphasis levels.
LB0A	47	I	A logic low at LB0A enables the internal loopback path from SIA_0± to SOA_0±. LB0A is internally pulled high.
LB0B	48	I	A logic low at LB0B enables the internal loopback path from SIB_0± to SOB_0±. LB0B is internally pulled high.
LB1A	23	I	A logic low at LB1A enables the internal loopback path from SIA_1± to SOA_1±. LB1A is internally pulled high.
LB1B	24	I	A logic low at LB1B enables the internal loopback path from SIB_1± to SOB_1±. LB1B is internally pulled high.
RSV	26	I	Reserve pin to support factory testing. This pin can be left open, or tied to GND, or tied to GND through an external pull-down resistor.
POWER			
V _{CC}	2, 8, 14, 20, 29, 35, 38, 44	P	V _{CC} = 3.3V ± 5%. Each V _{CC} pin should be connected to the V _{CC} plane through a low inductance path, typically with a via located as close as possible to the landing pad of the V _{CC} pin. It is recommended to have a 0.01 μF or 0.1 μF, X7R, size-0402 bypass capacitor from each V _{CC} pin to ground plane.
GND	5, 11, 17, 32, 41	P	Ground reference. Each ground pin should be connected to the ground plane through a low inductance path, typically with a via located as close as possible to the landing pad of the GND pin.
GND	DAP	P	Die Attach Pad (DAP) is the metal contact at the bottom side, located at the center of the WQFN-48 package. It should be connected to the GND plane with at least 4 via to lower the ground impedance and improve the thermal performance of the package.

Functional Description

The DS25MB200 is a signal conditioning 2:1 multiplexer and a 1:2 buffer designed to support port redundancy up to 2.5 Gbps. The high speed inputs are self-biased to about 1.3V and are designed for AC coupling. See [Figure 7](#) for details. The inputs are compatible to most AC coupling differential signals such as LVDS, LVPECL and CML. The DS25MB200 is not designed to operate with data rates below 250 Mbps or with a DC bias applied to the CML inputs or outputs. Most high speed links are encoded for DC balance and have been defined to include AC coupling capacitors allowing the DS25MB200 to be directly inserted into the datapath without any limitation. The ideal AC coupling capacitor value is often based on the lowest frequency component embedded within the serial link. A typical AC coupling capacitor value ranges between 100 and 1000nF. Some specifications with scrambled data may require a larger capacitor for optimal performance. To reduce unwanted parasitics around and within the AC coupling capacitor, a body size of 0402 is recommended. [Figure 6](#) shows the AC coupling capacitor placement in an AC test circuit.

Each input stage has a fixed equalizer that provides equalization to compensate about 5 dB of transmission loss from a short backplane trace (about 10 inches backplane). The output driver has Pre-emphasis (driver-side equalization) to compensate the transmission loss of the backplane that it is driving. The driver conditions the output signal such that the lower frequency and higher frequency pulses reach approximately the same amplitude at the end of the backplane, and minimize the deterministic jitter caused by the amplitude disparity. The DS25MB200 provides four steps of user-selectable Pre-emphasis ranging from 0, -3, -6 and -9 dB to handle different lengths of backplane. [Figure 2](#) shows a driver Pre-emphasis waveform. The Pre-emphasis duration is 188ps nominal, corresponds to 0.47 bit-width at 2.5 Gbps. The Pre-emphasis levels of switch-side and line-side can be individually programmed.

Table 1. LOGIC TABLE FOR MULTIPLEX CONTROLS

MUX_S0	Mux Function
0	MUX_0 select switch_B input, SIB_0±.
1 (default)	MUX_0 select switch_A input, SIA_0±.
MUX_S1	Mux Function
0	MUX_1 select switch_B input, SIB_1±.
1 (default)	MUX_1 select switch_A input, SIA_0±.

Table 2. LOGIC TABLE FOR LOOPBACK CONTROLS

LB0A	Loopback Function
0	Enable loopback from SIA_0± to SOA_0±.
1 (default)	Normal mode. Loopback disabled.
LB0B	Loopback Function
0	Enable loopback from SIB_0± to SOB_0±.
1 (default)	Normal mode. Loopback disabled.
LB1A	Loopback Function
0	Enable loopback from SIA_1± to SOA_1±.
1 (default)	Normal mode. Loopback disabled.
LB1B	Loopback Function
0	Enable loopback from SIB_1± to SOB_1±.
1 (default)	Normal mode. Loopback disabled.

Table 3. LINE-SIDE PRE-EMPHASIS CONTROLS

PreL_[1:0]	Pre-Emphasis Level in mV_{PP} (VODB)	De-Emphasis Level in mV_{PP} (VODPE)	Pre-Emphasis in dB (VODPE/VODB)	Typical FR4 board trace
0 0	1200	1200	0	10 inches
0 1	1200	849.53	-3	20 inches
1 0	1200	600	-6	30 inches
1 1 (default)	1200	425.78	-9	40 inches

Table 4. SWITCH-SIDE PRE-EMPHASIS CONTROLS

PreS_[1:0]	Pre-Emphasis Level in mV_{PP} (VODB)	De-Emphasis Level in mV_{PP} (VODPE)	Pre-Emphasis in dB (VODPE/VODB)	Typical FR4 board trace
0 0	1200	1200	0	10 inches
0 1	1200	849.53	-3	20 inches
1 0	1200	600	-6	30 inches
1 1 (default)	1200	425.78	-9	40 inches

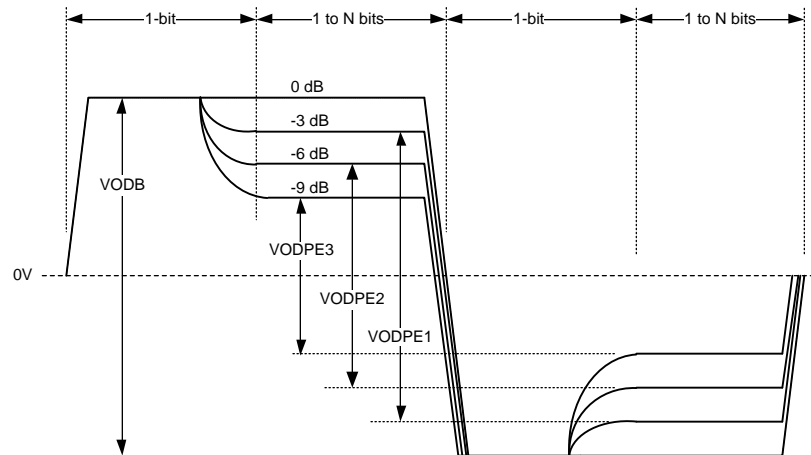


Figure 2. Driver Pre-Emphasis Differential Waveform (showing all 4 pre-emphasis steps)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})		-0.3V to 4V
CMOS/TTL Input Voltage		-0.3V to ($V_{CC} + 0.3V$)
CML Input/Output Voltage		-0.3V to ($V_{CC} + 0.3V$)
Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
Lead Temperature	Soldering, 4 sec	+260°C
Thermal Resistance, θ_{JA}		33.7°C/W
Thermal Resistance, θ_{JC-top}		20.7°C/W
Thermal Resistance, $\theta_{JC-bottom}$		5.8°C/W
Thermal Resistance, Φ_{JB}		18.2°C/W
ESD Rating HBM, 1.5 k Ω , 100 pF		6 kV

- (1) Absolute Maximum Ratings are the ratings beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits.
 (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Recommended Operating Ratings

	Min	Typ	Max	Units
Supply Voltage (V_{CC-GND})	3.135	3.3	3.465	V
Supply Noise Amplitude (10 Hz to 2 GHz)			50	mV _{PP}
Ambient Temperature	-40		85	°C
Case Temperature			100	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter		Test Conditions	Min	Typ ⁽¹⁾	Max	Units
LVC MOS DC SPECIFICATIONS						
V _{IH}	High Level Input Voltage		2.0		V _{CC} + 0.3	V
V _{IL}	Low Level Input Voltage		-0.3		0.8	V
I _{IH}	High Level Input Current	V _{IN} = V _{CC}	-10		10	μA
I _{IL}	Low Level Input Current	V _{IN} = GND	75	94	124	μA
R _{PU}	Pull-High Resistance			35		kΩ
RECEIVER SPECIFICATIONS						
V _{ID}	Differential Input Voltage Range	AC Coupled Differential Signal Below 1.25 Gbps Above 1.25 Gbps Measured at input pins.	100 100		1750 1560	mV _{P-P} mV _{P-P}
V _{ICM}	Common Mode Voltage at Receiver Inputs	Measured at receiver inputs reference to ground.		1.5		V
R _{ITD}	Input Differential Termination	On-chip differential termination between IN+ or IN-.	84	100	116	Ω
DRIVER SPECIFICATIONS						
V _{ODB}	Output Differential Voltage Swing without Pre-Emphasis	R _L = 100Ω ±1% PRES_1=PRE_0=0 PREL_1=PREL_0=0 Driver pre-emphasis disabled. Running K28.7 pattern at 2.5 Gbps. See Figure 6 for test circuit.	1000	1200	1400	mV _{P-P}
V _{PE}	Output Pre-Emphasis Voltage Ratio 20*log(VODPE/VODB)	R _L = 100Ω ±1% Running K28.7 pattern at 2.5 Gbps PREx_[1:0]=0 PREx_[1:0]=01 PREx_[1:0]=10 PREx_[1:0]=11 x=S for switch side pre-emphasis control x=L for line side pre-emphasis control See Figure 2 on waveform. See Figure 6 for test circuit.		0 -3 -6 -9		dB dB dB dB
t _{PE}	Pre-Emphasis Width	Tested at -9 dB pre-emphasis level, PREx[1:0]=11 x=S for switch side pre-emphasis control x=L for line side pre-emphasis control See Figure 5 on measurement condition.	125	188	400	ps
R _{OTSE}	Output Termination	On-chip termination from OUT+ or OUT- to V _{CC}	42	50	58	Ω
R _{OTD}	Output Differential Termination	On-chip differential termination between OUT+ and OUT-		100		Ω
ΔR _{OTSE}	Mis-Match in Output Termination Resistors	Mis-match in output terminations at OUT+ and OUT-			5	%
V _{OCM}	Output Common Mode Voltage		2.4		2.9	V
POWER DISSIPATION						
P _D	Power Dissipation	V _{DD} = 3.465V All outputs terminated by 100Ω ±1%. PREL_[1:0]=0, PRES_[1:0]=0 Running PRBS 2 ⁷ -1 pattern at 2.5 Gbps			1	W

(1) Typical parameters measured at V_{CC} = 3.3V, T_A = 25°C. They are for reference purposes and are not production-tested.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter		Test Conditions	Min	Typ ⁽¹⁾	Max	Units
AC CHARACTERISTICS						
t _R	Differential Low to High Transition Time	Measured with a clock-like pattern at 100 MHz, between 20% and 80% of the differential output voltage. Pre-emphasis disabled. Transition time is measured with fixture as shown in Figure 6, adjusted to reflect the transition time at the output pins.		80		ps
t _F	Differential High to Low Transition Time			80		ps
t _{PLH}	Differential Low to High Propagation Delay	Measured at 50% differential voltage from input to output.		0.5	2	ns
t _{PHL}	Differential High to Low Propagation Delay			0.5	2	ns
t _{SKP}	Pulse Skew	t _{PHL} - t _{PLH}			20	ps
t _{SKO}	Output Skew ⁽²⁾	Difference in propagation delay between two outputs in the same device.			200	ps
t _{SKPP}	Part-to-Part Skew	Difference in propagation delay between the same output from devices operating under identical conditions.			500	ps
t _{SM}	Mux Switch Time	Measured from V _{IH} or V _{IL} of the mux-control or loopback control to 50% of the valid differential output.		1.8	6	ns
RJ	Device Random Jitter ⁽³⁾	See Figure 6 for test circuit. Alternating-1-0 pattern. Pre-emphasis disabled. At 1.25 Gbps At 2.5 Gbps			2 2	psrms psrms
DJ	Device Deterministic Jitter ⁽⁴⁾	See Figure 6 for test circuit. Pre-emphasis disabled. Between 0.8 and 2.5 Gbps with PRBS7 pattern for DS25MB200 @ -40°C to 85°C			30	pspp
DR _{MAX}	Maximum Data Rate	Tested with alternating 1-0 pattern ⁽⁵⁾	2.5			Gbps
DR _{MIN}	Minimum Data Rate				0.6	Gbps

- (2) t_{SKO} is the magnitude difference in the propagation delays among data paths between switch A and switch B of the same port and similar data paths between port 0 and port 1. An example is the output skew among data paths from SIA_0± to LO_0±, SIB_0± to LO_0±, SIA_1± to LO_1± and SIB_1± to LO_1±. Another example is the output skew among data paths from LI_0± to SOA_0±, LI_0± to SOB_0±, LI_1± to SOA_1± and LI_1± to SOB_1±. t_{SKO} also refers to the delay skew of the loopback paths of the same port and between similar data paths between port 0 and port 1. An example is the output skew among data paths SIA_0± to SOA_0±, SIB_0± to SOB_0±, SIA_1± to SOA_1± and SIB_1± to SOB_1±.
- (3) Device output random jitter is a measurement of the random jitter contribution from the device. It is derived by the equation $\sqrt{RJ_{OUT}^2 - RJ_{IN}^2}$, where RJ_{OUT} is the random jitter measured at the output of the device in psrms, RJ_{IN} is the random jitter of the pattern generator driving the device.
- (4) Device output deterministic jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation (DJ_{OUT} - DJ_{IN}), where DJ_{OUT} is the peak-to-peak deterministic jitter measured at the output of the device in pspp, DJ_{IN} is the peak-to-peak deterministic jitter of the pattern generator driving the device.
- (5) For operation under 1 Gbps, encoded data transmission is recommended (i.e. 8b10b).

Timing Diagrams

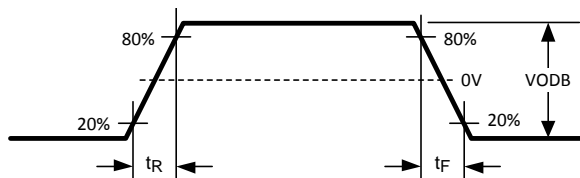


Figure 3. Driver Output Transition Time

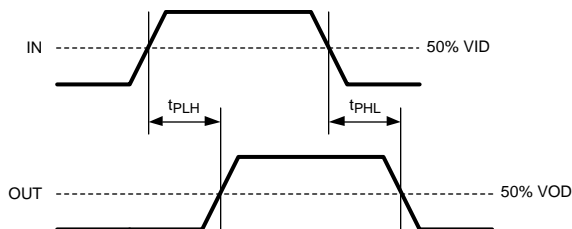


Figure 4. Propagation Delay from Input to Output

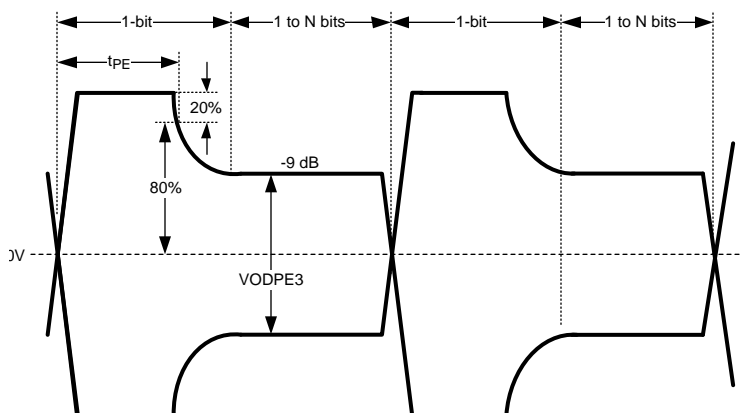


Figure 5. Test Condition for Output Pre-Emphasis Duration

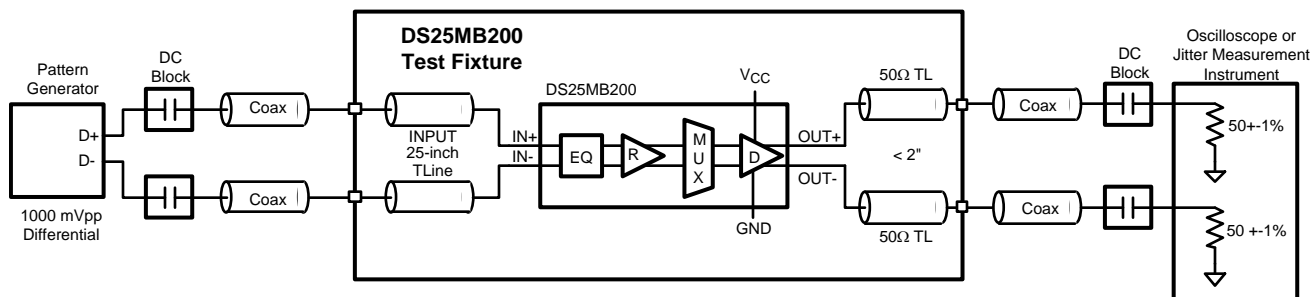


Figure 6. AC Test Circuit

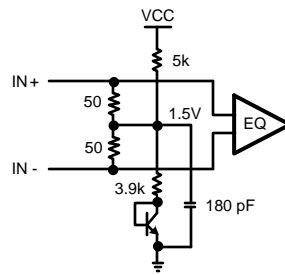


Figure 7. Receiver Input Termination and Biasing Circuit

APPLICATION INFORMATION

The DS25MB200 input equalizer provides equalization to compensate about 5 dB of transmission loss from a short backplane transmission line. For characterization purposes, a 25-inch FR4 coupled micro-strip board trace is used in place of the short backplane link. The 25-inch microstrip board trace has approximately 5 dB of attenuation between 375 MHz and 1.875 GHz, representing closely the transmission loss of the short backplane transmission line. The 25-inch microstrip is connected between the pattern generator and the differential inputs of the DS25MB200 for AC measurements.

Trace Length	Finished Trace Width W	Separation between Traces	Dielectric Height H	Dielectric Constant ϵ_R	Loss Tangent
25 inches	8.5 mil	11.5 mil	6 mil	3.8	0.022

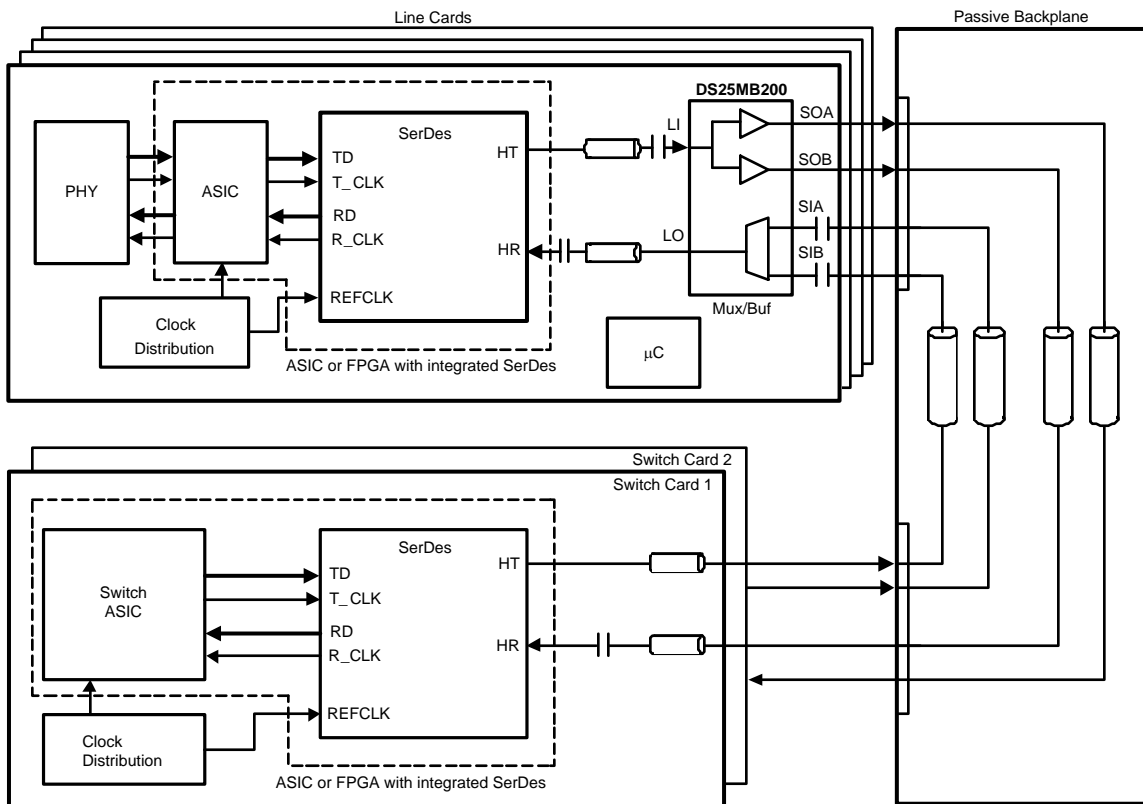


Figure 8. Application Diagram (showing data paths of port 0)

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS25MB200TSQ/NOPB	ACTIVE	WQFN	NJU	48	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	25MB200	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25MB200TSQ/NOPB	WQFN	NJU	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

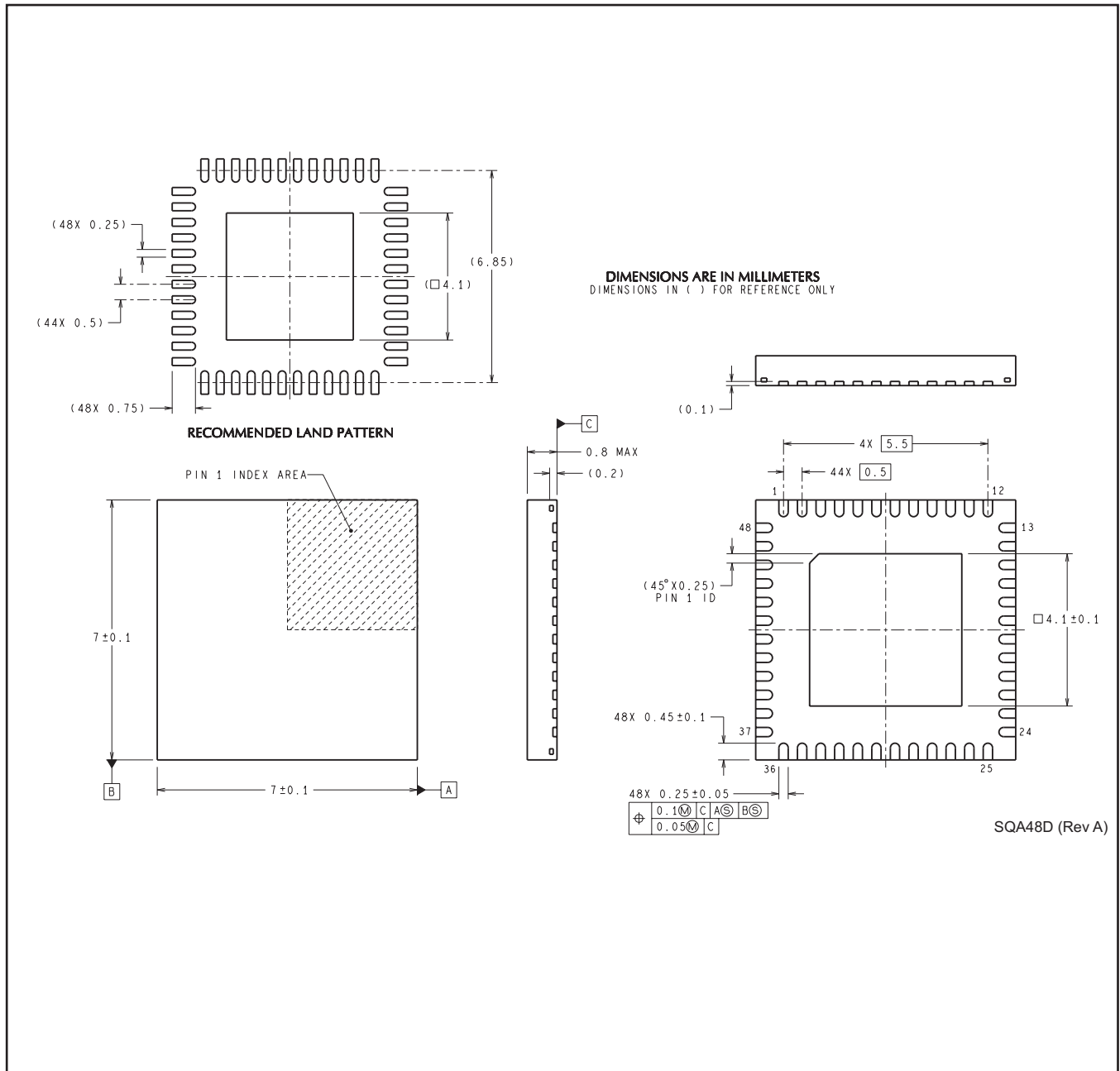
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25MB200TSQ/NOPB	WQFN	NJU	48	250	210.0	185.0	35.0

NJU0048D



SQA48D (Rev A)

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