THE DATASHEET OF

DS1647P-120+

www.win-source.net 0086-755-83957316

19-5596; Rev 10/10

DS1647/DS1647P
Nonvolatile Timekeeping RAM

www.maxim-ic.com

FEATURES

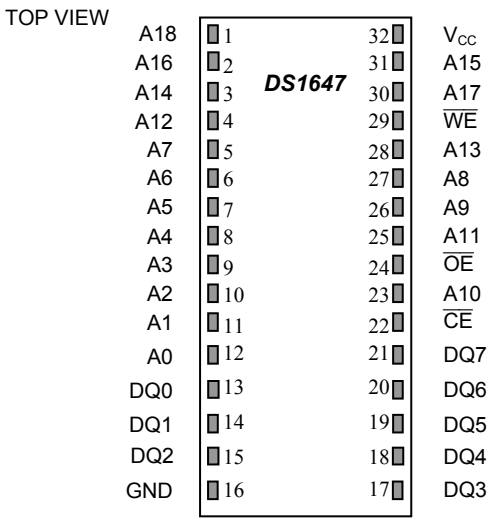
- Integrates NV SRAM, Real-Time Clock, Crystal, Power-Fail Control Circuit, and Lithium Energy Source
- Clock Registers Are Accessed Identically to the Static RAM. These Registers are Resident in the Eight Top RAM Locations.
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- BCD Coded Year, Month, Date, Day, Hours, Minutes, and Seconds with Leap Year Compensation Valid Through 2099
- Power-Fail Write Protection Allows for ±10% V_{CC} Power-Supply Tolerance
- DS1647 Only (DIP Module):
  Standard JEDEC Byte-Wide 128k x 8 RAM Pinout
- DS1647P Only (PowerCap Module Board):
  Surface Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal
  Replaceable Battery (PowerCap)
  Power-Fail Output
  Pin-for-Pin Compatible with Other Densities of DS164XP Timekeeping RAM

ORDERING INFORMATION

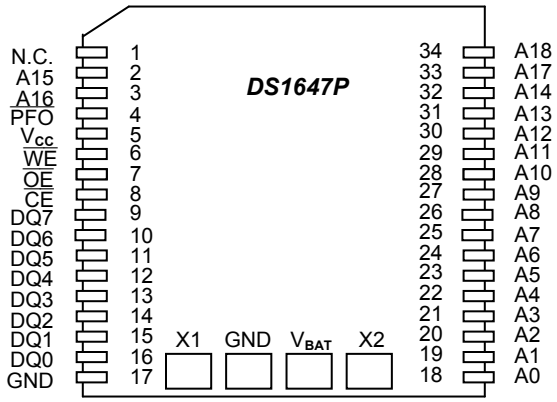
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK**
DS1647-120+	0°C to +70°C	32 EDIP (0.740a)	DS1647+120
DS1647P-120+	0°C to +70°C	34 PowerCap*	DS1647P+120

+Denotes a lead(Pb)-free/RoHS-compliant package.
**DS9034PCX+ or DS9034I-PCX+ required (must be ordered separately).*
***A "+" indicates lead(Pb)-free. The top mark includes a "+" symbol on lead(Pb)-free devices.*

PIN CONFIGURATIONS



32-Pin Encapsulated DIP Package
(32 Pin 740)



34-Pin PowerCap Module Board
(Uses DS9034PCX+ or DS9034I-PCX+ PowerCap)

PIN DESCRIPTION

PIN		NAME	FUNCTION
PDIP	PowerCap		
1	34	A18	Address Input
2	3	A16	
3	32	A14	
4	30	A12	
5	25	A7	
6	24	A6	
7	23	A5	
8	22	A4	
9	21	A3	
10	20	A2	
11	19	A1	
12	18	A0	
23	28	A10	
25	29	A11	
26	27	A9	
27	26	A8	
28	31	A13	
30	33	A17	
31	2	A15	
13	16	DQ0	Data Input/Output
14	15	DQ1	
15	14	DQ2	
17	13	DQ3	Data Input/Output
18	12	DQ4	
19	11	DQ5	
20	10	DQ6	
21	9	DQ7	
16	17	GND	Ground
22	8	$\overline{CE}$	Active-Low Chip Enable
24	7	$\overline{OE}$	Active-Low Output Enable
29	6	$\overline{WE}$	Active-Low Write Enable
32	5	V_{CC}	Power-Supply Input
—	4	$\overline{PFO}$	Active-Low Power-Fail Output, Open Drain. This pin requires a pullup resistor for proper operation.
—	1	N.C.	No Connection
—		X1, X2, V_{BAT}	Crystal Connections and Battery Connection

DESCRIPTION

The DS1647 is a 512k x 8 nonvolatile static RAM with a full-function real-time clock, which are both accessible in a byte-wide format. The nonvolatile timekeeping RAM is functionally equivalent to any JEDEC standard 512k x 8 SRAM. The device can also be easily substituted for ROM, EPROM and EEPROM, providing read/write nonvolatility and the addition of the real-time clock function. The real-time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1647 also contains its own power-fail circuitry, which deselects the device when the V_{CC} supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

PACKAGES

The DS1647 is available in two packages: 32-pin DIP and 34-pin PowerCap module. The 32-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1647P after the completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers. The part number for the PowerCap is DS9034PCX.

CLOCK OPERATIONS—READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1647 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the 7th most significant bit in the control register. As long as 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was present at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that clock accuracy is not affected by the access of data. All of the DS1647 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to 0.

The read bit must be a zero for a minimum of 500µs to ensure that the external registers are updated.

Figure 1. Block Diagram

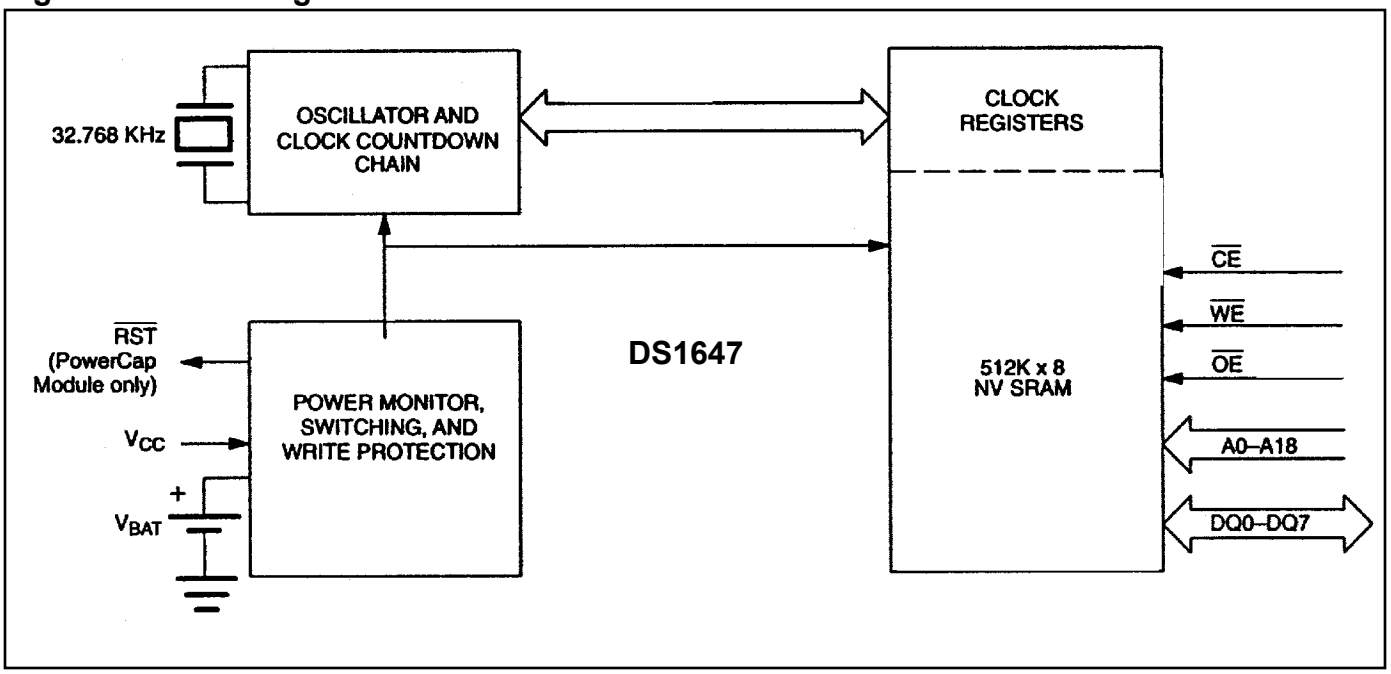


Table 1. Truth Table

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5V ±10%	V_{IH}	X	X	Deselect	High-Z	Standby
	X	X	X	Deselect	High-Z	Standby
	V_{IL}	X	V_{IL}	Write	Data In	Active
	V_{IL}	V_{IL}	V_{IH}	Read	Data Out	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z	Active
$<4.5V > V_{BAT}$	X	X	X	Deselect	High-Z	CMOS Standby
$<V_{BAT}$	X	X	X	Deselect	High-Z	Data-Retention Mode

SETTING THE CLOCK

The MSB Bit, B7, of the control register is the write bit. Setting the write bit to a 1, like the read bit halts updates to the DS1647 registers. The user can then load them with the correct day, date and time data in 24-hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the second's registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the second's register will toggle at 512Hz. When the seconds register is being read, the DQ0 line will toggle at the 512Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, and address for seconds register remain valid and stable).

CLOCK ACCURACY (DIP MODULE)

The DS1647 is guaranteed to keep time accuracy to within ±1 minute per month at +25°C. The RTC is calibrated at the factory by Dallas Semiconductor using nonvolatile tuning elements, and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. Clock accuracy is also affected by the electrical environment and caution should be taken to place the RTC in the lowest-level EMI section of the PC board layout. For additional information, refer to *Application Note 58*.

CLOCK ACCURACY (POWERCAP MODULE)

The DS1647 and DS9034PCX are each individually tested for accuracy. Once mounted together, the module will typically keep time accuracy to within ±1.53 minutes per month (35ppm) at +25°C. Clock accuracy is also affected by the electrical environment and caution should be taken to place the RTC in the lowest-level EMI section of the PC board layout. For additional information, refer to *Application Note 58*.

Table 2. Register Map—BANK1

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
7FFFF	—	—	—	—	—	—	—	—	Year	00–99
7FFFE	X	X	X	—	—	—	—	—	Month	01–12
7FFFD	X	X	—	—	—	—	—	—	Date	01–31
7FFFC	X	FT	X	X	X	—	—	—	Day	01–07
7FFFB	X	X	—	—	—	—	—	—	Hour	00–23
7FFFA	X	—	—	—	—	—	—	—	Minutes	00–59
7FFF9	$\overline{OSC}$	—	—	—	—	—	—	—	Seconds	00–59
7FFF8	W	R	X	X	X	X	X	X	Control	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

Note: *All indicated "X" bits are unused, but must be set to "0" when written to ensure proper clock operation.*

RETRIEVING DATA FROM RAM OR CLOCK

The DS1647 is in the read mode whenever $\overline{WE}$ (write enable) is high; $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip-enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1647 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring high to low transition of $\overline{WE}$ and $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA-RETENTION MODE

When V_{CC} is within nominal limits ($V_{CC} > 4.5V$) the DS1647 can be accessed as described above with read or write cycles. However, when V_{CC} is below the power-fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM are blocked from all access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. At this time the power-fail output signal ($\overline{PFO}$) will be driven active low and will remain active until V_{CC} returns to nominal levels. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

BATTERY LONGEVITY

The DS1647 has a lithium power source that is designed to provide energy for clock activity and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1647 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at +25°C with the internal clock oscillator running in the absence of V_{CC} power. Each DS1647 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{PF}, the lithium energy source is enabled for battery backup operation. Actual life expectancy of the DS1647 will be longer than 10 years since no lithium battery energy is consumed when V_{CC} is present.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to +6.0V
Operating Temperature Range (Noncondensing)……0°C to +70°C
Storage Temperature Range
EDIP .....-40°C to +85°C
PowerCap ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ……+260°C
Note: EDIP is wave or hand soldered only.
Soldering Temperature (reflow, PowerCap) .....+260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.2		V_{CC} + 0.3	V	
Logic 0 Voltage, All Inputs	V_{IL}	-0.3		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Average V_{CC} Power Supply Current	I_{CC1}			85	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC2}		3	6	mA	2, 3
CMOS Standby Current ($\overline{CE}$ = V_{CC} - 0.2V)	I_{CC3}		2	4.0	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA) (DQ0–DQ7)	V_{OH}	2.4			V	
Output Logic 0 Voltage (I_{OUT} = +2.1mA) (DQ0–DQ7, $\overline{PFO}$)	V_{OL}			0.4	V	
Write-Protection Voltage	V_{PF}	4.0		4.5	V	

CAPACITANCE

(T_A = +25°C)

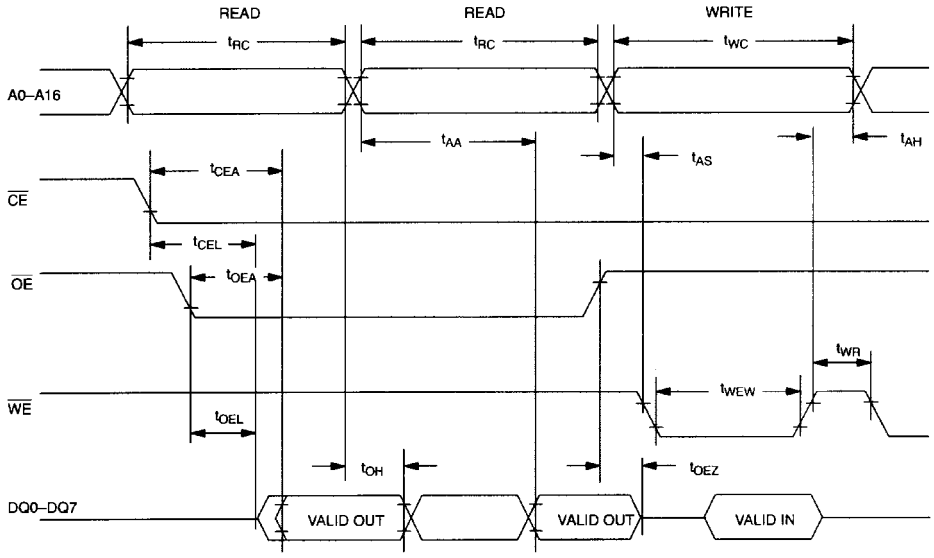
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Pins (Except DQ)	C_I			7	pF	
Capacitance on DQ Pins	C_{DQ}			10	pF	

AC ELECTRICAL CHARACTERISTICS

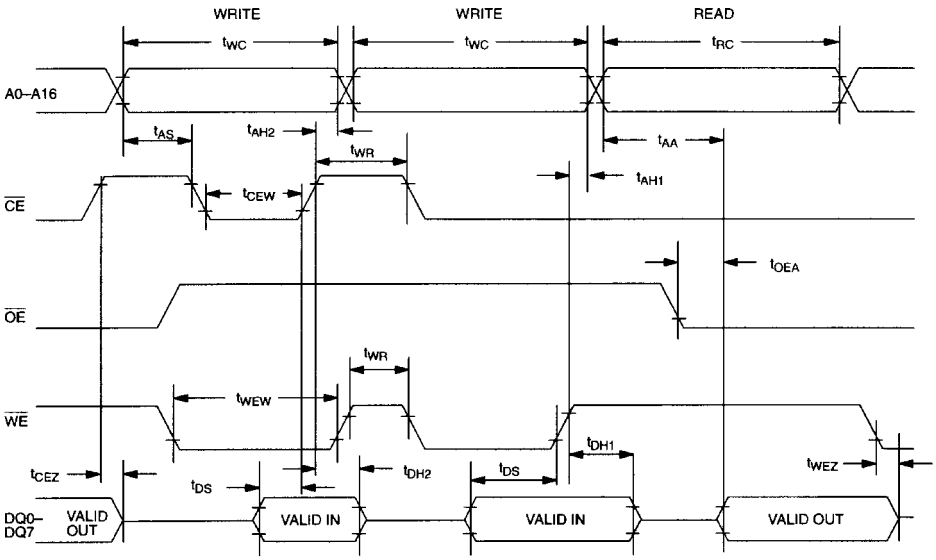
(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
Address Access Time	t_{AA}			120	ns	
$\overline{CE}$ Access Time	t_{CEA}			120	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			40	ns	
$\overline{OE}$ Access Time	t_{OEA}			100	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}			40	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5			ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
Output Hold from Address	t_{OH}	5			ns	
Write Cycle Time	t_{WC}	120			ns	
Address Setup Time	t_{AS}	0			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	100			ns	
Address Hold from End of Write	t_{AH1}	5			ns	5
	t_{AH2}	30				6
Write Pulse Width	t_{WEW}	75			ns	
$\overline{WE}$ Data Off Time	t_{WEZ}			40	ns	
$\overline{WE}$ or $\overline{CE}$ Inactive Time	t_{WR}	10			ns	
Data Setup Time	t_{DS}	85			ns	
Data Hold Time High	t_{DH1}	0			ns	5
	t_{DH2}	25				6

READ CYCLE TIMING



WRITE CYCLE TIMING

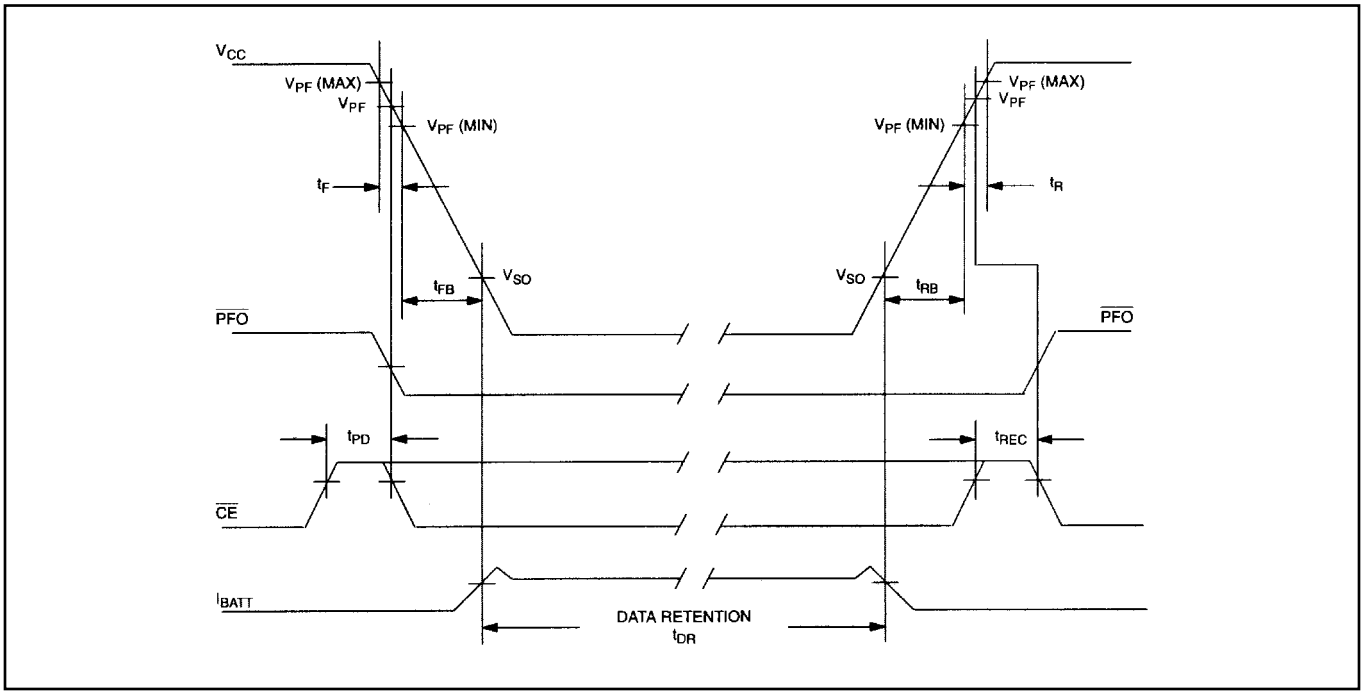


AC ELECTRICAL CHARACTERISTICS—POWER-UP/POWER-DOWN TIMING

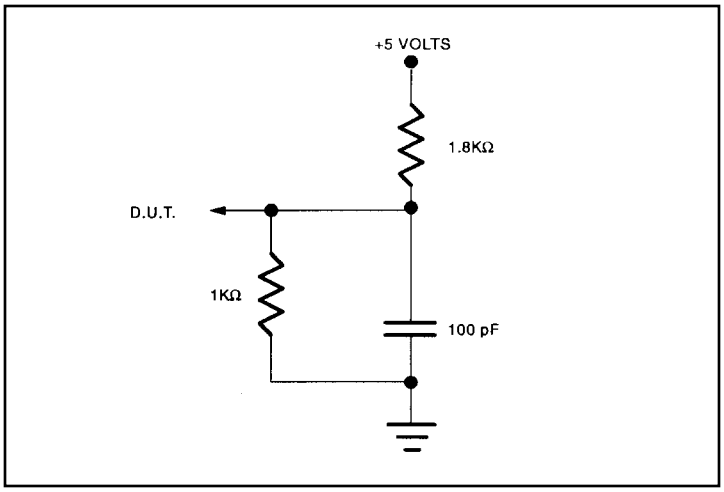
(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
$V_{PF\ (MAX)}$ to $V_{PF\ (MIN)}$ V_{CC} Fall Time	t_F	300			µs	
$V_{PF\ (MIN)}$ to V_{SO} V_{CC} Fall Time	t_{FB}	10			µs	
V_{SO} to $V_{PF\ (MIN)}$ V_{CC} Rise Time	t_{RB}	1			µs	
$V_{PF\ (MIN)}$ to $V_{PF\ (MAX)}$ V_{CC} Rise Time	t_R	0			µs	
Power-Up	t_{REC}	15		35	ms	
Expected Data-Retention Time +25°C (Oscillator On)	t_{DR}	10			years	4

POWER-DOWN/POWER-UP TIMING



OUTPUT LOAD



AC TEST CONDITIONS

Output Load: 50pF + 1TTL Gate
Input Levels: 0 to 3V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) All voltages are referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) Each DS1647 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined for DIP modules as a cumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
5) t_{AH1}, t_{DH1} are measured from $\overline{WE}$ going high.
6) t_{AH2}, t_{DH2} are measured from $\overline{CE}$ going high.
7) RTC Encapsulated DIP Modules (EDIP) can be successfully processed through conventional wave-soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used. See the PowerCap package drawing for details regarding the PowerCap package.

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 EDIP	MDT32+4	**21-0245**	—
34 PCAP	PC2+1	**21-0246**	—

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
10/10	Updated the *Ordering Information* table; updated the storage, lead, and soldering information in the *Absolute Maximum Ratings* section	1, 7

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