THE DATASHEET OF

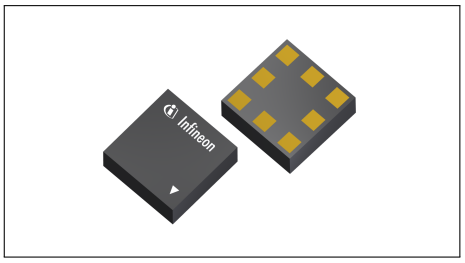
BGSA12UGL8E6327XTSA1

BGSA12UGL8

Low Resistance SPDT Antenna Aperture Switch

Features

- SPDT designed for high-linearity antenna aperture switching and RF tuning applications
- Ultra low R_{ON} resistance of 0.59 Ω at each port in ON state
- Low C_{OFF} capacitance of 270 fF at each port in OFF state
- > 40 V RF voltage OFF state handling
- Low harmonic generation
- Supply voltage range: 1.65 to 3.6 V
- Small form factor 1.1 mm x 1.1 mm
- RoHS and WEEE compliant package



1.1 x 1.1 mm^2

Application

- Impedance Tuning
- Antenna Tuning
- Inductance Tuning
- Tunable Filters

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram

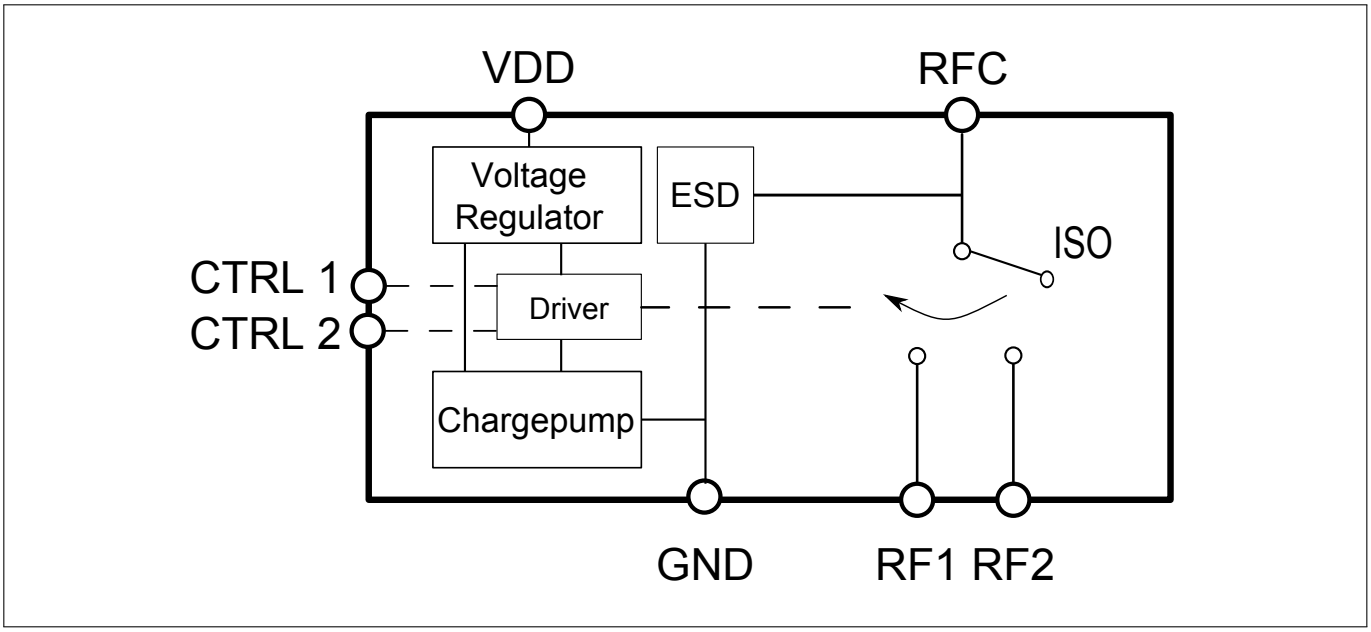
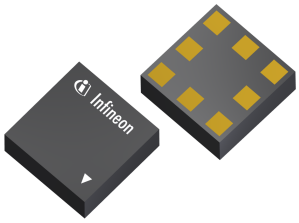


Table of Contents

1 Features



- SPDT designed for high-linearity antenna aperture switching and RF tuning applications
- Ultra low R_{ON} resistance of 0.59 Ω at each port in ON state
- Low C_{OFF} capacitance of 270 fF at each port in OFF state
- > 40 V RF voltage OFF state handling
- Low harmonic generation
- GPIO control interface - including 4 control states
- Supply voltage range: 1.65 to 3.6 V
- No RF parameter change within supply voltage range
- Small form factor 1.1 mm x 1.1 mm
- Suitable for EDGE/ CDMA/WCDMA/ C2K/ LTE Applications
- RoHS and WEEE compliant package

Description

The BGSA12UGL8 is a versatile Single Pole Double Throw (SPDT) RF antenna aperture switch optimized for low C_{OFF} as well as low R_{ON} enabling applications up to 6.0 GHz. This single supply chip integrates with a 2 bits control logic featuring also a low current standby mode. Unlike GaAs technology, the 0.1 dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Due to its very high RF voltage ruggedness, it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses in quality factors.

Product Name	Marking	Package
BGSA12UGL8	A	TSLP-8-1

2 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.4	–	–	GHz	[1]
Supply voltage [2]	V_{DD}	-0.5	–	6	V	only for infrequent and short duration time periods
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power	P_{RF_max}	–	–	41	dBm	Pulsed RF input duty cycle of 25 % and 4620 µs in ON-state, measured per 3GPP TS 45.005, test condition schematic in Fig. 2 and Fig. 3.
RF voltage	V_{RF_max}	–	–	50	V	Short term peaks (1 µs in 0.1 % duty cycle), exceeding typical linearity, R_{ON} and C_{OFF} parameters, in Isolation mode, test condition schematic in Fig. 1
ESD capability, CDM [3]	$V_{ESD,CDM}$	-1	–	+1	kV	
ESD capability, HBM [4]	$V_{ESD,HBM}$	-1	–	+1	kV	
ESD capability, system level (RF port) [5]	$V_{ESD,ANT}$	-8	–	+8	kV	RFx vs system GND, with 27 nH shunt inductor
Junction temperature	T_J	–	–	125	°C	–
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
Control Voltage Levels	V_{CTRL}	-0.7	–	3.3	V	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0 V.
[2] Note: Consider potential ripple voltages on top of V_{DD}. Including RF ripple, V_{DD} must not exceed the maximum ratings: $V_{DD} = V_{DC} + V_{RIPPLE}$.
[3] Field-Induced Charged-Device Model JS-002-2014. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1,5 kΩ, C = 100 pF).
[5] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

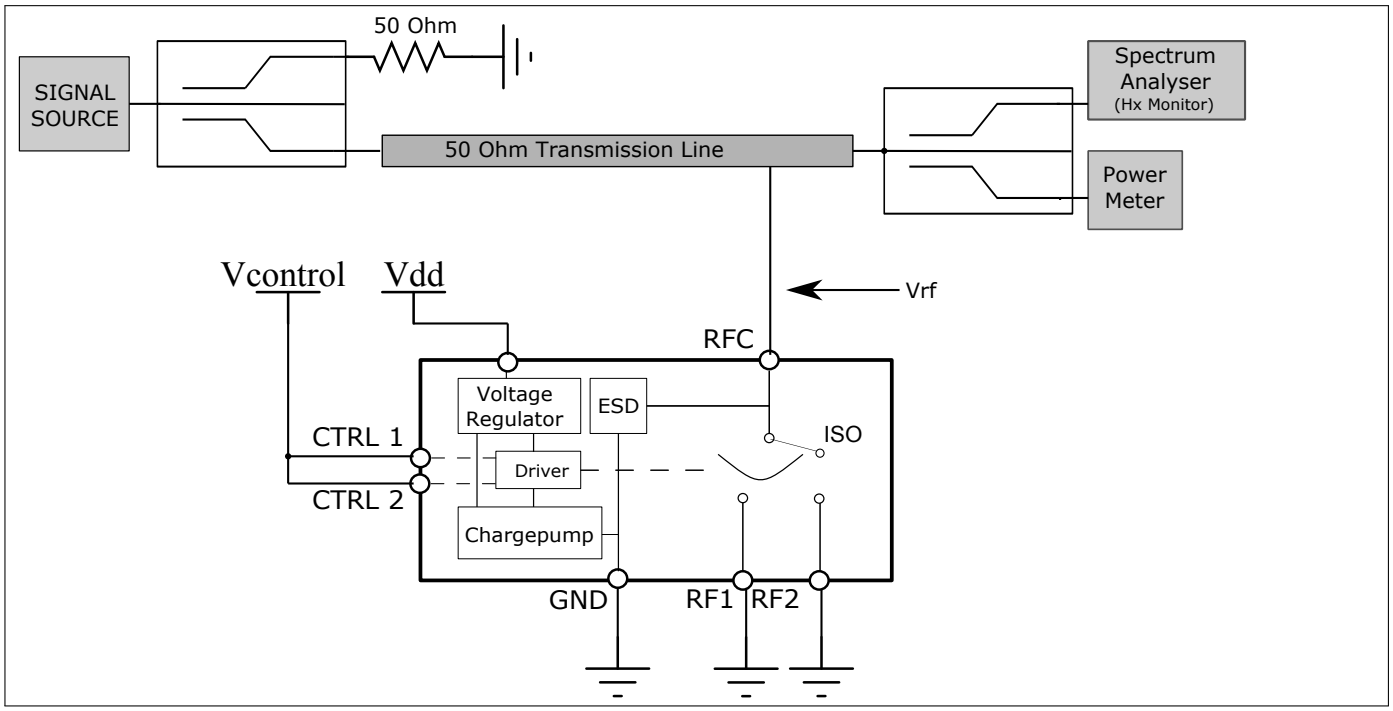


Figure 1: RF operating voltage measurement configuration - OFF mode

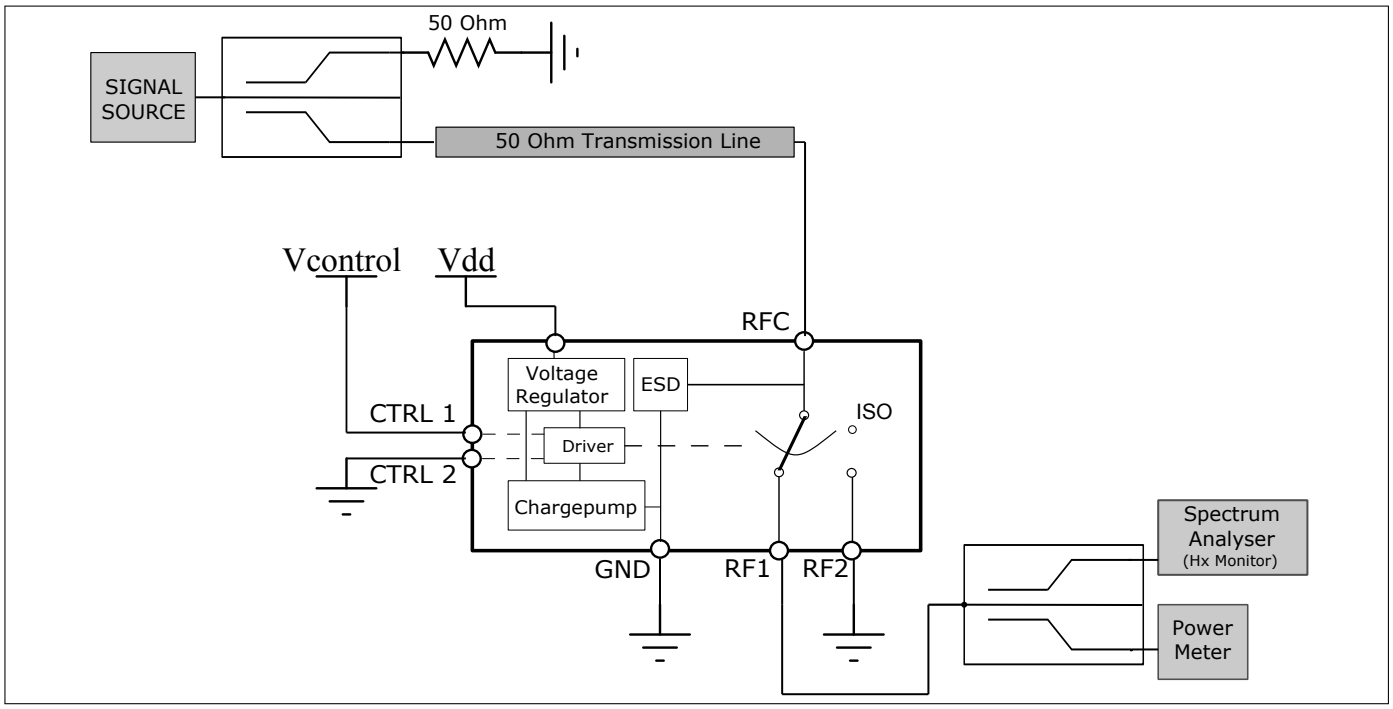


Figure 2: RF operating and Harmonics generation voltage measurement configuration - RF1 ON mode

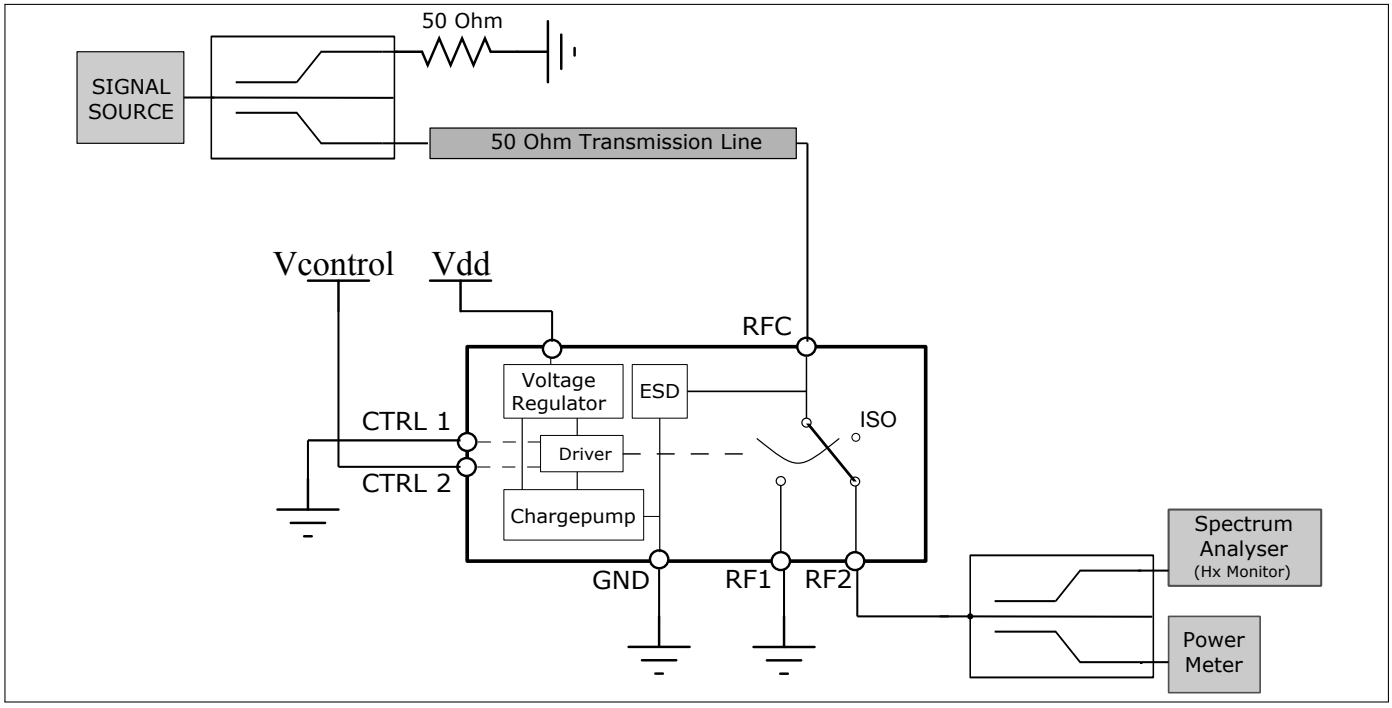


Figure 3: RF operating and Harmonics generation voltage measurement configuration - RF2 ON mode

3 DC Characteristics

Table 2: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.65	2.8	3.6	V	–
Supply current	I_{DD}	45	60	350[1]	µA	[1] T_A = 85 °C, P_{IN} = 40 dBm, ON mode
Supply current in low power mode	$I_{DD,LP}$	–	–	1	µA	T_A = −40 °C...+85 °C, V_{DD} = 1.65 - 3.6 V
Control voltage low	$V_{CTRL,low}$	0	–	0.45	V	–
Control voltage high	$V_{CTRL,high}$	1.2	1.8	2.85	V	$V_{CTRL,high} \ll V_{DD}$
Control current low	$I_{CTRL,low}$	-1	0	1	µA	–
Control current high	$I_{CTRL,high}$	-1	0	4	µA	$V_{CTRL,high} \ll V_{DD}$ 1 MΩ Pull-Down resistor at Control Pins
Ambient temperature	T_A	-40	25	85	°C	–
RF switching time	t_{ST}	4.7	5	5.5	µs	P_{IN} = 0 dBm, Z_0 = 50 Ω, T_A = −40 °C... +85 °C, V_{DD} = 1.65 - 3.6 V
Startup time	t_{PUP}	5	6	7	µs	Ref. Fig. 4 and Fig. 5

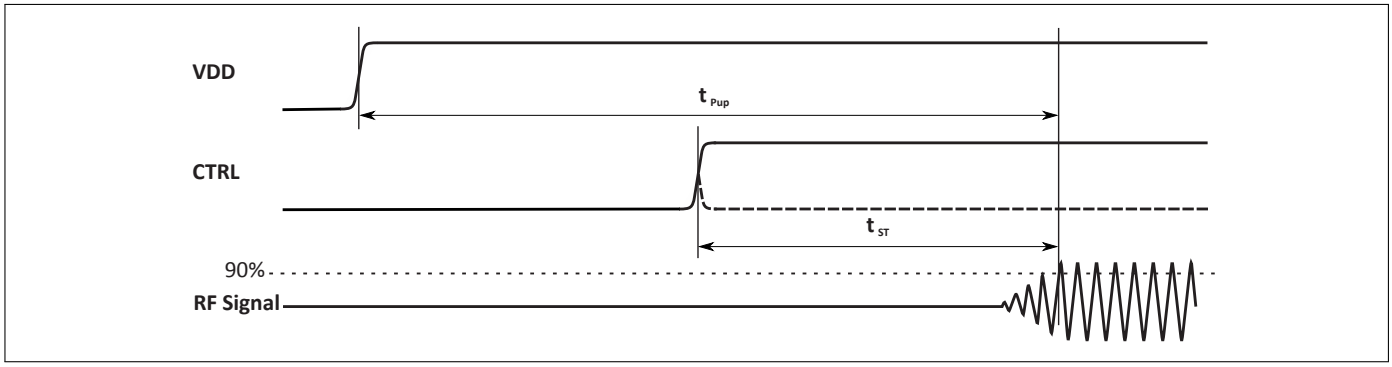


Figure 4: Power Up settling time and switching time

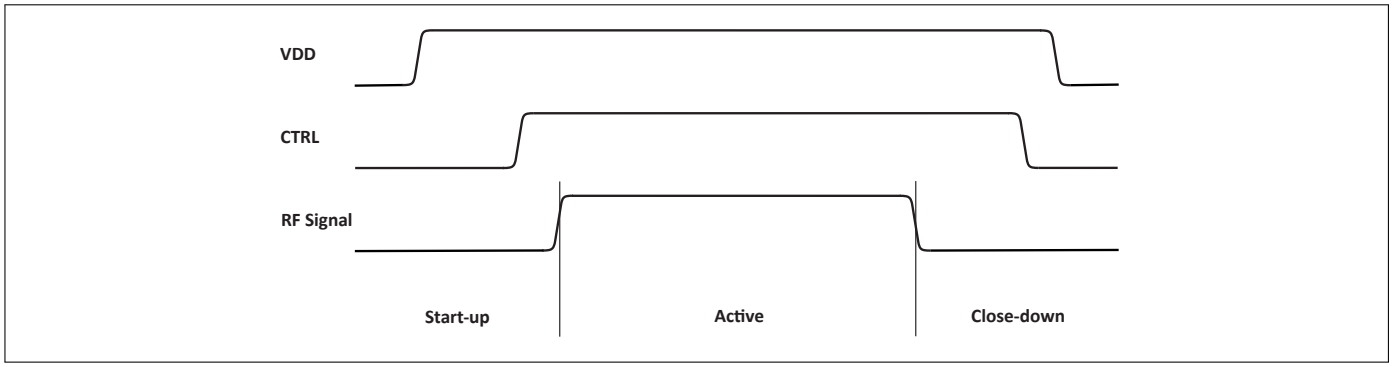


Figure 5: Timing of Control and RF signals for valid operation

4 RF Small Signal Characteristics

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Frequency range	f	0.4		6.0	GHz	
RF1 or RF2 to RFc ON DC resistance	R_{ON}	0.5	0.59	0.7	Ω	V_{DD} = 1.65 - 3.6 V, T_A = 25 °C, Four-terminal sensing method
RF1 or RF2 to RFc OFF DC resistance	R_{OFF}	38	42.5	45	kΩ	
RF1 or RF2 to RFc OFF capacitance	C_{OFF}	235	270	305	fF	V_{DD} = 1.65 - 3.6 V, T_A = 25 °C, extracted from Isolation (S21) measurement Z_0 = 50 Ω

Table 3: RF electrical parameters

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Insertion Loss: RF1 to RFc or RF2 to RFc (SPDT mode) [1,2,3]						
698 - 960 MHz	IL_{SPDT}	0.07	0.14	0.25	dB	V_{DD} = 1.65 - 3.6 V, Z_0 = 50 Ω, T_A = −40 °C...+85 °C
961 - 1710 MHz		0.20	0.26	0.39	dB	
1711 - 1910 MHz		0.24	0.31	0.45	dB	
1911 - 2169 MHz		0.33	0.39	0.55	dB	
2170 - 2690 MHz		0.40	0.48	0.65	dB	
3300 - 3800 MHz		0.69	0.88	1.25	dB	
3801 - 4800 MHz		0.69	1.2	1.75	dB	
4801 - 6000 MHz		1.3	1.9	2.3	dB	
Isolation: RF1 to RFc or RF2 to RFc (SPDT mode) [1,2,3]						
698 - 960 MHz	ISO_{SPDT}	23	24	25	dB	V_{DD} = 1.65 - 3.6 V, Z_0 = 50 Ω, T_A = −40 °C...+85 °C
961 - 1710 MHz		15.5	17	18	dB	
1711 - 1910 MHz		14.5	16	17	dB	
1911 - 2169 MHz		14	15	16	dB	
2170 - 2690 MHz		12	13.5	15	dB	
3300 - 3800 MHz		9.5	11	12	dB	
3801 - 4800 MHz		9	10.5	11.5	dB	
4801 - 6000 MHz		8	8.8	10.5	dB	

1) Valid for all RF power levels, no compression behavior
2) SOLT-calibrated, P_{IN} = 0 dBm
3) On application board without any matching components

Table 3: RF electrical parameters (continued)

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Isolation: RFc to RFx (Isolation mode, no switch selection)[1,2,3]						
698 - 960 MHz	ISO_{ISO}	17	18	19	dB	
961 - 1710 MHz		10.5	11.5	12.5	dB	
1711 - 1910 MHz		10	11	12	dB	
1911 - 2169 MHz		9	10	11	dB	VP_{DD} = 1.65 - 3.6 V, Z_0 = 50 Ω,
2170 - 2690 MHz		8	9	10	dB	T_A = −40 °C...+85 °C
3300 - 3800 MHz		7	8	9	dB	
3801 - 4800 MHz		6.5	7.5	8.5	dB	
4801 - 6000 MHz		5.5	7	8.5	dB	
Isolation: RF1 to RF2 or RF2 to RF1 (SPDT mode)[1,2,3]						
698 - 960 MHz	ISO_{SPDT}	19	21	23	dB	
961 - 1710 MHz		14	16	18	dB	
1711 - 1910 MHz		13	15	17	dB	
1911 - 2169 MHz		12	14	16	dB	V_{DD} = 1.65 - 3.6 V, Z_0 = 50 Ω,
2170 - 2690 MHz		11	13	15	dB	T_A = −40 °C...+85 °C
3300 - 3800 MHz		8	10	12	dB	
3801 - 4800 MHz		7	9	11	dB	
4801 - 6000 MHz		6	8	10	dB	
Isolation: RF1 to RF2 or RF2 to RF1 (Isolation mode, no switch selection)[1,2,3]						
698 - 960 MHz	ISO_{ISO}	34	36	38	dB	
961 - 1710 MHz		25	27	29	dB	
1711 - 1910 MHz		23	25	27	dB	
1911 - 2169 MHz		21	23	25	dB	V_{DD} = 1.65 - 3.6 V, Z_0 = 50 Ω,
2170 - 2690 MHz		18	20	22	dB	T_A = −40 °C...+85 °C
3300 - 3800 MHz		14	16	18	dB	
3801 - 4800 MHz		12	14	16	dB	
4801 - 6000 MHz		10	12	14	dB	

[1] Valid for all RF power levels, no compression behavior
[2] SOLT-calibrated, P_{IN} = 0 dBm
[3] On application board without any matching components

5 RF Large Signal Parameter

Table 4: RF large signal specifications at T_A = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Max. RF Operating Voltage	V_{RF_opr}	–	–	40	V	In Isolation mode, test condition schematic in Fig. 1 for H2/H3 < -40 dBm @ 50 Ω
Max. RF Operating Power	V_{RF_pwr}	–	–	40	dBm	RF1 or RF2 in ON mode, test condition schematic in Fig. 2 or Fig. 3 for H2/H3 < -40 dBm @ 50 Ω
Harmonic Generation up to 12.75 GHz						
All RF Ports - Second Order Harmonics	P_{H2}	95	105	-	dBc	25 dBm, 50 Ω, f_0 = 824 MHz, test condition in Fig. 2 an Fig. 3
All RF Ports - Third Order Harmonics	P_{H3}	110	120	–	dBc	25 dBm, 50 Ω, f_0 = 824 MHz, test condition in Fig. 2 an Fig. 3
All RF Ports - Second Order Harmonics	P_{H2}	80	90	–	dBc	36 dBm, 50 Ω, f_0 = 824 MHz, test condition in Fig. 2 an Fig. 3
All RF Ports - Third Order Harmonics	P_{H3}	90	100	–	dBc	36 dBm, 50 Ω, f_0 = 824 MHz, test condition in Fig. 2 an Fig. 3
All RF Ports - Third Order Harmonics	P_{H3}	90	100	–	dBc	36 dBm, 50 Ω, f_0 = 1800 MHz, test condition in Fig. 2 an Fig. 3
All RF Ports - Second Order Harmonics	P_{H2}	95	105	–	dBc	25 dBm, 50 Ω, f_0 = 1800 MHz, test condition in Fig. 2 an Fig. 3
All RF Ports - Third Order Harmonics	P_{H3}	110	120	–	dBc	25 dBm, 50 Ω, f_0 = 1800 MHz, test condition in Fig. 2 an Fig. 3
All RF Ports - Second Order Harmonics	P_{H2}	80	90	–	dBc	36 dBm, 50 Ω, f_0 = 1800 MHz, test condition in Fig. 2 an Fig. 3
Higher order harmonic products	P_{Hx}	105	–	–	dBc	25 dBm, 50 Ω
Intermodulation Distortion IMD2						
IIP2, low	$IIP2_L$	110	114	–	dBm	IIP2 conditions table 5
IIP2, high	$IIP2_H$	117	120	–	dBm	
Intermodulation Distortion IMD3						
IIP3	$IIP3$	71	75	–	dBm	IIP3 conditions table 6
SV LTE Intermodulation						
IIP3,SVLTE	$IIP3_{SV}$	71	75	–	dBm	SV-LTE conditions table 7

Table 5: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 6: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

Table 7: SV-LTE conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 5	872	827	23	872	14
Band 13	747	786	23	747	14
Band 20	878	833	23	2544	14

6 Logic Table

Table 8: Logic Table

CTRL 1	CTRL 2	Mode
0	0	Low power mode
0	1	RF2 connected to RFC
1	0	RF1 connected to RFC
1	1	Isolation mode (no switch selection)

7 Application Information

Pin Configuration and Function

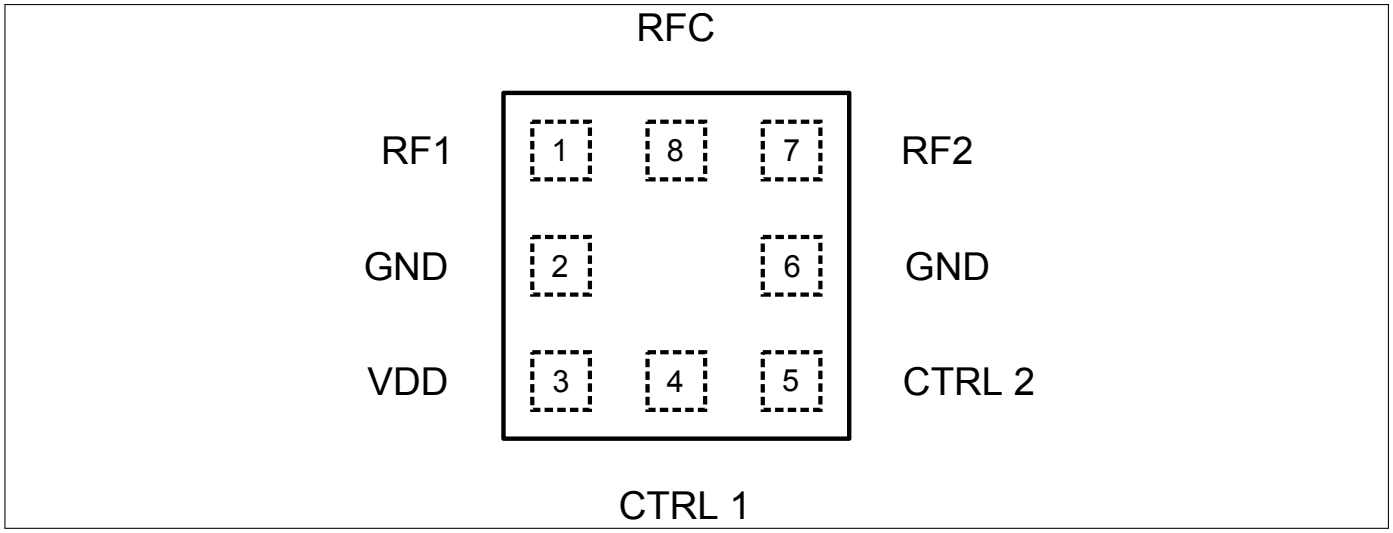


Figure 6: BGSA12UGL8 Pin Configuration (top view)

Table 9: Pin Definition and Function

Pin No.	Name	Function
1	RF1	RF port
2	GND	Ground
3	VDD	DC Supply Voltage
4	CTL1	Control Pin 1
5	CTL2	Control Pin 2
6	GND	Ground
7	RF2	RFport
8	RFC	Common RF

8 Package Information

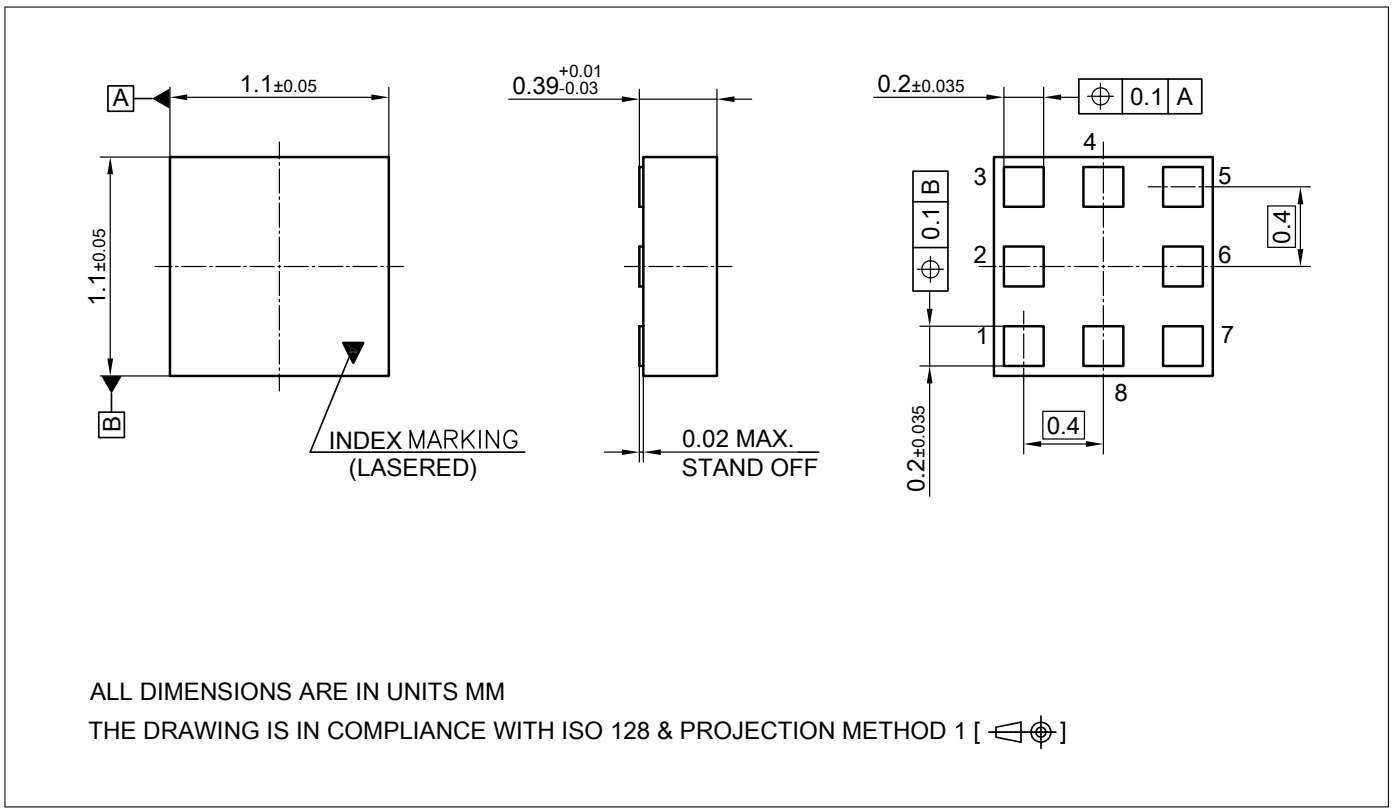


Figure 7: TSLP-8-1 Package Outline (top, side and bottom views)

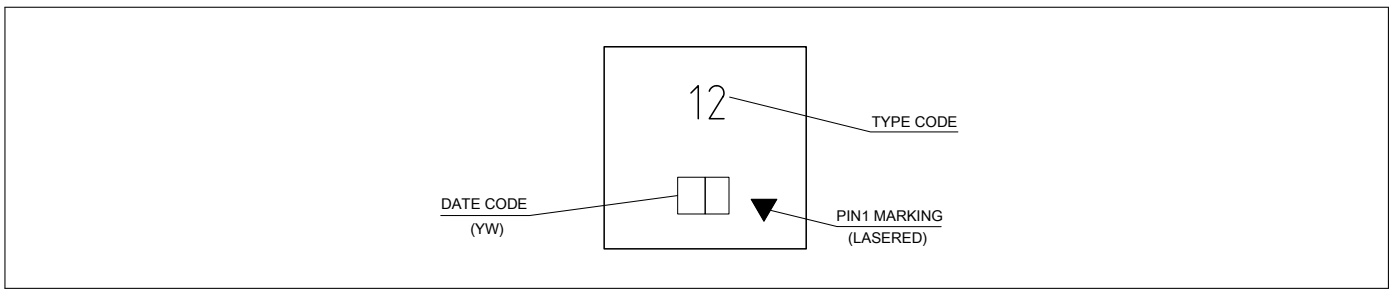


Figure 8: Marking Specification (top view): Date code digits Y and W defined in Table 10/11

Table 10: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2000	0	2010	0	2020	0
2001	1	2011	1	2021	1
2002	2	2012	2	2022	2
2003	3	2013	3	2023	3
2004	4	2014	4	2024	4
2005	5	2015	5	2025	5
2006	6	2016	6	2026	6
2007	7	2017	7	2027	7
2008	8	2018	8	2028	8
2009	9	2019	9	2029	9

Table 11: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

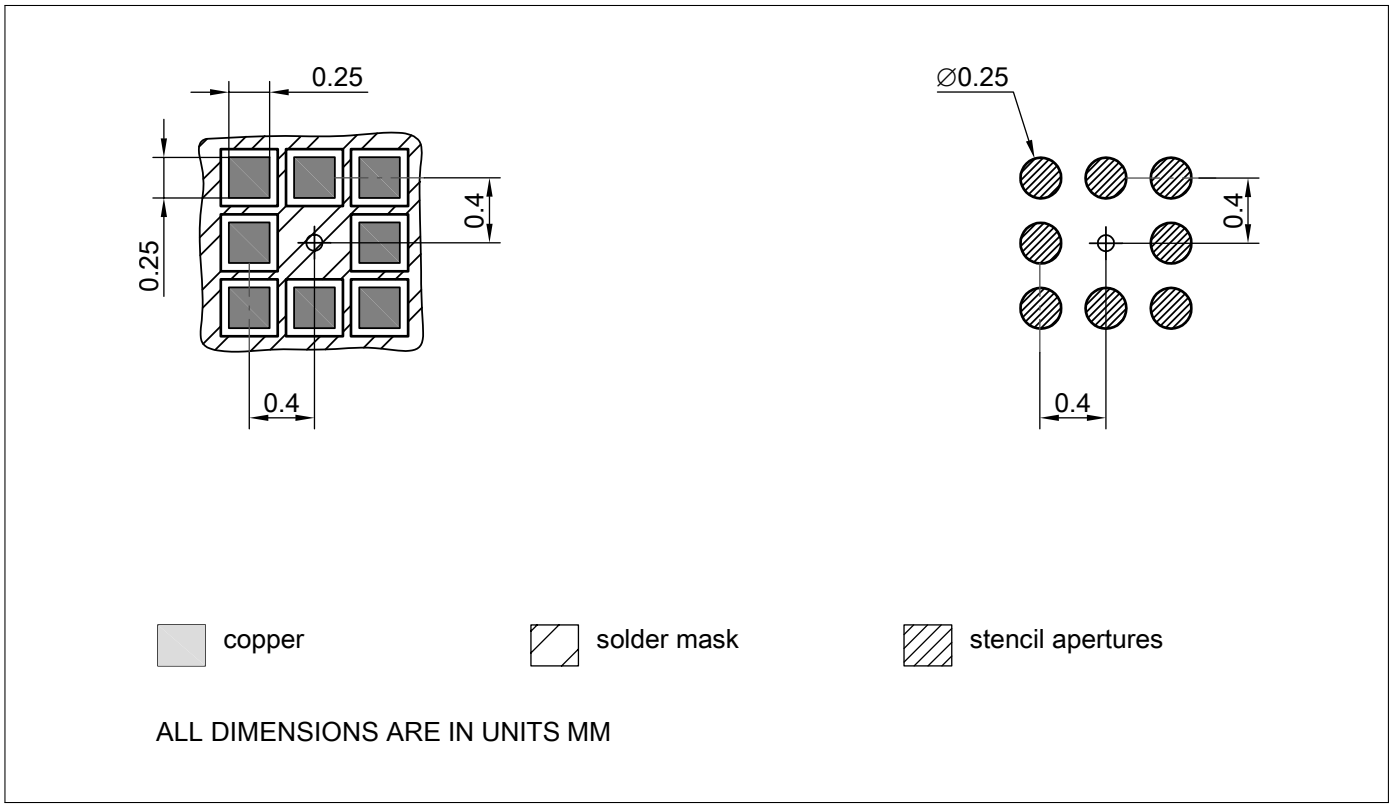


Figure 9: Footprint Recommendation

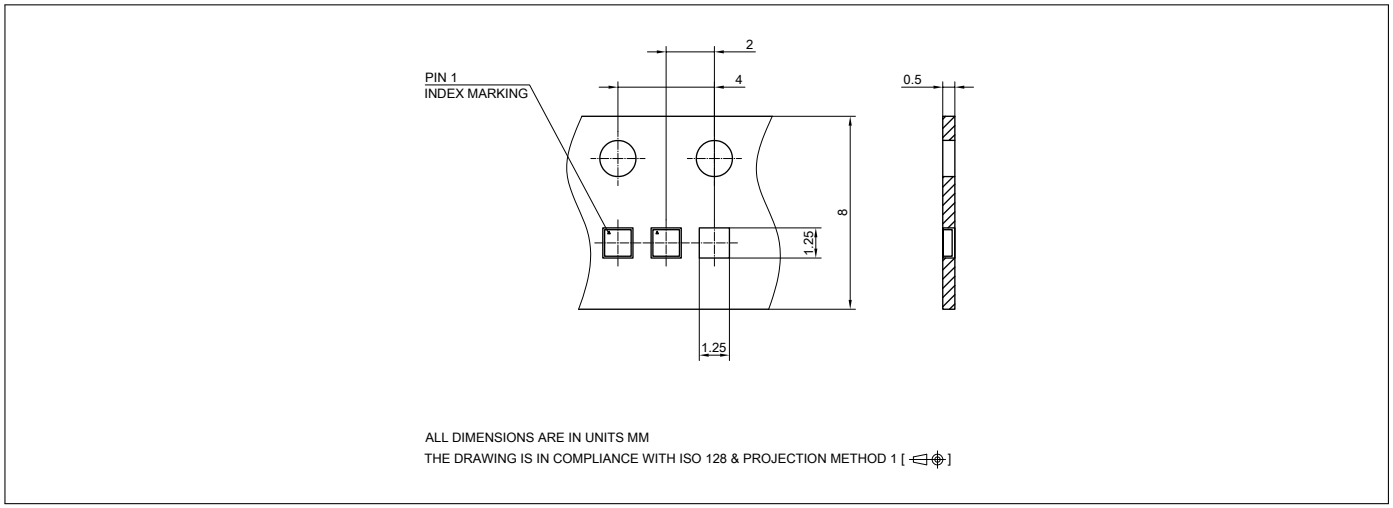


Figure 10: TSLP-8-1 Carrier Tape

Revision History	
Creation of document Revision 2.3, 2019-08-13	
Page or Item	**Subjects (major changes since previous revision)**
6	Updated Vddmin to 1.65V

Other Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2019-08-13
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
Doc_Number

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View BGSA12UGL8E6327XTSA1 on WIN SOURCE
- Infineon Technologies Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management